Advanced
Micro
Devices

Am486® Microprocessor Design Application Notes

Publication#19240 Rev: B Amendment/0
Issue Date: July 1995

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Am486® Microprocessor Family Phase Lock Loop (PLL) Clock Control

Application Note

Advanced Micro Devices

Significant system power savings can be achieved by using the Phase Lock Loop (PLL) clock control circuit outlined in this application note with any Am486 family microprocessor.

The Environmental Protection Agency's (EPA) "Energy Star" program, unveiled during the summer of 1992, provided the personal computer (PC) industry with a voluntary incentive to reduce desktop PC power consumption. The prime directive of the EPA's Energy Star program is that no more than 30 W will be consumed in low power mode for each of the following system components: the personal computer itself, the monitor, and the printer.

The Am486DX2-80 microprocessor serves as an example in this application note, illustrating how the Phase Lock Loop clock control circuit can enable your design to include an efficient and energy-saving clock control mechanism.

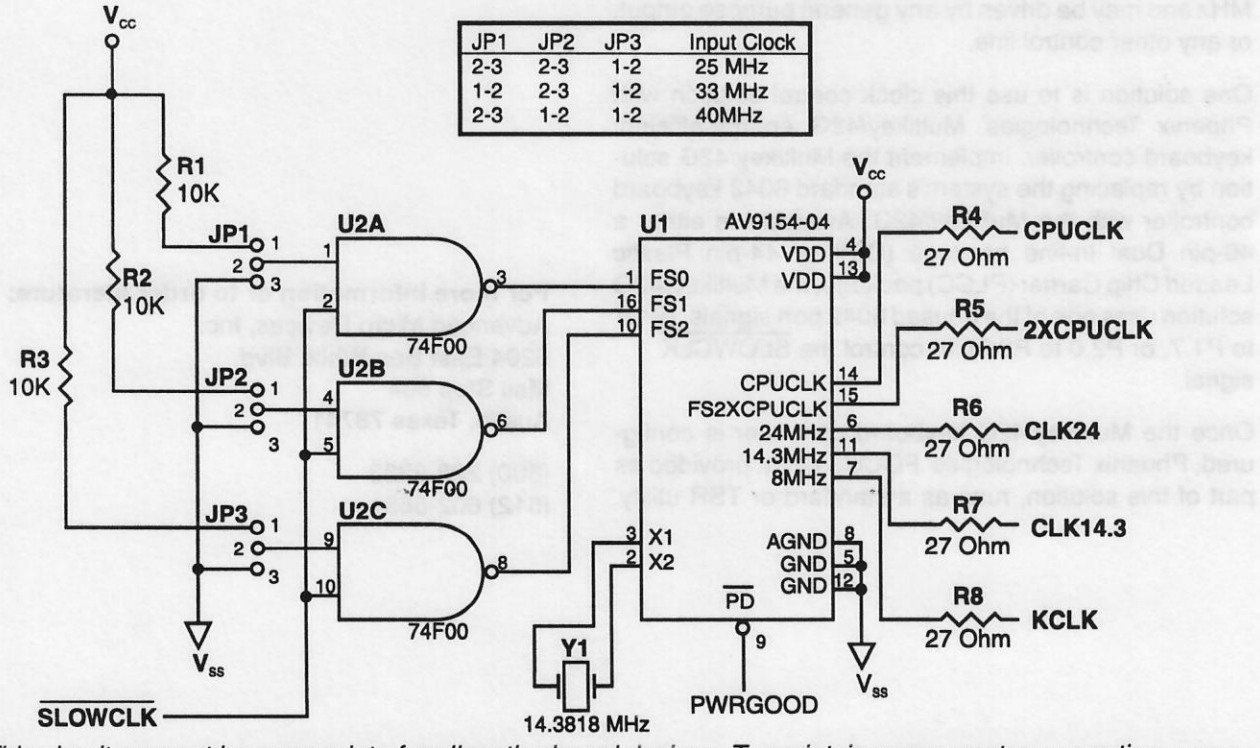
Power Consumption

The CPU accounts for a significant part of system power consumption. The data sheet typical I_{CC} for the 3.3-V Am486DX2-80 microprocessor is 640 mA, which translates to a typical power consumption of 2.1 W.

Using the simple Phase Lock Loop (PLL) clock control circuit with any member of the Am486DX microprocessor family, enables system power consumption to be significantly lowered. This feature assists designers in meeting the Energy Star requirements.

A typical motherboard, including an Am486DX2-80 CPU, consumes around 13 W, meaning that the CPU accounts for approximately 16 percent of the total motherboard power consumption. By controlling the clock, via the methods described in this application note, the CPU component of the motherboard power consumption can be reduced by approximately 90 percent. (See Table 1). Overall motherboard power consumption is also lowered by the reduced clock speed.

Figure 1 Phase Lock Loop (PLL) Clock Control Circuit



Note: *This circuit may not be appropriate for all motherboard designs. To maintain proper system operation, ensure all other system clocks conform to required specifications when implementing this circuit in a design.*

Publication #: **18495** Rev. **C** Amendment/**0**
Issue Date: **October 25, 1994**

SLOWCLK For Power Savings

Because Phase Lock Loop clocks are not static, they may not be turned off or driven at a frequency less than 8 MHz. Furthermore, the frequency of the CPU clock cannot be changed more than 0.1 percent cycle-to-cycle per the datasheet specification. The designer must ensure this specification is met or the PLL will lose its lock and unstable operation will result.

The SLOWCLK signal is common to all three of the 74F00 NAND gates, and is normally high. Following a user-defined time-out, SLOWCLK is driven low by any control line. With SLOWCLK low, the outputs of all three of the 74F00 NAND gates are high, which selects an output frequency of 8 MHz from the frequency generator. Once activity is detected, SLOWCLK goes high, re-selecting the full-on frequency. (See Figure 1).

Table 1. I_{CC} Values for Am486DX-80 CPU (V_{CC}=3.3 V)

Operating Frequency	Typical Power Supply Current (I_{CC})
8 MHz (SLOWCLK)	64 mA
80 MHz	640 mA

SLOWCLK CONTROL

The AV9154-04 slowly ramps the CPU clock down to 8 MHz and may be driven by any general purpose output, or any other control line.

One solution is to use this clock control solution with Phoenix Technologies' Multikey/42G energy-efficient keyboard controller. Implement the Multikey/42G solution by replacing the system's standard 8042 keyboard controller with the Mulitkey/42G. Available in either a 40-pin Dual In-line package (DIP) or 44-pin Plastic Leaded Chip Carrier (PLCC) package, the Multikey/42G solution uses one of the unused 8042 port signals, (P1.1 to P1.7, or P2.0 to P2.3), to control the SLOWCLK signal.

Once the Multikey/42G keyboard controller is configured, Phoenix Technologies' FOCUS utility, provided as part of this solution, runs as a standard or TSR utility. The FOCUS utility permits refinements to the initial configuration, such as timer settings, which turn off the hard disk(s) after a period of inactivity.

POWER SAVINGS

Clock control solutions, evaluated in the Advanced Micro Devices laboratory, have shown significant power savings of over 4 W. Placing a power-managed hard disk drive in standby mode can account for an additional system power savings of 2.2 W, resulting in a total possible system savings of 6.2 W.

Note: *Care should be taken when slowing the CPU clock in systems where other clocks are derivatives of the CPU clock. The designer must ensure that all system timing requirements are maintained when changing the frequency of the clock to the microprocessor.*

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Am486® Microprocessor Family Clock Gating Recommendations

Advanced Micro Devices

Application Note

Microprocessor motherboard design requires that special attention be paid to the design of the clock control circuitry. A designer must provide for timing control of the clock at startup. Keeping this requirement in mind, this application note provides three examples of clock delay circuits.

AMD® recommends that the CLK input to an Am486 microprocessor be grounded until V_{CC} has reached its normal operating level. Once V_{CC} reaches its normal operating level, the CPU is able to receive its specified clock frequency.

Methods of gating the CPU clock include:

- Using a chipset that does not clock the CPU until V_{CC} has fully ramped.
- Using a clock driver with an output enable.
- Using a clock clamping circuit to gate the CPU clock.

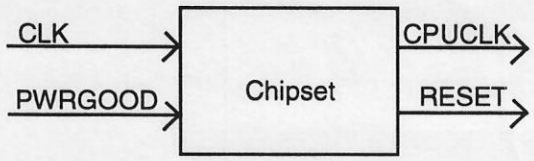
For proper operation of Am486 devices, the system timing must be maintained as illustrated in Figure 1. Good design practice dictates gating or "holding off" the CPU clock until the system V_{CC} has reached its normal operating voltage. The timing diagram illustrates that once V_{CC} reaches its operating voltage point (either 3.3 V or 5 V), and the PWRGOOD signal is active, RESET must be asserted for at least 1 ms to allow the CPUs internal PLL to lock prior to system operation.

Chipset with Internal Delay

Because many 486 core logic chipsets receive PWRGOOD and CLK as inputs and generate RESET and CPUCLK as outputs, they have the potential to incorporate an internal delay function, holding off the CPU until V_{CC} has reached it's normal operating voltage.

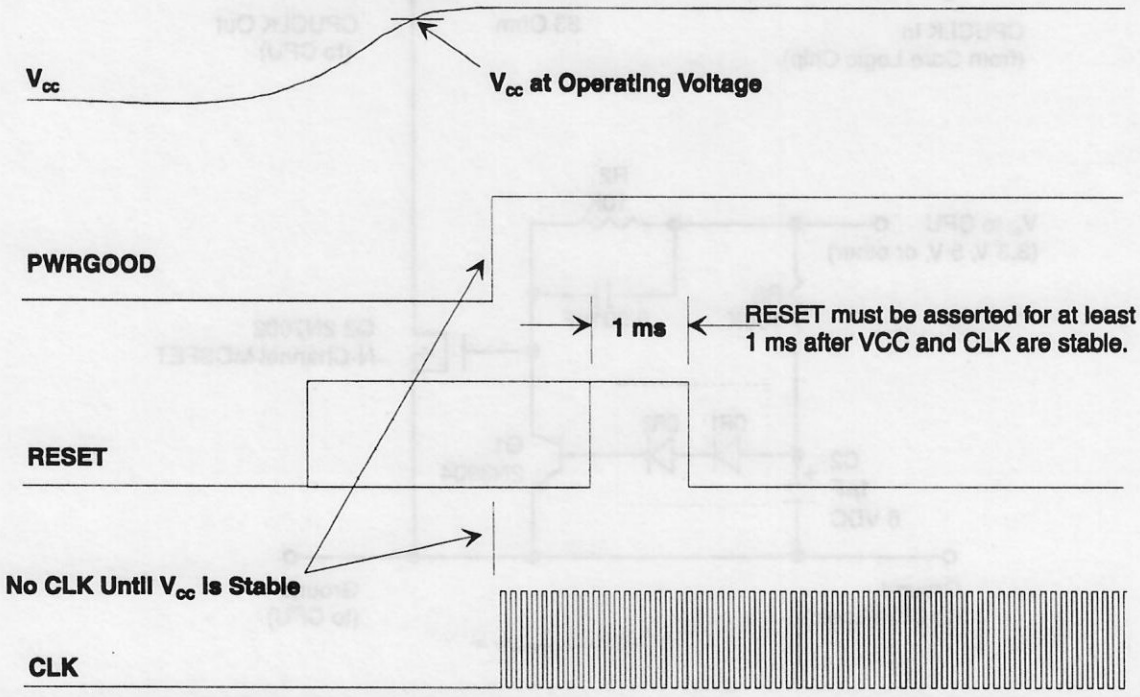
Figure 2 illustrates a chipset capable of providing internal clock gating.

Figure 2. Internal Delay Function of Chipset



Note: *Check your chipset's data sheet for specifics on your chipset's internal delay function.*

Figure 1. Timing Diagram of PicoPower Redwood Chipset Delay Function



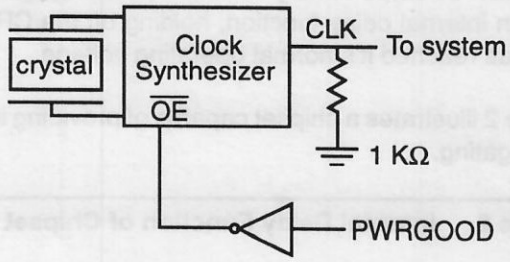
Publication #: 19195 Rev. B Amendment/0
Issue Date: November 1994

Clock Driver With Output Enable

A clock synthesizer (or other driver) with an output enable pin for the CPU clock can be used to prevent the CPU from being clocked until V_{CC} has reached its normal operating voltage.

The circuit in Figure 3 consists of a frequency generator with a dedicated $\overline{OE}$, which may be used to "hold off" or gate the clock until V_{CC} has reached its normal operating level using PWRGOOD as the output enable.

Figure 3. Clock Synthesizer With $\overline{OE}$



Clock Clamping Circuit

A third method of gating the CPU clock is to use a clock clamping circuit to effectively ground the clock input for a predetermined period of time.

In addition to delaying the CPU clock, the clock clamping circuit, shown in Figure 4, also prevents noise glitches on the clock signal from being sensed by the CPU during the power-on sequence when V_{CC} of the microprocessor is making the transition from 0 V to V_{CC} (e.g., 3.3 V or 5 V).

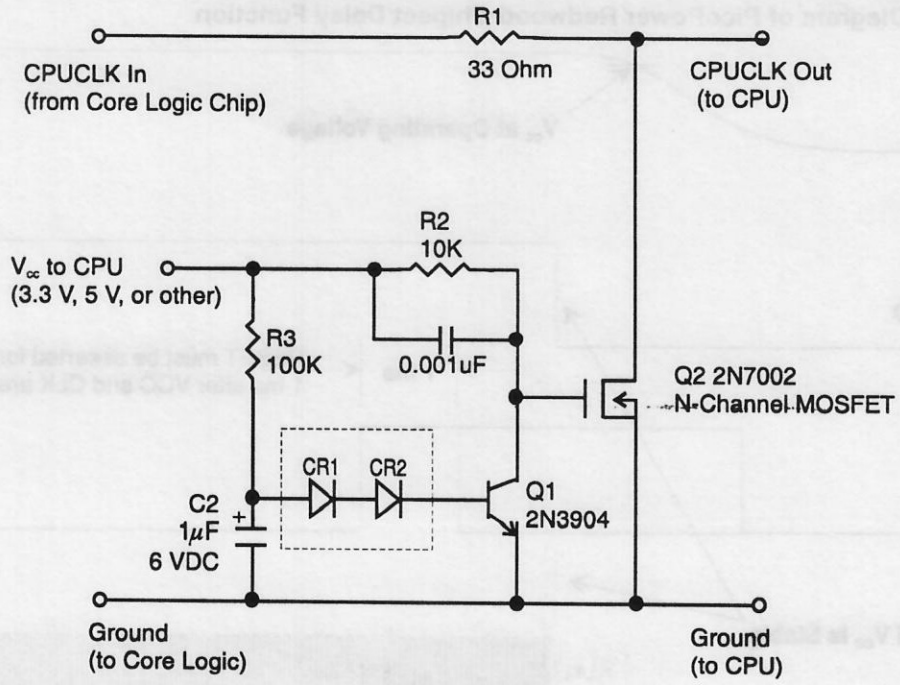
Microprocessor clock noise glitches usually are caused by one of the following conditions:

- bad clock generator start-up circuit design
- poor layout of the microprocessor printed circuit trace on the PC motherboard
- power supply ringing during transition from 0 V to V_{CC}
- a very long voltage slew rate (e.g., 100 ms).

In any case, the clock clamping circuit ensures that a clock signal glitch is not sensed by the microprocessor clock input circuit during startup.

CPU clock signal integrity is best maintained by passing the clock directly from the core logic.

Figure 4. Clock Clamping Circuit



Am486® Microprocessor Family System Design Considerations

Advanced Micro Devices

Application Note

This application note provides guidelines for using the Am486DX2 and Am486DX4 microprocessors in universal motherboard designs. This application note also adds information to accommodate processors with a selectable clock multiplier and writeback cache.

MULTIFUNCTIONAL SYSTEM DESIGNS

Advanced Micro Devices encourages the development of personal computer system board designs that incorporate multiple microprocessor types. This approach allows system designers to anticipate industry development and support optional functionality, include a selectable clock multiplier and writeback cache, all in a single versatile design. Figure 1 shows the recommended signal connections and jumper options for supporting a 486 microprocessor in a standard 168-pin PGA socket. Table 1 lists settings for JP1 and JP2. Table 2 lists the pinout differences for several commonly used microprocessors.

Figure 1. Multi-Type CPU Socket Connections

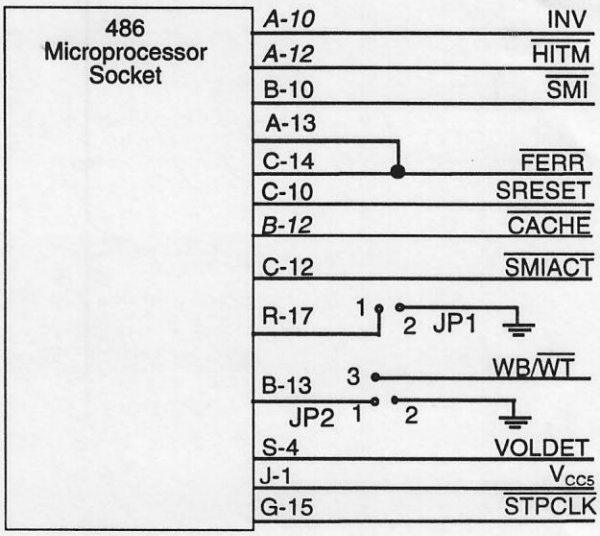


Table 1. Jumper Settings

Header	Processor	Jumper
JP1	Future Am486DX2	1-2
	Intel486DX4 and Future Am486DX4	None
JP2	Current Am486DX2	1-2
	Current Am486DX4	None
	Writeback Cache	1-3

Table 2. Microprocessor Pinout Differences

Pin No.	Am486DX4 CPU	Future 3 V Writeback Enhanced CPU	Am486DX2 CPU (V_{CC}=5 V)	Am486DX2 CPU (V_{CC}=3.3 V)	169-Pin OverDrive Socket[1]	i486DX2 SL-Enhanced	i486DX4
A-10	INC	INV	INC[2]	INC	INC	INC	INC
A-12	INC	$\overline{HITM}$	INC[2]	INC	INC	INC	INC
A-13	INC	INC	INC[2]	INC	$\overline{FERR}$	INC	INC
B-10	INC	$\overline{SMI}$	INC[2]	INC	$\overline{SMI}$	$\overline{SMI}$	$\overline{SMI}$
B-12	INC	$\overline{CACHE}$	INC[2]	INC	INC	INC	INC
B-13	CLKMUL	WB/$\overline{WT}$	INC[2]	CLKMUL[3]	INC	INC	INC
B-14	TMS	TMS	TMS	TMS	$\overline{UP}$	TMS	TMS
C-10	INC	SRESET	INC[2]	INC	INC	SRESET	SRESET
C-12	INC	$\overline{SMIACT}$	INC[2]	INC	$\overline{SMIACT}$	$\overline{SMIACT}$	$\overline{SMIACT}$
C-14	$\overline{FERR}$	$\overline{FERR}$	$\overline{FERR}$	$\overline{FERR}$	INC	$\overline{FERR}$	$\overline{FERR}$
G-15	INC	$\overline{STPCLK}$	INC	INC	$\overline{STPCLK}$	$\overline{STPCLK}$	$\overline{STPCLK}$
J-1	INC	INC	V_{CC}	INC	V_{CC}/V_{CC5}	V_{CC}	V_{CC5}
R-17	INC	CLKMUL[4]	INC	INC	INC/CLKMUL	INC	CLKMUL
S-4	VOLDET	VOLDET	NC	VOLDET	NC/VOLDET	NC	VOLDET

Notes:

1. *When using the 237-pin version, refer to the next higher number and letter (i.e., A-13 = B-14).*
2. *The INC indicates a design change from the NC pinout specifications in the published data sheets.*
3. *Pin B-13 **MUST BE** connected to V_{SS} for proper operation of current Am486DX2 microprocessor products.*
4. *Pin R-17 **MUST BE** connected to V_{SS} for proper operation of future Am486DX2 microprocessor products.*

Document #: 19178 Rev. B Amendment/0
Issue Date: November 1994

Am486® Microprocessor Family Low Voltage Power Supply Circuits

Application Note

Advanced Micro Devices

Am486 microprocessors manufactured using the CS-24 process feature a 5-V tolerant signal interface, but require a +3.3-V input for V_{CC}. For cost effectiveness, AMD® recommends the use of a voltage regulator circuit to generate the V_{CC} input from a regulated +5-V source. This application note describes two such circuits that provide a programmable voltage range (3.3–3.9 V). The note also includes filtering and routing guidelines for incorporating these circuits into a motherboard design.

BACKGROUND

The Am486 high-performance microprocessor family uses the CS-24 (0.5 micron) manufacturing process that incorporates 5-V I/O tolerance. This means that the device can accept both 3.3-V and 5-V input signals even though it requires 3.3-V input power. The input circuit protects the microprocessor from potential damage caused by the application of 5-V signals.

AMD has developed two circuit designs that can generate a selectable input voltage range (3.3 V–3.9 V) for the microprocessor V_{CC} source. The linear regulator circuit is the lower cost solution. The second option is a switching regulator that provides a higher efficiency output, but at a significant cost increase. Design requirements (higher efficiency vs. lower cost) determine which power solution to use in a specific system design.

A second basic issue in power supply circuit design is noise reduction. Excessive noise levels can impair proper operation and contribute to possible radio frequency transmissions that can affect compliance with national and international agency regulations. This application note provides some basic guidelines for reducing noise generated by or transmitted through the power supply circuits.

LINEAR REGULATOR POWER CIRCUIT

The lower cost linear regulator power circuit is shown in Figure 1. The circuit provides an output of +5 V or 3.3 V–3.9 V depending on the state of the VOLDET input from the microprocessor. On AMD processors manufactured using the CS-24 process, the VOLDET signal is set to the V_{SS} level used by the microprocessor. The actual output range produced by the regulator circuit depends on the ratio of the values of R1 and R2. Table 1 shows the recommended resistor sizes used to produce specific voltage outputs (V_{OUT}).

Figure 1 Variable Linear Regulator Microprocessor Power Supply Circuit

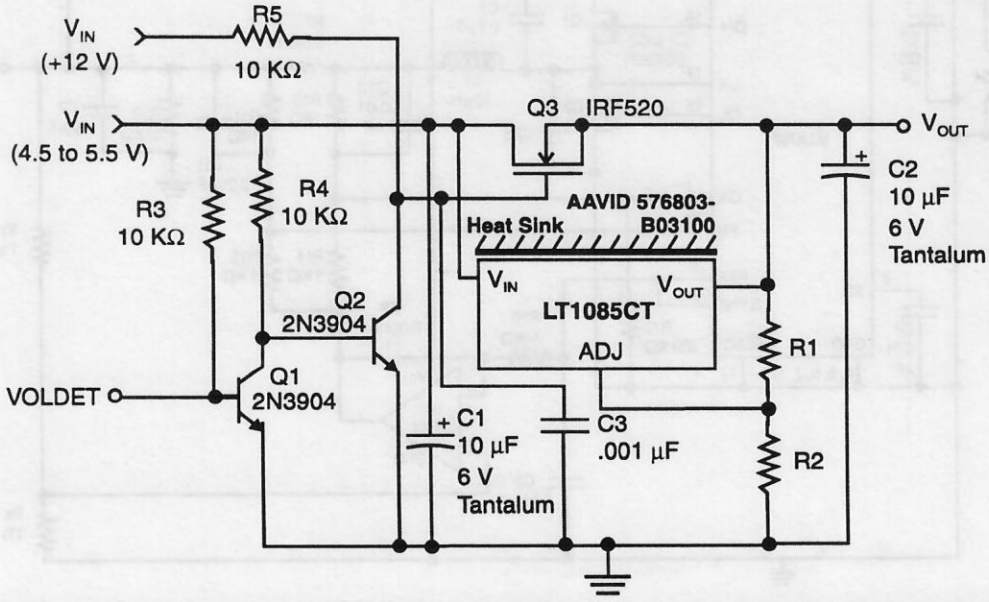


Table 1. R1 and R2 Resistor Values

V_{OUT}	R1	R2
3.3 V	124 Ω	205 Ω
3.45 V	124 Ω	218 Ω
3.6 V	124 Ω	234 Ω
3.75 V	124 Ω	249 Ω
3.9 V	124 Ω	264 Ω

Note: *All resistors are 1% tolerance.*

Document #: **19197** Rev. **C** Amendment/**0**
Issue Date: **May 1995**

SWITCHING REGULATOR CIRCUIT

The switching regulator power circuit is shown in Figure 2. The circuit provides a +5 V or a 3.3 V–3.9 V ± 2% output depending on the state of the VOLDET input generated by the microprocessor. The circuit has an efficiency of greater than 90%. On AMD processors manufactured using the CS-24 process, the VOLDET signal is set to the V_{SS} level used by the microprocessor. The actual output range produced by the regulator circuit depends on the ratio of the values of Rx and Ry. Table 2 shows the recommended resistor sizes used to produce a specific voltage output range.

Table 2. Rx and Ry Resistor Values

V_{OUT}	Rx	Ry
3.3 V	332 KΩ	0 Ω
3.45 V	332 KΩ	15 KΩ
3.6 V	332 KΩ	30.1 KΩ
3.75 V	332 KΩ	45.3 KΩ
3.9 V	332 KΩ	60.4 KΩ

Note: *Rx and Ry are 1% tolerance resistors.*

POWER SUPPLY NOISE REDUCTION

AMD recommends using a split power plane to isolate the microprocessor from the rest of the motherboard. This approach helps to reduce noise levels without having to use additional printed-circuit board (PCB) planes. Figure 3 shows an example diagram of the recommended PCB layout.

The split plane is made from a portion of copper that is cut out and isolated from the PCB 5-V power plane. This cutout region supplies a separate power source for the microprocessor and allows for the installation of critical bypass decoupling capacitors. The microprocessor power plane should overlap the output pin of the voltage regulator circuit to provide a low impedance current path.

Note: *Never split the ground plane; it provides a low impedance current sink and reference.*

Generous decoupling is recommended to ensure that clean power is supplied to the microprocessor. Figure 3 shows a possible layout for capacitor placement. Figure 4 indicates the recommended decoupling capacitor values.

Figure 2 Variable Switching Regulator Microprocessor Power Supply Circuit

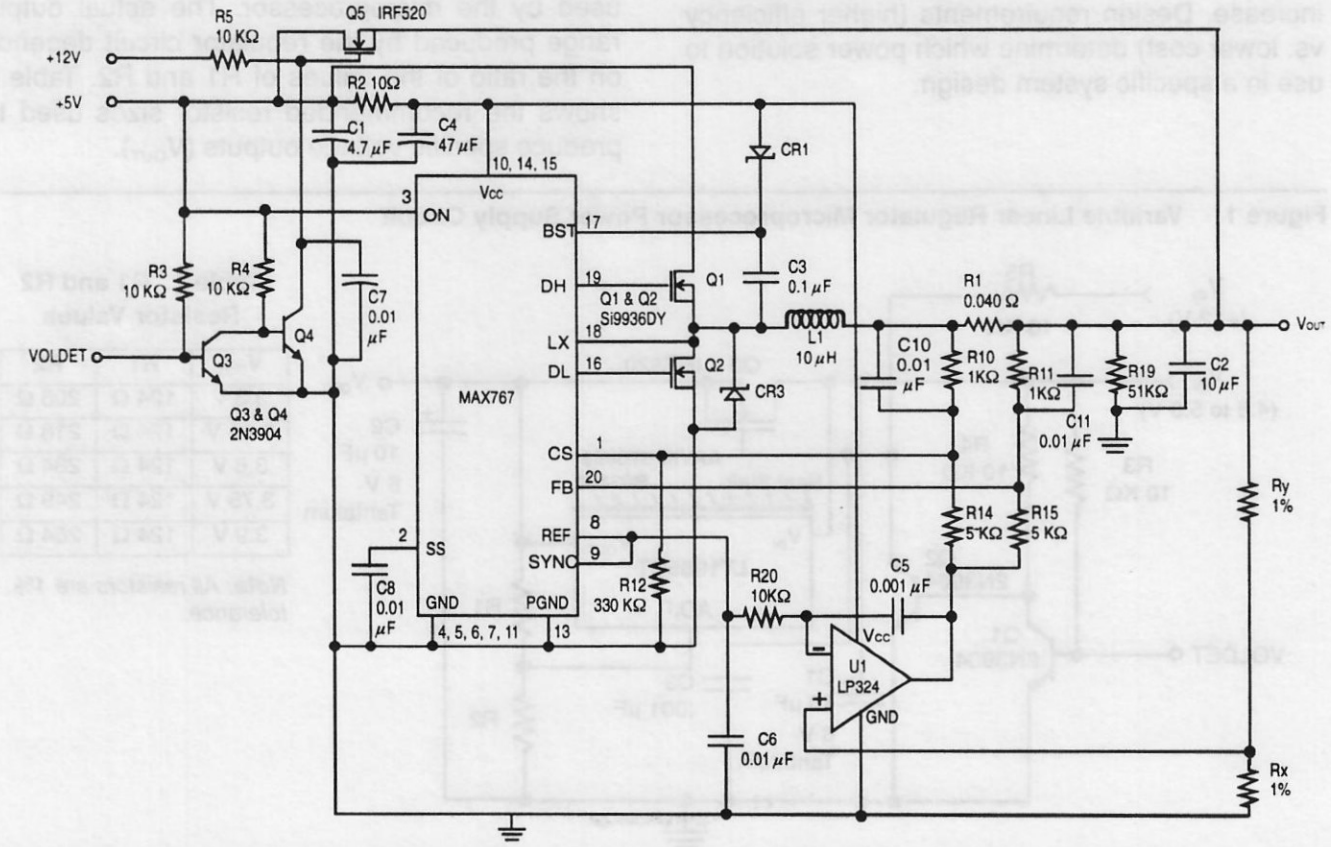


Figure 3 Split Power Plane Example

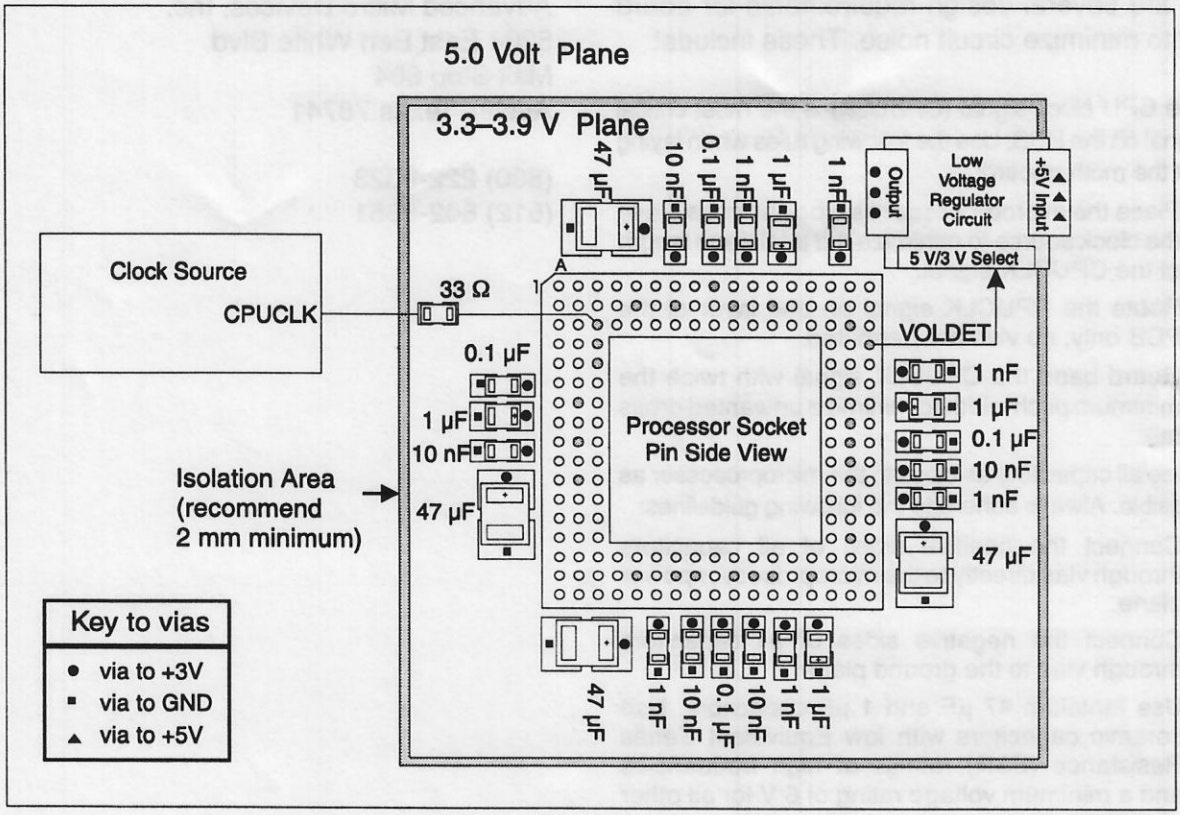
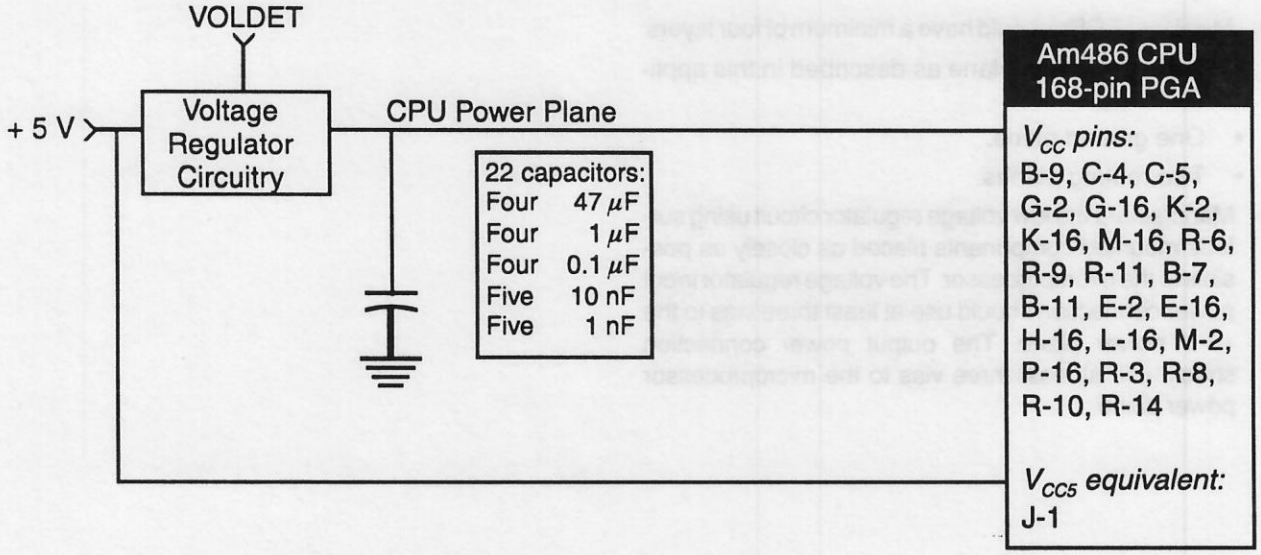


Figure 4 Recommended Decoupling Circuit



There are several design requirements for board layout to minimize circuit noise. These include:

1) The CPU clock signal (CPUCLK) is the most critical signal on the PCB. Use the following rules when laying out the motherboard:
   - Place the microprocessor as close as possible to the clock source to minimize the total trace length of the CPUCLK signal.
   - Route the CPUCLK signal on one layer of the PCB only; no vias are permitted.
   - Guard band the CPUCLK signal with twice the minimum pitch width to minimize unwanted cross talk.
2) Place all capacitors as close to the microprocessor as possible. Always adhere to the following guidelines:
   - Connect the positive sides of all capacitors through vias directly to the microprocessor power plane.
   - Connect the negative sides of all capacitors through vias to the ground plane.
   - Use tantalum 47 µF and 1 µF capacitors. Use ceramic capacitors with low Equivalent Series Resistance (ESR) ratings at high frequencies and a minimum voltage rating of 6 V for all other capacitor values.
   - If possible, position some of the capacitors on the PCB on the inside perimeter of the microprocessor socket to allow for closest placement to the CPU.
3) Multilayer PCBs should have a minimum of four layers:
   - One split power plane as described in this application note.
   - One ground plane.
   - Two routing planes.
4) Manufacture the low voltage regulator circuit using surface mounted components placed as closely as possible to the microprocessor. The voltage regulator input power connection should use at least three vias to the +5-V power plane. The output power connection should use at least three vias to the microprocessor power plane.

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Am486® CPU Thermal Management

Advanced Micro Devices

Application Note

This application note provides thermal management practices using a heat sink/fan combination. The heat sink/fan assembly helps to guardband against systems where the airflow is impacted by the addition of add-in cards or modules that can block the necessary airflow to the CPU.

OVERVIEW

Heat is generated by all semiconductors while operating. Most microprocessors to date have been able to dissipate the heat directly to the ambient air without heat sinks or fans. With faster processors that dissipate more heat than the slower processors, it is no longer possible to ignore thermal management. The objective is to ensure the generated heat is dissipated into the ambient air while a safe operating temperature is maintained.

There are several methods for keeping the processor cool. All of these methods include a combination of heat sink and airflow. In general, the trade-off is heat sink versus airflow. A smaller and less costly heat sink requires more airflow. Analogously, larger heat sinks require less airflow to maintain a safe case temperature.

There are several choices of motherboards and computer cases that manufacturers can use in their assembly. After receiving the system, the end customer can populate the system with a myriad of add-on cards and peripherals; hence, it is extremely difficult to guarantee that the processor will be adequately cooled in all the different combinations of systems.

AMD has researched several products that aid in thermal management design. The product that effectively provides thermal management at a reasonable cost is the heat sink and fan combination. This product consists of a small fan mounted on a heat sink. The fan is powered by the standard power supply and connects via a cable. The heat sink is clipped on or glued to the microprocessor. The heat sink adds between 11/16" to 3/4" of height to the processor. The space above the fan and to the sides of the processor should be cleared to allow for proper airflow. A typical heat sink and fan assembly is shown in Figure 1.

AMD has tested various fan/heat sink devices and found the Thermalloy 2321B-TCM cooling module to provide reliable operation.

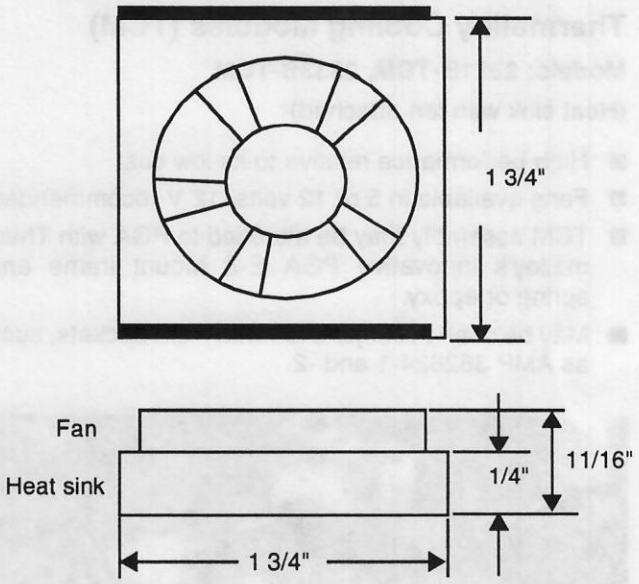

Figure 1. Heat Sink and Fan Assembly

HEAT SINKS AVAILABLE FOR Am486 CPUs

Thermalloy's Heat Sinks

Omnidirectional

Models: 2321B, 2332B, 2333B, 2342B

- 20% greater performance than extruded equivalents
- Heat Sinks may be bonded to the PGA with epoxy or with the PGA E-Z Mount frame (p/n 8317) and spring (p/n PF17)

Publication#18448 Rev: C Amendment/0
Issue Date: November 1994

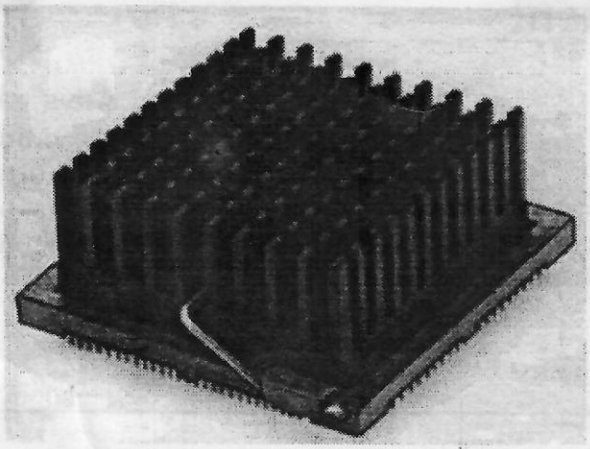

Figure 2. Omnidirectional Heat Sink

Thermalloy Cooling Modules (TCM)

Models: 2321B-TCM, 2333B-TCM

(Heat sink with fan attached)

- High performance relative to its low cost
- Fans available in 5 or 12 volts, 12 V recommended
- TCM assembly may be attached to PGA with Thermalloy's innovative PGA E-Z Mount frame and spring or epoxy.
- May be used in conjunction with PGA sockets, such as AMP 382624-1 and -2.

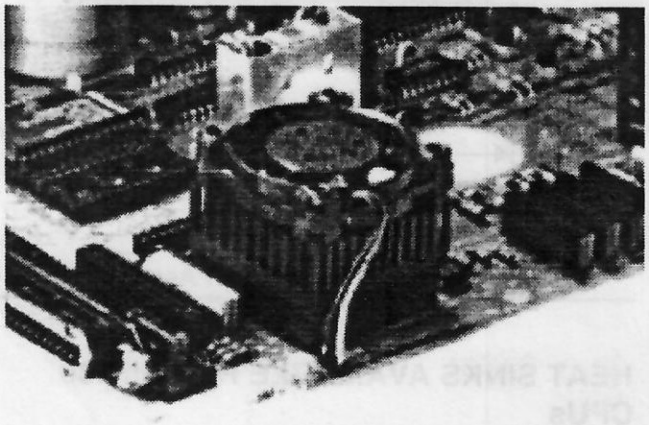

Figure 3. Thermalloy Cooling Module

Notes:

1. *Thermal paste is recommended in order to provide the best heat transfer.*
2. *When applying thermal paste, it should be applied in a thin, smooth even layer across the entire CPU package.*
3. *In **no** circumstance should an air gap exist between the CPU package and the heatsink. If a gap exits, the heatsink will provide little or not heat dissipation and therefore is useless.*

Other Available Heat Sinks

AMP Low Insertion Force PGA Sockets

Models: SCA17-1, SCA17-2

(Heat sink with tabs for spring clips)

- Spring clip (SCA17-x) attaches a Thermalloy pin fin heat sink (23xx series) to PGA in an AMP LIF PGA socket
- Clip easily snaps over the edges of the PGA socket and requires no special tools

AAVID's Heat Sinks

SINK-to-SOCKET Clip Heat Sinks

Models: 3333, 3334, 3335, 3336, 3337

(A clip that attaches the heat sink to an AMP Socket with the CPU in between)

- Removable heat sink and clip with built-in quick release/load latch

SINK-to-PROCESSOR Clip Heat Sinks

Models: 3600, 3331, 3601, 3602, 3603, 3329

(A clip that attaches the heat sink directly to the CPU)

- No keep-clear areas required
- Functions on socket or direct mount CPUs

PGA KLIPS Heat Sinks

(Uses PGA Klips for easy installation)

Bidirectional

Models: 3300, 3301, 3302, 340011

- Low cost heat sink
- Ideal for directional and high airflow patterns

Omnidirectional

Models: 3305, 3306, 3307, 340021

- Utilizes airflow from any direction
- Ideal for impingement airflow patterns

Fan-Sink Heat Sinks

Model 351055

(Heat sink that uses a fan)

- Low profile design
- Shrouded design maximizes cooling capacity

For Further Information Contact:

AAVID Engineering, Inc. U.S.A.: (603) 528-3400

Thermalloy, Inc. U.S.A.: (214) 243-4321
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APPENDIX–Background Information

Thermal Resistance

Thermal characteristics of integrated circuits (IC) have long been a major concern for both electronic product manufacturers and designers. This is because an increase in junction temperature can have an adverse effect on the long term performance and operating life of an IC. With the 486 CPU, for example, squeezing 1.2 million transistors on board and running at faster speeds, more heat is generated which can not be easily vented out of the computer with the usual fans. Unvented, the heat builds up and destroys the transistors. Heat sinks are finding their way into 486 systems but they may not be good enough for future generations of CPUs.

The maximum case temperature of some Am486 CPUs is specified to be 65°C. The cooling module must dissipate the heat into the ambient air, which must be below 65°C. How much lower the ambient temperature must be is given by the thermal resistance times the power. Therefore, to calculate the maximum ambient temperature that the processor with cooling module can operate, the following formula is used:

$$T_{Max-Ambient} = 65 - (P_{Max} \bullet \theta_{CA})$$

The maximum power consumption (P_{Max}) of the Am486 processor, is given as:

$$P_{Max} = 5.35\ [V] \bullet 1200\ [mA] = 6.3\ Watts$$

With unit 1 using the thermal grease, the maximum ambient temperature for safe operation will be:

$$T_{Max-Ambient} = 65 - (6.3 \bullet 3.3) = 44.21°C$$

For comparison, by using the Thermalloy 2321B-TCM, the maximum ambient temperature is:

$$T_{Max-Ambient} = 65 - (6.3 \bullet 1.4) = 56.18°C$$

When a transistor is turned on, power is dissipated equal to the product of the voltage across the collector junction and the current through it. As a result, the collector junction's temperature begins to rise. Eventually, a steady state is reached when the transistor dissipates the same energy supplied to it. This energy is in the form of heat and is given off through the case to the surrounding environment. The temperature depends upon the power level and the thermal resistance of the device package. Thermal resistance is the ability of the package to conduct heat away from the CPU and into the surrounding environment. A low thermal resistance value means that for a given amount of power, the integrated circuit junction will operate at a lower temperature, thereby providing a longer life time.

Several variables affect junction temperature. Some are controlled by the IC vendor, while others are controlled by the user and the environment in which the device is used. With the trend toward higher density circuits, increasing circuit complexity and increasing number of pin outs, total power dissipation is increasing. Hence, management of thermal characteristics remains a valid concern.

Thermal resistance (theta jc (θjc)) is expressed as the rise in the collector junction temperature (Tj) above the case temperature (Tc) per unit of power dissipated (P_d) in the device.

(1) $$\theta jc = (Tj - Tc) / (Pd)$$

Where θjc is expressed in °C/W.

Thermal resistance can also be calculated between junction temperature and ambient temperature (Ta).

(1a) $$\theta ja = (Tj - Ta) / (Pd)$$

Figure 4 illustrates the path of heat flow through a device with and without a heat sink, and Figure 5 shows a schematic representation of the thermal resistance paths between the junction and ambient temperatures.

The temperature of the junction (Tj) is related to the power dissipation and the ambient temperature (Ta) by the following equation:

$$Tj = (Pd \bullet \theta ja) + Ta$$

If a heat sink is applied, the heat passes from the case to the sink before being emitted into the air. The purpose of a heat sink is to increase the effective heat-dissipation area and quickly remove heat from the device, permitting the device to work at higher power levels. The heat sink provides an additional low-thermal resistance path from case to ambient air.

Once a certain case temperature is reached, the maximum power rating drops off linearly as shown in Figure 6. This is called the derating curve. The derating factor (Df) is a measure of how fast the curve drops off (i.e., the slope of the curve). Its units are in W/°C. Derating factor (Df) is the reciprocal of θjc.

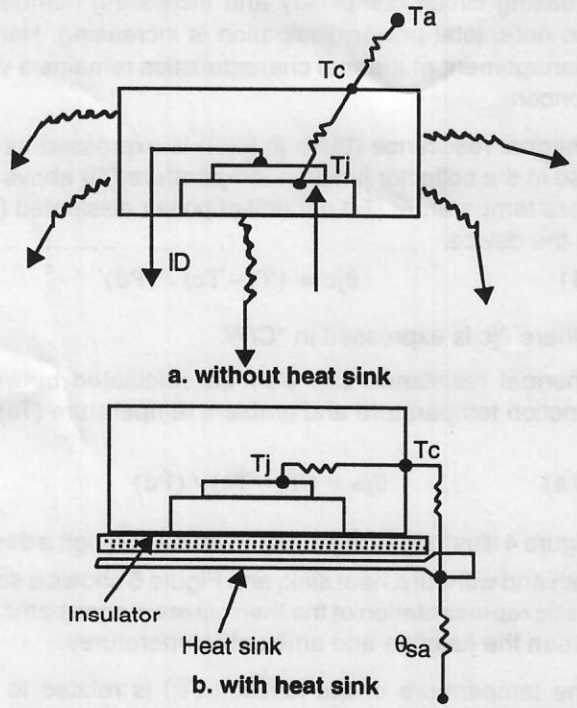
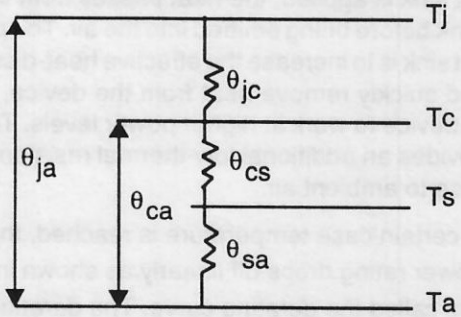


Figure 4. Heat Flow Path



Tj = Junction Temperature
Tc = Case Temperature
Ts = Sink Temperature
Ta = Air Temperature

Without heat sink
$\theta ja = \theta jc + \theta ca$

With heat sink
$\theta ja = \theta jc + \theta cs + \theta ja$

Figure 5. Thermal Resistance Paths (Schematic Representation)

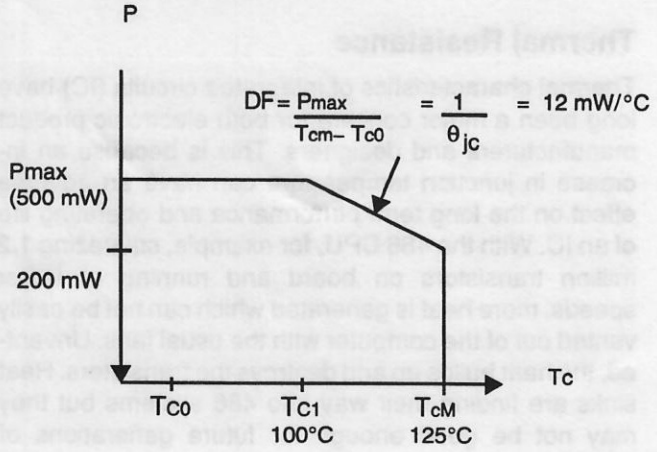


Figure 6. Derating Curve

Heat Transfer

Any discussion of heat transfer should begin with a brief overview of how heat is transferred. There are three mechanisms by which heat may be transferred: convection, radiation, and conduction.

Convection involves the transfer of heat by the mixing of fluid. It is the primary process for heat transfer from a solid to a liquid or gas in contact with it. The rate of convection heat flow is mainly a function of surface area, position of the solid in contact with the fluid, the fluids velocity and properties, and gravity force.

Thermal radiation is heat transferred by electromagnetic radiation. It exists always, but is the only means of heat transfer between entities separated by a vacuum.

Heat transfer by conduction involves the transfer of kinetic energy from one molecule to another. It is the primary mechanism for heat transfer between solids. Conduction heat transfer is governed by Fourier's law.

The thermal resistance equations, 1 and 1a, mentioned previously can be derived using Fourier's law stating that the rate of heat flow (P) through a material is proportional to the cross sectional area (A) of the material normal to the heat flow, the temperature gradient (T) along the thickness (x) of the material, and the thermal conductivity (K), a constant and a basic property of the material. The value of K is in units of W/°C-cm mathematically:

$$(2) \qquad P = KA \bullet (dT/dx) = (kA/x) \bullet (T2 - T1)$$

expressed in units of W/cm^2,

and hence:

$$(3) \qquad T = \theta \bullet P \text{ where } \theta = x/KA$$

Now look at the definition of heat capacity or the time rate of heat flow.

$$P = dQ/dt$$

Where Q is the quantity of heat in calories. Thus, P equals the power dissipation in watts.

$$P = cal/sec = watts$$

Equation 3 shows that:

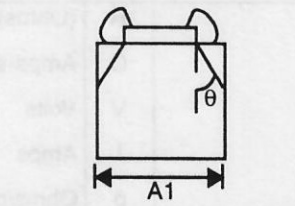
$$\theta = (T2 - T1)/Pd$$

Equation 3 illustrates that thermal resistance is a function of the geometry and thermal conductivity of the device, varying inversely with cross sectional area. Therefore, assuming that larger chip sizes are contained in larger packages, it can be concluded that the larger the device package area, the lower the thermal resistance.

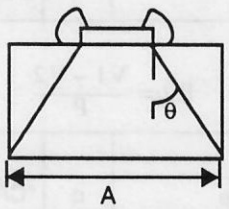
This can also be shown by understanding the concept of thermal spreading. Heat spreads both laterally and vertically through the IC layers, primarily by conduction. A cross sectional view of the die mounted on a substrate package is shown in Figure 7. The spread angle varies for each type of material.

In a small package with restricted thermal spreading, more heat builds up within the package area (i.e., a higher thermal constant). While in a larger package, increasing the area beyond full spreading does not effect the thermal constant because the area normal to the heat flow does not increase.

The graph in Figure 8a shows the relationship between thermal resistance (θ) and the device package area (A). Figure 8b shows the θjc versus the ratio of thickness (X) to the area (A).



Restricted Thermal Spreading



Full Thermal Spreading

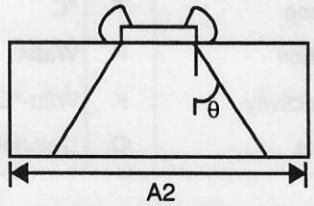
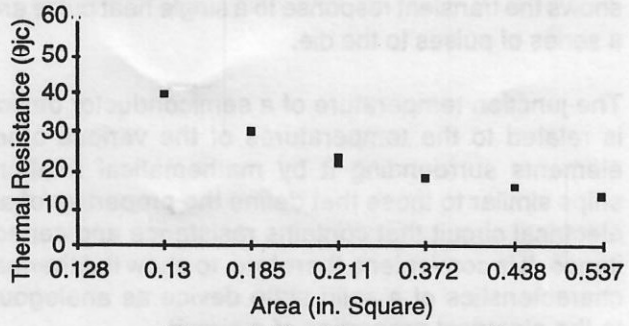
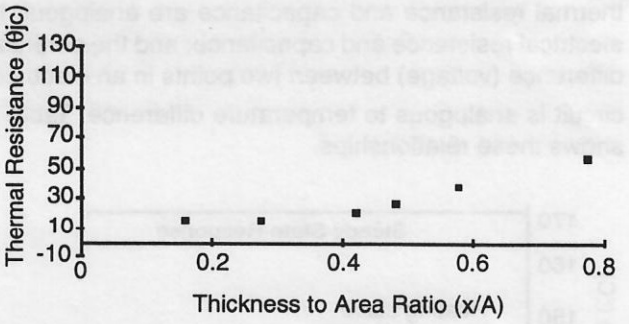


Figure 7. Spread Angles (A1<A<A2)



a. Thermal Resistance versus Area



b. Thermal Resistance versus Thickness

Figure 8. Thermal Resistance Curves

The challenge in computing the thermal resistance of the layers of a packaged device is in finding the boundaries with which to define the area of heat. This is not an easy task because the spread angle of heat varies for each type of material, increasing with larger thermal conductivity. Table 1 shows some spread angles of various materials.

Table 1. Material Spread Angles

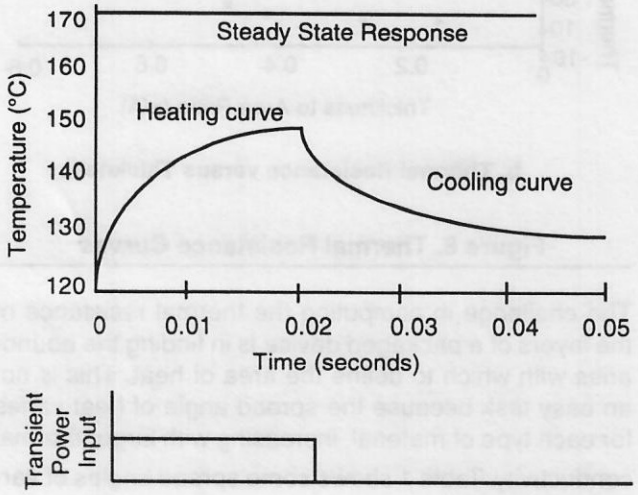
Material	Material Spread Angles
Silicon	40°
BeO	60°
Al2O3	25°
Kovar	25°
Epoxy	0°
Eutectic	0°
Copper	70°
Aluminum	65°

The model thus far has provided a means for predicting thermal conditions for a constant power input. In the case of a transient response to a pulse input of power, or a series of pulses, thermal capacitance is introduced. When the die is subjected to a short pulse of power, the layers below act as a thermal capacitor, absorbing and storing the thermal energy. Upon termination of the pulse, the die cools and the thermal energy is dissipated

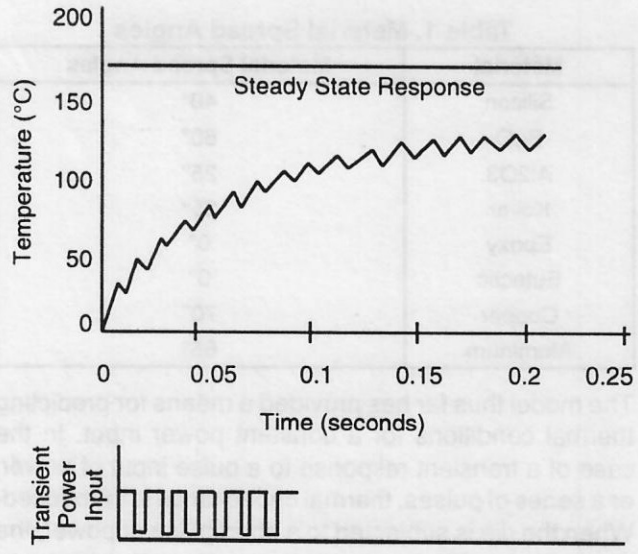
through the layers to the case of the device. Figure 9 shows the transient response to a single heat pulse and a series of pulses to the die.

The junction temperature of a semiconductor device is related to the temperatures of the various other elements surrounding it by mathematical relationships similar to those that define the properties of an electrical circuit that contains resistance and capacitance. It is convenient, therefore, to show the thermal characteristics of a solid state device as analogous to the electrical properties of a circuit.

The flow of heat is analogous to the flow of charge; thermal resistance and capacitance are analogous to electrical resistance and capacitance; and the potential difference (voltage) between two points in an electrical circuit is analogous to temperature difference. Table 2 shows these relationships.



a. 20-ms Heat Pulse



b. 9-ms Square Pulse with a 12-ms period

Figure 9. Transient Responses

Table 2. Comparison of Electrical Parameters to Analogous Thermal Parameters

Electrical		
Resistance	R	(Ohms)
Capacitance	C	Amps-sec/V
Voltage	V	Volts
Current	I	Amps
Conductivity	p	Ohms/cm^2
Charge	q	Coulomb
$R2 = \frac{V1 - V2}{P}$		
Thermal		
Thermal resistance	q	°C/W
Thermal capacitance	C	W-sec/°C
Temp. difference	T	°C
Power dissipation	P	Watts
Thermal conductivity	K	W/in-°C
Quantity of heat	Q	Calories
$\theta 2 = \frac{T1 - T2}{P}$		

Table 3. Comparison of Electrical Parameters to Analogous Thermal Parameter

Electrical		
Resistance	R	(Ohms)
Capacitance	C	Amps-sec/V
Voltage	V	Volts
Current	I	Amps
Conductivity	p	Ohms/cm^2
Charge	q	Coulomb
$R2 = \frac{V1 - V2}{P}$		
Thermal		
Thermal resistance	q	°C/W
Thermal capacitance	C	W-sec/°C
Temp. difference	T	°C
Power dissipation	P	Watts
Thermal conductivity	K	W/in-°C
Quantity of heat	Q	Calories
$\theta 2 = \frac{T1 - T2}{P}$		

Table 4. Comparison of Electrical Parameters to Analogous Thermal Parameters

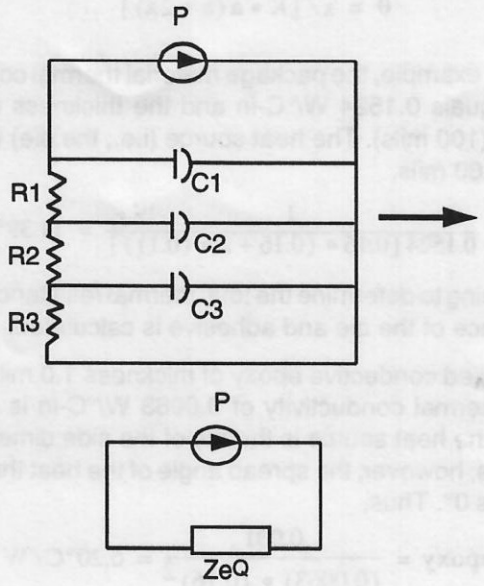
Electrical		
Resistance	R	(Ohms)
Capacitance	C	Amps-sec/V
Voltage	V	Volts
Current	I	Amps
Conductivity	p	Ohms/cm^2
Charge	q	Coulomb
$R2 = \frac{V1 - V2}{P}$		
Thermal		
Thermal resistance	q	°C/W
Thermal capacitance	C	W-sec/°C
Temp. difference	T	°C
Power dissipation	P	Watts
Thermal conductivity	K	W/in-°C
Quantity of heat	Q	Calories
$\theta 2 = \frac{T1 - T2}{P}$		

Thermal capacitance is equal to the product of the specific heat (H) of the material used in the sample and the Mass (M) of the sample; it is the quantity of heat absorbed by the sample when its temperature rises 1°C. Therefore, if a sample absorbs a quantity of heat (Q) when its temperature is increased from T1 to T2, the thermal capacitance of the sample, expressed in watt-seconds per °C, can be determined from the following equation:

$$C = \frac{Q}{T2 - T1}$$

Figure 10 shows the electro-thermal circuit for a three layer device. Thermal impedance, like electrical impedance, is a complex variable because of the time dependence associated with the thermal capacitance. In this circuit, the thermal resistances closest to the heat source are large because the cross section of the semiconductor is small (all the heat flows through a small area). Thermal resistance varies inversely with cross sectional area (as shown in equation 3). Thermal resistance becomes progressively smaller as distance from the semiconductor increases.

Since thermal capacitance varies directly with both specific heat and mass, the small mass of the semiconductor causes the thermal capacitance to be smallest at the heat source and to become pressively larger as distance from the heat source increases. The final thermal capacitance in the series is considered an infinite capacitance, which is electrically equivalent to a short across the end of the line



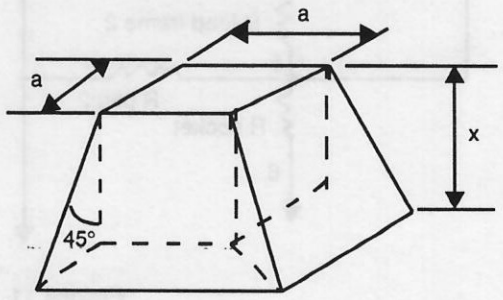
R = x/KA
C = p • c • v
p = density
c = heat capacity
v = volume

Figure 10. Electrothermal Circuit for a Three Layer Device

To simplify the equation, assume a steady state condition where capacitance does not play a role. Thus, for a three layer device (die, epoxy, and package), total thermal resistance equals three resistances in a series.

$$R_{die} + R_{epoxy} + R_{package}$$

Consider a square heat source of side dimension 'a' in contact with a package of thickness'x'. For simplicity, assume that the thermal spread angle of the material is 45°. Thus, the area is the truncated pyramid and theta is calculated by the following equation:



$$\theta = (1/K)\int dx/area \qquad area = f(x)$$

and therefore:

$$\theta = x/[K \bullet a(a+2x)]$$

For this example, the package material thermal conductivity equals 0.1524 W/°C-in and the thickness of 0.1 inches (100 mils). The heat source (i.e., the die) is 160 mils x 160 mils.

$$\theta pkg = \frac{1}{0.1524\,[0.16 \bullet (0.16+2 \bullet (0.1))]} = 11.39°C/W$$

Continuing to determine the total thermal resistance, the resistance of the die and adhesive is calculated.

Silver-filled conductive epoxy of thickness 1.0 mil, having a thermal conductivity of 0.0063 W/°C-in is used. Again, the heat source is the die of the side dimension 160 mils; however, the spread angle of the heat through epoxy is 0°. Thus,

$$\theta epoxy = \frac{0.001}{(0.0063) \bullet (0.16)^2} = 6.20°C/W$$

The thermal conductivity of silicon is 3.27 W/°C-in; die thickness is 20 mils and the heat source is the sum of the collector junction region totaling a dimension of approximately 10 mils.

$$\theta die = \frac{0.02}{3.27\,[(0.01) \bullet (0.01+2 \bullet (0.02))]} = 12.23°C/W$$

Therefore:

$$\theta_{die} + \theta_{epoxy} + \theta_{pkg}$$
$$= 12.23°C/W + 6.20°C/W + 11.39°C/W$$
$$\theta total = 29.82°C/W$$

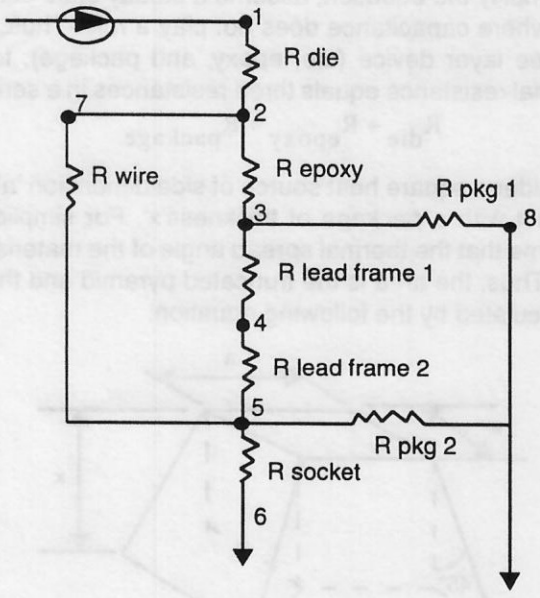
A more accurate calculation of θjc would also include the lead frame and wire bonding thermal resistances as described in Figure 11.

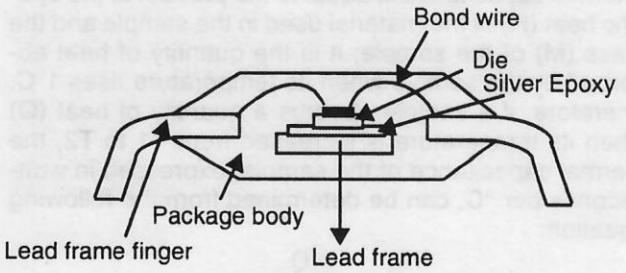
The graphs in Figure 12 illustrate how thermal resistance varies with package area and die size. All values were calculated as described above using the dimensions of LCC packages and associated die.

Thermal Properties of Materials

Several factors effect the thermal resistance of an IC package. Package variables include leadframe material and construction, case material and construction, and die attach method and material.

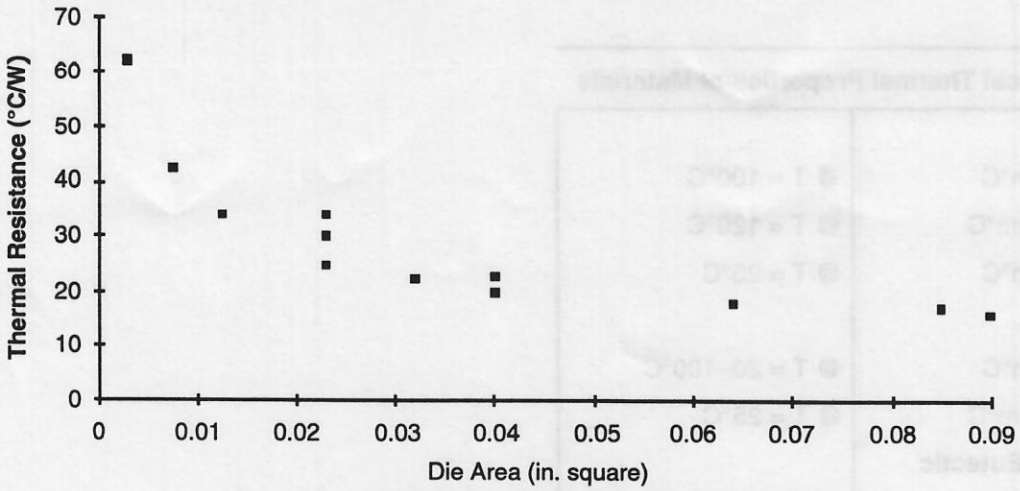
Accurate information on thermal properties of materials is not readily available. The thermal conductivity of ceramics, for example, is dependent on the purity of the material, and that of silicon dependent on temperature



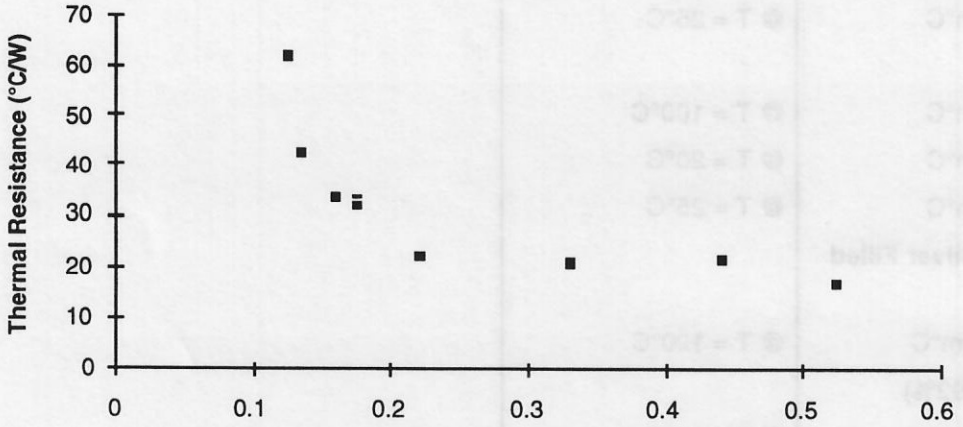


Nodes:
1. collector junction
2. within die under junction
3. lead frame surface
4. lead frame periphery
5. lead frame finger
6. ambient
7. bond pads
8. package bosy

Figure 11. Total Thermal Resistance



a. for various die sizes



b. for various packages

Figure 12. Calculated Thermal Resistance

Table 5 lists several materials and their thermal conductivity.

Table 5. Typical Thermal Properties of Materials

Silicon	
K = 1.05 W/cm°C	@ T = 100°C
K = 0.976 W/cm°C	@ T = 120°C
K = 1.29 W/cm°C	@ T = 25°C
Kovar	
K = 0.21 W/cm°C	@ T = 20–100°C
K = 0.134 W/cm°C	@ T = 25°C
Gold-Silicon Eutectic	
K = 2.96 W/cm°C	@ T = 25°C
K = 2.16 W/cm°C	@ T = 25°C
Beryllia	
K = 1.54 W/cm°C	@ T = 100°C
K = 2.05 W/cm°C	@ T = 20°C
K = 2.54 W/cm°C	@ T = 25°C
Conductive Silver Filled Epoxy	
K = 0.016 W/cm°C	@ T = 120°C
Alumina (90–92%)	
K = 0.06 W/cm°C	@ T = 25°C
K = 0.07 W/cm°C	@ T = 100°C
Solder	
K = 0.492 W/cm°C	@ T = 25°C
Sapphire	
K = 0.033 W/cm°C	@ T = 38°C
K = 0.026 W/cm°C	@ T = 93°C
K = 0.023 W/cm°C	@ T = 149°C

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