Am386™SXL

High-Performance, Low-Power, 32-Bit Microprocessor with 16-Bit Data Bus

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **25- and 20-MHz operating speeds**
- **True static design for long battery life in portable PCs**
  - —0 MHz (DC) minimum frequency
  - —Typical standby (DC) current < 0.08 mA
  - —Typical operating current < 165 mA at 20 MHz
  - —Wide range of chip set and BIOS support take advantage of standby mode capabilities
- **Lower heat dissipation facilitates elimination of cooling fan in desktop PCs**
- **Compatible with 386SX systems and software**
- **Pin-for-pin replacement of the Intel i386SX**
- **Supports 387SX-compatible math coprocessors**
- **100-pin PQFP package with optional protective ring for better lead coplanarity**
- **Advanced 0.8 micron CMOS technology**

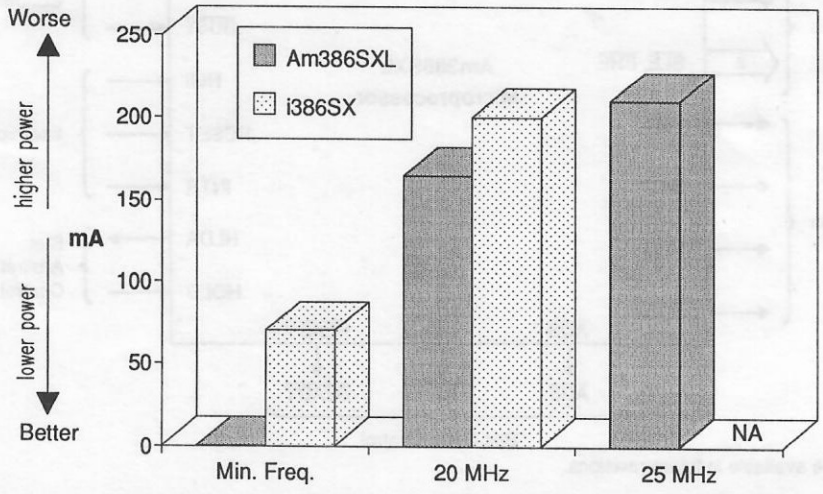
GENERAL DESCRIPTION

The Am386SXL microprocessor is a high-speed, true static implementation of the Intel i386SX. It is ideal for both desktop and battery-powered notebook personal computers. For notebooks, the Am386SXL microprocessor's true static design offers longer battery life with low operating power consumption and standby mode. At 20 MHz, this device offers a current which is 22% lower than the Intel i386SX. Standby mode allows the Am386SXL microprocessor to be clocked down to 0 MHz (DC) and retain full register contents. Typical current in standby mode is reduced to less than 0.08 mA—nearly a 1000× reduction in power consumption versus the Intel i386SX.

For desktop PCs, the Am386SXL microprocessor offers a 25% increase in the maximum operating speed, from 20 to 25 MHz. Also, this device offers lower heat dissipation, allowing system designers to remove or reduce the size and cost of the cooling fan.

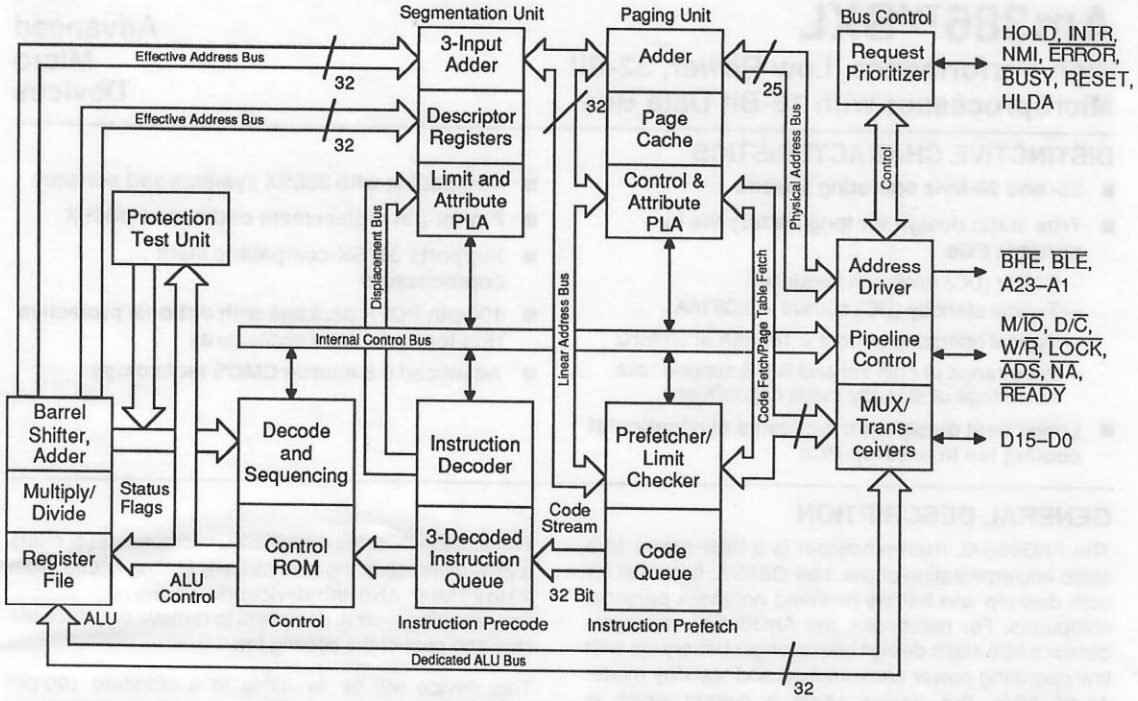
This device will be available in a standard 100-pin plastic quad flat pack (PQFP). This package may be shipped in an optional protective ring for better lead protection during manufacturing.

Typical Icc



Publication #: 15574 Rev. A Amendment: /0
Issue Date: March 1991

BLOCK DIAGRAM



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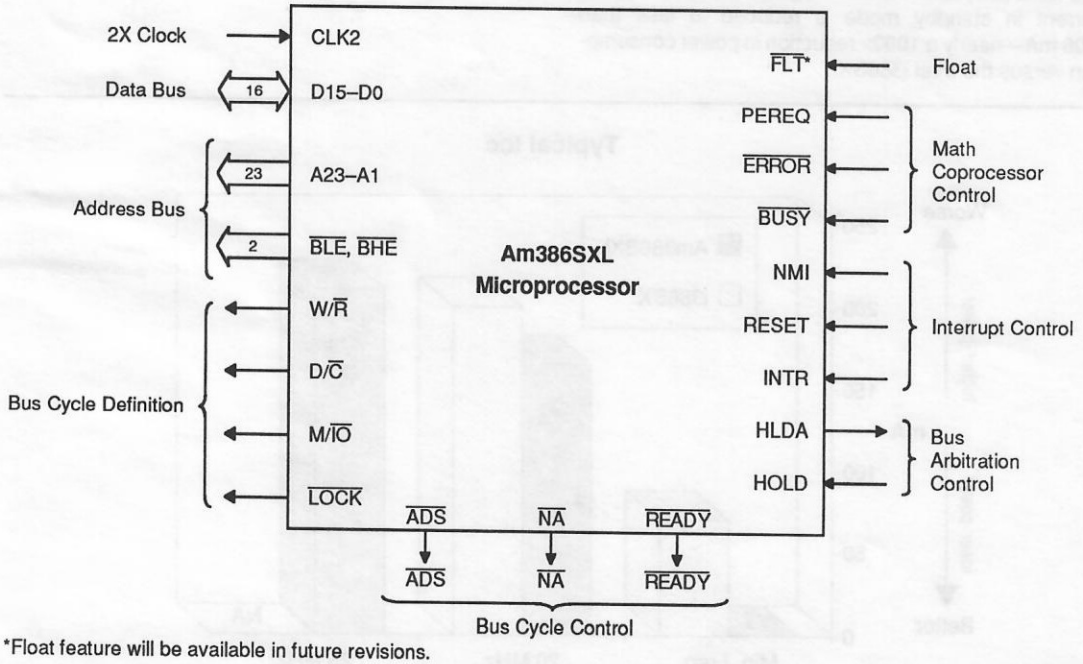
LOGIC SYMBOL



*Float feature will be available in future revisions.

15022B–003

FUNCTIONAL DESCRIPTION

True Static Operation

The Am386SXL microprocessor incorporates a true static design. Unlike dynamic circuit design, the Am386SXL microprocessor eliminates the minimum operating frequency restriction. It may be clocked from its maximum speed of 25 MHz all the way down to 0 MHz (DC). System designers can use this feature to design battery-powered notebook PCs with long battery life.

Standby Mode

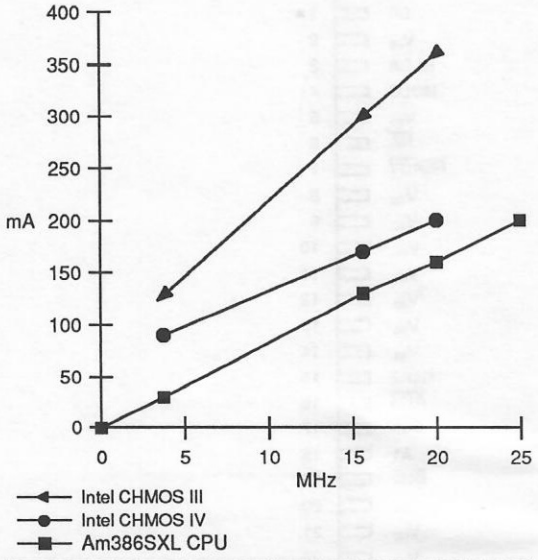
This true static design allows for a standby mode. At any operating speed (25 to 0 MHz), the Am386SXL microprocessor will retain its state (i.e., the contents of all its registers). By shutting off the clock completely, the device enters standby mode. Since power consumption is proportional to clock frequency, operating power consumption is reduced as the frequency is lowered. In standby mode, typical current draw is reduced to less than 0.08 mA at DC.

Not only does this feature improve battery life, but it also simplifies the design of power-conscious notebook computers in the following ways:

1. Eliminates the need for software in the BIOS to save and restore the contents of registers.
2. Allows simpler circuitry to control stopping of the clock since the system does not need to know what state the processor is in.

Lower Operating I_{CC}

True static design also allows lower operating I_{CC} when operating at any speed. See the following graph for typical current at operating speeds.



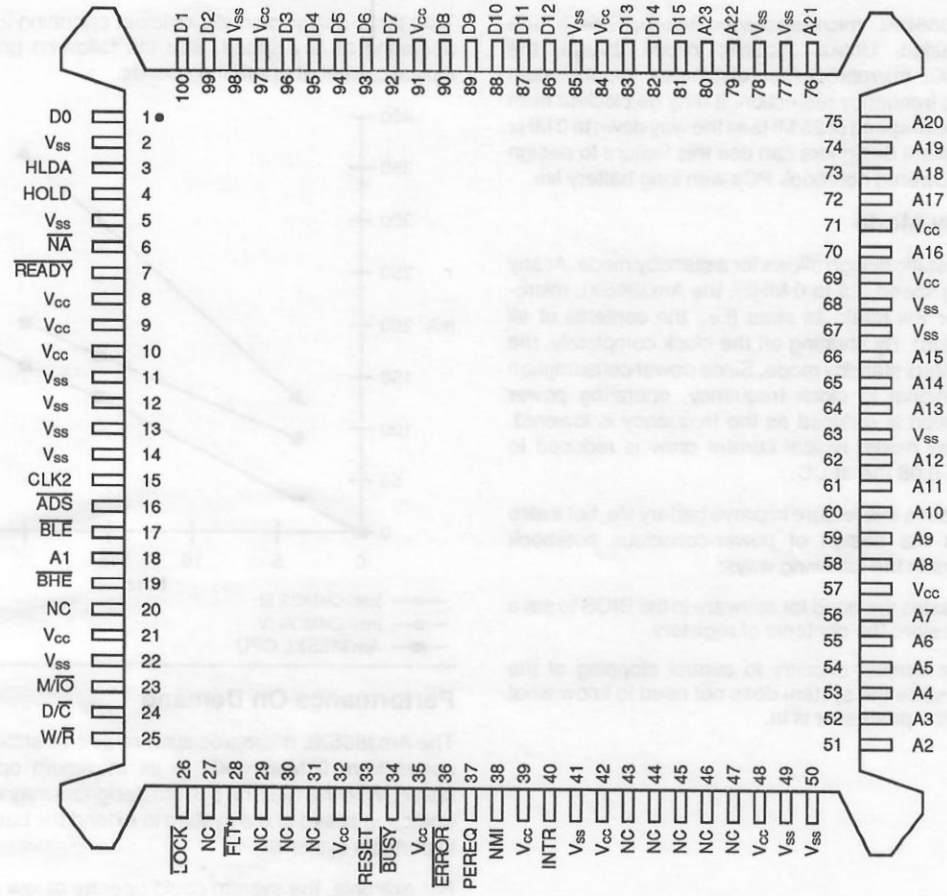
Performance On Demand

The Am386SXL microprocessor retains its state at any speed from 0 MHz (DC) to its maximum operating speed. With this feature, system designers may vary the operating speed of the system to extend the battery life in portable systems.

For example, the system could operate at low speeds during inactivity or polling operations. However, upon interrupt, the system clock can be increased up to its maximum speed. After a user-defined time-out period, the system can be returned to a low (or 0 MHz) operating speed without losing its state. This design maximizes battery life while achieving optimal performance.

CONNECTION DIAGRAM

Top View



Notes: NC = No Connect.
Pin 1 is marked for orientation.
*Float feature will be available in future revisions.

15022B–002

PIN DESIGNATIONS (Sorted by Pin Name)

Address		Data		Control		NC	V_{CC}	V_{SS}
Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin No.	Pin No.	Pin No.
A1	18	D0	1	$\overline{ADS}$	16	20	8	2
A2	51	D1	100	$\overline{BHE}$	19	27	9	5
A3	52	D2	99	$\overline{BLE}$	17	29	10	11
A4	53	D3	96	$\overline{BUSY}$	34	30	21	12
A5	54	D4	95	CLK2	15	31	32	13
A6	55	D5	94	D/$\overline{C}$	24	43	39	14
A7	56	D6	93	$\overline{ERROR}$	36	44	42	22
A8	58	D7	92	$\overline{FLT}$*	28	45	48	35
A9	59	D8	90	HLDA	3	46	57	41
A10	60	D9	89	HOLD	4	47	69	49
A11	61	D10	88	INTR	40		71	50
A12	62	D11	87	$\overline{LOCK}$	26		84	63
A13	64	D12	86	M/$\overline{IO}$	23		91	67
A14	65	D13	83	$\overline{NA}$	6		97	68
A15	66	D14	82	NMI	38			77
A16	70	D15	81	PEREQ	37			78
A17	72			$\overline{READY}$	7			85
A18	73			RESET	33			98
A19	74			W/$\overline{R}$	25			
A20	75							
A21	76							
A22	79							
A23	80							

PIN DESIGNATIONS (Sorted by Pin Number)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	D0	21	V_{CC}	41	V_{SS}	61	A11	81	D15
2	V_{SS}	22	V_{SS}	42	V_{CC}	62	A12	82	D14
3	HLDA	23	M/$\overline{IO}$	43	NC	63	V_{SS}	83	D13
4	HOLD	24	D/$\overline{C}$	44	NC	64	A13	84	V_{CC}
5	V_{SS}	25	W/$\overline{R}$	45	NC	65	A14	85	V_{SS}
6	$\overline{NA}$	26	$\overline{LOCK}$	46	NC	66	A15	86	D12
7	$\overline{READY}$	27	NC	47	NC	67	V_{SS}	87	D11
8	V_{CC}	28	$\overline{FLT}$*	48	V_{CC}	68	V_{SS}	88	D10
9	V_{CC}	29	NC	49	V_{SS}	69	V_{CC}	89	D9
10	V_{CC}	30	NC	50	V_{SS}	70	A16	90	D8
11	V_{SS}	31	NC	51	A2	71	V_{CC}	91	V_{CC}
12	V_{SS}	32	V_{CC}	52	A3	72	A17	92	D7
13	V_{SS}	33	RESET	53	A4	73	A18	93	D6
14	V_{SS}	34	$\overline{BUSY}$	54	A5	74	A19	94	D5
15	CLK2	35	V_{SS}	55	A6	75	A20	95	D4
16	$\overline{ADS}$	36	$\overline{ERROR}$	56	A7	76	A21	96	D3
17	$\overline{BLE}$	37	PEREQ	57	V_{CC}	77	V_{SS}	97	V_{CC}
18	A1	38	NMI	58	A8	78	V_{SS}	98	V_{SS}
19	$\overline{BHE}$	39	V_{CC}	59	A9	79	A22	99	D2
20	NC	40	INTR	60	A10	80	A23	100	D1

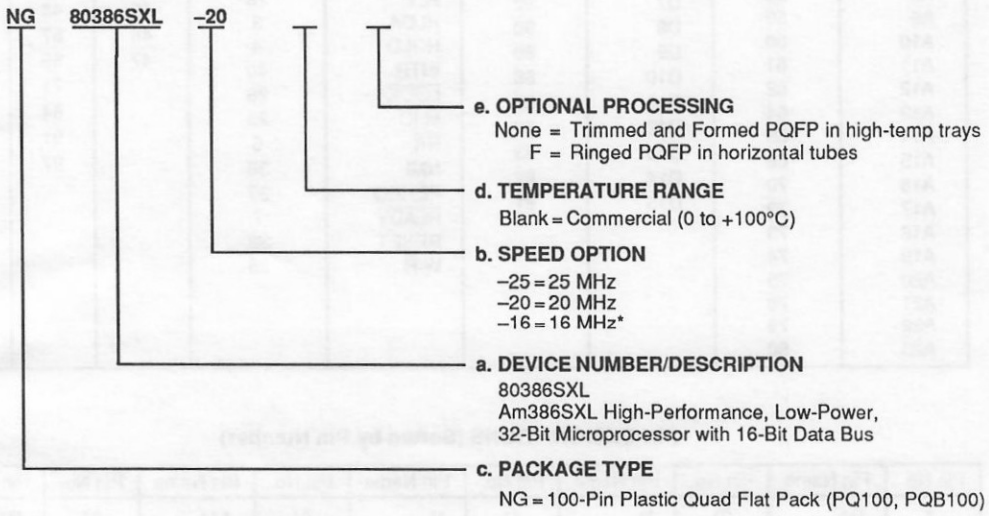
*Float feature will be available in future revisions.

ORDERING INFORMATION

Standard Products

AMD® standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number/Description
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations		
NG	80386SXL	–25 –20 –16* –25F –20F –16F*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

*Contact AMD for 16 MHz availability.

PIN DESCRIPTION

A23–A1
Address Bus (Outputs)

Outputs physical memory or port I/O addresses.

$\overline{ADS}$
Address Status (Active Low; Output)

Indicates that a valid bus cycle definition and address (W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{BHE}$, $\overline{BLE}$, and A23–A1) are being driven at the Am386SXL microprocessor pins.

$\overline{BHE}$, $\overline{BLE}$
Byte Enables (Active Low; Outputs)

Indicate which data bytes of the data bus take part in a bus cycle.

$\overline{BUSY}$
Busy (Active Low; Input)

Signals a busy condition from a processor extension.

CLK2
CLK2 (Input)

Provides the fundamental timing for the Am386SXL microprocessor.

D15–D0
Data Bus (Inputs/Outputs)

Inputs data during memory, I/O, and interrupt acknowledge read cycles; outputs data during memory and I/O write cycles.

D/$\overline{C}$
Data/Control (Output)

A bus cycle definition pin that distinguishes data cycles, either memory or I/O, from control cycles which are: interrupt acknowledge, halt, and code fetch.

$\overline{ERROR}$
Error (Active Low; Input)

Signals an error condition from a processor extension.

$\overline{FLT}$*
Float (Active Low; Input)

An input which forces all bi-directional and output signals, including HLDA, to the three-state condition.

HLDA
Bus Hold Acknowledge (Active High; Output)

Output indicates that the Am386SXL microprocessor has surrendered control of its logical bus to another bus master.

HOLD
Bus Hold Request (Active High; Input)

Input allows another bus master to request control of the local bus.

INTR
Interrupt Request (Active High; Input)

A maskable input that signals the Am386SXL microprocessor to suspend execution of the current program and execute an interrupt acknowledge function.

$\overline{LOCK}$
Bus Lock (Active Low; Output)

A bus cycle definition pin that indicates that other system bus masters are not to gain control of the system bus while it is active.

M/$\overline{IO}$
Memory/IO (Output)

A bus cycle definition pin that distinguishes memory cycles from input/output cycles.

$\overline{NA}$
Next Address (Active Low; Input)

Used to request address pipelining.

NC
No Connect

Should always be left unconnected. Connection of a NC pin may cause the processor to malfunction or be incompatible with future steppings of the Am386SXL microprocessor.

NMI
Non-Maskable Interrupt Request (Active High; Input)

A non-maskable input that signals the Am386SXL microprocessor to suspend execution of the current program and execute an interrupt acknowledge function.

PEREQ
Processor Extension Request (Active High; Input)

Indicates that the processor has data to be transferred by the Am386SXL microprocessor.

$\overline{READY}$
Bus Ready (Active Low; Input)

Terminates the bus cycle.

*Float feature will be available in future revisions.

RESET

Reset (Active High; Input)

Suspends any operation in progress and places the Am386SXL microprocessor in a known reset state.

V_{cc}

System Power (Active High; Input)

Provides the +5 V nominal DC supply input.

V_{ss}

System Ground (Input)

Provides the 0 V connection from which all inputs and outputs are measured.

$W/\overline{R}$

Write/Read (Output)

A bus cycle definition pin that distinguishes write cycles from read cycles.

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under bias . . . . . –65 to 110°C
Storage Temperature . . . . . –65 to 150°C

Stresses above those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGES

Supply Voltage with respect to V_{SS} . . . –0.5 V to 6.5 V
Voltage on other pins . . . . . –0.5 V to (V_{CC} + 0.5)V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

V_{CC} = 5 V ±10%; T_{CASE} = 0°C to 100°C

Symbol	Parameter Description	Notes	Min	Max	Unit
V_{IL}	Input Low Voltage		–0.3	+0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}+0.3	V
V_{ILC}	CLK2 Input Low Voltage		–0.3	+0.8	V
V_{IHC}	CLK2 Input High Voltage		V_{CC}–0.8	V_{CC}+0.3	V
V_{OL}	Output Low Voltage I_{OL} = 4 mA: A23–A1, D15–D0 I_{OL} = 5 mA: $\overline{BHE}$, $\overline{BLE}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, HLDA			0.45 0.45	V V
V_{OH}	Output High Voltage I_{OH} = 1.0 mA: A23–A1, D15–D0 I_{OH} = 0.2 mA: A23–A1, D15–D0 I_{OH} = 0.9 mA: $\overline{BHE}$, $\overline{BLE}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, HLDA I_{OH} = 0.18 mA: $\overline{BHE}$, $\overline{BLE}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, HLDA		 2.4 V_{CC}–0.5 2.4 V_{CC}–0.5		 V V V
I_{LI}	Input Leakage Current (for all pins except PEREQ, $\overline{BUSY}$, $\overline{FLT}$*, and $\overline{ERROR}$)	0 V ≤ V_{IN} ≤ V_{CC}		±15	µA
I_{IH}	Input Leakage Current (PEREQ pin)	V_{IH} = 2.4 V (Note 1)		200	µA
I_{IL}	Input Leakage Current ($\overline{BUSY}$, $\overline{ERROR}$, and $\overline{FLT}$* pins)	V_{IL} = 0.45 V (Note 2)		–400	µA
I_{LO}	Output Leakage Current	0.45 V ≤ V_{OUT} ≤ V_{CC}		±15	µA
I_{CC}	Supply Current CLK2 = 32 MHz: with –16** CLK2 = 40 MHz: with –20 CLK2 = 50 MHz: with –25	(Note 4) I_{CC} Typ = 135 mA (Note 3) I_{CC} Typ = 165 mA (Note 3) I_{CC} Typ = 210 mA (Note 3)		 160 200 250	 mA mA mA
I_{CCSB}	Standby Current	I_{CCSB} Typ = 0.08 mA (Note 5)		1	mA
C_{IN}	Input Capacitance	F_C = 1 MHz (Note 4)		10	pF
C_{OUT}	Output or I/O Capacitance	F_C = 1 MHz (Note 4)		12	pF
C_{CLK}	CLK2 Capacitance	F_C = 1 MHz (Note 4)		20	pF

Notes: Tested at the minimum operating frequency of the part.
*Float feature will be available in future revisions.
**Contact AMD for 16 MHz availability.

1. PEREQ input has an internal pull-down resistor.
2. $\overline{BUSY}$, $\overline{FLT}$*, and $\overline{ERROR}$ inputs each have an internal pull-up resistor.
3. I_{CC} Max measurement at worst case frequency, V_{CC}, and temperature, outputs unloaded.
4. Not 100% tested.
5. Inputs at rails, outputs unloaded, PEREQ Low, $\overline{ERROR}$ High, $\overline{BUSY}$ High, and $\overline{FLT}$* High.

SWITCHING CHARACTERISTICS

The switching characteristics given consist of output delays, input setup requirements, and input hold requirements. All switching characteristics are relative to the CLK2 rising edge crossing the 2.0 V level.

Switching characteristic measurement is defined by Figure 1. Inputs must be driven to the voltage levels indicated by Figure 1 when switching characteristics are measured. Output delays are specified with minimum and maximum limits measured, as shown. The minimum delay times are hold times provided to external circuitry. Input setup and hold times are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct operation.

Outputs $\overline{NA}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{BHE}$, $\overline{BLE}$, A23–A1, and HLDA only change at the beginning of phase one. D15–D0 (write cycles) only change at the beginning of phase two. The $\overline{READY}$, HOLD, $\overline{BUSY}$, $\overline{ERROR}$, PEREQ, $\overline{FLT}$*, and D15–D0 (read cycles) inputs are sampled at the beginning of phase one. The $\overline{NA}$, INTR, and NMI inputs are sampled at the beginning of phase two.

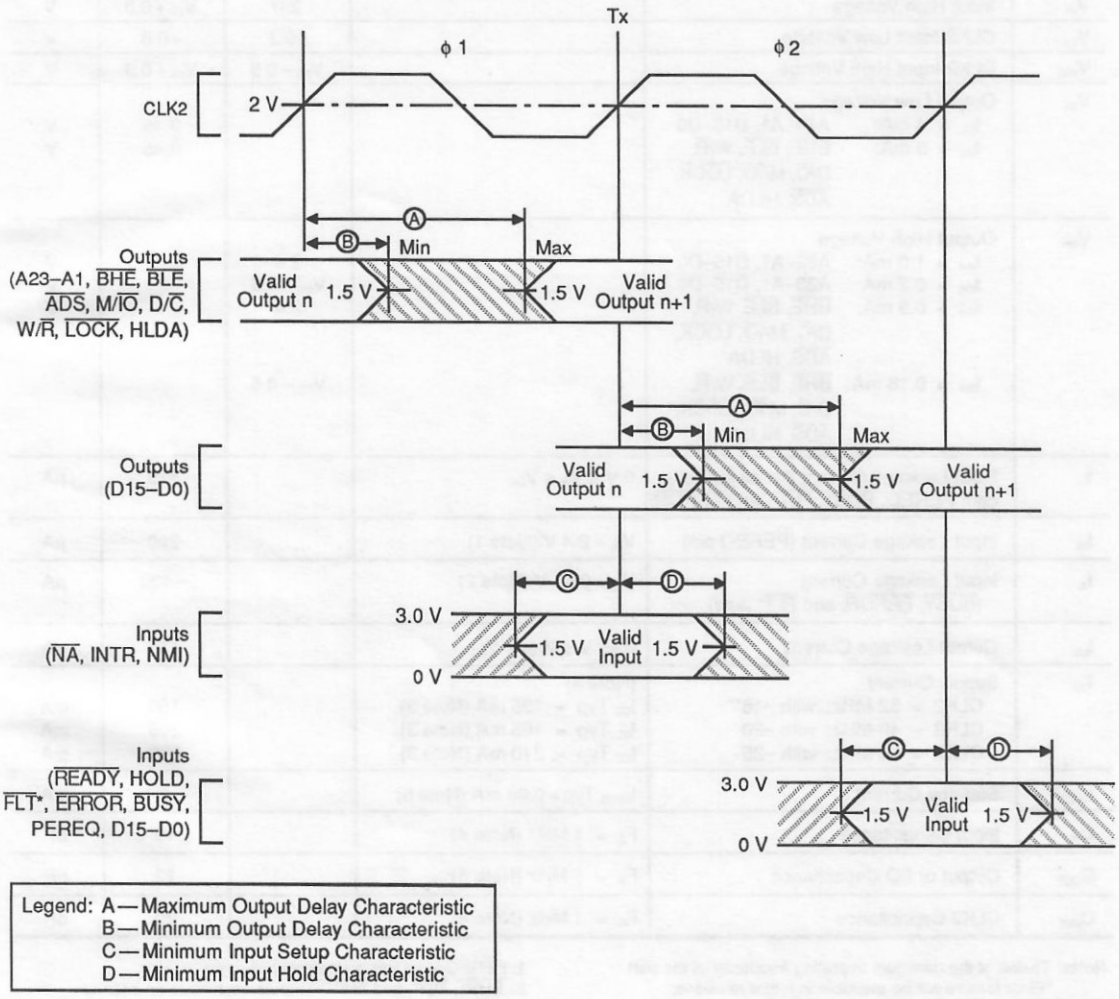


Figure 1. Drive Levels and Measurement Points for Switching Characteristics

*Float feature will be available in future revisions.

SWITCHING CHARACTERISTICS

Switching Characteristics at 25 MHz: V_{CC} = 5 V±10%; T_{CASE} = 0°C to 100°C

Symbol	Parameter Description	Notes	Ref. Figure	Min	Max	Unit
	Operating Frequency	Half CLK2 freq.		0	25	MHz
1	CLK2 Period		2	20		ns
2a	CLK2 High Time	at 2 V (Note 3)	2	7		ns
2b	CLK2 High Time	at (V_{CC}–0.8 V) (Note 3)	2	4		ns
3a	CLK2 Low Time	at 2 V (Note 3)	2	7		ns
3b	CLK2 Low Time	at 0.8 V (Note 3)	2	5		ns
4	CLK2 Fall Time	(V_{CC}–0.8 V) to 0.8 V (Note 3)	2		7	ns
5	CLK2 Rise Time	0.8 V to (V_{CC}–0.8 V) (Note 3)	2		7	ns
6	A23–A1 Valid Delay	C_L = 50 pF	5	4	21	ns
7	A23–A1 Float Delay	(Note 1)	6	4	30	ns
8	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ Valid Delay	C_L = 50 pF	5	4	21	ns
9	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ Float Delay	(Note 1)	6	4	30	ns
10	M/$\overline{IO}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$ Valid Delay	C_L = 50 pF	5	4	21	ns
11	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{ADS}$ Float Delay	(Note 1)	6	4	30	ns
12	D15–D0 Write Data Valid Delay	C_L = 50 pF	5	7	27	ns
12a	D15–D0 Write Data Hold Time	C_L = 50 pF		2		ns
13	D15–D0 Write Data Float Delay	(Note 1)	6	4	22	ns
14	HLDA Valid Delay	C_L = 50 pF	5	4	22	ns
15	$\overline{NA}$ Setup Time		4	5		ns
16	$\overline{NA}$ Hold Time		4	3		ns
19	$\overline{READY}$ Setup Time		4	9		ns
20	$\overline{READY}$ Hold Time		4	4		ns
21	D15–D0 Read Data Setup Time		4	7		ns
22	D15–D0 Read Data Hold Time		4	5		ns
23	HOLD Setup Time		4	15		ns
24	HOLD Hold Time		4	3		ns
25	RESET Setup Time		7	10		ns
26	RESET Hold Time		7	3		ns
27	NMI, INTR Setup Time	(Note 2)	4	6		ns
28	NMI, INTR Hold Time	(Note 2)	4	6		ns
29	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$* Setup Time	(Note 2)	4	6		ns
30	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$* Hold Time	(Note 2)	4	5		ns

Notes: *Float feature will be available in future revisions.

1. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
3. These are not tested. They are guaranteed by design characterization.

SWITCHING CHARACTERISTICS (continued)

Switching Characteristics at 20 MHz: V_{CC} = 5 V±10%; T_{CASE} = 0°C to 100°C

Symbol	Parameter Description	Notes	Ref. Figure	Min	Max	Unit
	Operating Frequency	Half CLK2 freq.		0	20	MHz
1	CLK2 Period		2	25		ns
2a	CLK2 High Time	at 2 V (Note 3)	2	8		ns
2b	CLK2 High Time	at (V_{CC}–0.8 V) (Note 3)	2	5		ns
3a	CLK2 Low Time	at 2 V (Note 3)	2	8		ns
3b	CLK2 Low Time	at 0.8 V (Note 3)	2	6		ns
4	CLK2 Fall Time	(V_{CC}–0.8 V) to 0.8 V (Note 3)	2		8	ns
5	CLK2 Rise Time	0.8 V to (V_{CC}–0.8 V) (Note 3)	2		8	ns
6	A23–A1 Valid Delay	C_L = 120 pF (Note 4)	5	4	30	ns
7	A23–A1 Float Delay	(Note 1)	6	4	32	ns
8	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ Valid Delay	C_L = 75 pF (Note 4)	5	4	30	ns
9	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ Float Delay	(Note 1)	6	4	32	ns
10a	M/$\overline{IO}$, D/$\overline{C}$ Valid Delay	C_L = 75 pF (Note 4)	5	4	28	ns
10b	W/$\overline{R}$, $\overline{ADS}$ Valid Delay	C_L = 75 pF (Note 4)	5	4	26	ns
11	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{ADS}$ Float Delay	(Note 1)	6	6	30	ns
12	D15–D0 Write Data Valid Delay	C_L = 120 p (Note 4)	5	4	38	ns
13	D15–D0 Write Data Float Delay	(Note 1)	6	4	27	ns
14	HLDA Valid Delay	C_L = 75 pF (Note 4)	5	4	28	ns
15	$\overline{NA}$ Setup Time		4	5		ns
16	$\overline{NA}$ Hold Time		4	12		ns
19	$\overline{READY}$ Setup Time		4	12		ns
20	$\overline{READY}$ Hold Time		4	4		ns
21	D15–D0 Read Data Setup Time		4	9		ns
22	D15–D0 Read Data Hold Time		4	6		ns
23	HOLD Setup Time		4	17		ns
24	HOLD Hold Time		4	5		ns
25	RESET Setup Time		7	12		ns
26	RESET Hold Time		7	4		ns
27	NMI, INTR Setup Time	(Note 2)	4	16		ns
28	NMI, INTR Hold Time	(Note 2)	4	16		ns
29	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$* Setup Time	(Note 2)	4	14		ns
30	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$* Hold Time	(Note 2)	4	5		ns

Notes: *Float feature will be available in future revisions.

1. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
3. These are not tested. They are guaranteed by design characterization.
4. Tested with C_L set at 50 pF and derated to support the indicated distributed capacitive load. See Figures 8–10 for the capacitive derating curve.

SWITCHING CHARACTERISTICS (continued)

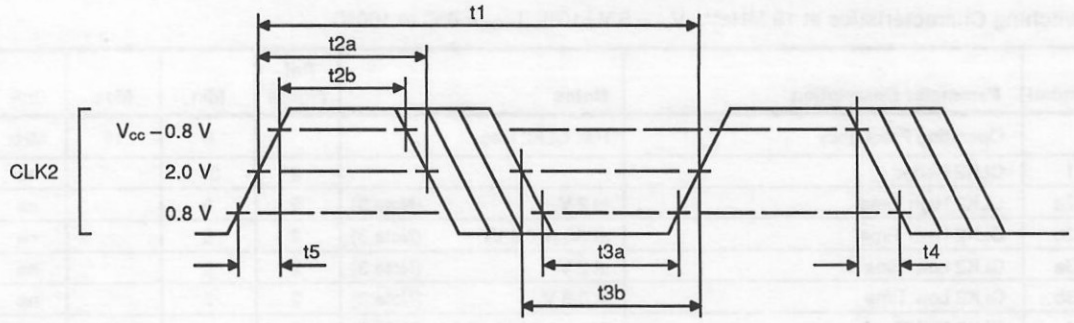
Switching Characteristics at 16 MHz:** V_{CC} = 5 V±10%; T_{CASE} = 0°C to 100°C

Symbol	Parameter Description	Notes	Ref. Figure	Min	Max	Unit
	Operating Frequency	Half CLK2 freq.		0	16	MHz
1	CLK2 Period		2	31		ns
2a	CLK2 High Time	at 2 V (Note 3)	2	9		ns
2b	CLK2 High Time	at (V_{CC}–0.8 V) (Note 3)	2	5		ns
3a	CLK2 Low Time	at 2 V (Note 3)	2	9		ns
3b	CLK2 Low Time	at 0.8 V (Note 3)	2	7		ns
4	CLK2 Fall Time	(V_{CC}–0.8 V) to 0.8 V (Note 3)	2		8	ns
5	CLK2 Rise Time	0.8 V to (V_{CC}–0.8 V) (Note 3)	2		8	ns
6	A23–A1 Valid Delay	C_L = 120 pF (Note 4)	5	4	36	ns
7	A23–A1 Float Delay	(Note 1)	6	4	40	ns
8	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ Valid Delay	C_L = 75 pF (Note 4)	5	4	36	ns
9	$\overline{BHE}$, $\overline{BLE}$, $\overline{LOCK}$ Float Delay	(Note 1)	6	4	40	ns
10	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, ADS Valid Delay	C_L = 75 pF (Note 4)	5	4	33	ns
11	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, ADS Float Delay	(Note 1)	6	6	35	ns
12	D15–D0 Write Data Valid Delay	C_L = 120 pF (Note 4)	5	4	40	ns
13	D15–D0 Write Data Float Delay	(Note 1)	6	4	35	ns
14	HLDA Valid Delay	C_L = 75 pF (Note 4)	5	4	33	ns
15	$\overline{NA}$ Setup Time		4	5		ns
16	$\overline{NA}$ Hold Time		4	21		ns
19	$\overline{READY}$ Setup Time		4	19		ns
20	$\overline{READY}$ Hold Time		4	4		ns
21	D15–D0 Read Data Setup Time		4	9		ns
22	D15–D0 Read Data Hold Time		4	6		ns
23	HOLD Setup Time		4	26		ns
24	HOLD Hold Time		4	5		ns
25	RESET Setup Time		7	13		ns
26	RESET Hold Time		7	4		ns
27	NMI, INTR Setup Time	(Note 2)	4	16		ns
28	NMI, INTR Hold Time	(Note 2)	4	16		ns
29	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$* Setup Time	(Note 2)	4	16		ns
30	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$* Hold Time	(Note 2)	4	5		ns

Notes: *Float feature will be available in future revisions.

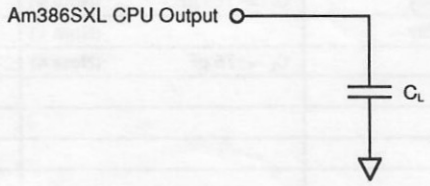
**Contact AMD for 16 MHz availability.

1. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
3. These are not tested. They are guaranteed by design characterization.
4. Tested with C_L set at 50 pF and derated to support the indicated distributed capacitive load. See Figures 8–10 for the capacitive derating curve.



15022B–031

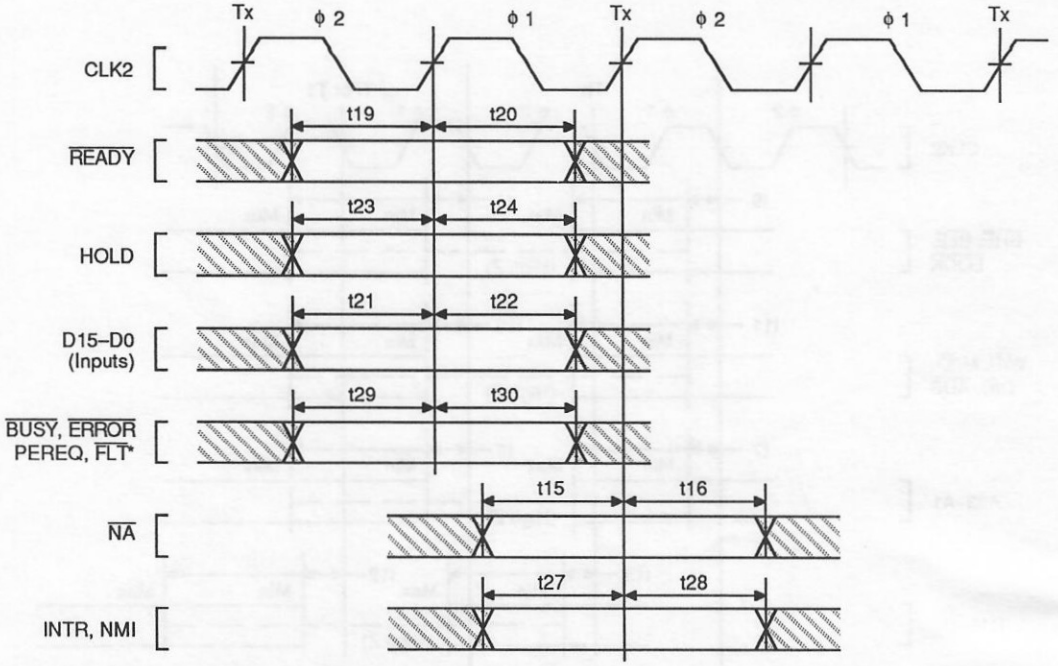
Figure 2. AC Test Waveform



15022B–032

Figure 3. AC Test Circuit

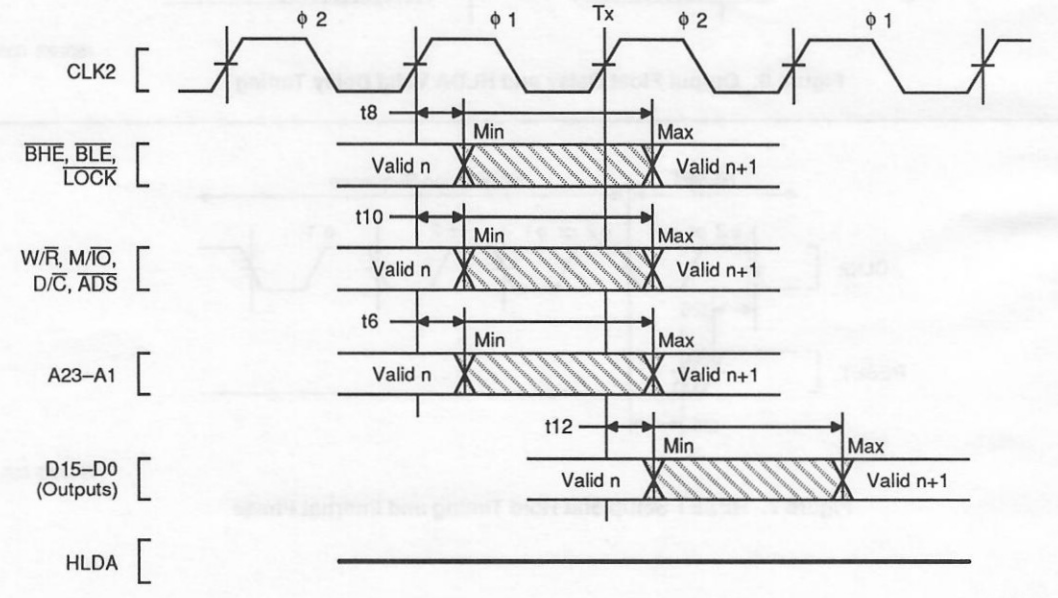
SWITCHING WAVEFORMS



*Float feature will be available in future revisions.

15022B–033

Figure 4. Input Setup and Hold Timing



15022B–034

Figure 5. Output Valid Delay Timing

SWITCHING WAVEFORMS (continued)

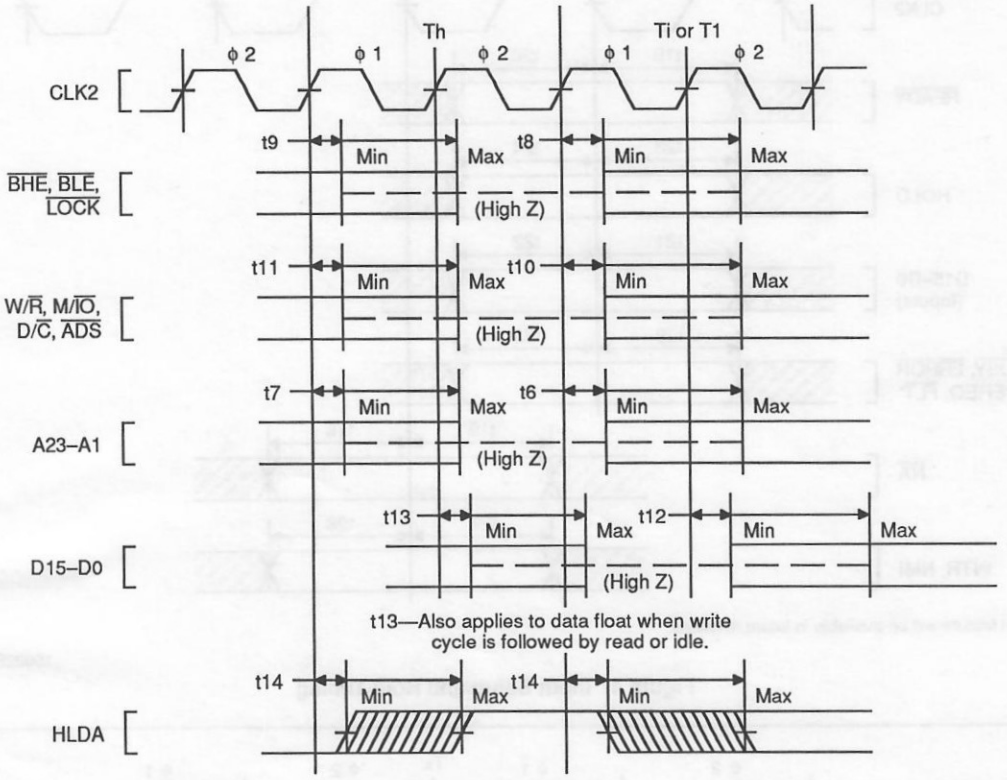


Figure 6. Output Float Delay and HLDA Valid Delay Timing

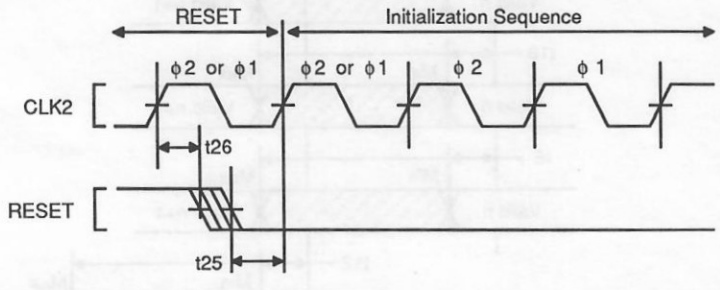


Figure 7. RESET Setup and Hold Timing and Internal Phase

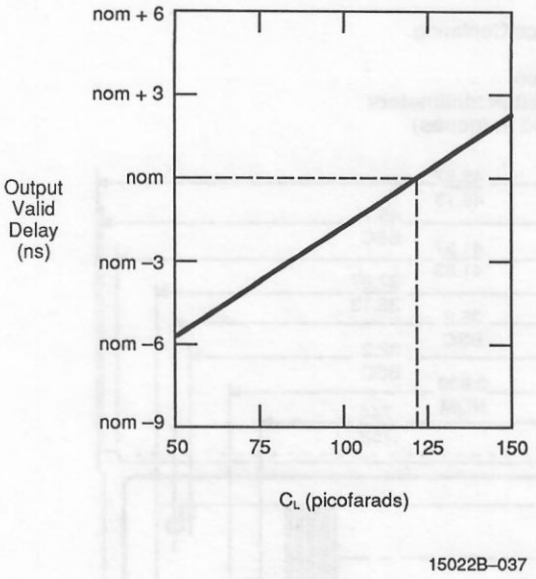


Figure 8. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature (C_L = 120 pF)

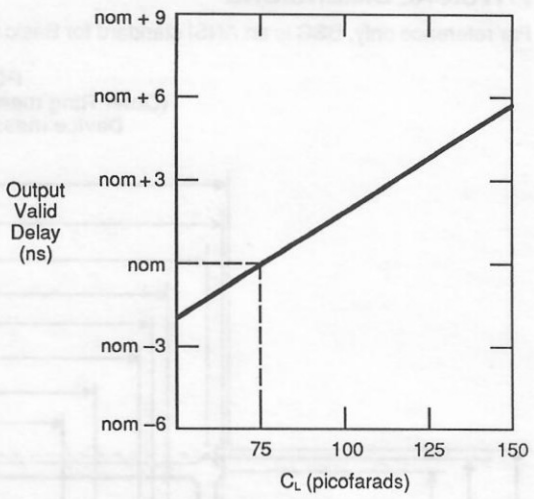


Figure 9. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature (C_L = 75 pF)

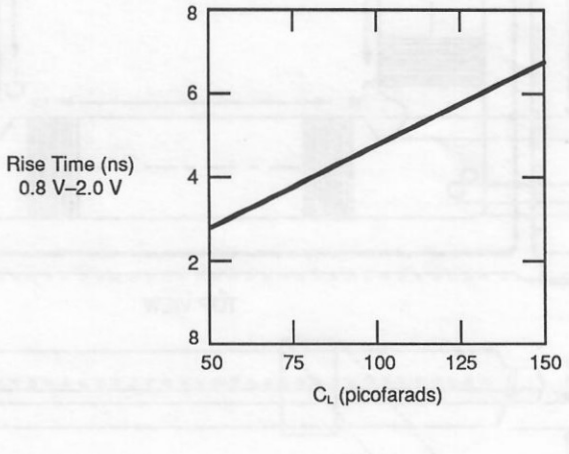
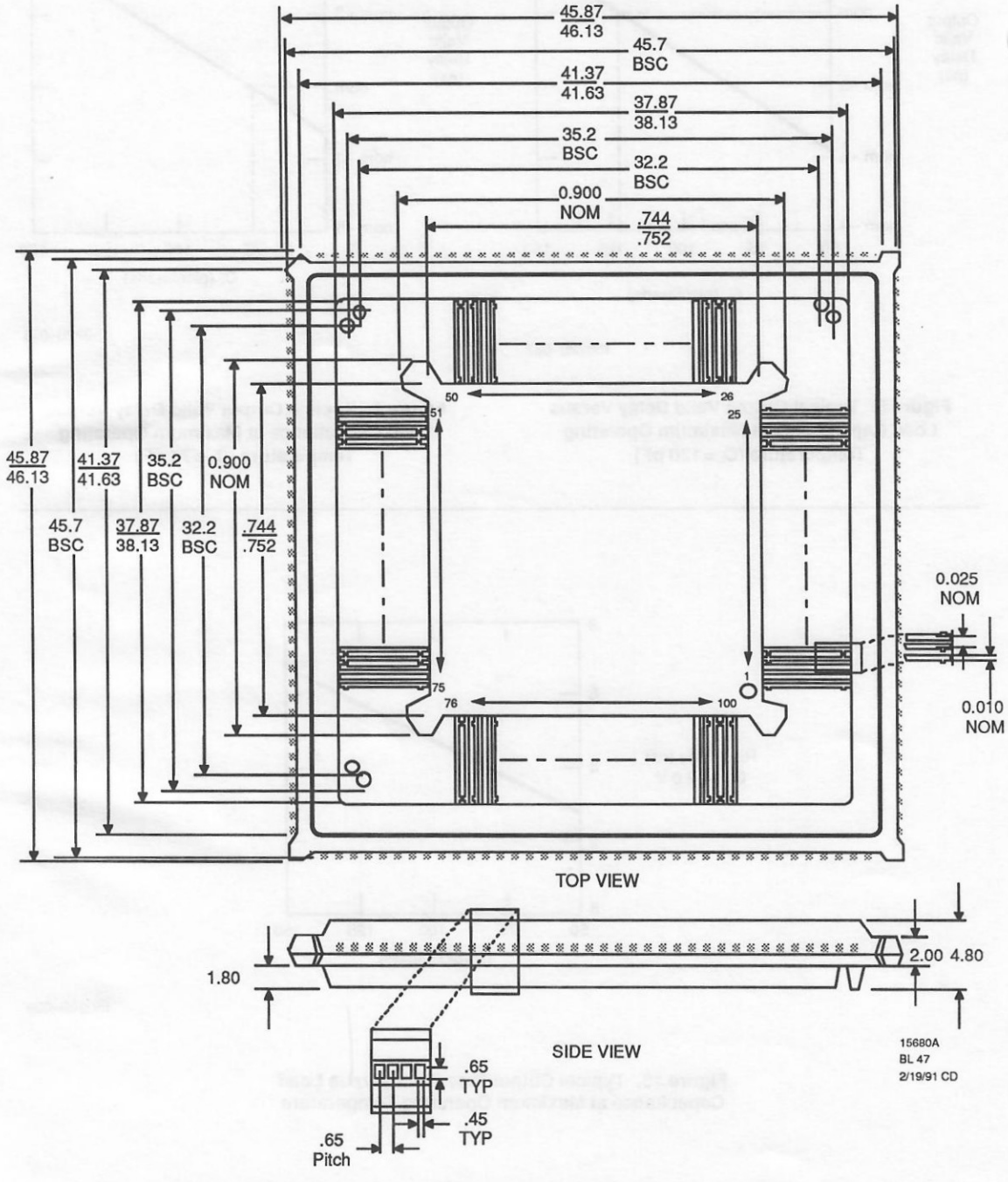


Figure 10. Typical Output Rise Time Versus Load Capacitance at Maximum Operating Temperature

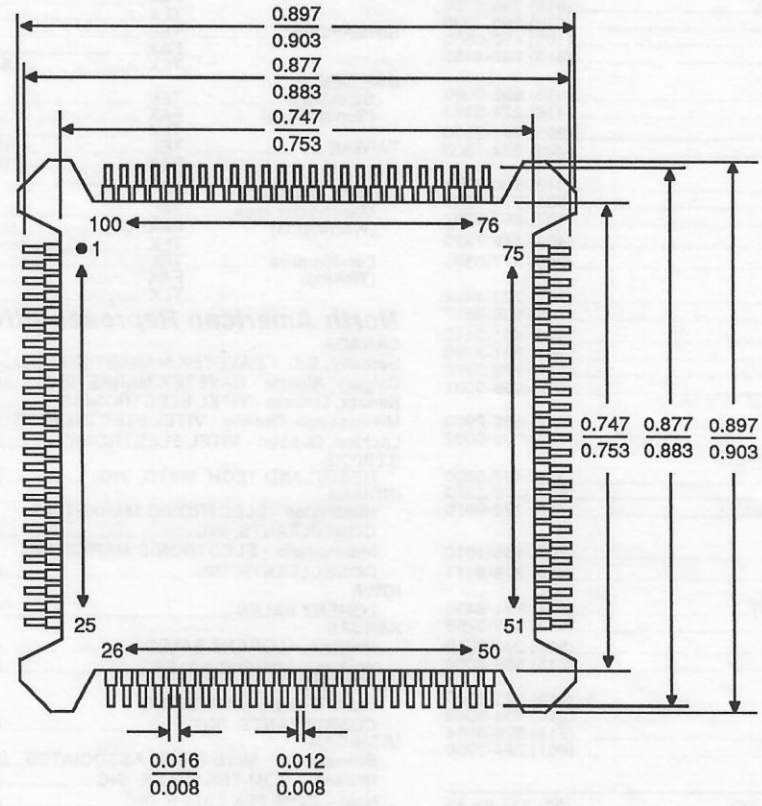
PHYSICAL DIMENSIONS

For reference only. BSC is an ANSI standard for Basic Space Centering.

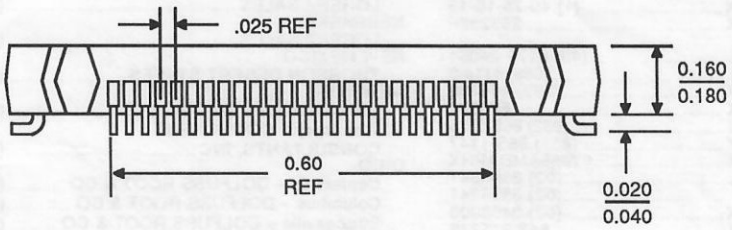
PQB100
(Outer Ring measured in millimeters
Device measured in inches)



PQ100
(measured in inches)



TOP VIEW



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