PRELIMINARY

Am386™DXLV

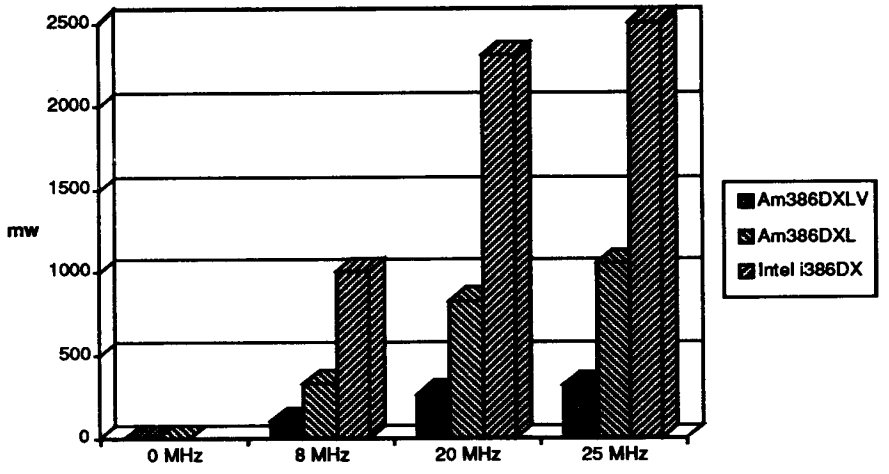
High-Performance, Low-Voltage, 32-Bit Microprocessor

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Operating voltage range 3.0 V to 5.5 V—ideal for portable PC applications**
  - —25 MHz operating frequency for 3.0 V to 5.5 V, 33 MHz operating frequency for 4.5 V to 5.5 V
  - —2X improvement in battery life over existing 5 V designs
  - —Wide range of chipsets and other logic available for 3 V systems with support for Standby Mode operation
  - —True static design for long battery life
  - —Power consumption 85% lower than Intel i386DX, 65% lower than Am386DXL processor
  - —Performance on demand (0 to 33 MHz)
- **SMM (System Management Mode) for system and power management**
  - —SMI (System Management Interrupt) for power management independent of processor operating mode and operating system
  - —SMI coupled with I/O instruction break feature provides transparent power off and auto resume of peripherals which may not be "power aware"
  - —SMI is non-maskable and has higher priority than NMI
  - —Automatic save and restore of the microprocessor state
  - —Wide range of chipsets supporting SMM available to allow product differentiation
- **Ideal for desktop PCs**
  - —Lower heat dissipation due to lower operating voltage allows elimination of fan
- **"Float" input to facilitate system debug and test**
- **Compatible with 386DX systems and software**
- **Supports 387DX-compatible math coprocessors**
- **132-pin PQFP package with optional protective ring for better lead coplanarity**
- **AMD® advanced 0.8 micron CMOS technology**

Typical Power Consumption



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GENERAL DESCRIPTION

The Am386DXLV microprocessor is a low-voltage, true static implementation of the Intel i386DX microprocessor. The operating voltage range is 3.0 V to 5.5 V. The low-voltage operation makes it ideal for both desktop and battery-powered portable personal computers. For desktop PCs, low heat dissipation allows the system designers to remove or reduce the size and cost of the system cooling fan. The Am386DXLV microprocessor operates at a maximum speed of 25 MHz from 3.0 to 5.5 V and at a maximum speed of 33 MHz from 4.5 to 5.5 V.

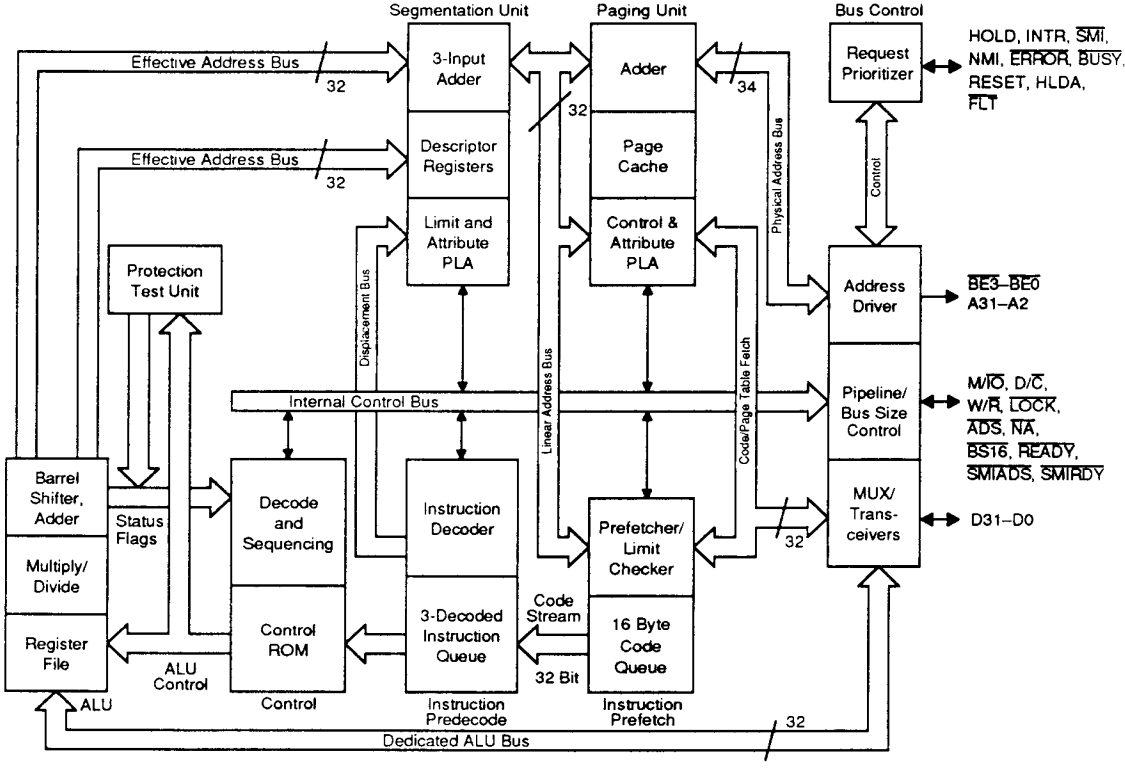
The Am386DXLV microprocessor's lower operating voltage and true static design enables longer battery life and/or lower weight for portable applications. At 25 MHz, this device has 80% lower operating Icc than the Intel i386DX. Lowering typical operating voltage from 5.0 V to 3.3 V doubles the battery life. Standby Mode allows the Am386DXLV microprocessor to be clocked down to 0 MHz (DC) and retain full register contents. In Standby Mode, typical current draw is 0.01 mA, a greater than 1000X reduction in power consumption versus the Intel i386DX or Intel i386SX.

The Am386DXLV processor is available in a small footprint 132-pin Plastic Quad Flat Pack (PQFP) package. This surface-mount package is 40% smaller than a PGA package, allowing smaller lower-cost board designs without the need for a socket.

Additionally, the Am386DXLV processors comes with SMM for system and power management. SMI is a non-maskable, higher priority interrupt than NMI and has its own code space (1 Mb). SMI can be coupled with the I/O instruction break feature to implement transparent power management of peripherals. SMM can be used by system designers to implement system and power management code independent of the operating system or the Processor Mode.

The Am386DXLV processor incorporates a float pin that places all outputs in a three-state mode to facilitate board test and debug.

BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

Benefits of Lower Operating Voltage

The Am386DXLV microprocessor has an operating voltage range of 3.0 V to 5.5 V. Low voltage allows for lower operating power consumption, longer battery life, and/or smaller batteries for notebook applications.

Because power is proportional to the square of voltage, reduction of the supply voltage from 5.0 V to 3.3 V reduces power consumption by 56%. This directly translates to a doubling of battery life for portable applications. Lower power consumption can also be used to reduce the size and weight of the battery. Thus, 3 V designs facilitate a reduction in the form factor. For desktop PCs, low power consumption means elimination of the cooling fan, thus reducing the size and noise of the PC.

A lower operating voltage results in a reduction of I/O voltage swings. This reduces noise generation providing a less hostile environment for board design. It also reduces electromagnetic radiation noise making it easier to obtain FCC approval.

SMM–System Management Mode

The Am386DXLV processor has a new System Management Mode (SMM) for system and power management. This mode consists of two features: System Management Interrupt (SMI) and I/O instruction break.

SMI–System Management Interrupt

SMI is implemented through the use of special bus interface pins. This interrupt method can be used to perform system management functions such as power management independent of Processor Operating Mode (Real, Protected, or Virtual 86 Modes).

SMI can also be invoked in software. This allows system software to communicate with SMI power management code. In addition, an instruction called UMOV allows data transfers between SMI and normal system memory spaces.

Activating the $\overline{SMI}$ pin invokes a sequence which saves the operating state of the processor into a separate SMM memory space, independent of the main system memory. After the state is saved, the processor is forced into Real Mode and begins execution at address FFFFFFF0h where a far jump to the SMM code is executed. This Real Mode code can perform its system management function and then resume execution of the normal system software by executing a special opcode sequence which will reload the saved processor state and continue execution in the main system memory space. See Figure 1 for a general flowchart of an SMM operation.

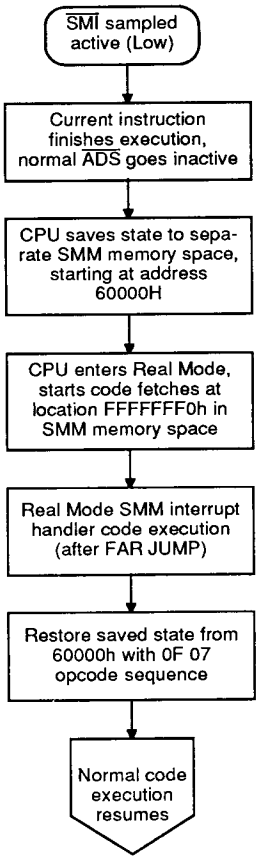


Figure 1. SMM Flow

CPU Interface—Pin Functions

The CPU interface for SMM consists of three pins dedicated to the SMI function. One pin, $\overline{SMI}$, is the new interrupt input. The other two pins, $\overline{SMIADS}$ and $\overline{SMIRDY}$, provide the control signals necessary for the separate SMI Mode memory space.

SMM Operation

The execution of a System Management Interrupt has four distinct phases: the initiation of the interrupt via $\overline{SMI}$, a processor state save, execution of the SMM interrupt code, and a processor state restore (to resume normal operation).

Interrupt Initiation

A System Management Interrupt is initiated by the driving of an active Low pulse on the $\overline{SMI}$ pin of at least four CLK2 periods. This pulse period will ensure recognition of the interrupt. The CPU will drive the $\overline{SMI}$ pin active after the completion of the current operation (active bus cycle, instruction execution, or both). The active drive of the pin by the CPU will be released at the end of the interrupt routine, following the last register read of the saved state.

An SMI cannot be masked off by the CPU, and it will always be recognized by the CPU, regardless of operating mode. This includes the Real, Protected, and Virtual 8086 Modes of the processor.

While the CPU is in SMI Mode, a bus hold request via the HOLD pin will be granted. The HLDA pin will go active after bus release and the $\overline{SMIADS}$ pin will float along with the other pins that normally float during a bus hold cycle.

Processor State Save

The first set of SMM bus transfer cycles after the CPU's recognition of an active SMI will be the processor saving its state to an external RAM array in a separate address space from main system memory. This is accomplished by using the $\overline{SMIADS}$ and $\overline{SMIRDY}$ pins for initiation and termination of bus cycles, instead of the $\overline{ADS}$ and $\overline{READY}$ pins. The 32-bit addresses to which the CPU saves its state are 60000H–600C8h and 60100h–60124h. These are fixed address locations for each register saved.

The value of $\overline{BS16}$ and $\overline{NA}$ will be ignored during the state save, only full 32-bit, non-pipelined cycles are generated for the state save cycles. In a zero wait state memory implementation, it will take approximately 630 CLK2 cycles to complete the save state operation. There are 61 data transfer cycles.

SMI Code Execution

After the processor state is saved to the separate SMM memory space, the execution of the SMI interrupt routine code begins. The processor enters Real Mode, sets most of the register values to "reset" values (those values normally seen after a CPU reset), and begins fetching code from address FFFFFFF0h in the separate SMM memory space. Normally, the first thing the interrupt routine code will do is a FAR JUMP to the Real Mode entry point for the SMI interrupt routine, which is also in SMM memory space.

Any Real Mode interrupt routine code can be executed, with the obvious exception of normal interrupt routines (which are deferred). The SMM code can be located anywhere within the 1 Mb Real Mode address space, except where the processor state is saved. I/O cycles, as a result of the IN, OUT, INS, and OUTS instructions, will go to the normal address space, utilizing the normal $\overline{ADS}$ and $\overline{READY}$ bus interface signals. This facilitates power management code manipulating system hardware registers as needed through the standard I/O subsystem; a separate I/O space does not need to be implemented.

Processor State Restore (Resuming Normal Execution)

Returning to normal code execution in the main system memory, including restoring the Processor Operating Mode, is accomplished by executing a special code sequence. This code invokes a restore CPU state operation which reloads the CPU registers from the saved data in the RAM controlled by $\overline{SMIADS}$ and $\overline{SMIRDY}$.

The ES:EDI register pair must point to physical address 60000h.Then the special opcode sequence 0Fh 07h should be executed to start the restore state operation. After completion of the restore state operation, the $\overline{SMI}$ pin will be deactivated by the CPU and normal code execution will continue at the point that it left off before the SMI occurred.

In a zero wait state memory implementation, it will take approximately 574 CLK2 cycles to complete the restore state operation. There are 61 data transfer cycles.

Software Features

There are several features of the SMI function that provide support for special operations during the execution of the system's software. These features involve the execution of reserved opcodes to induce specific SMI related operations.

Software SMI Generation

Besides hardware initiation of the System Management Interrupt via the $\overline{SMI}$ pin, there is also a software induced SMI mechanism. Generating a soft $\overline{SMI}$ involves setting a control bit in Debug Register 7 (DR7) and executing a reserved opcode (0F1H).

The functional sequence of the software-based SMI is identical to the hardware-based SMI with the exception that the $\overline{SMI}$ pin is not initially driven active by an external source. Upon execution of a soft SMI opcode, the $\overline{SMI}$ pin is driven active (Low) by the processor before the save state operation begins.

Memory Transfers to Main System Memory

While executing an SMI routine, the interrupt code can initiate memory data reads and writes to the main system memory using the normal $\overline{ADS}$ and $\overline{READY}$ pins. This is accomplished by using reserved opcodes that are special forms of the MOV instruction (called UMOV). The UMOV opcodes can move byte, word, or doubleword register operands to or from main system memory. Multiple data transfers using the normal $\overline{ADS}$ and $\overline{READY}$ pins will occur if the operands are misaligned relative to the effective address used. The UMOV opcodes are 0F10h, 0F11h, 0F12h, and 0F13h.

The UMOV instruction can use any of the 386 addressing modes, as specified in the ModR/M byte of the opcode. Note that the 16- and 32-bit versions are the same opcodes with the exception of the 066h operand size prefix. The $\overline{BS16}$ line is recognized during the normal memory space data transfer(s) initiated by these instructions.

I/O Instruction Break

The Am386DXLV processor has an I/O instruction break feature that allows the system logic to implement I/O trapping for peripheral devices. To enable the I/O instruction break feature, $\overline{IIBEN}$ must first be asserted active Low. On detecting an I/O instruction, the processor will prevent the execution unit from executing further instructions until $\overline{READY}$ is driven active Low by the system. Once $\overline{READY}$ is driven active, the execution unit will either immediately respond to any active interrupt request or continue executing instructions following the I/O instruction that caused the break.

The I/O instruction break feature can be used to allow system logic to implement I/O trapping for peripheral devices. On sensing an I/O instruction, the system can drive the $\overline{SMI}$ (or NMI or INTR) active before driving $\overline{READY}$ active. This ensures that the SMI service routine is executed immediately following the I/O instruction that caused the break. (If the I/O instruction break feature is not enabled via $\overline{IIBEN}$, several instructions after the I/O instruction that caused the break will execute before the SMI service routine is executed.) The SMI service routine can access the peripheral for which $\overline{SMI}$ was asserted and modify its state.

The SMI service routine will normally return to the instruction following the I/O instruction that caused the break. By modifying the saved state instruction pointer, the routine can choose to return to the I/O instruction that caused the break and re-execute that instruction. The default is to return to the following instruction (except for REP I/O strings). To re-execute the I/O instruction that caused the break, the SMI service routine must copy the I/O instruction pointer over the default pointer. This feature is particularly useful when an application program requests an access to a peripheral that has been powered down. The SMI service routine can restore power to the peripheral and initiate a re-execution sequence transparent to the application program. This re-execution feature should only be used if the $\overline{SMI}$ is in response to an I/O trap with $\overline{IIBEN}$ active.

Note that the I/O instruction break feature is not enabled for memory mapped I/O devices or for 80387 bus cycles even if $\overline{IIBEN}$ is active.

I/O Instruction Break Timing

The I/O Instruction Break feature requires that $\overline{SMI}$ be sampled active (Low) by the processor at least three CLK2 edges before the CLK2 edge that ends the I/O cycle with an active $\overline{READY}$ signal. This timing applies for both pipelined and non-pipelined cycles. If this timing constraint is not met, the next instruction may be executed by the internal execution unit prior to entering SMI Mode, but the $\overline{SMI}$ will be recognized eventually.

Depending on the state of the prefetch queue at the time that $\overline{SMI}$ is asserted, instruction fetch cycles may occur on the normal $\overline{ADS}$ interface before the SMI save state process begins with the assertion of $\overline{SMIADS}$. However, this fetched code will not be executed.

True Static Operation

The Am386DXLV microprocessor incorporates a true static design. Unlike dynamic circuit design, the Am386DXLV device eliminates the minimum operating frequency restriction. It may be clocked from its maximum speed of 33 MHz all the way down to 0 MHz (DC). System designers can use this feature to design true 32-bit battery-powered portable PCs with long battery life.

Standby Mode

This true static design allows for a Standby Mode. At any of its operating speeds (33 MHz to 0 MHz), the Am386DXLV microprocessor will retain its state (i.e., the contents of all of its registers). By shutting off the clock completely, the device enters Standby Mode. Since power consumption is a function of clock frequency, operating power consumption is reduced as the frequency is lowered. In Standby Mode, typical current draw is reduced to less than 0.01 mA at DC.

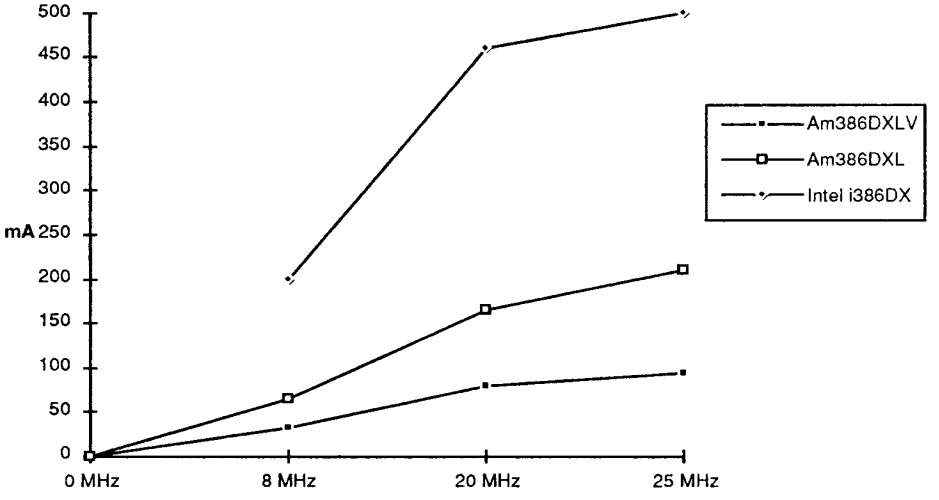
Not only does this feature save battery life, but it also simplifies the design of power-conscious notebook computers in the following ways.

1. Eliminates the need for software in BIOS to save and restore the contents of registers.
2. Allows simpler circuitry to control stopping of the clock since the system does not need to know what state the processor is in.

Lower Operating Icc

True static design also allows lower operating Icc when operating at any speed. See the following graph for typical current at operating speeds.

Typical Icc

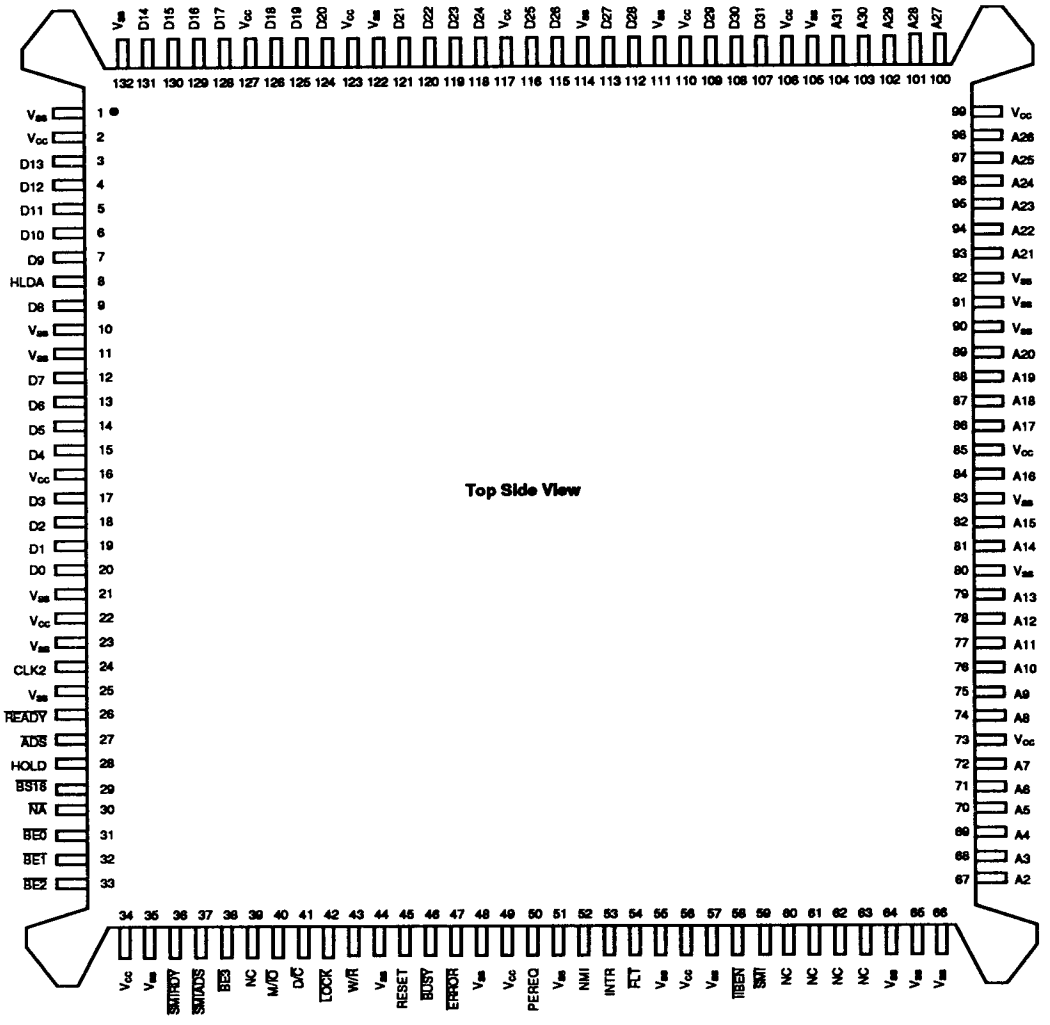


Performance on Demand

The Am386DXLV microprocessor retains its state at any speed from 0 MHz (DC) to its maximum operating speed. With this feature, system designers may vary the operating speed of the system to extend the battery life in portable systems.

For example, the system could operate at low speeds during inactivity or polling operations. However, upon interrupt, the system clock can be increased up to its maximum speed. After a user-defined time-out period, the system can be returned to a low (or a 0 MHz) operating speed without losing its state. This design maximizes battery life while achieving optimal performance.

CONNECTION DIAGRAMS
132-Lead Plastic Quad Flat Pack (PQFP) Package



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Note: Pin 1 is marked for orientation.

PQFP Pin Designations (Functional Grouping)

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A2	67	A24	96	D6	13	D28	112	V_{CC}	16	V_{SS}	51
A3	68	A25	97	D7	12	D29	109		22		55
A4	69	A26	98	D8	9	D30	108		34		57
A5	70	A27	100	D9	7	D31	107		49		64
A6	71	A28	101	D10	6	D/$\overline{C}$	41		56		65
A7	72	A29	102	D11	5	$\overline{ERROR}$	47		73		66
A8	74	A30	103	D12	4	$\overline{FLT}$	54		85		80
A9	75	A31	104	D13	3	HLDA	8		99		83
A10	76	$\overline{ADS}$	27	D14	131	HOLD	28		106		90
A11	77	$\overline{BE0}$	31	D15	130	$\overline{IIBEN}$	58		110		91
A12	78	$\overline{BE1}$	32	D16	129	INTR	53		117		92
A13	79	$\overline{BE2}$	33	D17	128	$\overline{LOCK}$	42		123		105
A14	81	$\overline{BE3}$	38	D18	126	M/$\overline{IO}$	40		127		111
A15	82	$\overline{BS16}$	29	D19	125	$\overline{NA}$	30	V_{SS}	1		114
A16	84	$\overline{BUSY}$	46	D20	124	NMI	52		10		122
A17	86	CLK2	24	D21	121	PEREQ	50		11		132
A18	87	D0	20	D22	120	$\overline{READY}$	26		21	W/$\overline{R}$	43
A19	88	D1	19	D23	119	RESET	45		23	NC	39
A20	89	D2	18	D24	118	$\overline{SMI}$	59		25		60
A21	93	D3	17	D25	116	$\overline{SMIADS}$	37		35		61
A22	94	D4	15	D26	115	$\overline{SMIRDY}$	36		44		62
A23	95	D5	14	D27	113	V_{CC}	2		48		63

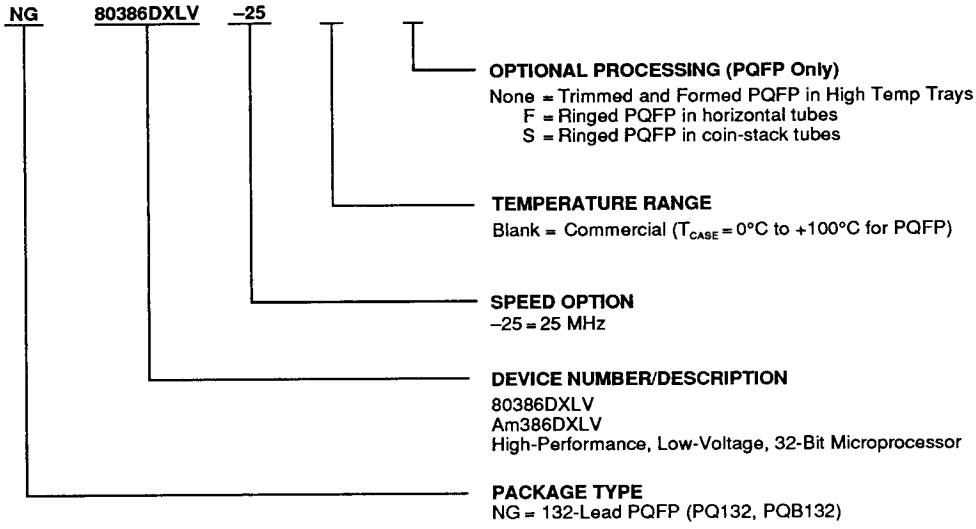
PQFP Pin Designations (Sorted by Pin No.)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	23	V_{SS}	45	RESET	67	A2	89	A20	111	V_{SS}
2	V_{CC}	24	CLK2	46	$\overline{BUSY}$	68	A3	90	V_{SS}	112	D28
3	D13	25	V_{SS}	47	$\overline{ERROR}$	69	A4	91	V_{SS}	113	D27
4	D12	26	$\overline{READY}$	48	V_{SS}	70	A5	92	V_{SS}	114	VSS
5	D11	27	$\overline{ADS}$	49	V_{CC}	71	A6	93	A21	115	D26
6	D10	28	HOLD	50	PEREQ	72	A7	94	A22	116	D25
7	D9	29	$\overline{BS16}$	51	V_{SS}	73	V_{CC}	95	A23	117	V_{CC}
8	HLDA	30	$\overline{NA}$	52	NMI	74	A8	96	A24	118	D24
9	D8	31	$\overline{BE0}$	53	INTR	75	A9	97	A25	119	D23
10	V_{SS}	32	$\overline{BE1}$	54	$\overline{FLT}$	76	A10	98	A26	120	D22
11	V_{SS}	33	$\overline{BE2}$	55	V_{SS}	77	A11	99	V_{CC}	121	D21
12	D7	34	V_{CC}	56	V_{CC}	78	A12	100	A27	122	V_{SS}
13	D6	35	V_{SS}	57	V_{SS}	79	A13	101	A28	123	V_{CC}
14	A5	36	$\overline{SMIRDY}$	58	$\overline{IIBEN}$	80	V_{SS}	102	A29	124	D20
15	D4	37	$\overline{SMIADS}$	59	$\overline{SMI}$	81	A14	103	A30	125	D19
16	V_{CC}	38	$\overline{BE3}$	60	NC	82	A15	104	A31	126	D18
17	D3	39	NC	61	NC	83	V_{SS}	105	V_{SS}	127	V_{CC}
18	D2	40	M/$\overline{IO}$	62	NC	84	A16	106	V_{CC}	128	D17
19	D1	41	D/$\overline{C}$	63	NC	85	V_{CC}	107	D31	129	D16
20	D0	42	$\overline{LOCK}$	64	V_{SS}	86	A17	108	D30	130	D15
21	V_{SS}	43	W/$\overline{R}$	65	V_{SS}	87	A18	109	D29	131	D14
22	V_{CC}	44	V_{SS}	66	V_{SS}	88	A19	110	V_{CC}	132	V_{SS}

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

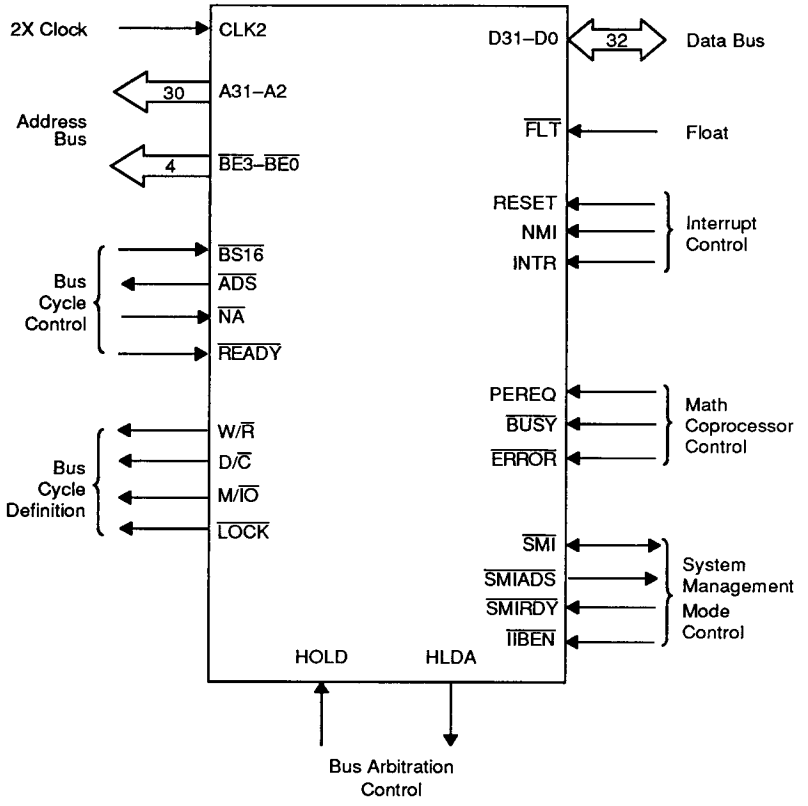


Valid Combinations		
NG	80386DXLV	–25 –25F –25S

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

LOGIC SYMBOL



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PIN DESCRIPTION

A31–A2
Address Bus (Outputs)
Outputs physical memory or port I/O addresses.

$\overline{ADS}$
Address Status (Active Low; Output)
Indicates that a valid bus cycle definition and address (W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{BE3}$–$\overline{BE0}$, and A31–A2) are being driven at the Am386DXLV microprocessor pins.

$\overline{BE3}$–$\overline{BE0}$
Byte Enable (Active Low; Outputs)
Indicates which data bytes of the data bus take part in a bus cycle.

$\overline{BS16}$
Bus Size 16 (Active Low; Input)
Allows direct connection of 32-bit and 16-bit data buses. $\overline{BS16}$ has an internal pullup resistor.

$\overline{BUSY}$
Busy (Active Low; Input)
Signals a busy condition from a processor extension. $\overline{BUSY}$ has an internal pullup resistor.

CLK2
Clock (Input)
Provides the fundamental timing for the Am386DXLV microprocessor.

D31–D0
Data Bus (Inputs/Outputs)
Inputs data during memory, I/O, and interrupt acknowledge read cycles and outputs data during memory and I/O write cycles.

D/$\overline{C}$
Data/Control (Output)
A bus cycle definition pin that distinguishes data cycles, either memory or I/O, from control cycles (which are interrupt acknowledge, halt, and instruction fetching).

$\overline{ERROR}$
Error (Active Low; Input)
Signals an error condition from a processor extension. $\overline{ERROR}$ has an internal pullup resistor.

$\overline{FLT}$
Float (Active Low; Input)
An input signal which forces all bi-directional and output signals, including HLDA, to the three-state condition. $\overline{FLT}$ has an internal pullup resistor.

HLDA
Bus Hold Acknowledge (Active High; Output)
Indicates that the Am386DXLV microprocessor has surrendered control of its local bus to another bus master.

HOLD
Bus Hold Request (Active High; Input)
Allows another bus master to request control of the local bus.

$\overline{IIBEN}$
I/O Instruction Break Enable (Active Low; Input)
Enables the I/O instruction break feature. $\overline{IIBEN}$ has an internal pullup resistor.

INTR
Interrupt Request (Active High; Input)
A maskable input that signals the Am386DXLV microprocessor to suspend execution of the current program and execute an interrupt acknowledge function.

$\overline{LOCK}$
Bus Lock (Active Low; Output)
A bus cycle definition pin that indicates that other system bus masters are denied access to the system bus while it is active.

M/$\overline{IO}$
Memory I/O (Output)
A bus cycle definition pin that distinguishes memory cycles from input/output cycles.

$\overline{NA}$
Next Address (Active Low; Input)
Used to request address pipelining.

NC
No Connect
Should always remain unconnected. Connection of an NC pin may cause the processor to malfunction or be incompatible with future steppings of the Am386DXLV microprocessor.

NMI
Non-Maskable Interrupt Request (Active High; Input)
A non-maskable input that signals the Am386DXLV microprocessor to suspend execution of the current program and execute an interrupt acknowledge function.

PEREQ
Processor Extension Request (Active High; Input)
Indicates that the processor extension has data to be transferred by the Am386DXLV microprocessor. PEREQ has an internal pulldown resistor.

$\overline{READY}$
Bus Ready (Active Low; Input)
Terminates the bus cycle.

RESET
Reset (Active High; Input)
Suspends any operation in progress and places the Am386DXLV microprocessor in a known reset state.

$\overline{SMI}$
System Management Interrupt (Active Low; Input/Output)
A non-maskable interrupt pin which signals the Am386DXLV microprocessor to suspend execution and enter System Management Mode. $\overline{SMI}$ has an internal pullup resistor.

$\overline{SMIADS}$

SMI Address Status (Active Low, Three-State; Output)

Indicates that a valid bus cycle definition and address (W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{BE3}$–$\overline{BE0}$, and A31–A2) are being driven at the Am386DXLV microprocessor pins while in System Management Mode.

$\overline{SMIRDY}$

SMI Ready (Active Low; Input)

This input terminates the current bus cycle to the SMM address space in the same manner the $\overline{READY}$ pin does for the Normal Mode address space. $\overline{SMIRDY}$ has an internal pullup resistor.

V_{CC}

System Power (Active High; Input)

Provides the DC supply input.

V_{SS}

System Ground (Input)

Provides 0-V connection from which all inputs and outputs are measured.

W/$\overline{R}$

Write/Read (Output)

A bus cycle definition pin that distinguishes write cycles from read cycles.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . −65°C to +150°C
Ambient Temperature Under Bias . . −65°C to +125°C

Stresses above those listed may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

OPERATING RANGES

Voltage on Other Pins . . . . . −0.5 V to V_{CC} +0.5 V
Supply Voltage with Respect to V_{SS} . . −0.5 V to +7 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL Operating Ranges

V_{CC} = 3.0 V to 3.6 V; T_{CASE} = 0°C to +100°C

Symbol	Parameter Description	Notes	Preliminary Min	Preliminary Max	Unit
V_{IL}	Input Low Voltage	(Note 1)	−0.3	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.3	V
V_{ILC}	CLK2 Input Low Voltage	(Note 1)	−0.3	0.8	V
V_{IHC}	CLK2 Input High Voltage 25 MHz		V_{CC} − 0.6	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage I_{OL} = 0.5 mA: A31–A2, D31–D0 I_{OL} = 0.5 mA: $\overline{BE3}$–$\overline{BE0}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, $\overline{SMIADS}$, HLDA I_{OL} = 2 mA: A31–A2, D31–D0 I_{OL} = 2.5 mA: $\overline{BE3}$–$\overline{BE0}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, $\overline{SMIADS}$, HLDA	(Note 5)		0.2 0.2 0.45 0.45	V V V V
V_{OH}	Output High Voltage I_{OH} = 0.1 mA: A31–A2, D31–D0 I_{OH} = 0.1 mA: $\overline{BE3}$–$\overline{BE0}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, $\overline{SMIADS}$, HLDA I_{OH} = 0.5 mA: A31–A2, D31–D0 I_{OH} = 0.5 mA: $\overline{BE3}$–$\overline{BE0}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, $\overline{SMIADS}$, HLDA	(Note 5)	V_{CC} − 0.2 V_{CC} − 0.2 V_{CC} − 0.45 V_{CC} − 0.45		V V V V
I_{LI}	Input Leakage Current (All pins except $\overline{BS16}$, PEREQ, $\overline{IIBEN}$ $\overline{BUSY}$, $\overline{FLT}$, $\overline{ERROR}$, $\overline{SMI}$, and $\overline{SMIRDY}$)	0 V ≤ V_{IN} ≤ V_{CC}		±15	µA
I_{IH}	Input Leakage Current (PEREQ Pin)	V_{IH} = V_{CC} − 0.1 V V_{IH} = 2.4 V (Note 2)		300 200	µA
I_{IL}	Input Leakage Current ($\overline{BS16}$, $\overline{BUSY}$, $\overline{FLT}$, $\overline{ERROR}$, $\overline{SMI}$, $\overline{IIBEN}$, and $\overline{SMIRDY}$)	V_{IL} = 0.1 V V_{IL} = 0.45 V (Note 3)		−300 −200	µA
I_{LO}	Output Leakage Current	0.1 V ≤ V_{OUT} ≤ V_{CC}		±15	µA
I_{CC}	Supply Current CLK2 = 40 MHz: Oper. Freq. 20 MHz CLK2 = 50 MHz: Oper. Freq. 25 MHz	 I_{CC} Typ = 80 I_{CC} Typ = 95		 110 135	 mA mA
I_{CCSB}	Standby Current	I_{CCSB} Typ = 10		150	µA
C_{IN}	Input or I/O Capacitance	F_C = 1 MHz (Note 4)		10	pF
C_{OUT}	Output Capacitance	F_C = 1 MHz (Note 4)		12	pF
C_{CLK}	CLK2 Capacitance	F_C = 1 MHz (Note 4)		20	pF

Notes: 1. The Min value, −0.3, is not 100% tested.
2. PEREQ input has an internal pulldown resistor.
3. $\overline{BS16}$, $\overline{BUSY}$, $\overline{FLT}$, $\overline{ERROR}$, $\overline{SMI}$, $\overline{SMIRDY}$, and $\overline{IIBEN}$ inputs each have an internal pullup resistor.
4. Not 100% tested.
5. Outputs are CMOS and will pull rail to rail if the load is not resistive.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C
Ambient Temperature Under Bias . . –65°C to +125°C

Stresses above those listed may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

OPERATING RANGES

Voltage on Other Pins ..... –0.5 V to V_{CC} +0.5 V
Supply Voltage with Respect to V_{SS} ..... –0.5 V to +7 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL Operating Ranges

V_{CC} = 3.6 V to 5.5 V; T_{CASE} = 0°C to +100°C

Symbol	Parameter Description	Notes	Preliminary Min	Preliminary Max	Unit
V_{IL}	Input Low Voltage	(Note 1)	–0.3	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.3	V
V_{ILC}	CLK2 Input Low Voltage	(Note 1)	–0.3	0.8	V
V_{IHC}	CLK2 Input High Voltage 20 MHz 25, 33 MHz		 V_{CC} – 0.8 3.7	 V_{CC} + 0.3 V_{CC} + 0.3	 V V
V_{OL}	Output Low Voltage I_{OL} = 4 mA: A31–A2, D31–D0 I_{OL} = 5 mA: $\overline{BE3}$–$\overline{BE0}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, $\overline{SMIADS}$, HLDA	(Note 5)		 0.45 0.45	 V V
V_{OH}	Output High Voltage I_{OH} = 1 mA: A31–A2, D31–D0 I_{OH} = 0.9 mA: $\overline{BE3}$–$\overline{BE0}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, $\overline{SMIADS}$, HLDA	(Note 5)	 2.4 2.4		 V V
I_{LI}	Input Leakage Current (All pins except $\overline{BS16}$, PEREQ, $\overline{IIBEN}$, $\overline{BUSY}$, $\overline{FLT}$, $\overline{SMI}$, $\overline{SMIRDY}$, and $\overline{ERROR}$)	0 V ≤ V_{IN} ≤ V_{CC}		±15	µA
I_{IH}	Input Leakage Current (PEREQ Pin)	V_{IH} = 2.4 V (Note 2)		200	µA
I_{IL}	Input Leakage Current ($\overline{BS16}$, $\overline{BUSY}$, $\overline{FLT}$, $\overline{SMI}$, $\overline{SMIRDY}$, $\overline{IIBEN}$, and $\overline{ERROR}$)	V_{IL} = 0.45 (Note 3)		–400	µA
I_{LO}	Output Leakage Current	0.45 V ≤ V_{OUT} ≤ V_{CC}		±15	µA
I_{CC}	Supply Current CLK2 = 40 MHz: Oper. Freq. 20 MHz CLK2 = 50 MHz: Oper. Freq. 25 MHz CLK2 = 66 MHz: Oper. Freq. 33 MHz	 I_{CC} Typ = 165 I_{CC} Typ = 210 I_{CC} Typ = 275		 200 250 330	 mA mA mA
I_{CCSB}	Standby Current	I_{CCSB} Typ = 0.02 mA		150	µA
C_{IN}	Input or I/O Capacitance	F_C = 1 MHz (Note 4)		10	pF
C_{OUT}	Output Capacitance	F_C = 1 MHz (Note 4)		12	pF
C_{CLK}	CLK2 Capacitance	F_C = 1 MHz (Note 4)		20	pF

Notes: 1. The Min value, –0.3, is not 100% tested.
2. PEREQ input has an internal pulldown resistor.
3. $\overline{BS16}$, $\overline{BUSY}$, $\overline{FLT}$, $\overline{ERROR}$, $\overline{SMI}$, $\overline{SMIRDY}$, and $\overline{IIBEN}$ inputs each have an internal pullup resistor.
4. Not 100% tested.
5. Outputs are CMOS and will pull rail to rail if the load is not resistive.

SWITCHING CHARACTERISTICS

The switching characteristics consist of output delays, input setup requirements, and input hold requirements. All characteristics are relative to the CLK2 rising edge crossing the 2.0 V level.

Switching characteristic measurement is defined by Figure 2. Inputs must be driven to the voltage levels indicated by this diagram. Am386DXLV CPU output delays are specified with minimum and maximum limits measured as shown. The minimum Am386DXLV microprocessor delay times are hold times provided to external circuitry. Am386DXLV microprocessor input setup and hold time are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct Am386DXLV microprocessor operation.

Outputs W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{BE3}$–$\overline{BE0}$, $\overline{ADS}$, A31–A2, HLDA, and $\overline{SMIADS}$ only change at the beginning of phase one. D31–D0 (write cycles) only change at the beginning of phase two. The $\overline{READY}$, HOLD, $\overline{BUSY}$, $\overline{ERROR}$, PEREQ, $\overline{FLT}$, D31–D0, and $\overline{SMIRDY}$ (read cycles) inputs are sampled at the beginning of phase one. The $\overline{NA}$, $\overline{BS16}$, INTR, NMI, and $\overline{SMI}$ inputs are sampled at the beginning of phase two.

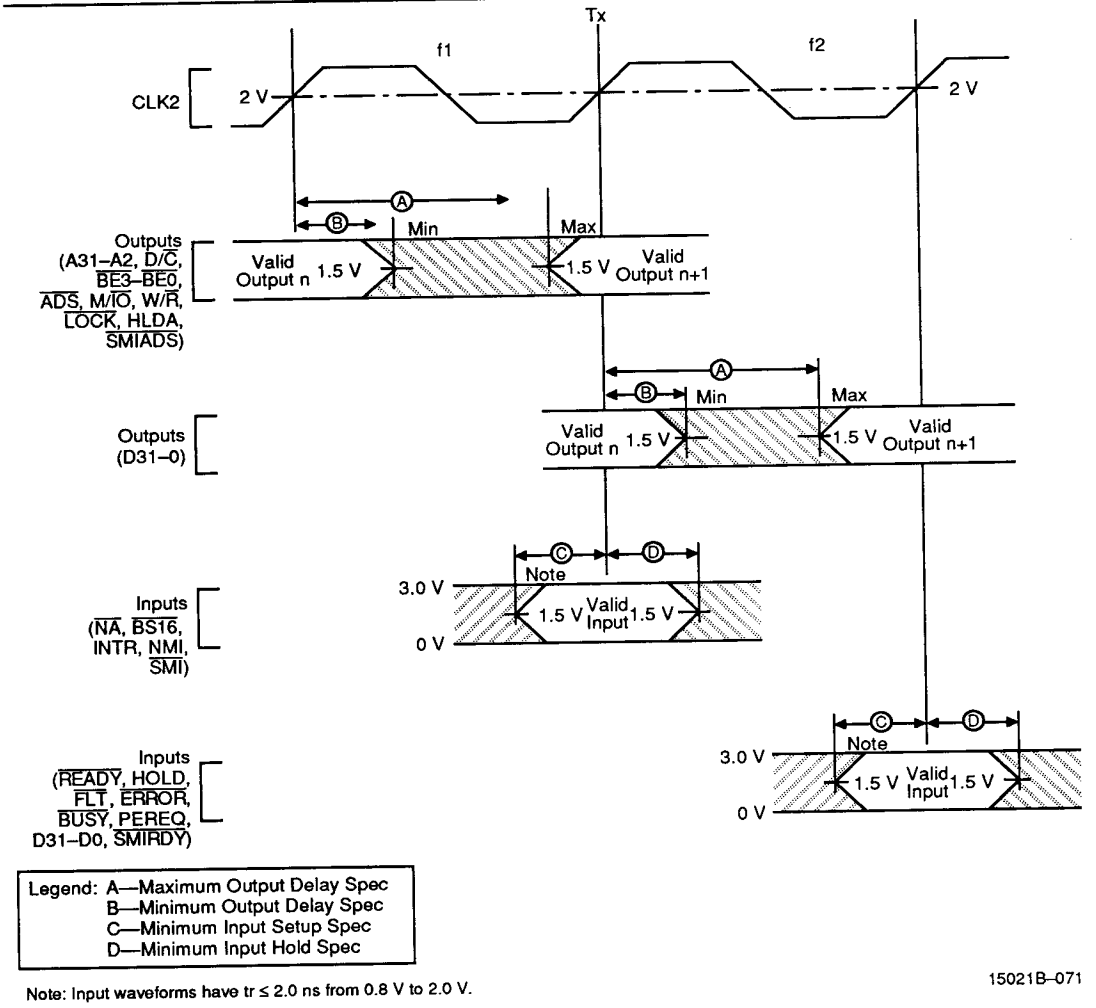


Figure 2. Drive Levels and Measurement Points

SWITCHING CHARACTERISTICS over operating range at 33 MHz

V_{CC} = 4.5 V to 5.5 V; T_{CASE} = 0°C to +100°C

No.	Parameter Description	Notes	Ref Figures	Preliminary Min	Preliminary Max	Unit
	Operating Frequency	Half of CLK2 Freq		0	33.3	MHz
1	CLK2 Period		4	15.0		ns
2a	CLK2 High Time	at 2 V	4	6.25		ns
2b	CLK2 High Time	at 3.7 V	4	4.5		ns
3a	CLK2 Low Time	at 2 V	4	6.25		ns
3b	CLK2 Low Time	at 0.8 V	4	4.5		ns
4	CLK2 Fall Time	3.7 V to 0.8 V (Note 3)	4		4	ns
5	CLK2 Rise Time	0.8 V to 3.7 V (Note 3)	4		4	ns
6	A31–A2 Valid Delay	C_L = 50 pF	3, 6	4	15	ns
7	A31–A2 Float Delay	(Note 1)	10	4	20	ns
8	$\overline{BE3}$–$\overline{BE0}$, $\overline{LOCK}$ Valid Delay	C_L = 50 pF	3, 6	4	15	ns
9	$\overline{BE3}$–$\overline{BE0}$, $\overline{LOCK}$ Float Delay	(Note 1)	10	4	20	ns
10	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$ Valid Delay	C_L = 50 pF	3, 6	4	15	ns
10a	$\overline{ADS}$ Valid Delay	C_L = 50 pF	2, 6	4	14.5	ns
10s	$\overline{SMIADS}$ Valid Delay	C_L=50 pF	2, 6	4	23	ns
11	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{ADS}$ Float Delay	(Note 1)	10	4	20	ns
11s	$\overline{SMIADS}$ Float Delay	(Note 1)	10	4	20	ns
12	D31–D0 Write Data Valid Delay	C_L = 50 pF (Note 4)	6, 7, 9	7	24	ns
12a	D31–D0 Write Data Hold Time	C_L = 50 pF	3, 8	2		ns
13	D31–D0 Float Delay	(Note 1)	10	4	17	ns
14	HLDA Valid Delay	C_L = 50 pF	3, 10	4	20	ns
15	$\overline{NA}$ Setup Time		5	5		ns
16	$\overline{NA}$ Hold Time		5	2		ns
17	$\overline{BS16}$ Setup Time		5	5		ns
18	$\overline{BS16}$ Hold Time		5	2		ns
19	$\overline{READY}$ Setup Time		5	7		ns
19s	$\overline{SMIRDY}$ Setup Time		5	7		ns
20	$\overline{READY}$ Hold Time		5	4		ns
20s	$\overline{SMIRDY}$ Hold Time		5	4		ns
21	D31–D0 Read Setup Time		5	5		ns
22	D31–D0 Read Hold Time		5	3		ns
23	HOLD Setup Time		5	11		ns
24	HOLD Hold Time		5	2		ns
25	RESET Setup Time		11	5		ns
26	RESET Hold Time		11	2		ns
27	NMI, INTR Setup Time	(Note 2)	5	5		ns
27s	$\overline{SMI}$ Setup Time		5	5		ns
28	NMI, INTR Hold Time	(Note 2)	5	5		ns
28s	$\overline{SMI}$ Hold Time		5	5		ns
29	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$ Setup Time	(Note 2)	5	5		ns
30	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$ Hold Time	(Note 2)	5	4		ns

Notes: 1. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
3. Rise and fall times are not tested.
4. Min time not 100% tested.

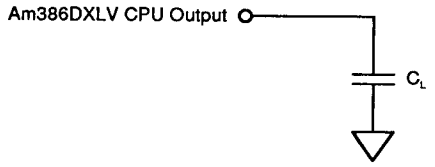
SWITCHING CHARACTERISTICS over operating range at 25 MHz

V_{CC} = 3.0 V to 5.5 V; T_{CASE} = 0°C to +100°C

No.	Parameter Description	Notes	Ref Figures	Preliminary Min	Preliminary Max	Unit
	Operating Frequency	Half of CLK2 Freq		0	25	MHz
1	CLK2 Period		4	20		ns
2a	CLK2 High Time	at 2 V	4	7		ns
2b	CLK2 High Time	at 3.7 V	4	4		ns
3a	CLK2 Low Time	at 2 V	4	7		ns
3b	CLK2 Low Time	at 0.8 V	4	5		ns
4	CLK2 Fall Time	3.7 V to 0.8 V (Note 3)	4		7	ns
5	CLK2 Rise Time	0.8 V to 3.7 V (Note 3)	4		7	ns
6	A31–A2 Valid Delay	C_L = 50 pF	3, 6	4	21	ns
7	A31–A2 Float Delay	(Note 1)	10	4	30	ns
8	$\overline{BE3}$–$\overline{BE0}$ Valid Delay	C_L = 50 pF	3, 6	4	24	ns
8a	$\overline{LOCK}$ Valid Delay	C_L = 50 pF	3, 6	4	21	ns
9	$\overline{BE3}$–$\overline{BE0}$, $\overline{LOCK}$ Float Delay	(Note 1)	10	4	30	ns
10	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{ADS}$ Valid Delay	C_L = 50 pF	3, 6	4	21	ns
10s	$\overline{SMIADS}$ Valid Delay	C_L=50pF	3, 6	4	25	ns
11	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{ADS}$ Float Delay	(Note 1)	10	4	30	ns
11s	$\overline{SMIADS}$ Float Delay	(Note 1)	10	4	30	ns
12	D31–D0 Write Data Valid Delay	C_L = 50 pF	6, 7, 9	7	27	ns
12a	D31–D0 Write Data Hold Time	C_L = 50 pF	3, 8	2		ns
13	D31–D0 Float Delay	(Note 1)	10	4	22	ns
14	HLDA Valid Delay	C_L = 50 pF	3, 10	4	22	ns
15	$\overline{NA}$ Setup Time		5	7		ns
16	$\overline{NA}$ Hold Time		5	3		ns
17	$\overline{BS16}$ Setup Time		5	7		ns
18	$\overline{BS16}$ Hold Time		5	3		ns
19	$\overline{READY}$ Setup Time		5	9		ns
19s	$\overline{SMIRDY}$ Setup Time		5	9		ns
20	$\overline{READY}$ Hold Time		5	4		ns
20s	$\overline{SMIRDY}$ Hold Time		5	4		ns
21	D31–D0 Read Setup Time		5	7		ns
22	D31–D0 Read Hold Time		5	5		ns
23	HOLD Setup Time		5	15		ns
24	HOLD Hold Time		5	3		ns
25	RESET Setup Time		11	10		ns
26	RESET Hold Time		11	3		ns
27	NMI, INTR Setup Time	(Note 2)	5	6		ns
27s	$\overline{SMI}$ Setup Time		5	6		ns
28	NMI, INTR Hold Time	(Note 2)	5	6		ns
28s	$\overline{SMI}$ Hold Time		5	6		ns
29	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$ Setup Time	(Note 2)	5	6		ns
30	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$, $\overline{FLT}$ Hold Time	(Note 2)	5	5		ns

Notes: 1. Float condition occurs when maximum output current becomes less than I_{LO} magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
3. Rise and fall times are not tested.

SWITCHING CHARACTERISTICS (continued)



C_L includes all parasitic capacitances.

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Figure 3. AC Test Load

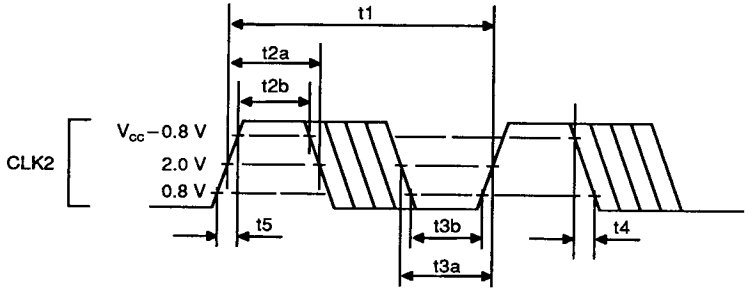

Figure 4. CLK2 Timing

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SWITCHING WAVEFORMS

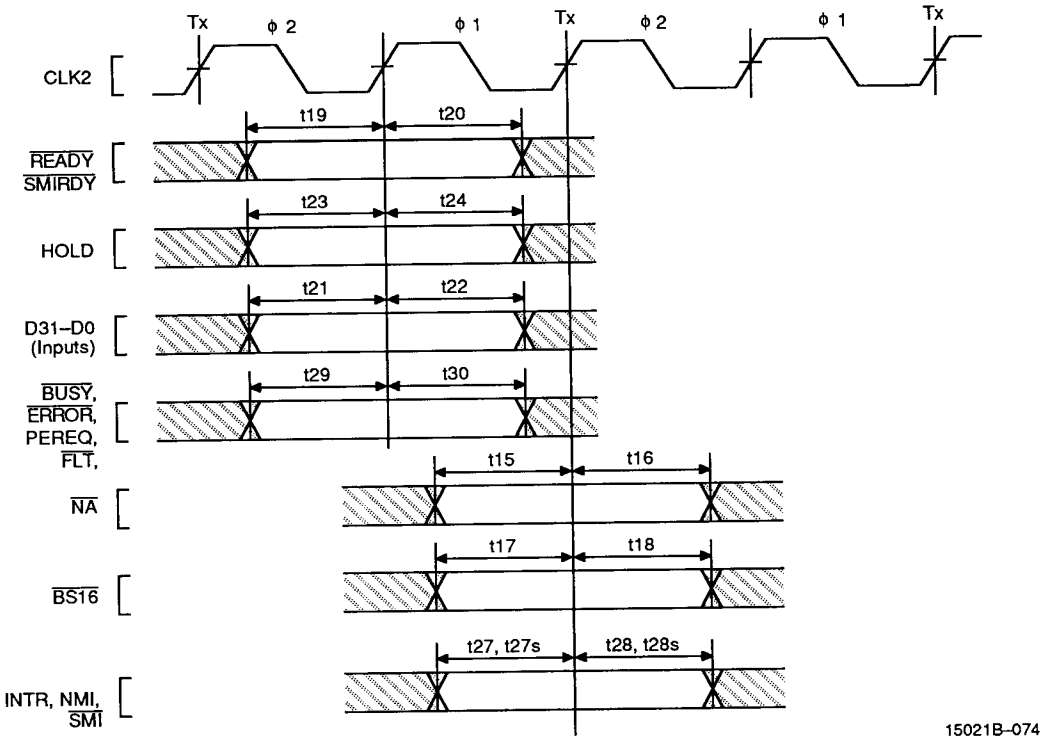

Figure 5. Input Setup and Hold Timing

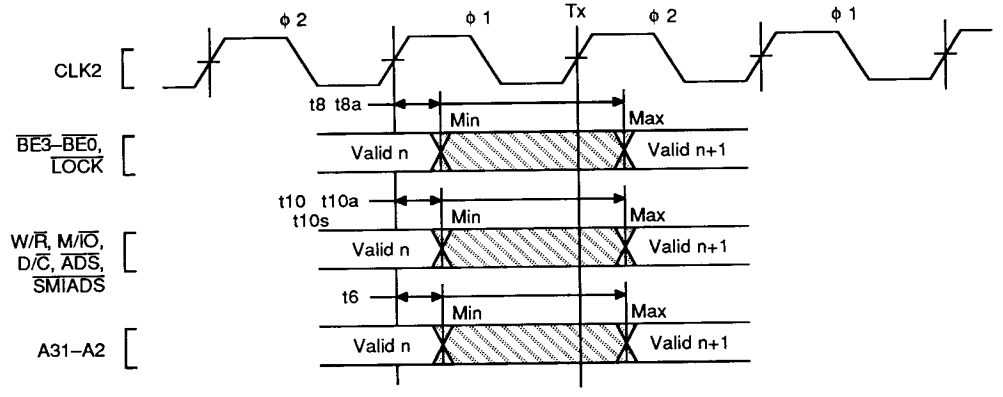

Figure 6. Output Valid Delay Timing

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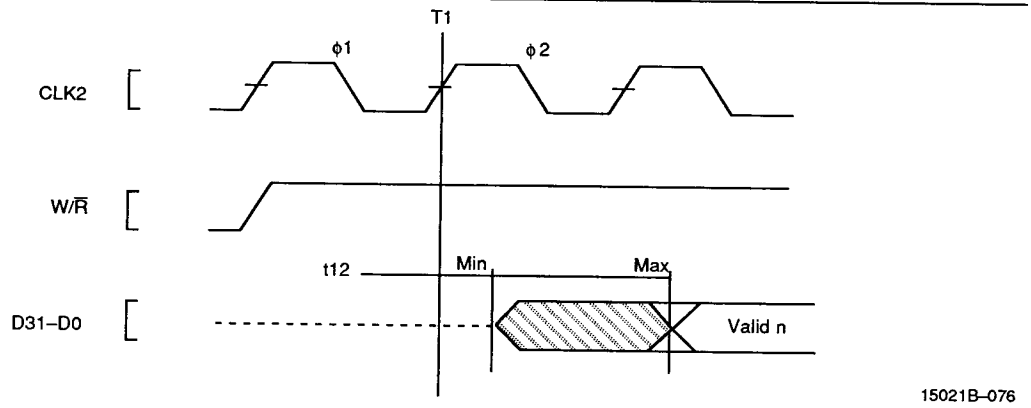


Figure 7. Write Data Valid Delay Timing (25 and 33 MHz)

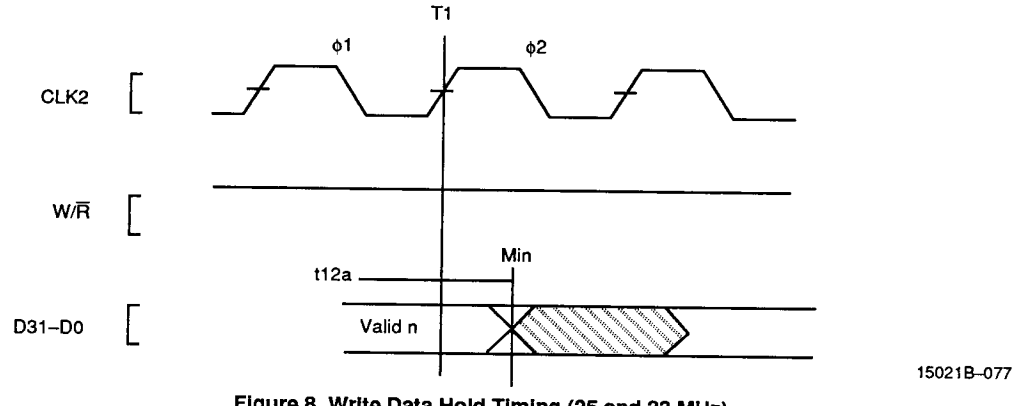


Figure 8. Write Data Hold Timing (25 and 33 MHz)

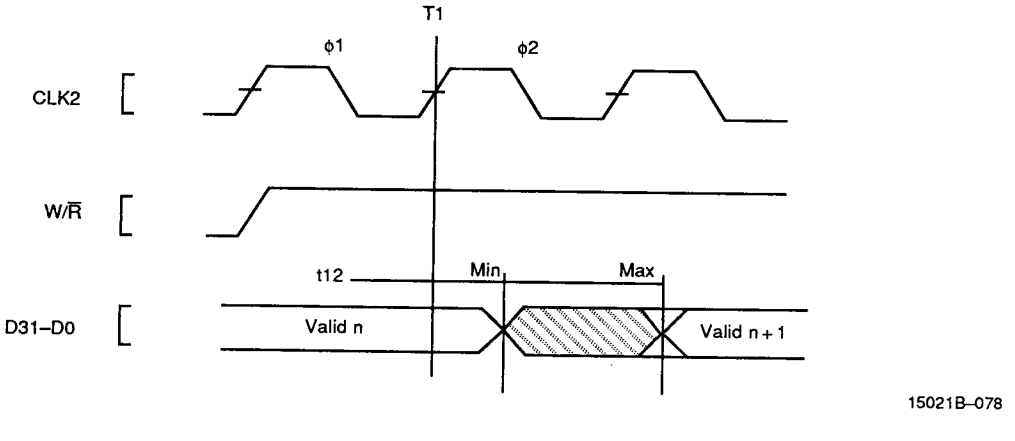


Figure 9. Write Data Valid Delay Timing (20 MHz)

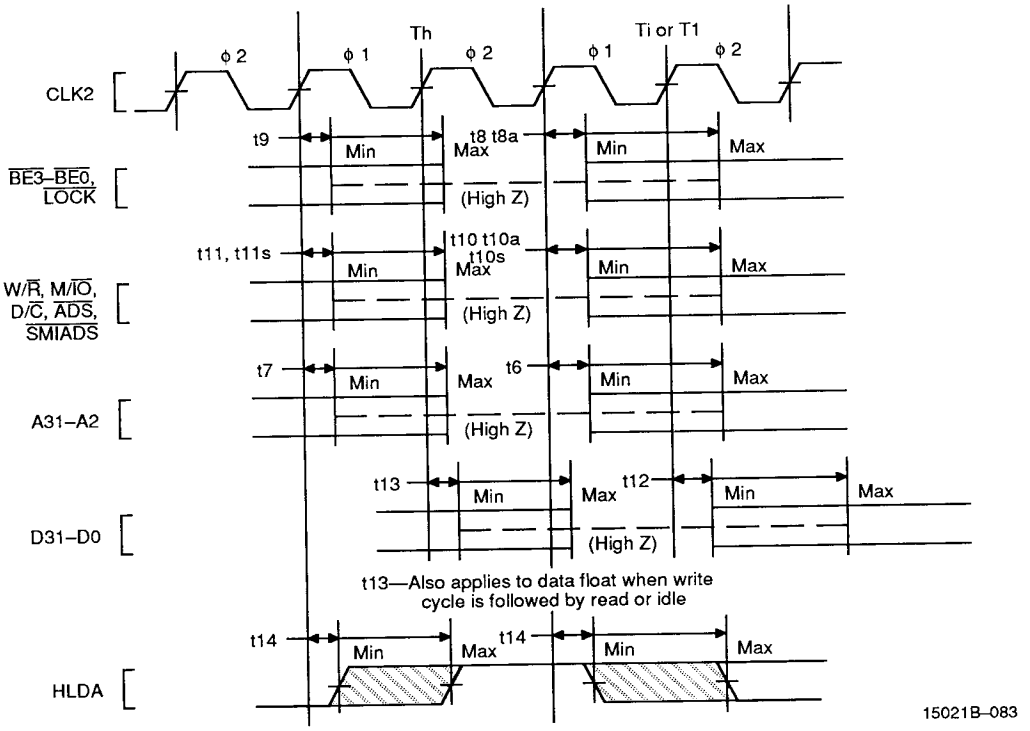
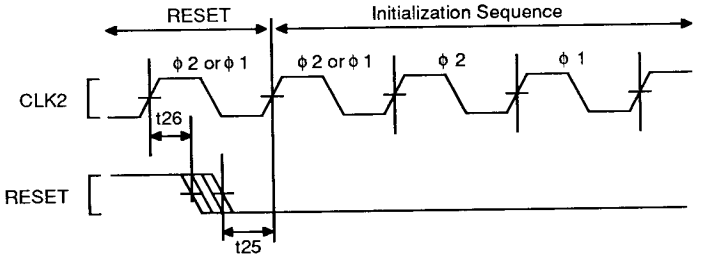


Figure 10. Output Float Delay and HLDA Valid Delay Timing



The second internal processor phase following RESET High-to-Low transition (provided t25 and t26 are met) is φ2.

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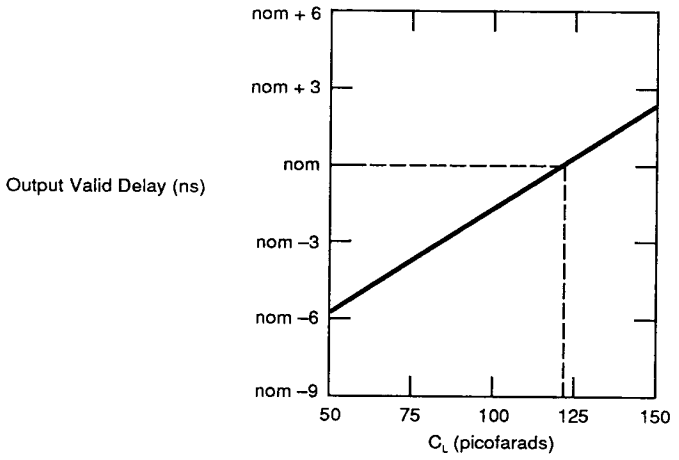
Figure 11. RESET Setup and Hold Timing and Internal Phase



Note: This graph will not be linear outside of the C_L range shown.

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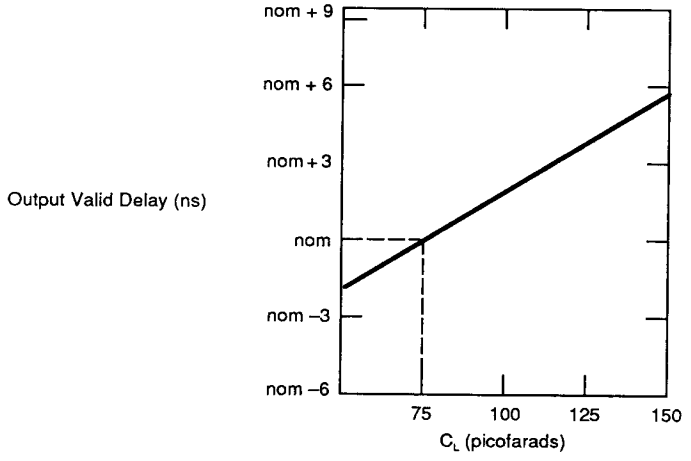
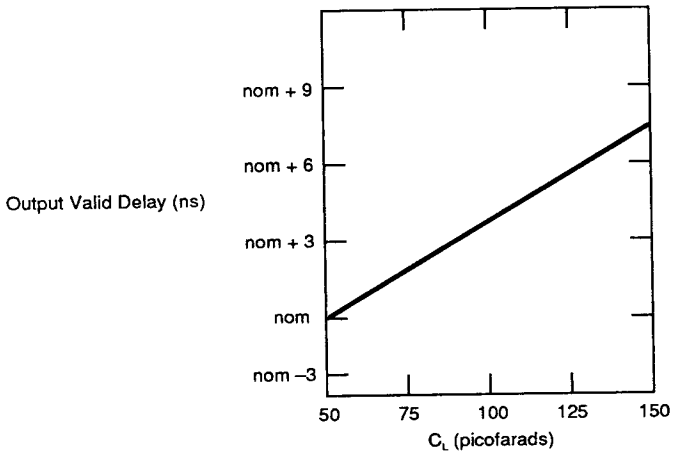
Figure 12. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature (C_L=120 pF)



Note: This graph will not be linear outside of the C_L range shown.

15021B–080

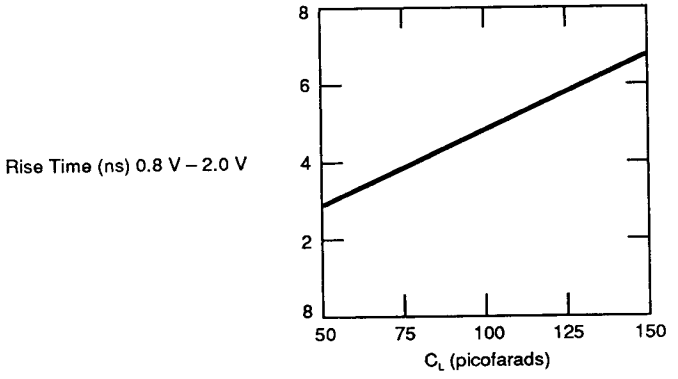
Figure 13. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature (C_L = 75 pF)



Note: This graph will not be linear outside of the C_L range shown.

15021B–081

Figure 14. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature (C_L = 50 pF)



Note: This graph will not be linear outside of the C_L range shown.

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Figure 15. Typical Output Rise Time Versus Load Capacitance at Maximum Operating Temperature