Am386™DXL

High-Performance, Low-Power, 32-Bit Microprocessor

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Ideal for portable PCs**
  - –True static design for long battery life
  - –Typical standby Icc < 0.08 mA at DC
  - –Typical operating Icc < 275 mA at 33 MHz
  - –Lower power consumption than Intel 386DX or Intel 386SX
  - –Small footprint 132-pin PQFP package*
  - –Wide range of chip sets and BIOS available to support standby mode capabilities
  - –Performance on demand (0 to 40 MHz)
- **Ideal for desktop PCs**
  - –40-, 33-, 25-, and 20-MHz operating speeds
  - –Lower heat dissipation facilitates fan reduction or elimination for cost savings and size/noise reduction
  - –Pin-for-pin replacement for Intel 386DX
- **Compatible with 386DX systems and software**
- **Supports 387DX-compatible math coprocessors**
- **AMD® advanced 0.8 micron CMOS technology**

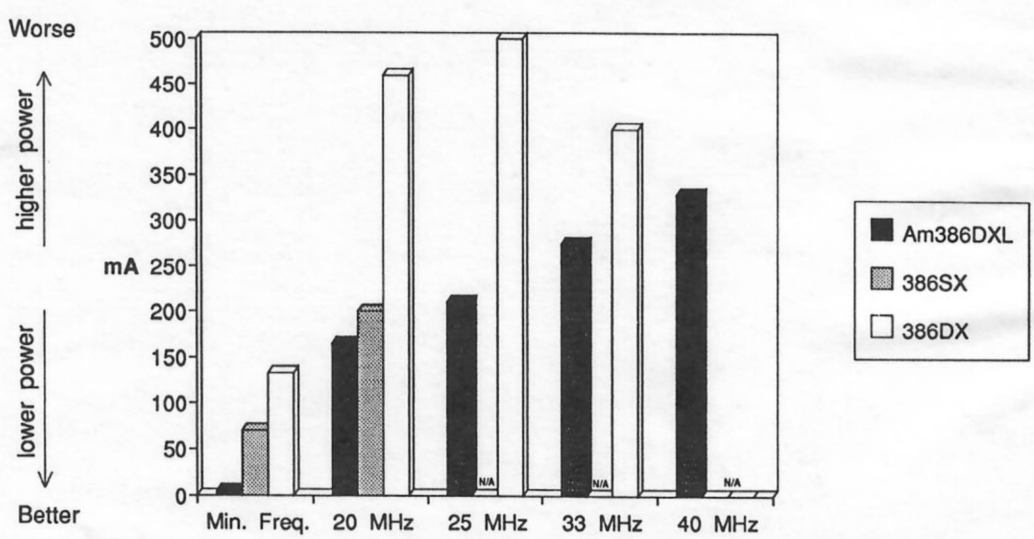
GENERAL DESCRIPTION

The Am386DXL microprocessor is a high-speed, true static implementation of the Intel 386DX microprocessor. It is ideal for both desktop and battery-powered portable personal computers. For desktop PCs, the Am386DXL microprocessor offers a 21% increase in the maximum operating speed from 33 to 40 MHz. Also, this device offers lower heat dissipation, allowing system designers to remove or reduce the size and cost of the system cooling fan.

For portables, the Am386DXL microprocessor's true static design offers longer battery life with low operating power consumption and standby mode. At 33 MHz, this device has 40% lower operating Icc than the Intel 386DX. Standby mode allows the Am386DXL microprocessor to be clocked down to 0 MHz (DC) and retain full register contents. In standby mode, typical current draw is less than 0.08 mA, a nearly 1000x reduction in power consumption versus the Intel 386DX or Intel 386SX.

Additionally, the Am386DXL microprocessor will be available in a small footprint 132-pin plastic quad flat pack (PQFP) package*. This surface-mount package is 40% smaller than a PGA package, allowing smaller, lower-cost board designs without the need for a socket.

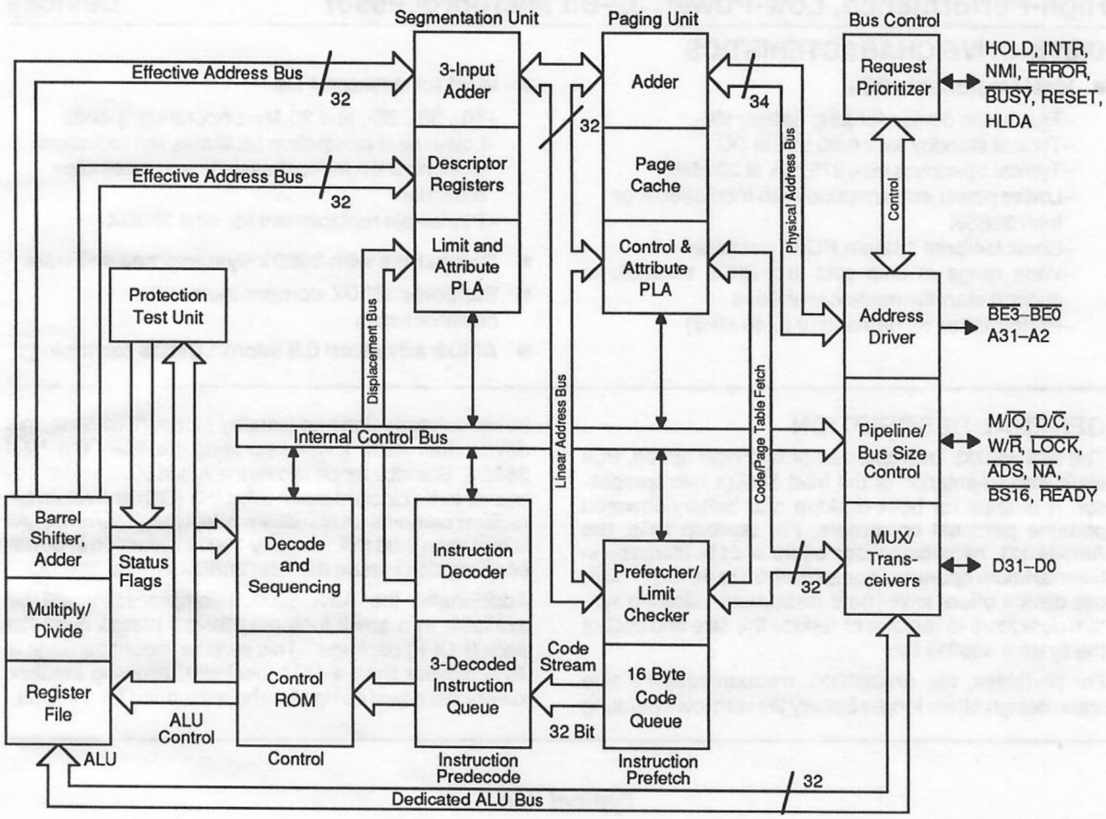
Typical Icc



*Preliminary Information

Publication # 15484 Rev. A Amendment /0
Issue Date: March 1991

BLOCK DIAGRAM



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INTRODUCTION

AMD is proud to provide the Am386DXL microprocessor at a time when the personal computer market requires alternatives. Alternate source manufacturers traditionally increase availability, add features, and broaden the market. AMD has focused significant engineering resources to bring you these benefits.

AMD's track record with the 80286 shows that we were first to raise the performance of the 80286 from 8 MHz to 10, 12, and 16 MHz. We were first to offer new packaging technology with a smaller, lower cost PLCC. Today, over 90% of all 80286s sold use PLCC packaging. AMD is committed to similar advances with the Am386DXL microprocessor.

The Am386DXL microprocessor is more than just a re-creation of the Intel 386DX. Highly skilled engineers in our Austin, Texas facility, added enhancements to the microprocessor through the use of our advanced 0.8 micron CMOS technology. These enhancements include a true static design, a low cost small footprint PQFP package, and an increase in the maximum operating speed to 40 MHz. The true static design allows for lower operating power consumption, as well as standby mode for lower heat dissipation in desktop PCs and longer battery life in portables.

AMD engineered the Am386DXL microprocessor to insure compatibility with the installed base of hardware and software for the 386-based personal computers. The Am386DXL microprocessor is your solution to meet the demand for high-performance, 32-bit desktop and portable personal computers.

FUNCTIONAL DESCRIPTION

True Static Operation

The Am386DXL microprocessor incorporates a true static design. Unlike dynamic circuit design, the Am386DXL device eliminates the minimum operating frequency restriction. It may be clocked from its maximum speed of 40 MHz all the way down to 0 MHz (DC). System designers can use this feature to design true 32-bit battery-powered portable PCs with long battery life.

Standby Mode

This true static design allows for a standby mode. At any of its operating speeds (40 MHz to DC), the Am386DXL microprocessor will retain its state (i.e., the contents of all of its registers). By shutting off the clock completely, the device enters standby mode. Since power consumption is a function of clock frequency, operating power consumption is reduced as the frequency is lowered. In standby mode, typical current draw is reduced to less than 0.08 mA at DC.

Not only does this feature save battery life, but it also simplifies the design of power-conscious notebook computers in the following ways.

1. Eliminates the need for software in BIOS to save and restore the contents of registers.
2. Allows simpler circuitry to control stopping of the clock (since) the system does not need to know what state the processor is in.

Lower Operating I_{CC}

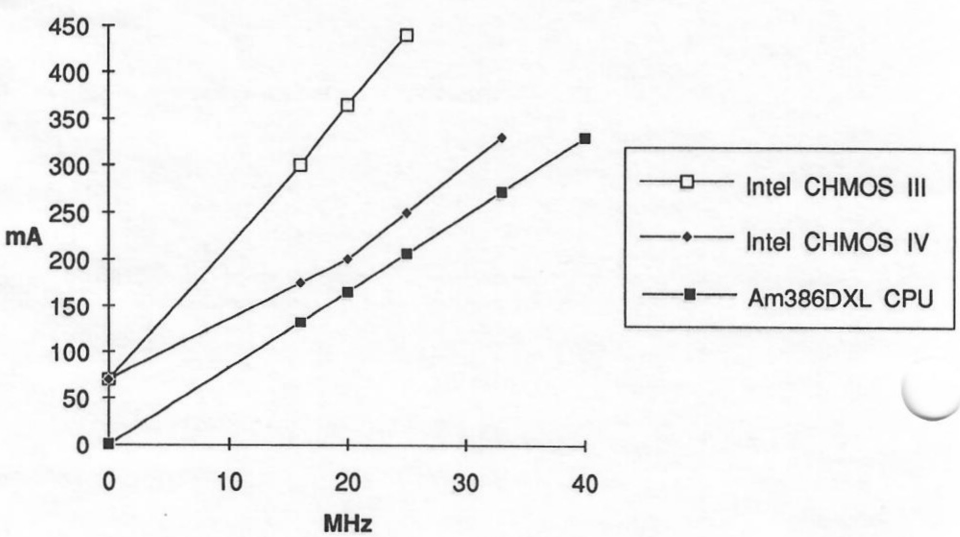
True static design also allows lower operating I_{CC} when operating at any speed. See the following graph for typical current at operating speeds.

Performance On Demand

The Am386DXL microprocessor retains its state at any speed from 0 MHz (DC) to its maximum operating speed (20, 25, 33, or 40 MHz). With this feature, system designers may vary the operating speed of the system to extend the battery life in portable systems.

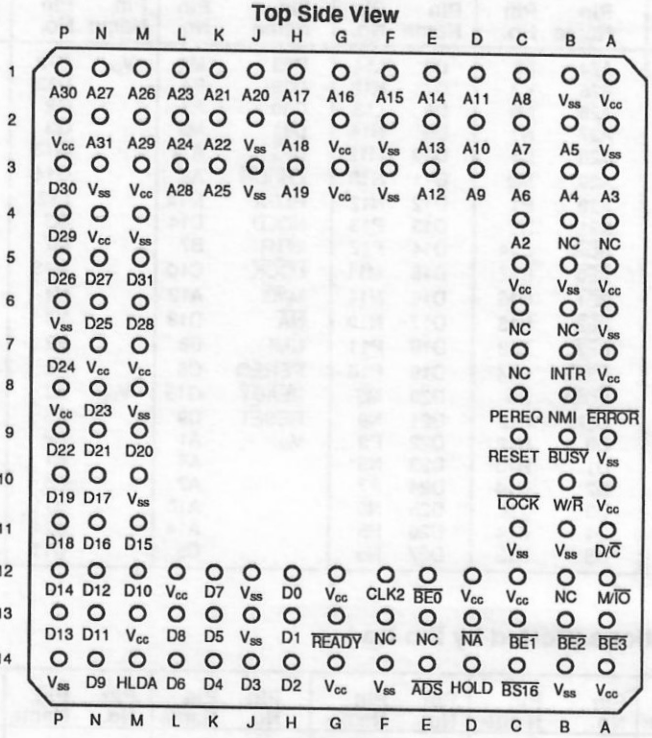
For example, the system could operate at low speeds during inactivity or polling operations. However, upon interrupt, the system clock can be increased up to its maximum speed. After a user-defined time-out period, the system can be returned to a low (or 0 MHz) operating speed without losing its state. This design maximizes battery life while achieving optimal performance.

Typical Icc

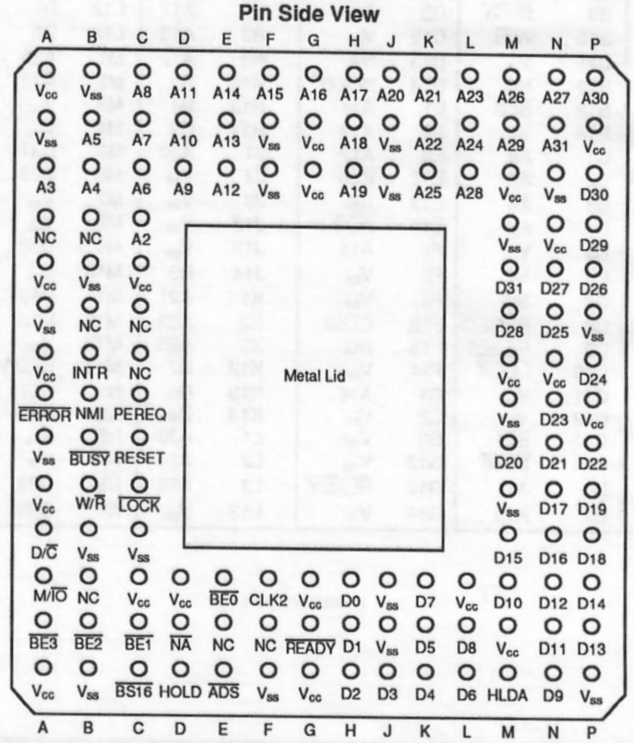


CONNECTION DIAGRAMS
132-Lead Ceramic Pin Grid Array (PGA) Package

Top Side View



Pin Side View



PGA Pin Designations (Functional Grouping)

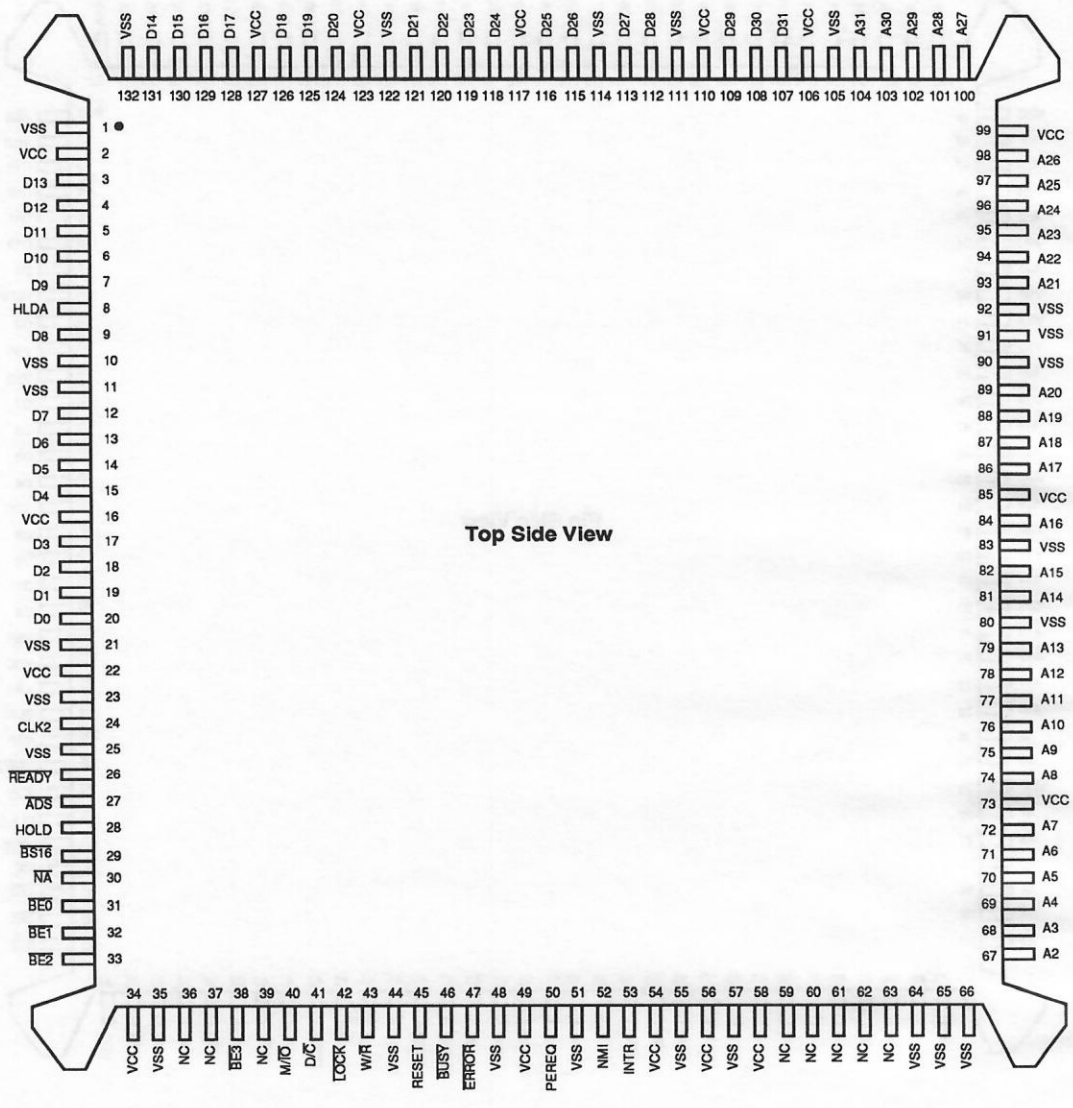
Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A2	C4	A24	L2	D6	L14	D28	M6	V_{CC}	C12	V_{SS}	F2
A3	A3	A25	K3	D7	K12	D29	P4		D12		F3
A4	B3	A26	M1	D8	L13	D30	P3		G2		F14
A5	B2	A27	N1	D9	N14	D31	M5		G3		J2
A6	C3	A28	L3	D10	M12	D/$\overline{C}$	A11		G12		J3
A7	C2	A29	M2	D11	N13	$\overline{ERROR}$	A8		G14		J12
A8	C1	A30	P1	D12	N12	HLDA	M14		L12		J13
A9	D3	A31	N2	D13	P13	HOLD	D14		M3		M4
A10	D2	$\overline{ADS}$	E14	D14	P12	INTR	B7		M7		M8
A11	D1	$\overline{BE0}$	E12	D15	M11	$\overline{LOCK}$	C10		M13		M10
A12	E3	$\overline{BE1}$	C13	D16	N11	M/$\overline{IO}$	A12		N4		N3
A13	E2	$\overline{BE2}$	B13	D17	N10	$\overline{NA}$	D13		N7		P6
A14	E1	$\overline{BE3}$	A13	D18	P11	NMI	B8		P2		P14
A15	F1	$\overline{BS16}$	C14	D19	P10	PEREQ	C8		P8	W/$\overline{R}$	B10
A16	G1	$\overline{BUSY}$	B9	D20	M9	$\overline{READY}$	G13	V_{SS}	A2	NC	A4
A17	H1	CLK2	F12	D21	N9	RESET	C9		A6		B4
A18	H2	D0	H12	D22	P9	V_{CC}	A1		A9		B6
A19	H3	D1	H13	D23	N8		A5		B1		B12
A20	J1	D2	H14	D24	P7		A7		B5		C6
A21	K1	D3	J14	D25	N6		A10		B11		C7
A22	K2	D4	K14	D26	P5		A14		B14		E13
A23	L1	D5	K13	D27	N5		C5		C11		F13

PGA Pin Designations (Sorted by Pin No.)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	V_{CC}	B9	$\overline{BUSY}$	D3	A9	H1	A17	L13	D8	N7	V_{CC}
A2	V_{SS}	B10	W/$\overline{R}$	D12	V_{CC}	H2	A18	L14	D6	N8	D23
A3	A3	B11	V_{SS}	D13	$\overline{NA}$	H3	A19	M1	A26	N9	D21
A4	NC	B12	NC	D14	HOLD	H12	D0	M2	A29	N10	D17
A5	V_{CC}	B13	$\overline{BE2}$	E1	A14	H13	D1	M3	V_{CC}	N11	D16
A6	V_{SS}	B14	V_{SS}	E2	A13	H14	D2	M4	V_{SS}	N12	D12
A7	V_{CC}	C1	A8	E3	A12	J1	A20	M5	D31	N13	D11
A8	$\overline{ERROR}$	C2	A7	E12	$\overline{BE0}$	J2	V_{SS}	M6	D28	N14	D9
A9	V_{SS}	C3	A6	E13	NC	J3	V_{SS}	M7	V_{CC}	P1	A30
A10	V_{CC}	C4	A2	E14	$\overline{ADS}$	J12	V_{SS}	M8	V_{SS}	P2	V_{CC}
A11	D/$\overline{C}$	C5	V_{CC}	F1	A15	J13	V_{SS}	M9	D20	P3	D30
A12	M/$\overline{IO}$	C6	NC	F2	V_{SS}	J14	D3	M10	V_{SS}	P4	D29
A13	$\overline{BE3}$	C7	NC	F3	V_{SS}	K1	A21	M11	D15	P5	D26
A14	V_{CC}	C8	PEREQ	F12	CLK2	K2	A22	M12	D10	P6	V_{SS}
B1	V_{SS}	C9	RESET	F13	NC	K3	A25	M13	V_{CC}	P7	D24
B2	A5	C10	$\overline{LOCK}$	F14	V_{SS}	K12	D7	M14	HLDA	P8	V_{CC}
B3	A4	C11	V_{SS}	G1	A16	K13	D5	N1	A27	P9	D22
B4	NC	C12	V_{CC}	G2	V_{CC}	K14	D4	N2	A31	P10	D19
B5	V_{SS}	C13	$\overline{BE1}$	G3	V_{CC}	L1	A23	N3	V_{SS}	P11	D18
B6	NC	C14	$\overline{BS16}$	G12	V_{CC}	L2	A24	N4	V_{CC}	P12	D14
B7	INTR	D1	A11	G13	$\overline{READY}$	L3	A28	N5	D27	P13	D13
B8	NMI	D2	A10	G14	V_{CC}	L12	V_{CC}	N6	D25	P14	V_{SS}

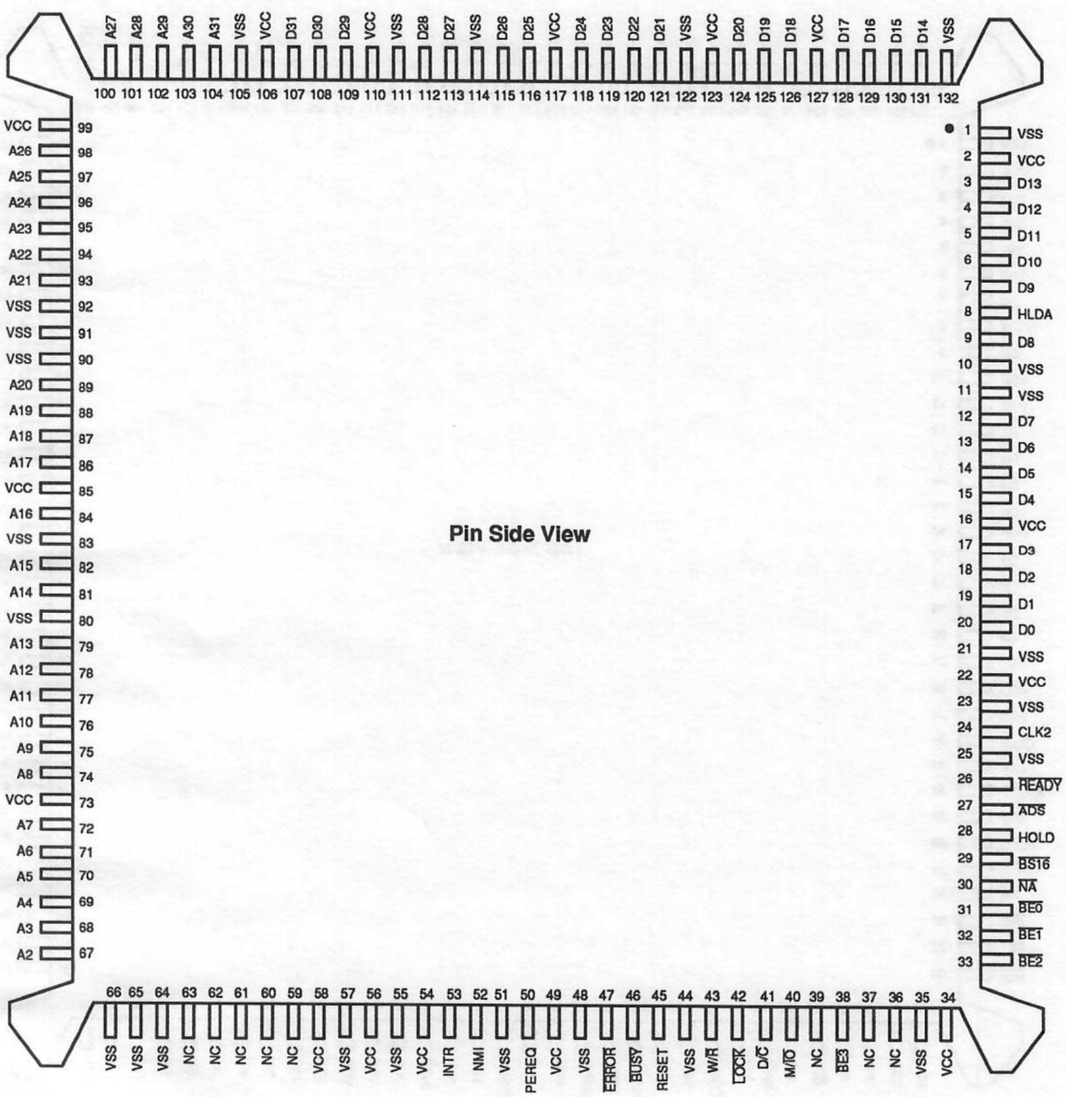
CONNECTION DIAGRAMS

132-Lead Plastic Quad Flat Pack (PQFP) Package*



Notes: Pin 1 is marked for orientation.
*Preliminary Information.

CONNECTION DIAGRAMS (continued)



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Note: Pin 1 is marked for orientation.

PQFP Pin Designations* (Functional Grouping)

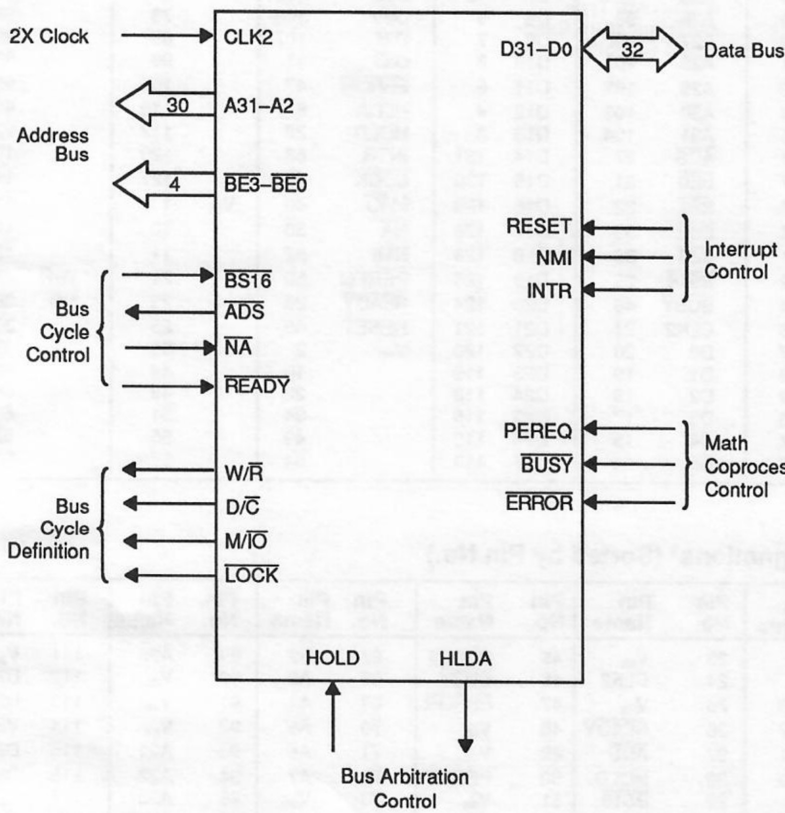
Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
A2	67	A24	96	D6	13	D28	112	V_{CC}	56	V_{SS}	64
A3	68	A25	97	D7	12	D29	109		58		65
A4	69	A26	98	D8	9	D30	108		73		66
A5	70	A27	100	D9	7	D31	107		85		80
A6	71	A28	101	D10	6	D/$\overline{C}$	41		99		83
A7	72	A29	102	D11	5	$\overline{ERROR}$	47		106		90
A8	74	A30	103	D12	4	HLDA	8		110		91
A9	75	A31	104	D13	3	HOLD	28		117		92
A10	76	$\overline{ADS}$	27	D14	131	INTR	53		123		105
A11	77	$\overline{BE0}$	31	D15	130	$\overline{LOCK}$	42		127		111
A12	78	$\overline{BE1}$	32	D16	129	M/$\overline{IO}$	40	V_{SS}	1		114
A13	79	$\overline{BE2}$	33	D17	128	$\overline{NA}$	30		10		122
A14	81	$\overline{BE3}$	38	D18	126	NMI	52		11		132
A15	82	$\overline{BS16}$	29	D19	125	PEREQ	50		21	W/$\overline{R}$	43
A16	84	$\overline{BUSY}$	46	D20	124	$\overline{READY}$	26		23	NC	36
A17	86	CLK2	24	D21	121	RESET	45		25		37
A18	87	D0	20	D22	120	V_{CC}	2		35		39
A19	88	D1	19	D23	119		16		44		59
A20	89	D2	18	D24	118		22		48		60
A21	93	D3	17	D25	116		34		51		61
A22	94	D4	15	D26	115		49		55		62
A23	95	D5	14	D27	113		54		57		63

PQFP Pin Designations* (Sorted by Pin No.)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{SS}	23	V_{SS}	45	$\overline{RESET}$	67	A2	89	A20	111	V_{SS}
2	V_{CC}	24	CLK2	46	$\overline{BUSY}$	68	A3	90	V_{SS}	112	D28
3	D13	25	V_{SS}	47	$\overline{ERROR}$	69	A4	91	V_{SS}	113	D27
4	D12	26	$\overline{READY}$	48	V_{SS}	70	A5	92	V_{SS}	114	VSS
5	D11	27	$\overline{ADS}$	49	V_{CC}	71	A6	93	A21	115	D26
6	D10	28	HOLD	50	PEREQ	72	A7	94	A22	116	D25
7	D9	29	$\overline{BS16}$	51	V_{SS}	73	V_{CC}	95	A23	117	V_{CC}
8	HLDA	30	$\overline{NA}$	52	NMI	74	A8	96	A24	118	D24
9	D8	31	$\overline{BE0}$	53	INTR	75	A9	97	A25	119	D23
10	V_{SS}	32	$\overline{BE1}$	54	V_{CC}	76	A10	98	A26	120	D22
11	V_{SS}	33	$\overline{BE2}$	55	V_{SS}	77	A11	99	V_{CC}	121	D21
12	D7	34	V_{CC}	56	V_{CC}	78	A12	100	A27	122	V_{SS}
13	D6	35	V_{SS}	57	V_{SS}	79	A13	101	A28	123	V_{CC}
14	A5	36	NC	58	V_{CC}	80	V_{SS}	102	A29	124	D20
15	D4	37	NC	59	NC	81	A14	103	A30	125	D19
16	V_{CC}	38	$\overline{BE3}$	60	NC	82	A15	104	A31	126	D18
17	D3	39	NC	61	NC	83	V_{SS}	105	V_{SS}	127	V_{CC}
18	D2	40	M/$\overline{IO}$	62	NC	84	A16	106	V_{CC}	128	D17
19	D1	41	D/$\overline{C}$	63	NC	85	V_{CC}	107	D31	129	D16
20	D0	42	$\overline{LOCK}$	64	V_{SS}	86	A17	108	D30	130	D15
21	V_{SS}	43	W/$\overline{R}$	65	V_{SS}	87	A18	109	D29	131	D14
22	V_{CC}	44	V_{SS}	66	V_{SS}	88	A19	110	V_{CC}	132	V_{SS}

*Preliminary Information

LOGIC SYMBOL



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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number/Description**
b. Package Type
c. Temperature Range
d. Speed Option

A 80386DXL -33

c. TEMPERATURE RANGE

Blank = Commercial (T_C = 0 to +85°C for PGA)
(T_C = 0 to +100°C for PQFP*)

d. SPEED OPTION

–40 = 40 MHz
–33 = 33 MHz
–25 = 25 MHz
–20 = 20 MHz

a. DEVICE NUMBER/DESCRIPTION

80386DXL
Am386DXL High-Performance, Low-Power, 32-Bit Microprocessor

b. PACKAGE TYPE

A = 132-Lead Ceramic Pin Grid Array (PGA 132)
NG = 132-Lead Plastic Quad Flat Pack* (PQ132, PQB132)

Valid Combinations		
A	80386DXL	–40 –33 –25 –20

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. All speeds may not be available in all package combinations. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

*Preliminary Information.

PIN DESCRIPTION

A31–A2

Address Bus (Outputs)

Outputs physical memory or port I/O addresses.

$\overline{\text{ADS}}$

Address Status (Active Low; Output)

Indicates that a valid bus cycle definition and address (W/$\overline{\text{R}}$, D/$\overline{\text{C}}$, M/$\overline{\text{IO}}$, $\overline{\text{BE0}}$, $\overline{\text{BE1}}$, $\overline{\text{BE2}}$, $\overline{\text{BE3}}$, and A31–A2) are being driven at the Am386DXL microprocessor pins.

$\overline{\text{BE3}}$–$\overline{\text{BE0}}$

Byte Enables (Active Low; Outputs)

Indicate which data bytes of the data bus take part in a bus cycle.

$\overline{\text{BS16}}$

Bus Size 16 (Active Low; Input)

Allows direct connection of 32-bit and 16-bit data buses.

$\overline{\text{BUSY}}$

Busy (Active Low; Input)

Signals a busy condition from a processor extension.

CLK2

Clock (Input)

Provides the fundamental timing for the Am386DXL microprocessor.

D31–D0

Data Bus (Inputs/Outputs)

Inputs data during memory, I/O, and interrupt acknowledge read cycles; and outputs data during memory and I/O write cycles.

D/$\overline{\text{C}}$

Data/Control (Output)

A bus cycle definition pin that distinguishes data cycles, either memory or I/O, from control cycles which are: interrupt acknowledge, halt, and instruction fetching.

$\overline{\text{ERROR}}$

Error (Active Low; Input)

Signals an error condition from a processor extension.

HLDA

Bus Hold Acknowledge (Active High; Output)

Indicates that the Am386DXL microprocessor surrendered control of its local bus to another bus master.

HOLD

Bus Hold Request (Active High; Input)

Allows another bus master to request control of the local bus.

INTR

Interrupt Request (Active High; Input)

A maskable input that signals the Am386DXL microprocessor to suspend execution of the current program and execute an interrupt acknowledge function.

$\overline{\text{LOCK}}$

Bus Lock (Active Low; Output)

A bus cycle definition pin that indicates that other system bus masters are denied access to the system bus while it is active.

M/$\overline{\text{IO}}$

Memory I/O (Output)

A bus cycle definition pin that distinguishes memory cycles from input/output cycles.

$\overline{\text{NA}}$

Next Address (Active Low; Input)

Used to request address pipelining.

NC

No Connect

Should always remain unconnected. Connection of a NC pin may cause the processor to malfunction or be incompatible with future steppings of the Am386DXL microprocessor.

NMI

Non-Maskable Interrupt Request (Active High; Input)

A non-maskable input that signals the Am386DXL microprocessor to suspend execution of the current program and execute an interrupt acknowledge function.

PEREQ

Processor Extension Request (Active High; Input)

Indicates that the processor extension has data to be transferred by the Am386DXL microprocessor.

$\overline{\text{READY}}$

Bus Ready (Active Low; Input)

Terminates the bus cycle.

RESET

Reset (Active High; Input)

Suspends any operation in progress and places the Am386DXL microprocessor in a known reset state.

V_{CC}

System Power (Active High; Input)

Provides the +5 V nominal DC supply input.

V_{SS}

System Ground (Input)

System ground provides 0 V connection from which all inputs and outputs are measured.

W/$\overline{\text{R}}$

Write/Read (Output)

A bus cycle definition pin that distinguishes write cycles from read cycles.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... –65°C to +150°C
Case Temperature Under Bias .... –65°C to +110°C
Supply Voltage with Respect to Vss .... –0.5 V to +6.5 V
Voltage on Other Pins .... –0.5 V to Vcc +0.5 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

DC CHARACTERISTICS over COMMERCIAL operating ranges

V_{CC} = 5 V ±5%; T_{CASE} = 0°C to +85°C (PGA)
V_{CC} = 5 V ±10%; T_{CASE} = 0°C to +100°C (PQFP*)

Symbol	Parameter Description	Notes	Min	Max	Unit
V_{IL}	Input Low Voltage	(Note 1)	–0.3	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.3	V
V_{ILC}	CLK2 Input Low Voltage	(Note 1)	–0.3	0.8	V
V_{IHC}	CLK2 Input High Voltage 20 MHz 25, 33, and 40 MHz		 V_{CC} – 0.8 3.7	 V_{CC} + 0.3 V_{CC} + 0.3	 V V
V_{OL}	Output Low Voltage I_{OL} = 4 mA: A31–A2, D31–D0 I_{OL} = 5 mA: $\overline{BE3}$–$\overline{BE0}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, HLDA			 0.45 0.45	 V V
V_{OH}	Output High Voltage I_{OH} = 1 mA: A31–A2, D31–D0 I_{OH} = 0.9 mA: $\overline{BE3}$–$\overline{BE0}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{ADS}$, HLDA		 2.4 2.4		 V V
I_{LI}	Input Leakage Current (All pins except $\overline{BS16}$, PEREQ, $\overline{BUSY}$, and $\overline{ERROR}$)	0 V ≤ V_{IN} ≤ V_{CC}		±15	µA
I_{IH}	Input Leakage Current (PEREQ Pin)	V_{IH} = 2.4 V (Note 2)		200	µA
I_{IL}	Input Leakage Current ($\overline{BS16}$, $\overline{BUSY}$, and $\overline{ERROR}$)	V_{IL} = 0.45 (Note 3)		–400	µA
I_{LO}	Output Leakage Current	0.45 V ≤ V_{OUT} ≤ V_{CC}		±15	µA
I_{CC}	Supply Current CLK2 = 40 MHz: with –20 CLK2 = 50 MHz: with –25 CLK2 = 66 MHz: with –33 CLK2 = 80 MHz: with –40	(Note 4) I_{CC} Typ = 165 I_{CC} Typ = 210 I_{CC} Typ = 275 I_{CC} Typ = 330		 200 250 330 400	 mA mA mA mA
I_{CCSB}	Standby Current	I_{CCSB} Typ = 0.08 mA (Notes 4, 5)		1	mA
C_{IN}	Input or I/O Capacitance	F_C = 1 MHz (Note 4)		10	pF
C_{OUT}	Output Capacitance	F_C = 1 MHz (Note 4)		12	pF
C_{CLK}	CLK2 Capacitance	F_C = 1 MHz (Note 4)		20	pF

Notes: 1. The Min value, –0.3, is not 100% tested.
2. PEREQ input has an internal pulldown resistor.
3. $\overline{BS16}$, $\overline{BUSY}$, and $\overline{ERROR}$ inputs each have an internal pullup resistor.
4. Not 100% tested.
5. Measurement taken with $\overline{BS16}$, $\overline{BUSY}$, and $\overline{ERROR}$ at V_{CC} voltage level.

*Preliminary Information.

SWITCHING CHARACTERISTIC over operating range

V_{CC} = 5 V ±5%; T_{CASE} = 0°C to +85°C

No.	Parameter Description	Notes	Ref Figure	40 MHz Min	40 MHz Max	Unit
	Operating Frequency	Half of CLK2 Freq		0	40	MHz
1	CLK2 Period		3	12.5		ns
2a	CLK2 High Time	at 2 V	3	5		ns
2b	CLK2 High Time	at 3.7 V	3	3.25		ns
3a	CLK2 Low Time	at 2 V	3	5		ns
3b	CLK2 Low Time	at 0.8 V	3	3.25		ns
4	CLK2 Fall Time	3.7 V to 0.8 V (Note 3)	3		4	ns
5	CLK2 Rise Time	0.8 V to 3.7 V (Note 3)	3		4	ns
6	A31–A2 Valid Delay	C_L = 50 pF	2, 5, 13	4	15	ns
7	A31–A2 Float Delay	(Note 1)	13	4	20	ns
8	$\overline{BE3}$–$\overline{BE0}$, $\overline{LOCK}$ Valid Delay	C_L = 50 pF	2, 5, 13	4	15	ns
9	$\overline{BE3}$–$\overline{BE0}$, $\overline{LOCK}$ Float Delay	(Note 1)	13	4	20	ns
10	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$ Valid Delay	C_L = 50 pF	2, 5, 13	4	15	ns
10a	$\overline{ADS}$ Valid Delay	C_L = 50 pF	2, 5, 13	4	14.5	ns
11	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{ADS}$ Float Delay	(Note 1)	13	4	20	ns
12	D31–D0 Write Data Valid Delay	C_L = 50 pF (Note 4)	2, 6, 13	7	24	ns
12a	D31–D0 Write Data Hold Time	C_L = 50 pF	2, 7	2		ns
13	D31–D0 Float Delay	(Note 1)	13	4	17	ns
14	HLDA Valid Delay	C_L = 50 pF	2, 13	4	20	ns
15	$\overline{NA}$ Setup Time		4	5		ns
16	$\overline{NA}$ Hold Time		4	2		ns
17	$\overline{BS16}$ Setup Time		4	5		ns
18	$\overline{BS16}$ Hold Time		4	2		ns
19	$\overline{READY}$ Setup Time		4	7		ns
20	$\overline{READY}$ Hold Time		4	4		ns
21	D31–D0 Read Setup Time		4	5		ns
22	D31–D0 Read Hold Time		4	3		ns
23	HOLD Setup Time		4	11		ns
24	HOLD Hold Time		4	2		ns
25	RESET Setup Time		14	5		ns
26	RESET Hold Time		14	2		ns
27	NMI, INTR Setup Time	(Note 2)	4	5		ns
28	NMI, INTR Hold Time	(Note 2)	4	5		ns
29	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$ Setup Time	(Note 2)	4	5		ns
30	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$ Hold Time	(Note 2)	4	4		ns

Notes: 1. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific clock period.
3. Rise and fall times are not tested.
4. Min time not 100% tested.

SWITCHING CHARACTERISTIC over operating range

V_{CC} = 5 V ±5%; T_{CASE} = 0°C to +85°C

No.	Parameter Description	Notes	Ref Figures	33 MHz Min	33 MHz Max	Unit
	Operating Frequency	Half of CLK2 Freq		0	33.3	MHz
1	CLK2 Period		3	15.0		ns
2a	CLK2 High Time	at 2 V	3	6.25		ns
2b	CLK2 High Time	at 3.7 V	3	4.5		ns
3a	CLK2 Low Time	at 2 V	3	6.25		ns
3b	CLK2 Low Time	at 0.8 V	3	4.5		ns
4	CLK2 Fall Time	3.7 V to 0.8 V (Note 3)	3		4	ns
5	CLK2 Rise Time	0.8 V to 3.7 V (Note 3)	3		4	ns
6	A31–A2 Valid Delay	C_L = 50 pF	2, 5, 13	4	15	ns
7	A31–A2 Float Delay	(Note 1)	13	4	20	ns
8	$\overline{BE3}$–$\overline{BE0}$, $\overline{LOCK}$ Valid Delay	C_L = 50 pF	2, 5, 13	4	15	ns
9	$\overline{BE3}$–$\overline{BE0}$, $\overline{LOCK}$ Float Delay	(Note 1)	13	4	20	ns
10	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$ Valid Delay	C_L = 50 pF	2, 5, 13	4	15	ns
10a	$\overline{ADS}$ Valid Delay	C_L = 50 pF	2, 5, 13	4	14.5	ns
11	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{ADS}$ Float Delay	(Note 1)	13	4	20	ns
12	D31–D0 Write Data Valid Delay	C_L = 50 pF (Note 4)	2, 6, 13	7	24	ns
12a	D31–D0 Write Data Hold Time	C_L = 50 pF	2, 7	2		ns
13	D31–D0 Float Delay	(Note 1)	13	4	17	ns
14	HLDA Valid Delay	C_L = 50 pF	2, 13	4	20	ns
15	$\overline{NA}$ Setup Time		4	5		ns
16	$\overline{NA}$ Hold Time		4	2		ns
17	$\overline{BS16}$ Setup Time		4	5		ns
18	$\overline{BS16}$ Hold Time		4	2		ns
19	$\overline{READY}$ Setup Time		4	7		ns
20	$\overline{READY}$ Hold Time		4	4		ns
21	D31–D0 Read Setup Time		4	5		ns
22	D31–D0 Read Hold Time		4	3		ns
23	HOLD Setup Time		4	11		ns
24	HOLD Hold Time		4	2		ns
25	RESET Setup Time		14	5		ns
26	RESET Hold Time		14	2		ns
27	NMI, INTR Setup Time	(Note 2)	4	5		ns
28	NMI, INTR Hold Time	(Note 2)	4	5		ns
29	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$ Setup Time	(Note 2)	4	5		ns
30	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$ Hold Time	(Note 2)	4	4		ns

Notes:
1. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
3. Rise and fall times are not tested.
4. Min time not 100% tested.

SWITCHING CHARACTERISTIC over operating range

V_{CC} = 5 V ±5; T_{CASE} = 0°C to +85°C (PGA)
V_{CC} = 5 V ±10%; T_{CASE} = 0°C to +100°C (PQFP*)

No.	Parameter Description	Notes	Ref Figures	25 MHz Min	25 MHz Max	Unit
	Operating Frequency	Half of CLK2 Freq		0	25	MHz
1	CLK2 Period		3	20		ns
2a	CLK2 High Time	at 2 V	3	7		ns
2b	CLK2 High Time	at 3.7 V	3	4		ns
3a	CLK2 Low Time	at 2 V	3	7		ns
3b	CLK2 Low Time	at 0.8 V	3	5		ns
4	CLK2 Fall Time	3.7 V to 0.8 V (Note 3)	3		7	ns
5	CLK2 Rise Time	0.8 V to 3.7 V (Note 3)	3		7	ns
6	A31–A2 Valid Delay	C_L = 50 pF	2, 5, 13	4	21	ns
7	A31–A2 Float Delay	(Note 1)	13	4	30	ns
8	$\overline{BE3}$–$\overline{BE0}$ Valid Delay	C_L = 50 pF	2, 5, 13	4	24	ns
8a	$\overline{LOCK}$ Valid Delay	CL = 50 pF	2, 5, 13	4	21	ns
9	$\overline{BE3}$–$\overline{BE0}$, $\overline{LOCK}$ Float Delay	(Note 1)	13	4	30	ns
10	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{ADS}$ Valid Delay	C_L = 50 pF	2, 5, 13	4	21	ns
11	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{ADS}$ Float Delay	(Note 1)	13	4	30	ns
12	D31–D0 Write Data Valid Delay	C_L = 50 pF	2, 6, 13	7	27	ns
12a	D31–D0 Write Data Hold Time	C_L = 50 pF	2, 7	2		ns
13	D31–D0 Float Delay	(Note 1)	13	4	22	ns
14	HLDA Valid Delay	C_L = 50 pF	2, 13	4	22	ns
15	$\overline{NA}$ Setup Time		4	7		ns
16	$\overline{NA}$ Hold Time		4	3		ns
17	$\overline{BS16}$ Setup Time		4	7		ns
18	$\overline{BS16}$ Hold Time		4	3		ns
19	$\overline{READY}$ Setup Time		4	9		ns
20	$\overline{READY}$ Hold Time		4	4		ns
21	D31–D0 Read Setup Time		4	7		ns
22	D31–D0 Read Hold Time		4	5		ns
23	HOLD Setup Time		4	15		ns
24	HOLD Hold Time		4	3		ns
25	RESET Setup Time		14	10		ns
26	RESET Hold Time		14	3		ns
27	NMI, INTR Setup Time	(Note 2)	4	6		ns
28	NMI, INTR Hold Time	(Note 2)	4	6		ns
29	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$ Setup Time	(Note 2)	4	6		ns
30	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$ Hold Time	(Note 2)	4	5		ns

Notes: 1. Float condition occurs when maximum output current becomes less than I_{LO} magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
3. Rise and fall times are not tested.

*Preliminary Information.

SWITCHING CHARACTERISTIC over operating range

V_{CC} = 5 V ±5%; T_{CASE} = 0°C to +85°C (PGA)
V_{CC} = 5 V ±10%; T_{CASE} = 0°C to +100°C (PQFP*)

No.	Parameter Description	Notes	Ref Figures	20 MHz Min	20 MHz Max	Unit
	Operating Frequency	Half of CLK2 Freq		0	20	MHz
1	CLK2 Period		3	25		ns
2a	CLK2 High Time	at 2 V	3	8		ns
2b	CLK2 High Time	at (V_{CC}–0.8 V)	3	5		ns
3a	CLK2 Low Time	at 2 V	3	8		ns
3b	CLK2 Low Time	at 0.8 V	3	6		ns
4	CLK2 Fall Time	(V_{CC}–0.8 V) to 0.8 V (Note 3)	3		8	ns
5	CLK2 Rise Time	0.8 V to (V_{CC}–0.8 V) (Note 3)	3		8	ns
6	A31–A2 Valid Delay	C_L = 120 pF	2, 5, 13	4	30	ns
7	A31–A2 Float Delay	(Note 1)	13	4	32	ns
8	$\overline{BE3}$–$\overline{BE0}$ Valid Delay	C_L = 75 pF	2, 5, 13	4	30	ns
9	$\overline{BE3}$–$\overline{BE0}$, $\overline{LOCK}$ Float Delay	(Note 1)	13	4	32	ns
10	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{ADS}$ Valid Delay	C_L = 75 pF	2, 5, 13	4	28	ns
11	W/$\overline{R}$, M/$\overline{IO}$, D/$\overline{C}$, $\overline{ADS}$ Float Delay	(Note 1)	13	4	30	ns
12	D31–D0 Write Data Valid Delay	C_L = 120 pF	2, 8, 13	4	38	ns
13	D31–D0 Float Delay	(Note 1)	13	4	27	ns
14	HLDA Valid Delay	C_L = 75 pF	2, 13	6	28	ns
15	$\overline{NA}$ Setup Time		4	9		ns
16	$\overline{NA}$ Hold Time		4	14		ns
17	$\overline{BS16}$ Setup Time		4	13		ns
18	$\overline{BS16}$ Hold Time		4	21		ns
19	$\overline{READY}$ Setup Time		4	12		ns
20	$\overline{READY}$ Hold Time		4	4		ns
21	D31–D0 Read Setup Time		4	11		ns
22	D31–D0 Read Hold Time		4	6		ns
23	HOLD Setup Time		4	17		ns
24	HOLD Hold Time		4	5		ns
25	RESET Setup Time		14	12		ns
26	RESET Hold Time		14	4		ns
27	NMI, INTR Setup Time	(Note 2)	4	16		ns
28	NMI, INTR Hold Time	(Note 2)	4	16		ns
29	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$ Setup Time	(Note 2)	4	14		ns
30	PEREQ, $\overline{ERROR}$, $\overline{BUSY}$ Hold Time	(Note 2)	4	5		ns

Notes: 1. Float condition occurs when maximum output current becomes less than I_{LO} magnitude. Float delay is not 100% tested.
2. These inputs are allowed to be asynchronous to CLK2. The setup and hold specifications are given for testing purposes, to assure recognition within a specific CLK2 period.
3. Rise and fall times are not tested.

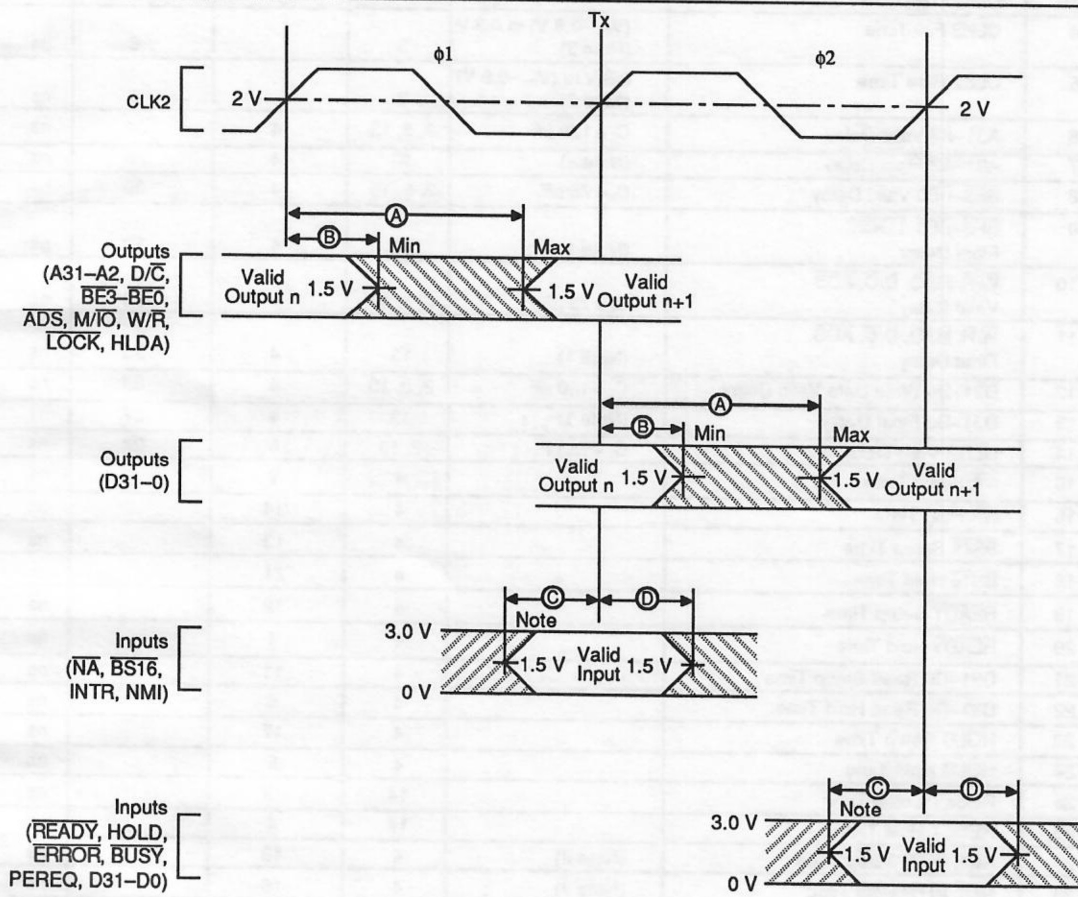
*Preliminary Information.

SWITCHING WAVEFORMS

The switching characteristics consist of output delays, input setup requirements, and input hold requirements. All characteristics are relative to the CLK2 rising edge crossing the 2.0 V level.

Switching characteristic measurement is defined by Figure 1. Inputs must be driven to the voltage levels indicated by this diagram. Am386DXL microprocessor output delays are specified with minimum and maximum limits, measured as shown. The minimum Am386DXL microprocessor delay times are hold times provided to external circuitry. Am386DXL microprocessor input setup and hold times are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct Am386DXL microprocessor operation.

Outputs $\overline{NA}$, W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$, $\overline{LOCK}$, $\overline{BE3}$–$\overline{BE0}$, A31–A2, and HLDA only change at the beginning of phase one. D31–D0 (write cycles) only change at the beginning of phase two. The $\overline{READY}$, HOLD, $\overline{BUSY}$, $\overline{ERROR}$, PEREQ, and D31–D0 (read cycles) inputs are sampled at the beginning of phase one. The $\overline{NA}$, $\overline{BS16}$, INTR, and NMI inputs are sampled at the beginning of phase two.

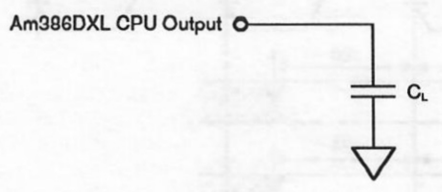


Legend: A—Maximum Output Delay Spec
B—Minimum Output Delay Spec
C—Minimum Input Setup Spec
D—Minimum Input Hold Spec

Note: Input waveforms have tr ≤ 2.0 ns from 0.8 V to 2.0 V.

15021B–071

Figure 1. Drive Levels and Measurement Points



C_L includes all parasitic capacitances.

Figure 2. AC Test Loads

15021B–072

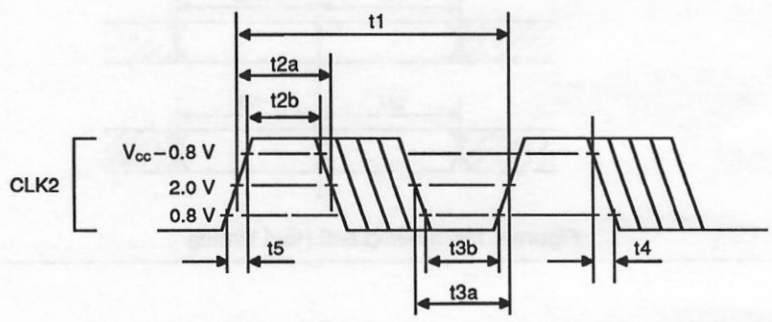
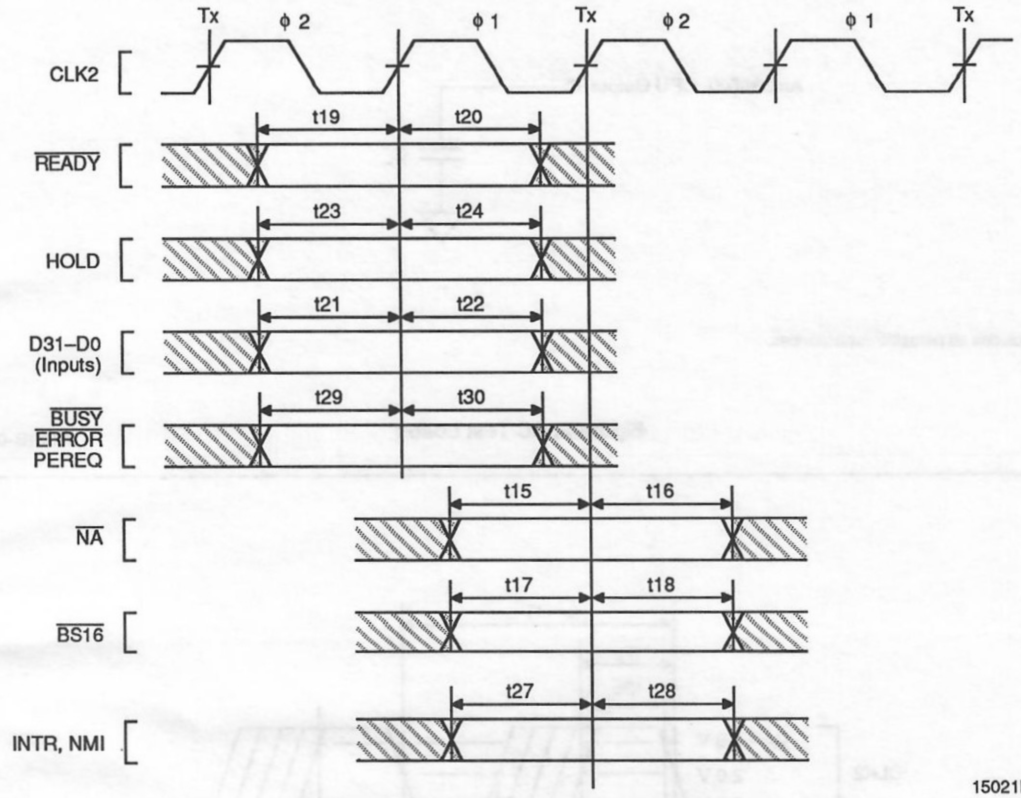


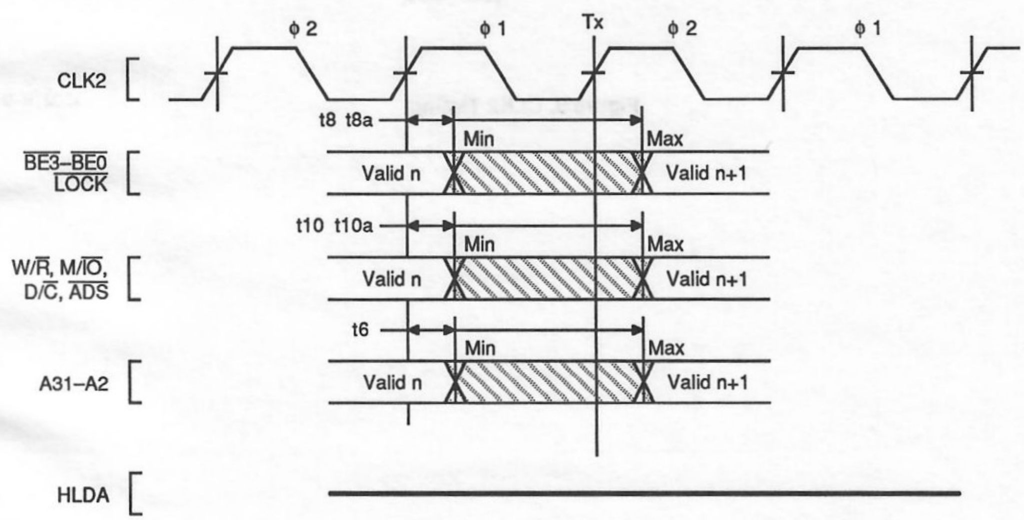
Figure 3. CLK2 Timing

15021B–073



15021B–074

Figure 4. Input Setup and Hold Timing



15021B–075

Figure 5. Output Valid Delay Timing

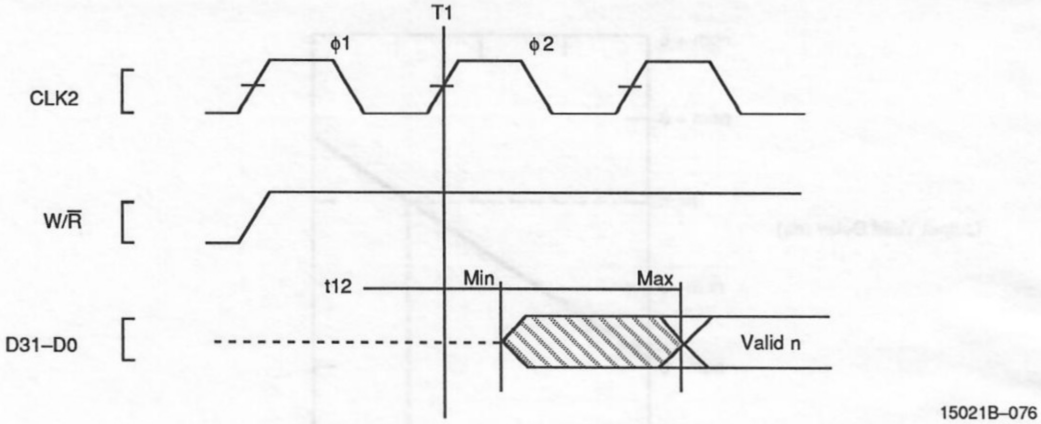


Figure 6. Write Data Valid Delay Timing (25, 33, and 40 MHz)

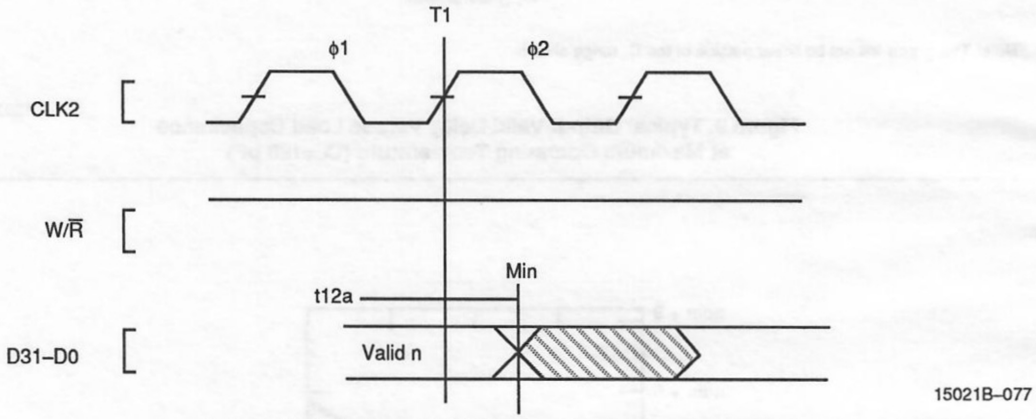


Figure 7. Write Data Hold Timing (25, 33, and 40 MHz)

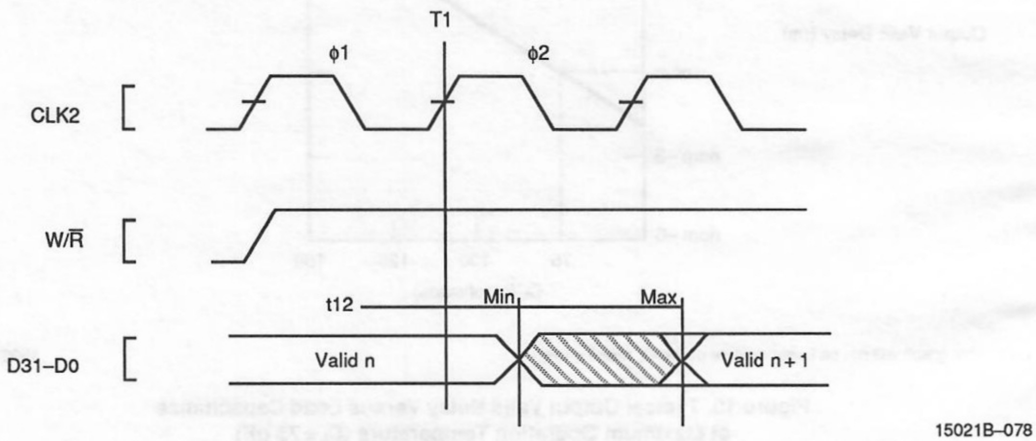
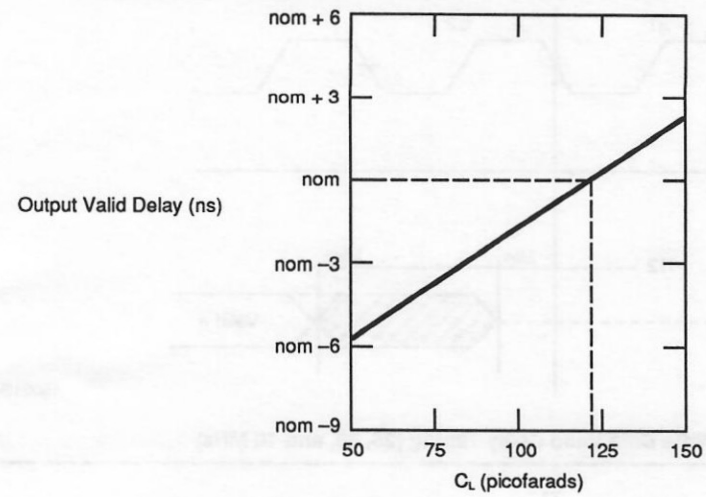


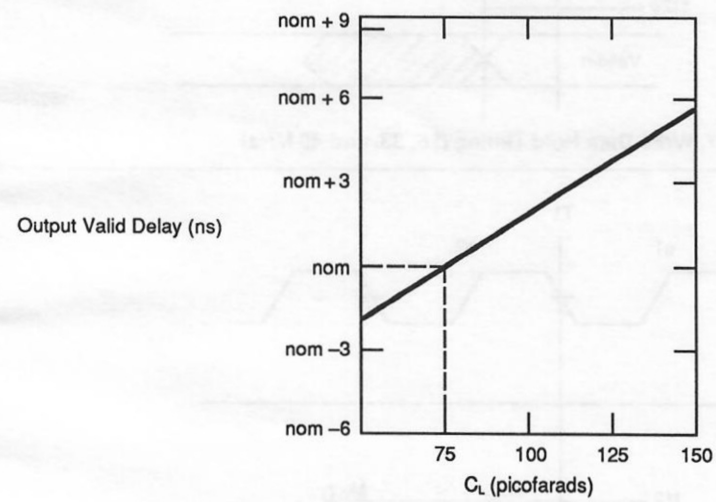
Figure 8. Write Data Valid Delay Timing (20 MHz)



Note: This graph will not be linear outside of the C_L range shown.

15021B–079

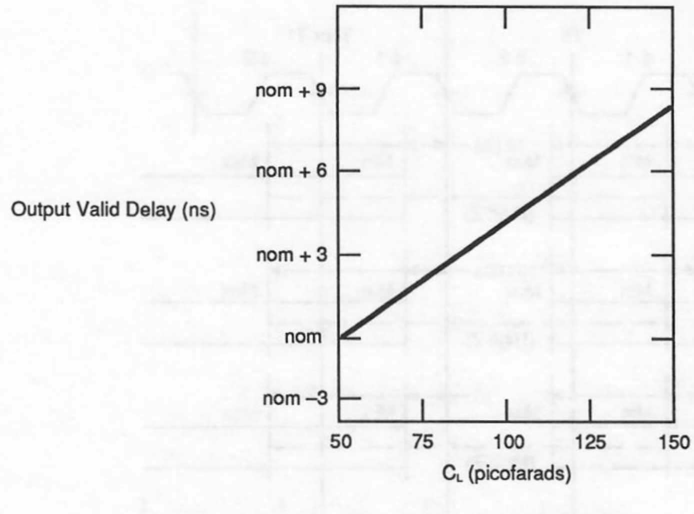
Figure 9. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature (C_L=120 pF)



Note: This graph will not be linear outside of the C_L range shown.

15021B–080

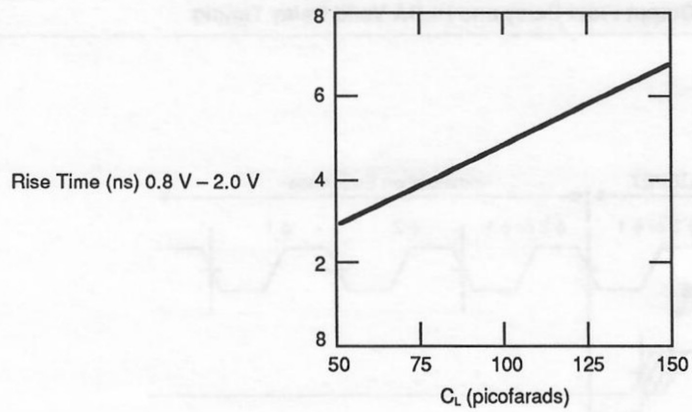
Figure 10. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature (C_L=75 pF)



Note: This graph will not be linear outside of the C_L range shown.

15021B–081

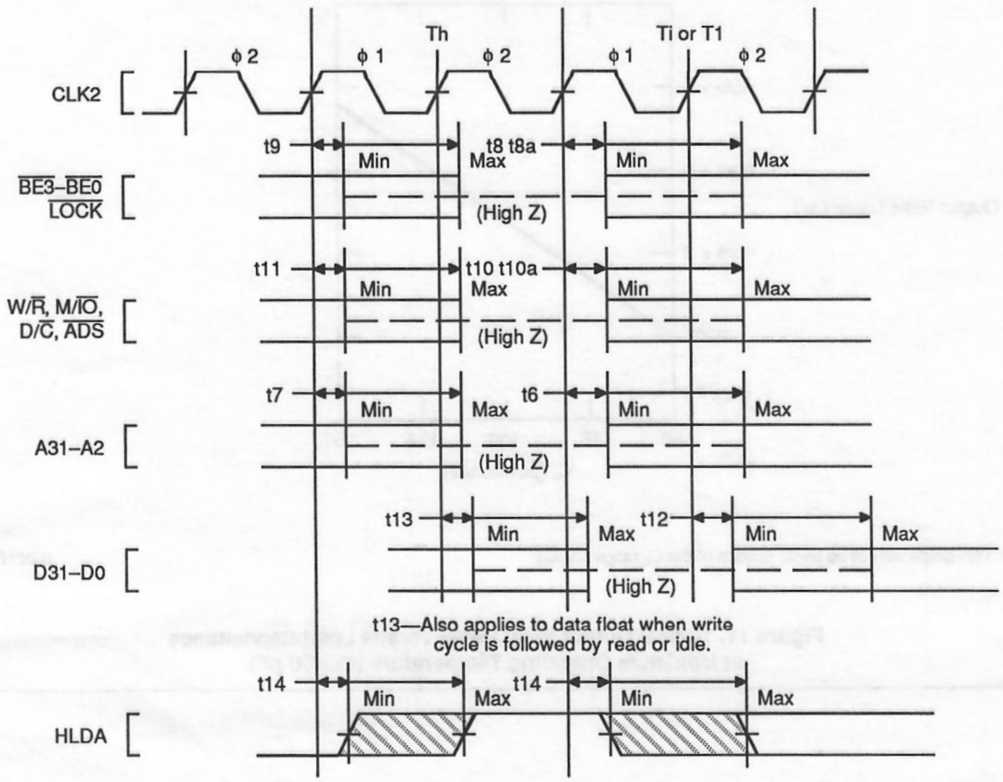
Figure 11. Typical Output Valid Delay Versus Load Capacitance at Maximum Operating Temperature (C_L = 50 pF)



Note: This graph will not be linear outside of the C_L range shown.

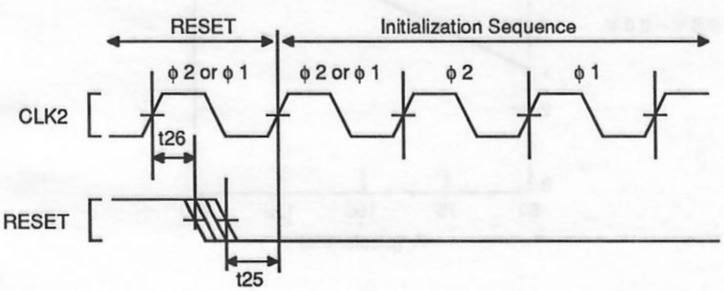
15021B–082

Figure 12. Typical Output Rise Time Versus Load Capacitance at Maximum Operating Temperature



15021B–083

Figure 13. Output Float Delay and HLDA Valid Delay Timing



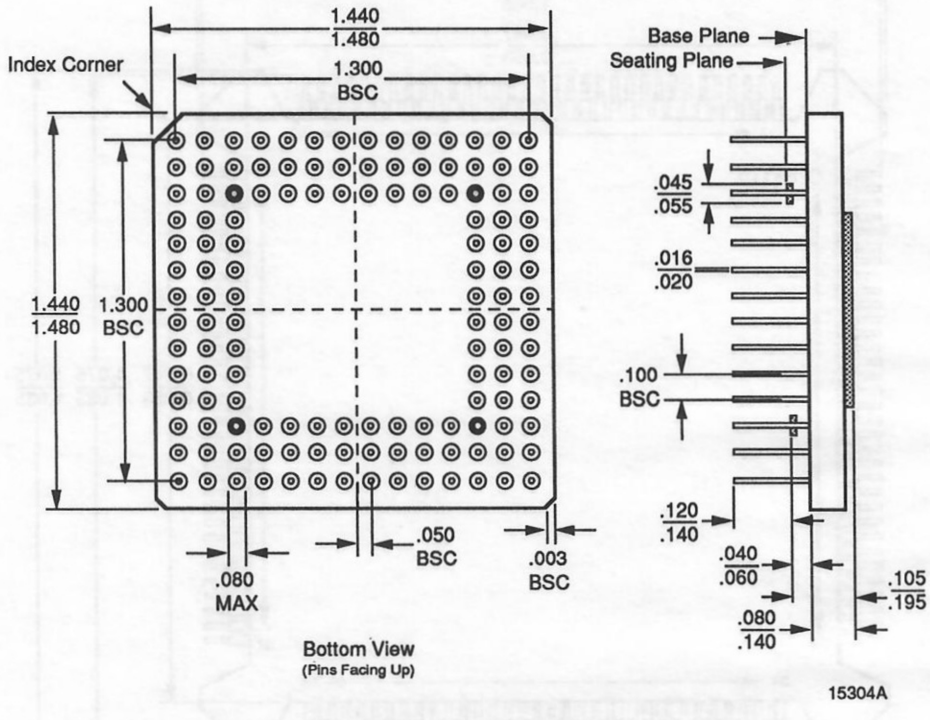
The second internal processor phase following RESET High-to-Low transition (provided t25 and t26 are met) is ϕ2.

Figure 14. RESET Setup and Hold Timing and Internal Phase

15021B–084

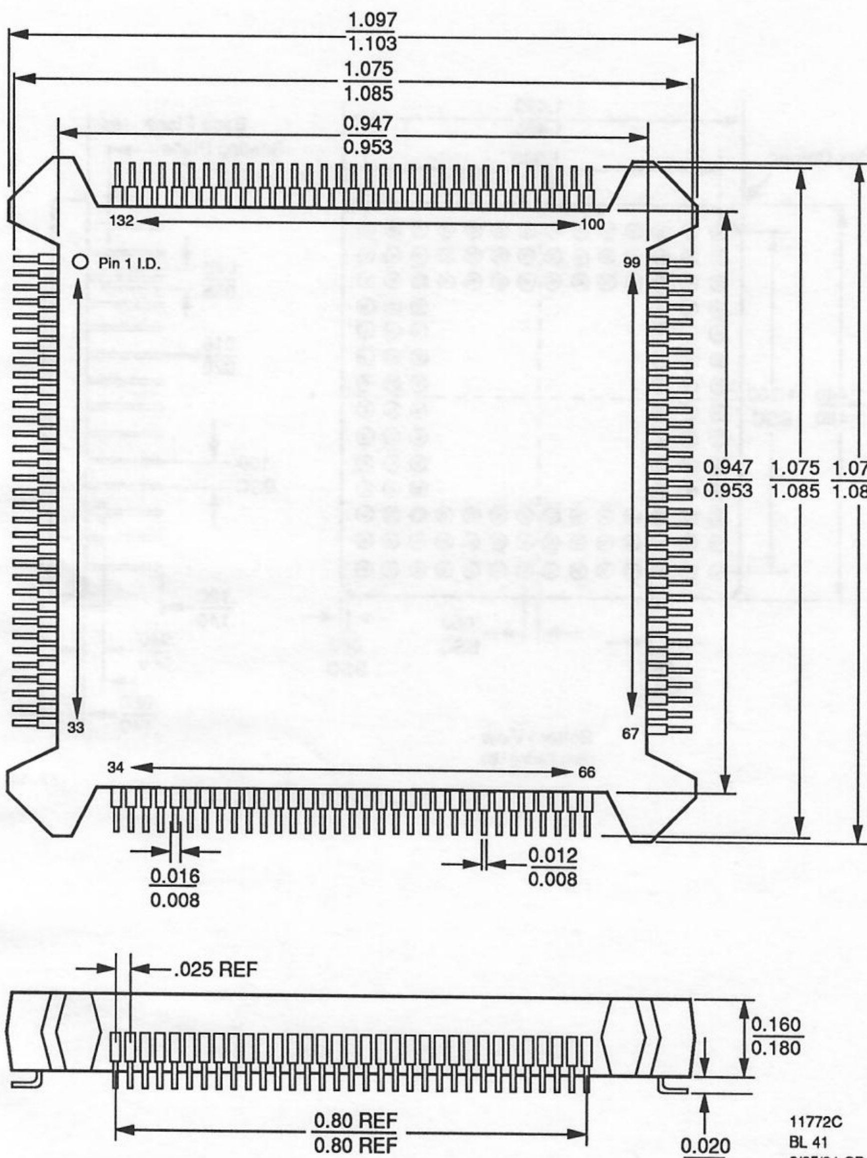
PHYSICAL DIMENSIONS

PGA 132
Measured in Inches



PHYSICAL DIMENSIONS (continued)

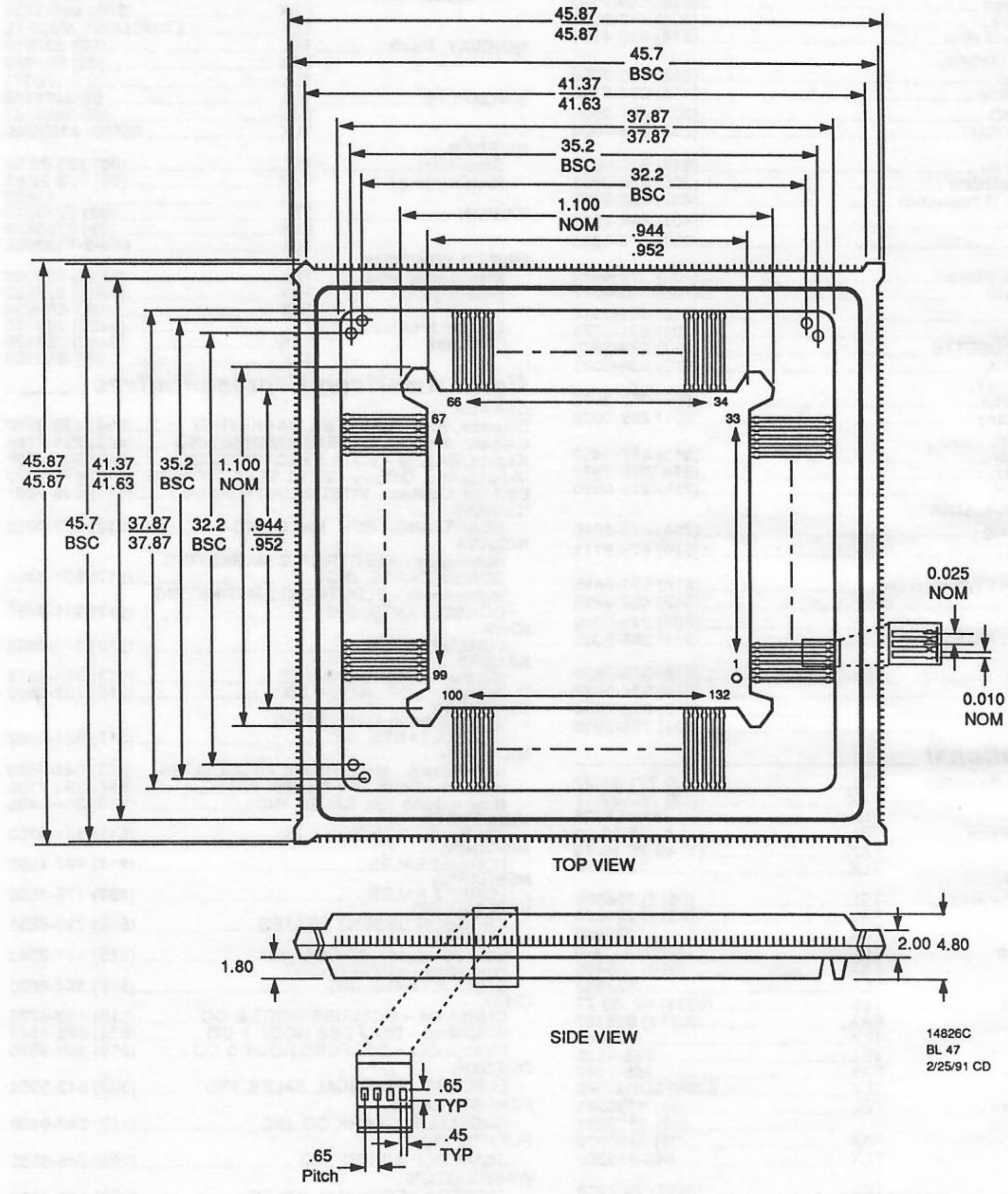
PQ132
Measured in Inches



11772C
BL 41
2/25/91 CD

PHYSICAL DIMENSIONS (continued)

PQB132
Outer Ring Measured in Millimeters
Device Measured in Inches



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