Dual Async Adapter/A Technical Reference

68X2217

80X0823

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Description

The Dual Async Adapter/A is a fully programmable serial adapter that has two serial asynchronous communications ports. The adapter is designed to work in systems that use the Micro Channel™ architecture. For more information about the channel, refer to the system *Technical Reference* manual.

Each port can add and remove a start bit, parity bit, and stop bits. A programmable baud-rate generator allows operation from 50 baud to 19,200 baud. The adapter supports 5-, 6-, 7-, and 8-bit characters with 1, 1-1/2, or 2 stop bits. A fully prioritized interrupt system controls transmit, receive, error, line status, and data set interrupts. Diagnostic capabilities provide loopback functions of transmit/receive and input/output signals. Total system load (for example, competing I/O devices) will limit the practical total number of concurrent ports and the speed of each port.

Other features include:

- Full double buffering in the character mode, eliminating the need for precise synchronization
- False-start bit detection
- Line-break generation and detection.

The major components of the adapter are two NS16550 Asynchronous Communications Controllers. The NS16550 controller is functionally compatible with the NS16450 controller. To programs, the NS16550 appears to be identical to the IBM Personal Computer AT® Serial/Parallel adapter. Support for the controller on the Dual Async Adapter/A is restricted to the functions which are identical to the NS16450. Using the controller in the FIFO mode may result in non-detectable data errors.

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Two right-angle, nine-pin, D-shell connectors (male) are mounted on the rear of the adapter.

The following figure is a block diagram of the adapter:

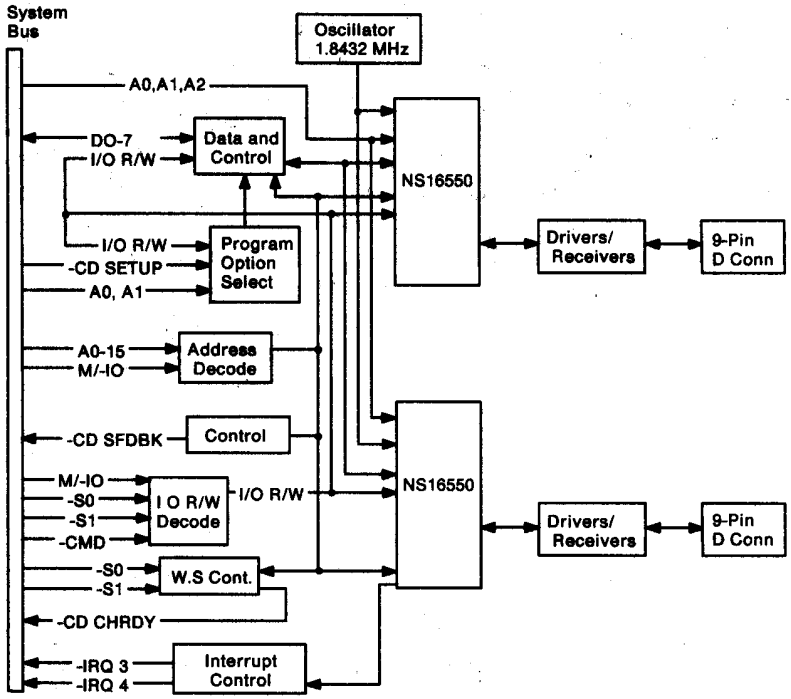


Figure 1-1. Adapter Block Diagram

Programmable Option Select (POS)

Before the adapter can be used it must be initialized by the system. The Programmable Option Select (POS) registers eliminate the need to manually initialize the adapter for a particular configuration. The power-on self-test uses the POS registers to:

- Identify the adapter.
- Enable adapter port 1 or adapter ports 1 and 2.
- Assign adapter ports. These ports can be assigned as serial modes 1 through 8.
- Enable the adapter.

Warning: IBM recommends that programmable options be set only through the System Configuration Utilities. Direct setting of the POS registers and/or CMOS RAM POS parameters can result in multiple assignment of the same system resource, improper operation of the feature, loss of data, or possible damage to the system or options. If application programs use adapter identification (ID) information, compatibility problems between systems or options may result.

The POS registers are only accessible by the system when -CD SETUP on the channel is active. Address lines A0 through A2 select the registers as shown in the following figure:

-CD SETUP	Address Line A2 A1 A0	Register
L	L L L	POS Register 0 - Adapter ID
L	L L H	POS Register 1 - Adapter ID
L	L H L	POS Register 2 - Option Select
H	X X X	Normal Operation

Figure 1-2. Register Selection

POS Registers 0 and 1

These read-only registers contain the hard-wired adapter ID.

When -CD SETUP is active, the hard-wired adapter ID (hex EEFF) is read by the system. POS Register 1 is the most-significant byte and POS Register 0 is the least-significant byte of the adapter ID.

POS Register 2

Programmable adapter options are written to this read/write register. Bit definitions for POS register 2 are shown in the following figure:

Bit	Function
7	Adapter Port Enable
6 - 4	Adapter Port 2 Mode Selection
3 - 1	Adapter Port 1 Mode Selection
0	Adapter Enable

Figure 1-3. POS Register 2

Note: All bits in POS Register 2 are cleared to 0 at power-on.

Bit 7 When this bit is set to 1, adapter port 1 is enabled. When this bit is cleared to 0, adapter ports 1 and 2 are enabled.

Bits 6 - 1 Mode selection is made by writing bits 3 - 1 for adapter port 1 and bits 6 - 4 for adapter port 2 as shown in the following figure:

Adapter Port 1 Bits 3 2 1	Mode Selected	Adapter Port 2 Bits 6 5 4
0 0 0	Serial 1	0 0 0
0 0 1	Serial 2	0 0 1
0 1 0	Serial 3	0 1 0
0 1 1	Serial 4	0 1 1
1 0 0	Serial 5	1 0 0
1 0 1	Serial 6	1 0 1
1 1 0	Serial 7	1 1 0
1 1 1	Serial 8	1 1 1

Figure 1-4. Mode Selection

Bit 0 When the bit is set to 1 the adapter is enabled. When this bit is cleared to 0 the adapter is disabled. When the adapter is disabled, it will not respond to any I/O or memory commands except the Memory Refresh command or POS reads and writes. No interrupt requests will be driven. A 'channel reset' clears this bit to 0.

Controller Accessible Registers

The controller has a number of accessible registers. The system uses these registers to control adapter operations and to transmit and receive data. The controller register I/O addresses and interrupt levels are:

Register	Serial Mode 1	2	3	4	5	6	7	8
RBR (DLAB = 0)	03F8	02F8	3220	3228	4220	4228	5220	5228
THR (DLAB = 0)	03F8	02F8	3220	3228	4220	4228	5220	5228
IER (DLAB = 0)	03F9	02F9	3221	3229	4221	4229	5221	5229
IIR	03FA	02FA	3222	322A	4222	422A	5222	522A
LCR	03FB	02FB	3223	322B	4223	422B	5223	522B
MCR	03FC	02FC	3224	322C	4224	422C	5224	522C
LSR	03FD	02FD	3225	322D	4225	422D	5225	522D
MSR	03FE	02FE	3226	322E	4226	422E	5226	522E
SCR	03FF	02FF	3227	322F	4227	422F	5227	522F
DLL (DLAB = 1)	03F8	02F8	3220	3228	4220	4228	5220	5228
DLM (DLAB = 1)	03F9	02F9	3221	3229	4221	4229	5221	5229
Interrupt Level	4	3	3	3	3	3	3	3

Figure 1-5. Controller I/O Address and Interrupt Level Assignments

Definitions of the abbreviations in Figure 1-5 are as follows:

DLAB: Divisor Latch Access Bit
DLL: Divisor Latch (LSB)
DLM: Divisor Latch (MSB)
IER: Interrupt Enable Register
IIR: Interrupt Identification Register (Read Only)
LCR: Line Control Register
LSR: Line Status Register (Read Only)
MCR: Modem Control Register
MSR: Modem Status Register
RBR: Receiver Buffer Register (Read Only)
SCR: Scratch Pad Register
THR: Transmitter Holding Register (Write Only)

Transmitter Holding Register

The Transmitter Holding register contains the character to be sent. Bit 0 is the least-significant bit and the first bit sent serially as shown in the following figure:

Bit	Function
7	Data Bit 7
6	Data Bit 6
5	Data Bit 5
4	Data Bit 4
3	Data Bit 3
2	Data Bit 2
1	Data Bit 1
0	Data Bit 0

Figure 1-6. Transmitter Holding Register

Receiver Buffer Register

The Receiver Buffer register contains the received character. Bit 0 is the least-significant bit and the first bit received serially as shown in the following figure:

Bit	Function
7	Data Bit 7
6	Data Bit 6
5	Data Bit 5
4	Data Bit 4
3	Data Bit 3
2	Data Bit 2
1	Data Bit 1
0	Data Bit 0

Figure 1-7. Receiver Buffer Register

Programmable Baud-Rate Generator

The controller has a programmable baud-rate generator that can divide the clock input (1.8432 MHz) by any divisor from 1 to 65,535. The output frequency of the baud-rate generator is the baud rate multiplied by 16. Two 8-bit divisor latches store the divisor in a 16-bit binary format. These divisor latches must be loaded during adapter initialization to ensure desired operation of the baud-rate generator. When either of the divisor latches is loaded, a 16-bit baud counter is immediately loaded. This prevents long counts on the first load.

The divisor latches are shown in the following figures:

Divisor Latch (Least Significant Bit)

Bit	Function
7	Bit 7
6	Bit 6
5	Bit 5
4	Bit 4
3	Bit 3
2	Bit 2
1	Bit 1
0	Bit 0

Figure 1-8. Divisor Latch

Divisor Latch (Most Significant Bit)

Bit	Function
7	Bit 7
6	Bit 6
5	Bit 5
4	Bit 4
3	Bit 3
2	Bit 2
1	Bit 1
0	Bit 0

Figure 1-9. Divisor Latch

Figure 1-10 on page 8 illustrates the use of the baud-rate generator with a frequency of 1.8432 MHz. For baud rates of 19,200 and below, the error obtained is minimal.

Note: In no case should the data speed be greater than 19,200 baud.

Desired Baud Rate	Divisor Used to Generate 16x Clock (Decimal)	(Hex)	Percent Error Difference Between Desired and Actual
50	2304	0900	--
75	1536	0600	--
110	1047	0417	0.026
134.5	857	0359	0.058
150	768	0300	--
300	384	0180	--
600	192	00C0	--
1200	96	0060	--
1800	64	0040	--
2000	58	003A	0.69
2400	48	0030	--
3600	32	0020	--
4800	24	0018	--
7200	16	0010	--
9600	12	000C	--
19200	6	0006	--

Figure 1-10. Baud Rates at 1.8432 MHz

Interrupt Enable Register

This 8-bit register allows the four types of controller interrupts to separately activate the 'chip-interrupt' output signal. The interrupt system can be totally disabled by clearing bits 0 through 3 of the Interrupt Enable register. Similarly, by setting the appropriate bits of this register to 1, selected interrupts can be enabled. Disabling the interrupts will inhibit the 'chip-interrupt' output signal from the controller. All other system functions operate normally, including the setting of the Line Status and Modem Status registers.

Bit	Function
4 - 7	Reserved = 0
3	Modem-Status Interrupt
2	Receiver-Line-Status Interrupt
1	Transmitter-Holding-Register-Empty
0	Received Data Available Interrupt

Figure 1-11. Interrupt Enable Register

Bits 4 - 7 Reserved. These bits are always cleared to 0.

Bit 3 When set to 1, this bit enables the modem-status interrupt.

Bit 2 When set to 1, this bit enables the receiver-line-status interrupt.

Bit 1 When set to 1, this bit enables the transmitter-holding-register-empty interrupt.

Bit 0 When set to 1, this bit enables the received-data-available interrupt.

Interrupt Identification Register

In order to minimize programming overhead during data character transfers, the controller prioritizes interrupts into four levels:

- Priority 1 - Receiver-line-status
- Priority 2 - Received-data-available
- Priority 3 - Transmitter-holding-register-empty
- Priority 4 - Modem status.

Information about a pending interrupt is stored in the Interrupt Identification register. When the Interrupt Identification register is addressed, the pending interrupt with the highest priority is held and no other interrupts are acknowledged until the system microprocessor services that interrupt.

Bit	Function
7 - 3	Reserved = 0
2	Interrupt ID, Bit 1
1	Interrupt ID, Bit 0
0	Interrupt Pending = 0

Figure 1-12. Interrupt Identification Register

Bits 7 - 3 Reserved. These bits are always cleared to 0.

Bits 2 - 1 These two bits identify the pending interrupt with the highest priority as shown in Figure 1-13 on page 10.

Bit 0 When this bit is set to 1, no interrupt is pending and polling (if used) continues. When this bit is cleared to 0, an interrupt is pending and the contents of this register can be used as a pointer to the appropriate interrupt service routine.

This bit can be used in either hard-wired, prioritized, or polled conditions to indicate if an interrupt is pending.

Bits 2 - 0 select Interrupt Control Functions as shown in the following figure:

Bits 2 1 0	Priority	Type	Cause	Interrupt Reset Control
0 0 1	-	None	None	-
1 1 0	Highest	Receiver Line Status	Overrun, Parity, or Framing Error or Break Interrupt	Read the Line Status Register
1 0 0	Second	Received Data Available	Data in Receiver Buffer	Read the Receiver Buffer Register
0 1 0	Third	Transmitter Holding Register Empty	Transmitter Holding Register is Empty	Read Interrupt Identification Register or Write to Transmitter Holding Register
0 0 0	Fourth	Modem Status	Change in Signal Status from Modem	Read the Modem Status Register

Figure 1-13. Interrupt Control Functions

Line Control Register

The format of asynchronous communications is programmed through the Line Control register.

Bit	Function
7	Divisor Latch Access Bit
6	Set Break
5	Stuck Parity
4	Even Parity Select
3	Parity Enable
2	Number of Stop Bits
1	Word Length Select, Bit 1
0	Word Length Select, Bit 0

Figure 1-14. Line Control Register

Bit 7 This bit must be set to 1 during a read or write operation to gain access to the divisor latches of the baud-rate generator. It must be cleared to 0 to gain access to the Receiver Buffer, Transmitter Holding, or Interrupt Enable registers.

Bit 6 When this bit is set to 1 set-break is enabled, serial output is forced to the spacing state and remains there regardless of other transmitter activity. When this bit is cleared to 0, set-break is disabled.

Bit 5 When bits 5, 4, and 3 are set to 1, the parity bit is sent and checked as a logical 0. When bits 5 and 3 are set to 1, and bit 4 is cleared to 0, the parity bit is sent and checked as a logical 1.

Bit 4 When this bit and bit 3 are set to 1, an even number of logical 1's are transmitted and checked in the data word bits and parity bit. When this bit is cleared to 0, and bit 3 is set to 1, an odd number of logical 1's are transmitted and checked in the data word bits and parity bit.

Bit 3 When set to 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit. (The parity bit is used to produce an even or odd number of 1's when the data-word bits and the parity bit are summed.)

Bit 2 This bit, along with bits 0 and 1, specifies the number of stop bits in each serial character that is sent or received as shown in the following figure:

Bit 2	Word Length *	Number of Stop Bits
0	N/A	1
1	5-Bits	1-1/2
1	6-Bits	2
1	7-Bits	2
1	8-Bits	2

* Word Length is specified by bits 0 - 1 in this register.

Figure 1-15. Word Length

Bits 0 - 1 These two bits specify the number of bits in each serial character that is sent or received. Word length is selected as shown in the following figure:

Bits 1 0	Word Length
0 0	5-Bits
0 1	6-Bits
1 0	7-Bits
1 1	8-Bits

Figure 1-16. Word Length

Modem Control Register

This 8-bit register controls the data exchange with the modem, data set, or peripheral device emulating a modem.

Bit	Function
7 - 5	Reserved = 0
4	Loop
3	Out 2
2	Out 1
1	Request-to-Send
0	Data-Terminal-Ready

Figure 1-17. Modem Control Register

Bits 7 - 5 Reserved. These bits are always cleared to 0.

Bit 4 This bit provides a loopback feature for diagnostic testing of the adapter. When bit 4 is set to 1:

- Transmitter-serial-output is set to the marking state
- Receiver-serial-input is disconnected
- Output of the Transmitter Shift register is "looped back" to the Receiver Shift register input

  Note: The Transmitter and Receiver Shift registers are not accessible NS16550 registers.

- The modem control inputs (CTS, DSR, DCD, and RI) are disconnected

- The modem control outputs (DTR, RTS, OUT 1, and OUT 2) are internally connected to the four modem control inputs
- The modem control output pins are forced inactive.

When the adapter is in the diagnostic mode, transmitted data is immediately received. This feature allows the system microprocessor to verify the transmit-data and receive-data paths of the adapter.

When the adapter is in the diagnostic mode, the receiver and transmitter interrupts are fully operational. The modem control interrupts are also operational, but their sources are the lower four bits of the Modem Control register instead of the four modem control input signals. The interrupts are still controlled by the Interrupt Enable register.

Bit 3 This bit controls the 'output 2' (OUT 2) signal which is an auxiliary user-designated interrupt enable signal. OUT 2 is used to control the interrupt signal to the channel. Setting this bit to 1 enables the interrupt. Clearing this bit to 0 disables the interrupt.

Bit 2 This bit controls the 'output 1' (OUT 1) signal which is an auxiliary user-designated output signal. When set to 1, OUT 1 is forced active. When cleared to 0, OUT 1 is forced inactive.

Bit 1 This bit controls the 'request-to-send' (RTS) controller output signal. When set to 1, RTS is forced active. When cleared to 0, RTS is forced inactive.

Bit 0 This bit controls the 'data-terminal-ready' (DTR) controller output signal. When set to 1, DTR is forced active. When cleared to 0, DTR is forced inactive.

Line Status Register

This 8-bit register provides the system microprocessor with status information about the data transfer.

Bit	Function
7	Reserved = 0
6	Transmitter Shift Register Empty (TEMT)
5	Transmitter Holding Register Empty (THRE)
4	Break Interrupt (BI)
3	Framing Error (FE)
2	Parity Error (PE)
1	Overrun Error (OR)
0	Data Ready (DR)

Figure 1-18. Line Status Register

Bit 7 Reserved. This bit is always cleared to 0.

Bit 6 This bit is set to 1 when the Transmitter Holding register and the Transmitter Shift register are both empty. This bit is cleared to 0 when either the Transmitter Holding register or the Transmitter Shift register contains a data character.

Bit 5 This bit indicates that the adapter is ready to accept a new character for transmission. This bit is set to 1 when a character is transferred from the Transmitter Holding register into the Transmitter Shift register. This bit is cleared to 0 when the system microprocessor loads the Transmitter Holding register.

This bit also causes the adapter to issue an interrupt to the system microprocessor when bit 1 in the Interrupt Enable register is set to 1.

Bit 4 This bit is set to 1 when the received data input is held in the spacing state for longer than a fullword transmission (the total time of the start bit + data bits + parity + stop bits).

Note: Bits 1 through 4 are the error conditions that produce a receiver line-status interrupt whenever any of the corresponding conditions are detected.

Bit 3 This bit is set to 1 when the stop bit following the last data bit or parity bit is at a spacing level. This indicates that the received character did not have a valid stop bit.

Bit 2 This bit is set to 1 when a parity error is detected (the received character does not have the correct even or odd parity, as selected by the even-parity-select bit). This bit is cleared to 0 when the system microprocessor reads the contents of the Line Status register.

Bit 1 When it is set to 1, this bit indicates that data in the Receiver Buffer register was not read by the system microprocessor before the next character was transferred into the Receiver Buffer register, destroying the previous character. This bit is cleared to 0 when the system microprocessor reads the contents of the Line Status register.

Bit 0 This bit is set to 1 when a complete incoming character has been received and transferred into the Receiver Buffer register. This bit is cleared to 0 by reading the Receiver Buffer register.

Modem Status Register

This 8-bit register provides the current state of the control lines from the modem (or external device) to the system microprocessor. In addition, bits 3 - 0 of the this register provide change information. These four bits are set to logical 1 whenever a control input from the modem changes state. They are reset to logical 0 whenever the system microprocessor reads this register.

Bit	Function
7	Data-Carrier-Detect
6	Ring Indicator
5	Data-Set-Ready
4	Clear-to-Send
3	Delta-Data-Carrier-Detect
2	Trailing Edge Ring Indicator
1	Delta-Data-Set-Ready
0	Delta-Clear-to-Send

Figure 1-19. Modem Status Register

Bit 7 This bit is the inverted 'data-carrier-detect' (DCD) modem control input signal. If bit 4 of the Modem Control register is set to 1, this bit is equivalent to bit 3 in the Modem Control register.

Bit 6 This bit is the inverted 'ring-indicator' (RI) modem control input signal. If bit 4 of the Modem Control register is set to 1, this bit is equivalent to bit 2 in the Modem Control register.

Bit 5 This bit is the inverted 'data-set-ready' (DSR) modem control input signal. If bit 4 of the Modem Control register is set to 1, this bit is equivalent to bit 0 in the Modem Control register.

Bit 4 This bit is the inverted 'clear-to-send' (CTS) modem control input signal. If bit 4 of the Modem Control register is set to 1, this bit is equivalent to bit 1 in the Modem Control register.

Bit 3 When set to 1, this bit indicates that the DCD modem control input signal has changed state since the last time it was read by the system microprocessor.

Note: Whenever bit 0, 1, 2, or 3 is set to 1, a modem status interrupt is generated.

Bit 2 When set to 1, this bit indicates that the RI modem control input signal has changed from an active condition to an inactive condition.

Bit 1 When set to 1, this bit indicates that the DSR modem control input signal has changed state since the last time it was read by the system microprocessor.

Bit 0 When set to 1, this bit indicates that the CTS modem control input signal has changed state since the last time it was read by the system microprocessor.

Scratch Pad Register

This register does not control the adapter in any way. It can be used by the system microprocessor to temporarily hold data.

Modem Control Input Signals

The following are input signals from the modem or external device to the controller. Bits 7 - 4 in the Modem Status register indicate the condition of these signals. Bits 3 - 0 in the Modem Status register monitor these signals to indicate when the modem changes state.

Clear to Send (CTS): When active, this signal indicates that the modem is ready for the adapter to transmit data.

Data Set Ready (DSR): When active, this signal indicates the modem or data set is ready to establish the communications link and transfer data with the controller.

Ring Indicator (RI): When active, this signal indicates the modem or data set detected a telephone ringing signal.

Data Carrier Detect (DCD): When active, this signal indicates that the modem or data set detected a data carrier.

Modem Control Output Signals

The following are controller output signals. They are all set inactive upon a master reset operation. These signals are controlled by bits 3 - 0 in the Modem Control register.

Data Terminal Ready (DTR): When active, this signal informs the modem or data set that the controller is ready to communicate.

Request to Send (RTS): When active, this signal informs the modem or data set that the controller is ready to send data.

Output 1 (OUT 1): This signal is pulled high.

Output 2 (OUT 2): User-designated output. This signal controls interrupts to the system.

Interrupts

Two interrupt lines are provided to the system. Interrupt level 4 (IRQ4) is for serial mode 1 and interrupt level 3 (IRQ3) is for serial modes 2 through 8. To allow the adapter to send interrupts to the system, bit 3 of the Modem Control register must be set to 1. At this point, any interrupts allowed by the Interrupt Enable register will cause an interrupt.

Hardware Interrupts

Hardware interrupts are level-sensitive for systems using the Micro Channel architecture while systems using the Personal Computer type I/O channel design have edge-sensitive hardware interrupts. On edge-sensitive interrupt systems, the interrupt controller clears its internal interrupt-in-progress latch when the interrupt routine sends an End-of-Interrupt (EOI) command to the controller. The EOI is sent whether the incoming interrupt request to the controller is active or inactive.

In level-sensitive systems, the interrupt-in-progress latch is readable at an I/O address bit position. This latch is read during the interrupt service routine and may be reset by the read operation or may require an explicit reset.

Note: Designers may wish to limit the number of devices sharing an interrupt level for performance and latency considerations.

The interrupt controller on level-sensitive systems requires the interrupt request to be inactive at the time the EOI is sent; otherwise, a "new" interrupt request will be detected and another microprocessor interrupt caused.

To avoid this problem, a level-sensitive interrupt handler must clear the interrupt condition (usually by a Read or Write to an I/O port on the device causing the interrupt). After clearing the interrupt condition, a JMP $+2 should be executed prior to sending the EOI to the interrupt controller. This ensures that the interrupt request is removed prior to re-enabling the interrupt controller. Another JMP $+2 should be executed after sending the EOI, but prior to enabling the interrupt through the Set Interrupt Enable Flag (STI) command.

Serial Data Format

The serial data format is as follows:

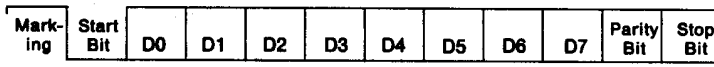


Figure 1-20. Serial Data Format

Data bit 0 is the first bit to be transmitted or received. The adapter automatically inserts the start bit, the correct parity bit, if programmed to do so, and the stop bits (1, 1-1/2, or 2 depending on the command in the Line Control register).

During the transmission of data, the marking condition will be used to denote the binary state 1, and the spacing condition is used to denote the binary state 0.

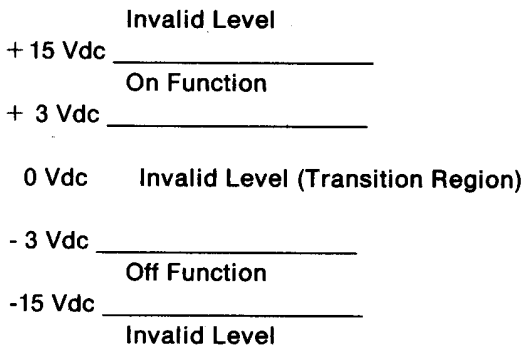
Voltage Interchange Information

The signal is considered in the *marking* condition when the voltage on the interchange circuit, measured at the interface point, is more negative than -3 Vdc with respect to signal ground. The signal is considered in the *spacing* condition when the voltage is more positive than +3 Vdc with respect to signal ground. The region between +3 Vdc and -3 Vdc is defined as the transition region, and considered an invalid level. The voltage that is more negative than -15 Vdc or more positive than +15 Vdc is also considered an invalid level.

Interchange Voltage	Binary State	Signal Condition	Interface Control Function
Positive Voltage	Binary 0	Spacing	On
Negative Voltage	Binary 1	Marking	Off

Figure 1-21. Voltage Levels

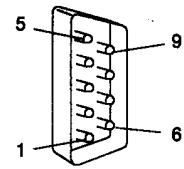
The following shows the voltages in relation to the functions and invalid levels.



Connectors

The adapter provides an EIA RS-232C interface. Two 9-pin, D-shell connectors (male) are provided to attach peripheral devices. The top connector is port 1 and the bottom connector is port 2.

The voltage interface is a serial interface. It supports the following data and control signals:



Pin No.	Signal Flow	Signal Name
1	I	Data Carrier Detect
2	I	Received Data
3	O	Transmitted Data
4	O	Data-Terminal-Ready
5	N/A	Signal Ground
6	I	Data-Set-Ready
7	O	Request-to-Send
8	I	Clear-to-Send
9	I	Ring Indicator

Figure 1-22. Connector Pin Assignments

The RS-232C drivers and receivers convert these signals to or from TTL or EIA voltage levels. These signals are sampled or generated by the adapter. These signals can then be sensed by the system microprocessor to determine the state of the interface or peripheral device.

Voltage Requirements

The adapter requires the following voltages:

- +5 Vdc
- +12 Vdc
- -12 Vdc.

Notes:

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