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(71) Applicant: **International Business Machines Corporation**
Old Orchard Road
Armonk, N.Y. 10504(US)

(72) Inventor: **Lenta, Jorge Eduardo**
5499 Fox Hollow Drive
Boca Raton, FL 33486(US)
Inventor: **Medford, Mitchell Eric**
955 Egret Circle, Apt 302B
Delray Beach, FL 33444(US)

(74) Representative: **Blakemore, Frederick Norman**
IBM United Kingdom Limited Intellectual Property Department Hursley Park
Winchester Hampshire SO21 2JN(GB)

(54) **Computer system for enabling a choice of errordetection technologies.**

(57) This invention relates to a computer system having enhanced memory access capabilities, a memory element enabling such enhancement, and a method of operation of a personal computer. The invention contemplates that enhanced capabilities will be attained by enabling a choice between error detection technologies used.

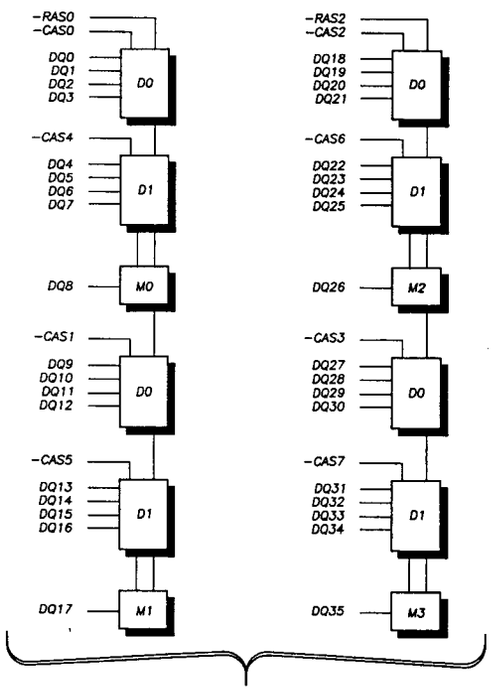

Fig. 5

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This invention relates to a computer system having enhanced memory access capabilities, a memory element enabling such enhancement, and a method of operation of such a computer.

Personal computer systems in general and IBM personal computers in particular have attained widespread use for providing computer power to many segments of today's modern society. Personal computer systems can usually be defined as a desk top floor standing, or portable microcomputer that consists of a system unit having a single system processor and associated volatile and non-volatile memory, a display monitor, a keyboard, one or more diskette drives, a fixed disk storage, and an optional printer. One of the distinguishing characteristics of these systems is the use of a motherboard or system planar to electrically connect these components together. These systems are designed primarily to give independent computing power to a single user and are inexpensively priced for purchase by individuals or small businesses. Examples of such personal computer systems are IBM's PERSONAL COMPUTER AT and IBM's PERSONAL SYSTEM/2 Models 25, 30, L40SX, 50, 55, 65, 70, 80, 90 and 95.

These systems can be classified into two general families. The first family, usually referred to as Family I Models, use a bus architecture exemplified by the IBM PERSONAL, COMPUTER AT and other "IBM compatible" machines. The second family referred to as Family II Models, use IBM s MICRO CHANNEL bus architecture exemplified by IBM's PERSONAL SYSTEM/2 Models 50 through 95. The Family I models typically have used the popular INTEL 8088 or 8086 microprocessor as the system processor. These processors have the ability to address one megabyte of memory. The Family II models typically use the high speed INTEL 80286, 80386, and 80486 microprocessors which can operate in a real mode to emulate the slower speed INTEL 8086 microprocessor or a protected mode which extends the addressing range from 1 megabyte to 4 Gigabytes for some models. In essence, the real mode feature of the 80286, 80386, and 80486 processors provide hardware compatibility with software written for the 8086 and 8088 microprocessors.

Data being processed in high performance personal computers such as some of those mentioned above is conventionally written to, stored in and read from dynamic random access memory (DRAM) using conventional data storage technology. While such technology has been quite successful, persons skilled in the arts of computer design and use have known for some time that all DRAM has inherent soft errors. That is, data written to, stored in or read from DRAM will contain errors over time. The degree to which such errors interfere with personal computer operation will vary with the particular application for which the computer is being used. An error rate acceptable for a personal computer used only for word processing may be found completely unacceptable for a personal computer used as a file server supporting financial record keeping and analysis applications necessary to the operation of an ongoing business venture.

Recognizing the inherency of DRAM data or soft errors, most personal computer designers have adopted some known technology for guarding against adverse effects of such errors. The most common such technology is known as parity checking or parity. With parity checking, each predetermined number of bits of data used for transferring or storing information is accompanied by a parity bit used to validate the accuracy of the data bits. One typical arrangement uses one parity bit for eight data bits. Typically, such a parity design will detect an error of a single bit in a word. An alternate technology is known as error correcting code or ECC. ECC (depending upon its implementation) can detect errors of one or more bits in a word and can correct errors of one bit in a word. ECC typically adds to the data bits defining a word from four to seven bits used in the error detection and correction routines. ECC is, as a general matter, known and the present invention relies upon such known technology.

Prior to the present invention, personal computer designers and users essentially have been faced with the parity or ECC choice at a very early level in determining personal computer system capabilities. In particular, a user concerned with achieving high levels of performance (in the sense of minimizing the impact of DRAM soft errors) would be compelled to select a machine designed to have ECC capability, even if many applications to be supported by that machine would be satisfactorily served by parity memory.

Further, there has been a trend over recent time toward packaging of memory elements in more readily handled forms. With increasing density of memory elements, in terms of quantities of data words stored, memory elements have moved from single chips to single inline memory modules (SIMM) and toward what has become known as DRAM cards. A DRAM card is a packaging of memory elements mounted on a substrate within a protective sleeve or enclosure and coupled to the remainder of a computer system by an appropriate pin and socket connection. In one form, such a DRAM card may have dimensions of approximately fifty four millimeters wide by eighty five millimeters long by three millimeters thick. It is contemplated that such dimensions may vary and will be reduced as technological advances permit. One advantage of DRAM cards is that such memory elements are readily removed and replaced form computer systems and may be handled by users almost as easily as the well known floppy disks with which all

personal computer users are familiar. However, even with such development of the applicable technology, parity and ECC memory elements have remained non-interchangeable. That is, a user of a machine first configured for parity memory elements and wishing to change to ECC memory elements would be required to remove and replace all memory elements to effect the desired conversion.

With the foregoing in mind, it is an object of this invention to provide a computer system for enabling a choice of error detection technologies.

Accordingly the present invention provides a computer system comprising:

a processor;

a plurality of socket connectors, each for receiving a volatile memory element, one of said socket connectors being addressable for connecting with memory elements having devices addressable for handling data bits in a first predetermined word length and the remainder of said socket connectors being addressable for connecting with memory elements having devices addressable for handling data bits in any selected one of multiples of two, four and eight times the predetermined word length; and

a memory controller coupled to said processor for issuing row and column address signals determining the physical location in available volatile memory elements of data written thereto and stored therein and read therefrom;

said memory controller directing to said one socket connector data bit words representing error correcting code and directing to another of said socket connectors data bit words representing data associated with the error correcting code directed to said one socket connector.

A memory element is also provided which is capable of being fully accessed by memory control signals, namely row address and column address signals (respectively RAS and CAS).

Thus a personal computer is provided in which a user has the possibility of readily selecting between parity and ECC technologies for detecting DRAM errors. A user of a personal computer system is permitted to readily adjust the error detection technology used to particular applications of the system.

Such a personal computer can be operated in such a manner that memory elements may be used in common in a selected one of either parity or ECC error detection technologies. An allocation of the data bits necessary for the error detection technologies is made between two memory elements.

An embodiment of the invention will now be described, by way of example only, with reference to the accompanying drawing, in which:

Figure 1 is a perspective view of a personal computer embodying this invention;

Figure 2 is an exploded perspective view of certain elements of the personal computer of Figure 1 including a chassis, a cover, and a planar board and illustrating certain relationships among those elements;

Figure 3 is a schematic view of certain components of the personal computer of Figures 1 and 2;

Figure 4 is a perspective view of a memory element in accordance with the present invention in the form of a DRAM card;

Figure 5 is a schematic representation of one arrangement of DRAM within a card such as that of Figure 4;

Figure 6 is a schematic representation of a second arrangement of DRAM within a card such as that of Figure 4; and

Figure 7 through 17 are schematic illustrations of portions of the personal computer of Figures 1 through 3 showing adaptation of the personal computer to varying amounts of DRAM memory and varying error detection technology.

While the present invention will be described more fully hereinafter with reference to the accompanying drawings, in which a preferred embodiment of the present invention is shown, it is to be understood at the outset of the description which follows that persons of skill in the appropriate arts may modify the invention here described while still achieving the favorable results of this invention. Accordingly, the description which follows is to be understood as being a broad, teaching disclosure directed to persons of skill in the appropriate arts, and not as limiting upon the present invention.

Referring now more particularly to the accompanying drawings, a microcomputer embodying the present invention is there shown and generally indicated at 10 (Figure 1). As mentioned hereinabove, the computer 10 may have an associated monitor 1, keyboard 12 and printer or plotter 14. The computer 10 has a cover 15 which cooperates with a chassis 19 in defining an enclosed, shielded volume for receiving electrically powered data processing and storage components for processing and storing digital data, as shown in Figure 2. At least certain of these components are mounted on a multilayer planar 20 or motherboard which is mounted on the chassis 19 and provides a means for electrically interconnecting the components of the computer 10 including those identified above and such other associated elements as floppy disk drives, various forms of direct access storage devices, accessory cards or boards, and the like.

The chassis 19 has a base and a rear panel (Figure 2) and defines at least one open bay for receiving a data storage device such as a disk drive for magnetic or optical disks, a tape backup drive, or the like. In the illustrated form, an upper bay 22 is adapted to receive peripheral drives of a first size (such as those known as 3.5 inch drives). A floppy disk drive, a removable media direct access storage device capable of receiving a diskette inserted thereinto and using the diskette to receive, store and deliver data as is generally known, may be provided in the upper bay 22.

Prior to relating the above structure to the present invention, a summary of the operation in general of the personal computer system 10 may merit review. Referring to Figure 3, there is shown a block diagram of a personal computer system illustrating the various components of the computer system such as the system 10 in accordance with the present invention, including components mounted on the planar 20 and the connection of the planar to the I/O slots and other hardware of the personal computer system. Connected to the planar is the system processor 32. While any appropriate microprocessor can be used as the CPU 32, one suitable microprocessor is the 80386 which is sold by INTEL. The CPU 32 is connected by a high speed CPU local bus 34 to a bus interface control unit 35, to volatile random access memory (RAM) 36 here shown as DRAM cards, and to BIOS ROM 38 in which is stored instructions for basic input/output operations to the CPU 32. The BIOS ROM 38 includes the BIOS that is used to interface between the I/O devices and the operating system of the microprocessor 32. Instructions stored in ROM 38 can be copied into RAM 36 to decrease the execution time of BIOS. Preferably, each DRAM card present is received in a corresponding one of a plurality of socket connectors provided for receiving the cards and connecting to the pins provided.

While the present invention is described hereinafter with particular reference to the system block diagram of Figure 3, it is to be understood at the outset of the description which follows that it is contemplated that the apparatus and methods in accordance with the present invention may be used with other hardware configurations of the planar board. For example, the system processor could be an Intel 80286 or 80486 microprocessor.

Returning now to Figure 3, the CPU local bus 34 (comprising data, address and control components) also provides for the connection of the microprocessor 32 with a math coprocessor 39 and a Small Computer Systems Interface (SCSI) controller 40. The SCSI controller 40 may, as is known to persons skilled in the arts of computer design and operation, be connected or connectable with Read Only Memory (ROM) 41, RAM 42, and suitable external devices of a variety of types as facilitated by the I/O connection indicated to the right in the Figure. The SCSI controller 40 functions as a storage controller in controlling storage memory devices such as fixed or removable media electromagnetic storage devices (also known as hard and floppy disk drives), electro-optical, tape and other storage devices.

The bus interface controller (BIC) 35 couples the CPU local bus 34 with an I/O bus 44 and serves a number of other functions, including that of memory controller as pointed out more fully hereinafter. By means of the I/O bus 44, the BIC 35 is coupled with an optional feature bus such as a MICRO CHANNEL bus having a plurality of I/O slots for receiving MICRO CHANNEL adapter cards 45 which may be further connected to an I/O device or memory (not shown). The I/O bus 44 includes address, data, and control components.

Coupled along the I/O bus 44 are a variety of I/O components such as a video signal processor 46 which is associated with video RAM (VRAM) for storing graphic information (indicated at 48) and for storing image information (indicated at 49). Video signals exchanged with the processor 46 may be passed through a Digital to Analog Converter (DAC) 50 to a monitor or other display device. Provision is also made for connecting the VSP 46 directly with what is here referred to as a natural image input/output, which may take the form of a video recorder/player, camera, etc. The I/O bus 44 is also coupled with a Digital Signal Processor (DSP) 51 which has associated instruction RAM 52 and data RAM 54 available to store software instructions for the processing of signals by the DSP 51 and data involved in such processing. The DSP 51 provides for processing of audio inputs and outputs by the provision of an audio controller 55, and for handling of other signals by provision of an analog interface controller 56. Lastly, the I/O bus 44 is coupled with a input/output controller 58 with associated Electrical Erasable Programmahle Read Only Memory (EEPROM) 59 by which inputs and outputs are exchanged with conventional peripherals including floppy disk drives, a printer or plotter 14, keyboard 12, a mouse or pointing device (not shown), and by means of a serial port.

Turning now more specifically to the present invention, the following discussion will contemplate that data may be written to memory, stored in memory, and read from memory in data widths of eight, sixteen or thirty two bits. Typically, one parity bit is provided for each eight bits, so that a thirty two bit wide data transfer has four parity bits. The number of ECC bits needed to permit ECC operation varies with the functions desired and with the data width. In particular, ECC may be operated with single hit error correction

without double bit error detection (herein "Mode I") or single bit error correction with double bit error detection (herein "Mode II"). For an eight bit data width, four ECC bits enable Mode I operation, while five bits are necessary for Mode II. Five bits enable Mode I operation for sixteen bit wide data transfer, and six enable Mode II. Six bits enable Mode I for thirty two bit wide transfers, and seven enable Mode II.

The present invention is embodied in part in a memory element in the form of a DRAM card 60 (Figure 4). The DRAM card 60 has a substrate mounting memory chips, and enclosing cover facilitating handling of the card, and a plurality of pins providing for connection to the memory chips housed within the enclosure. As generally described to this point, the DRAM card may accord fully with engineering specifications published by cooperating engineering design groups such as the JEDEC Solid State Products Engineering Council and the Japan Electronics Industry Development Association. The memory chips may, for example, be one megabyte by four chips with eight chips per card, or greater densities as such chips become available.

Prior to the present invention, it was usual for error detection technologies to be supported by placement of the necessary bits immediately adjacent to data bits. Thus if an eight bit word was to have a single parity bit, then a thirty two bit wide transfer capability would require a thirty six bit storage capability. A thirty two bit wide transfer capability using ECC would require up to three additional bits, normally placed adjacent the data bits and disrupting normal memory element allocation which assumes parity error detection technology.

The present invention is distinguished by providing a DRAM card design (herein referred to as a memory element) in which a plurality of memory chips arranged in an array are each provided with accessibility for RAS and CAS, as shown in Figure 5. In that figure, the accessibility of RAS0 and RAS2 and of CAS0 through CAS7 will be noted. Lines for such signals are, in accordance with this invention, brought out through the connector provided for receiving such a DRAM card. Prior art DRAM cards (not shown) used with parity error detection technology typically have certain of the CAS lines indicated in Figure 5 tied together internally, namely CAS0 and CAS4, CAS1 and CAS5, CAS2 and CAS6, and CAS3 and CAS7.

The present invention also contemplates that DRAM cards may be designed with four banks of memory chips, and such a design is illustrated in Figure 6. As with the card of Figure 5, the card of Figure 6 has a plurality of memory chips arranged in an array and each provided with accessibility for RAS and CAS. Note the accessibility of RAS0 through RAS3 and CAS0 through CAS7.

The DRAM cards of the present invention as illustrated in Figure 5 and 6 have the capability of operating either as parity cards or as ECC cards, as will be brought out more fully hereinafter.

The present invention is also distinguished by providing that the personal computer system 10 accommodates operation in either parity or ECC manners. This characteristic will be addressed more fully hereinafter with reference to Figures 7 through 17, in which a number of examples of such operational capability are given. At this point in the description, it is sufficient to note that the BIC 35 provides the function, among others, of a memory controller capable of addressing physical memory locations within the DRAM 36. Further, the DRAM cards contemplated by this invention are received in a plurality of socket connectors provided on the planar board 20, each of which is indicated schematically in Figure 7 through 17 at 61.

The present invention is further distinguished by the sharing of physical memory addresses between two DRAM cards in order to accommodate the writing, storage and reading of the additional bits needed to achieve ECC operation. That is, cards of the types illustrated in Figures 4 through 6 may be inserted into any one of the plurality of socket connectors provided and may function, at the election of a user configuring the system 10, as either parity or ECC memory. However, if a DRAM card inserted in a first position is to be used as an ECC memory, then certain of the ECC bits necessary for the intended function are written, stored and read from a physical location to be found on a second card. Further, the total number of ECC bits required are derived by using the parity bits otherwise normally stored on the first card with bits stored in what would normally be data bit physical addresses in the second card.

By way of illustration of these principles, if such a combination of cards is used to provide ECC operation in an eight bit wide data transfer, then data bits at D0 through D3 on the second card, accessed by RAS0 and CAS0, are used with the parity bit at M0 on the first card to provide five ECC bits. Similarly, data bits at D4 through D7, accessed by RAS0 and CAS4, are used with a parity bit at M1. Data bits at D9 through D12, accessed by RAS0 and CAS1, are used with a parity bit at M2. Data bits at D13 through D17, accessed by RAS0 and CAS5, are used with a parity bit at M3. When such a combination of cards is used to provide ECC operation in a sixteen bit wide data transfer, then data bits at D0 through D3 on the second card, accessed by RAS0 and CAS0, are used with parity bits at M0 and M1 on the first card to provide six ECC bits. Similarly, data bits at D4 through D7, accessed by RAS0 and CAS4, are used with parity bits at M2 and M3. Data bits at D9 through D12, accessed by RAS0 and CAS1, are used with parity bits at M0 and

M1. Data bits at D13 through D17, accessed by RAS0 and CAS5, are used with parity bits at M2 and M3. When such a combination of cards is used to provide ECC operation in a thirty two bit wide data transfer, then data bits at D0 through D3 on the second card, accessed by RAS0 and CAS0, are used with parity bits at M0 through M2 on the first card to provide seven ECC bits. Similarly, data bits at D4 through D7, accessed by RAS0 and CAS4, are used with parity bits at M0 through M2. Data bits at D9 through D12, accessed by RAS0 and CAS1, are used with parity bits at M0 through M2. Data bits at D13 through D17, accessed by RAS0 and CAS5, are used with parity bits at M0 through M2. As will be understood, M0 through M3 are the parity bits existing on a DRAM card which might otherwise be intended for parity operation, one per byte available on the card. D0 through D17 are sixteen (D8 being unused) of the thirty two available data bits in such a card. Each four bits in the ECC function card (called the second card in the discussion above), combined with parity bits available in the parity card (called the first card in the discussion above), forms the ECC code needed for the eight, sixteen and thirty two bit (one byte, two byte and four byte) wide transfers. This analysis does not discuss additional available bits D18 through D35, which are also used in a similar manner for ECC generation for additional memory.

It is to be noted that, if CAS0 and CAS4, CAS1 and CAS5, CAS2 and CAS6, and CAS3 and CAS7 are connected externally of the memory element 60, then the memory element will operate as a DRAM card with parity error detection. This is one of the ways in which a single memory element can be employed in both parity and ECC operations. With the card design of Figure 5, some data bits are connected externally and individual CAS control allows four bit operation. Such four bit control, coupled with the parity bits as described above, provides the five to seven ECC bits needed for one, two or four byte data width single bit correction and double bit detection.

The design of Figure 6 functions similarly to that of Figure 5 while allowing greater capability.

The knowledgeable reader will appreciate that there is a relationship between the memory capability of a memory element 60 in accordance with this invention and the total amount of memory locations which can be supported in ECC operation. The following tables will illustrate such relationships.

Four Megabyte Memory Element						
ECC Bit	SBC	DBD	Data Width	Memory Maximum	RMW 8 bit	RMW 16 bit
4	Yes	No	8	8MB	No	No
5	Yes	Yes	8	8MB	No	No
5	Yes	No	16	16MB	Yes	No
6	Yes	Yes	16	16MB	Yes	No
6	Yes	No	32	32MB	Yes	Yes
7	Yes	Yes	32	32MB	Yes	Yes

Eight Megabyte Memory Element						
ECC Bit	SBC	DBD	Data Width	Memory Maximum	RMW 8 bit	RMW 16 bit
4	Yes	No	8	16MB	No	No
5	Yes	Yes	8	16MB	No	No
5	Yes	No	16	32MB	Yes	No
6	Yes	Yes	16	32MB	Yes	No
6	Yes	No	32	64MB	Yes	Yes
7	Yes	Yes	32	64MB	Yes	Yes

In the tables, the first column indicates the number of ECC bits with which the row is concerned, while the second and third columns identify whether Single Bit Correction (SBC) and Double Bit Detection (DBD) are performed. The Maximum Memory column identifies the maximum number of physical memory address which can be handled, and the RMW (for read/modify/write) columns indicate whether or not such operations will be required for eight and sixteen bit writes.

For a given number of ECC bits, there is a corresponding maximum amount of memory which can be supported by a memory element in accordance with this invention when used as an ECC card (that is, a DRAM card in which ECC bits alone are written, stored and from which such bits are read). There is also a choice of data width that a user may choose, with sufficient flexibility to accommodate least cost and best

performance requirements. For example, from the Four Megabyte table, such a memory element may be used in an ECC system to support up to thirty two megabytes of memory, with read/modify/write (RMW in the table) operations on eight and sixteen bit writes. The same card can be setup to support eight megabytes of memory with no penalty of RMW on eight and sixteen bits writes. There is also a choice of six ECC bits which is midway of the others. The Eight Megabyte table illustrates similar availabilities.

Applications of the present invention are schematically illustrated in Figures 7 through 17. Each of these figures shows a simplified schematic of a portion of the computer system 10 as illustrated in Figure 3, namely the BIC 35 and the socket connectors in which DRAM cards 60 may be received. In the Figures, some socket connectors are sometimes shown as Empty, in order that a full range of performance variations may be indicated. In Figures 7 through 12, one socket connector is served by RAS0 through RAS3 lines from the memory controller function of the BIC 35, and functions as the connection point for a DRAM card used as what is here referred to as an ECC card. The function of the card inserted into that socket is to receive the additional ECC bits which, when combined with parity bits received by cards inserted into other sockets, will provide the ECC function described above. The ECC card, and the socket into which such a card would be inserted, is used only for the ECC function described and not for other data.

In the example of Figure 7, the machine has been configured with eight megabytes of memory by the insertion of two four megabyte memory elements (as in Figure 5) into two sockets. With an ECC card absent, the memory functions with parity detection only.

In Figure 8, a four megabyte memory element has been inserted into the ECC socket, enabling the use of eight megabytes of memory with five bit ECC.

In Figure 9, the user of the system of Figure 8 has presumably decided that current needs are for twelve megabytes of memory, and that parity detection is sufficient. Thus the user may remove the memory element from the ECC socket and relocate it to another socket for use as parity memory.

Figure 10 illustrates the manner in which the user of the system of Figure 9 could return to ECC operation, obtaining the best performance for the twelve megabytes of installed memory by using an eight megabyte memory element (as in Figure 6) in the ECC socket. In Figure 10, all sockets in the illustrated set are filled, opening the possibility of relocating the memory elements used as memory requirements may vary.

Figure 11 illustrates such a change, where the eight megabyte memory element has been switched with one of the four megabyte memory elements, to give sixteen megabytes of active memory used with six bit ECC. Figure 12 illustrates the next step, in which active memory is again at sixteen megabytes, while higher performance ECC is attained by using an eight megabyte ECC Card.

The arrangements of Figure 13 through 17 differ from those found in Figures 7 through 12 in that lines for CAS4 through CAS7 have been added for what has been identified as the ECC socket in the earlier figures. This allows the DRAM card inserted into that socket to be used as parity memory in addition to being used as ECC memory as described herein. Figures 13 and 14 generally parallel Figures 7 and 8 as described above. However, Figure 15 illustrates the use of a simple software instruction to use what had been (in Figure 14) the ECC card as a parity memory card, thereby increasing the memory to twelve megabytes. Figure 16 parallels Figure 11 described above, while Figure 17 parallels Figure 12.

As will be understood from a careful consideration of the description above, the present invention contemplates a particular organization of a memory element (in which particular access is possible to the memory chips in an array); of a personal computer system (in which a memory controller function accesses memory elements in a particular way to distribute ECC data between two physical memory elements); and of a method of operating a personal computer system (in which physical memory elements may be readily moved from location to location while varying the error detection technology employed).

In the drawings and specifications there has been set forth a preferred embodiment of the invention and, although specific terms are used, the description thus given uses terminology in a generic and descriptive sense only and not for purposes of limitation.

Claims

1. A computer system comprising:

a processor;

a plurality of socket connectors, each for receiving a volatile memory element, one of said socket connectors being addressable for connecting with memory elements having devices addressable for

handling data bits in a first predetermined word length and the remainder of said socket connectors being addressable for connecting with memory elements having devices addressable for handling data bits in any selected one of multiples of two, four and eight times the predetermined word length; and

a memory controller coupled to said microprocessor for issuing row and column address signals determining the physical location in available volatile memory elements of data written thereto and stored therein and read therefrom,

said memory controller directing to said one socket connector data bit words representing error correcting code and directing to another of said socket connectors data bit words representing data associated with the error correcting code directed to said one socket connector.

2. A computer system as claimed in Claim 1 comprising: a data bus, the processor being coupled directly to said data bus, the plurality of socket connectors being coupled directly to said data bus, one of said socket connectors being configured for connecting with memory elements having devices addressable for handling data bits in four bit words and the remainder of said socket connectors being configured for connecting with memory elements having devices addressable for handling data bits in any selected one of eight, sixteen and thirty two bit words; and

wherein the memory controller is in the form of a bus interface controller coupled directly to said data bus for providing communications between the data bus and an input/output data bus.

3. A computer system as claimed in Claim 1 or Claim 2 comprising:

one or more volatile memory elements, each mounted in a corresponding one of said plurality of socket connectors and having:

a substrate;

a plurality of dynamic random access memory devices mounted in an array on said substrate, said devices being arranged in banks and pages for receiving data bits written to and stored in and read from said devices;

a plurality of signal conducting pathways on said substrate connecting to said devices for transferring data bits thereto and therefrom;

a connector coupled to said pathways for coupling said devices to a personal computer system; and

a protective enclosure encompassing said substrate and said devices and said connector;

said pathways and said devices together providing for access of column address signals to each of said devices and of row address signals to each of said banks of said devices, whereby data bits written to and stored in and read from said devices may be handled in any selected one of the predetermined word length and multiples of two, four and eight times the predetermined word length.

4. A personal computer system comprising:

a microprocessor;

a plurality of socket connectors, each for receiving a volatile memory element, one of said socket connectors being addressable for connecting with memory elements having devices addressable for handling data bits in any selected one of a first predetermined word length and multiples of two, four and eight times the predetermined word length and the remainder of said socket connectors being addressable for connecting with memory elements having devices addressable for handling data bits in any selected one of multiples of two, four and eight times the predetermined word length;

a plurality of volatile memory elements, each mounted in a corresponding one of said plurality of

socket connectors and having:

a substrate;

a plurality of dynamic random access memory devices mounted in an array on said substrate, said devices being arranged in banks and pages for receiving data bits written to and stored in and read from said devices;

a plurality of signal conducting pathways on said substrate connecting to said devices for transferring data bits thereto and therefrom;

a connector coupled to said pathways for coupling said devices to a personal computer system; and

a protective enclosure encompassing said substrate and said devices and said connector;

one of said volatile memory elements being mounted in said one socket connector and having said pathways and said devices together providing for access of column address signals to each of said devices and of row address signals to each of said banks of said devices, whereby data bits written to and stored in and read from said devices may be handled in any selected one of the first predetermined word length and multiples of two, four and eight times the predetermined word length;

the remainder of said volatile memory elements each being mounted in a corresponding one of said remainder of said socket connectors and having said pathways and said devices together providing for access of column address signals to pairs of said devices and of row address signals to each of said banks of said devices, whereby data bits written to and stored in and read from said devices may be handled in any selected one of multiples of two, four and eight times the predetermined word length; and

a bus interface controller coupled to said socket connectors for issuing row and column address signals determining the physical location in available volatile memory elements of data written thereto and stored therein and read therefrom;

said bus interface controller selectively enabling the direction to said one socket connector and said one of said volatile memory elements mounted therein of data bit words representing error correcting code and the direction to another of said socket connectors and the other of said volatile memory elements mounted therein data bit words representing data associated with error correcting code directed to said one socket connector.

5. A personal computer system comprising:

a microprocessor;

a plurality of socket connectors, each for receiving a volatile memory elements, one of said socket connectors being configured for connecting with memory elements having devices addressable for handling data bits in a first predetermined word length and the remainder of said socket connectors being configured for connecting with memory elements having devices addressable for handling data bits in any selected one of multiples of two, four and eight times the predetermined word length;

a plurality of volatile memory elements, each mounted in a corresponding one of said plurality of socket connectors and having:

a substrate;

a plurality of dynamic random access memory devices mounted in an array on said substrate, said devices being arranged in banks and pages for receiving data bits written to and stored in and read from said devices;

a plurality of signal conducting pathways on said substrate connecting to said devices for transferring data bits thereto and therefrom;

a connector coupled to said pathways for coupling said devices to a personal computer system; and

a protective enclosure encompassing said substrate and said devices and said connector;

one of said volatile memory elements being mounted in said one socket connector and having said pathways and said devices together providing for access of column address signals to each of said devices and of row address signals to each of said banks of said devices, whereby data bits written to and stored in and read from said devices may be handled in the first predetermined word length;

the remainder of said volatile memory elements each being mounted in a corresponding one of said remainder of said socket connectors and having said pathways and said devices together providing for access of column address signals to pairs of said devices and of row address signals to each of said banks of said devices, whereby data bits written to and stored in and read from said devices may be handled in any selected one of multiples of two, four and eight times the predetermined word length; and

a bus interface controller coupled directly to said socket connectors for issuing row and column address signals determining the physical location in available volatile memory elements of data written thereto and stored therein and read therefrom;

said bus interface controller directing to said one socket connector and said one of said volatile memory elements mounted therein data bit words representing error correcting code and directing to another of said socket connectors and the other of said volatile memory elements mounted therein data bit words representing data associated with error correcting code directed to said one socket connector.

6. A personal computer system comprising:

a microprocessor;

a plurality of socket connectors, each for receiving a volatile memory element, one of said socket connectors being a software selectable parity/ECC connector addressable for connecting with memory elements having devices addressable for handling data bits in any selected one of a first predetermined word length and multiples of two, four and eight times the predetermined word length and the remainder of said socket connectors being parity connectors addressable for connecting with memory elements having devices addressable for handling data bits in any selected one of multiples of two, four and eight times the predetermined word length;

a plurality of volatile memory elements, each mounted in a corresponding one of said plurality of socket connectors and having:

a substrate;

a plurality of dynamic random access memory devices mounted in an array on said substrate, said devices being arranged in banks and pages for receiving data bits written to and stored in and read from said devices;

a plurality of signal conducting pathways on said substrate connecting to said devices for transferring data bits thereto and therefrom;

a connector coupled to said pathways for coupling said devices to a personal computer system; and

a protective enclosure encompassing said substrate and said devices and said connector;

one of said volatile memory elements being a parity/ECC memory element mounted in said one parity/ECC connector and having said pathways and said devices thereof together providing for access of column address signals to each of said devices and of row address signals to each of said banks of said devices, whereby data bits written to and stored in and read from said devices may be handled in any selected one of the first predetermined word length and multiples of two, four and eight times the predetermined word length;

the remainder of said volatile memory elements each being a parity memory element mounted in a corresponding one of said parity connector remainder of said socket connectors and having said pathways and said devices together providing for access of column address signals to pairs of said devices and of row address signals to each of said banks of said devices, whereby data bits written to and stored in and read from said devices may be handled in any selected one of multiples of two, four and eight times the predetermined word length; and

a bus interface controller coupled to said socket connectors for issuing row and column address signals determining the physical location in available volatile memory elements of data written thereto and stored therein and read therefrom;

said bus interface controller selectively enabling the direction to said parity/ECC connector and said parity/ECC memory element of data bit words representing error correcting code and the direction to one of said parity socket connectors and the parity memory element mounted therein data bit words representing data associated with error correcting code directed to said parity/ECC socket connector.

7. A personal computer system comprising:

a microprocessor;

a plurality of socket connectors, each for receiving a volatile memory elements, one of said socket connectors being an ECC connector configured for connecting with memory elements having devices addressable for handling data bits in a first predetermined word length and the remainder of said socket connectors being parity connectors configured for connecting with memory elements having devices addressable for handling data bits in any selected one of multiples of two, four and eight times the predetermined word length;

a plurality of volatile memory elements, each mounted in a corresponding one of said plurality of socket connectors and having:

a substrate;

a plurality of dynamic random access memory devices mounted in an array on said substrate, said devices being arranged in banks and pages for receiving data bits written to and stored in and read from said devices;

a plurality of signal conducting pathways on said substrate connecting to said devices for transferring data bits thereto and therefrom;

a connector coupled to said pathways for coupling said devices to a personal computer system; and

a protective enclosure encompassing said substrate and said devices and said connector;

one of said volatile memory elements being an ECC memory element mounted in said ECC connector and having said pathways and said devices together providing for access of column address signals to each of said devices and of row address signals to each of said banks of said devices, whereby data bits written to and stored in and read from said devices may be handled in the first predetermined word length;

the remainder of said volatile memory elements each being parity memory elements mounted in a corresponding one of said parity connectors and having said pathways and said devices together providing for access of column address signals to pairs of said devices and of row address signals to each of said banks of said devices, whereby data bits written to and stored in and read from said devices may be handled in any selected one of multiples of two, four and eight times the predetermined word length; and

a bus interface controller coupled directly to said socket connectors for issuing row and column address signals determining the physical location in available volatile memory elements of data written thereto and stored therein and read therefrom;

said bus interface controller directing to said ECC connector and said ECC memory elements mounted therein data bit words representing error correcting code and directing to one of said parity connectors and the parity memory element mounted therein data bit words representing data associated with error correcting code directed to said ECC connector.

8. A memory element for a computer system as claimed in any preceding claim comprising :

a substrate;

a plurality of dynamic random access memory devices mounted in an array on said substrate, said devices being arranged in banks and pages for receiving and retaining data bits written to and stored in and read from said devices;

a plurality of signal conducting pathways on said substrate connecting to said devices for transferring data bits thereto and therefrom;

a connector coupled to said pathways for coupling said devices to a computer system; and

a protective enclosure encompassing said substrate and said pathways and said devices and said connector;

said pathways and said devices together providing for access of column address signals to each of said devices and of row address signals to each of said banks of said devices, whereby data bits written to and stored in and read from said devices may be handled in any selected one of a first predetermined word length and multiples of two, four and eight times that word length.

9. A memory element as claimed in Claim 9 wherein:

data bits written to and stored in and read from said devices may be handled in any selected one of four, eight, sixteen and thirty two bit words.

10. A method of operating a computer comprising:

parity memory elements for receiving, storing and permitting reading of parity data comprising data bits and associated parity bits; and

ECC memory elements for receiving, storing and permitting reading of error correcting code associated with parity data and comprising error correction bits and permitting a selection between parity and error correction code error detection, the method comprising the step of:

selecting between parity error detection and error correction code error detection; and

in the event parity error detection is selected, writing and reading data only to and from parity memory elements;

in the event error correction code error detection is selected, coordinating the writing and reading of data to and from parity memory elements and the writing and reading of associated error correcting

code to and from ECC memory elements.

11. A method of operating a personal computer, parity memory elements for receiving, storing and permitting reading of parity data comprising data bits and associated parity bits; and

ECC memory elements for receiving, storing and permitting reading of error correcting code associated with parity data and comprising error correction bits;

using error correction code error detection, the method comprising the step of:

coordinating the writing and reading of data to and from parity memory elements and the writing and reading of associated error correcting code to and from ECC memory elements.

12. A method according to Claim 11 wherein parity bits associated with parity data written to and stored in and read from parity memory elements are combined with associated error correction code bits written to and stored in and read from ECC memory elements for supplying an error correction code block to be used in performing error detection.

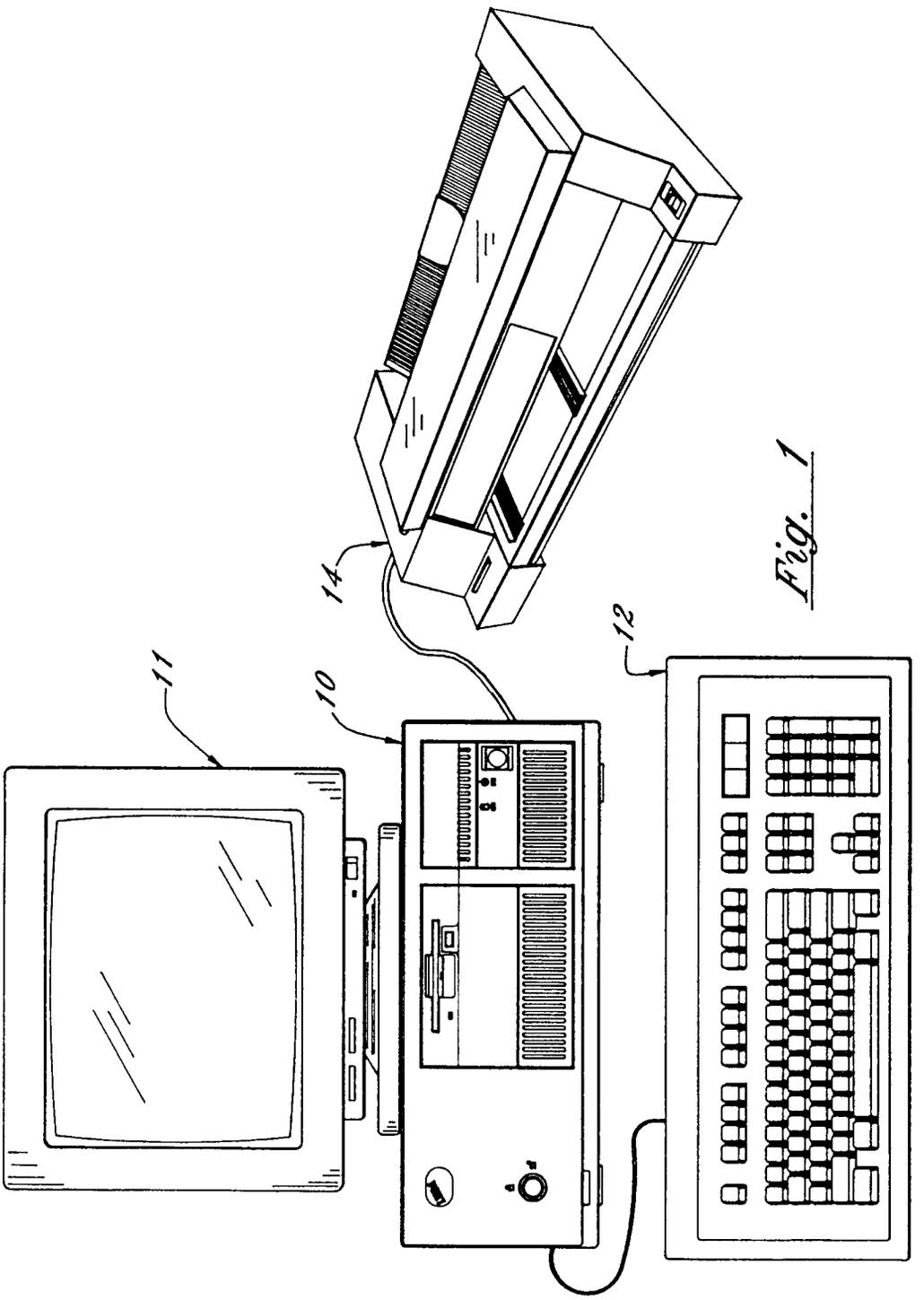


Fig. 1

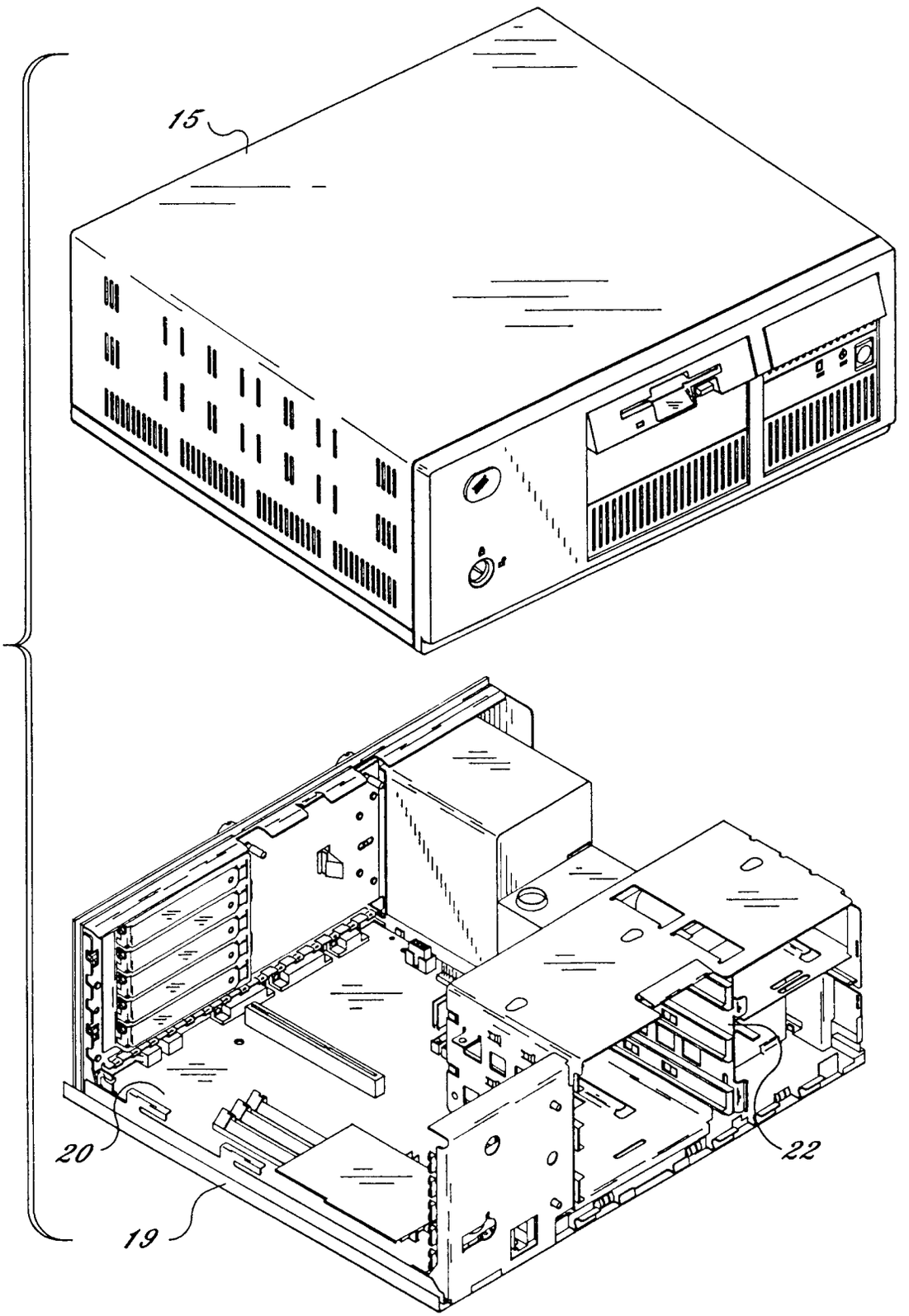
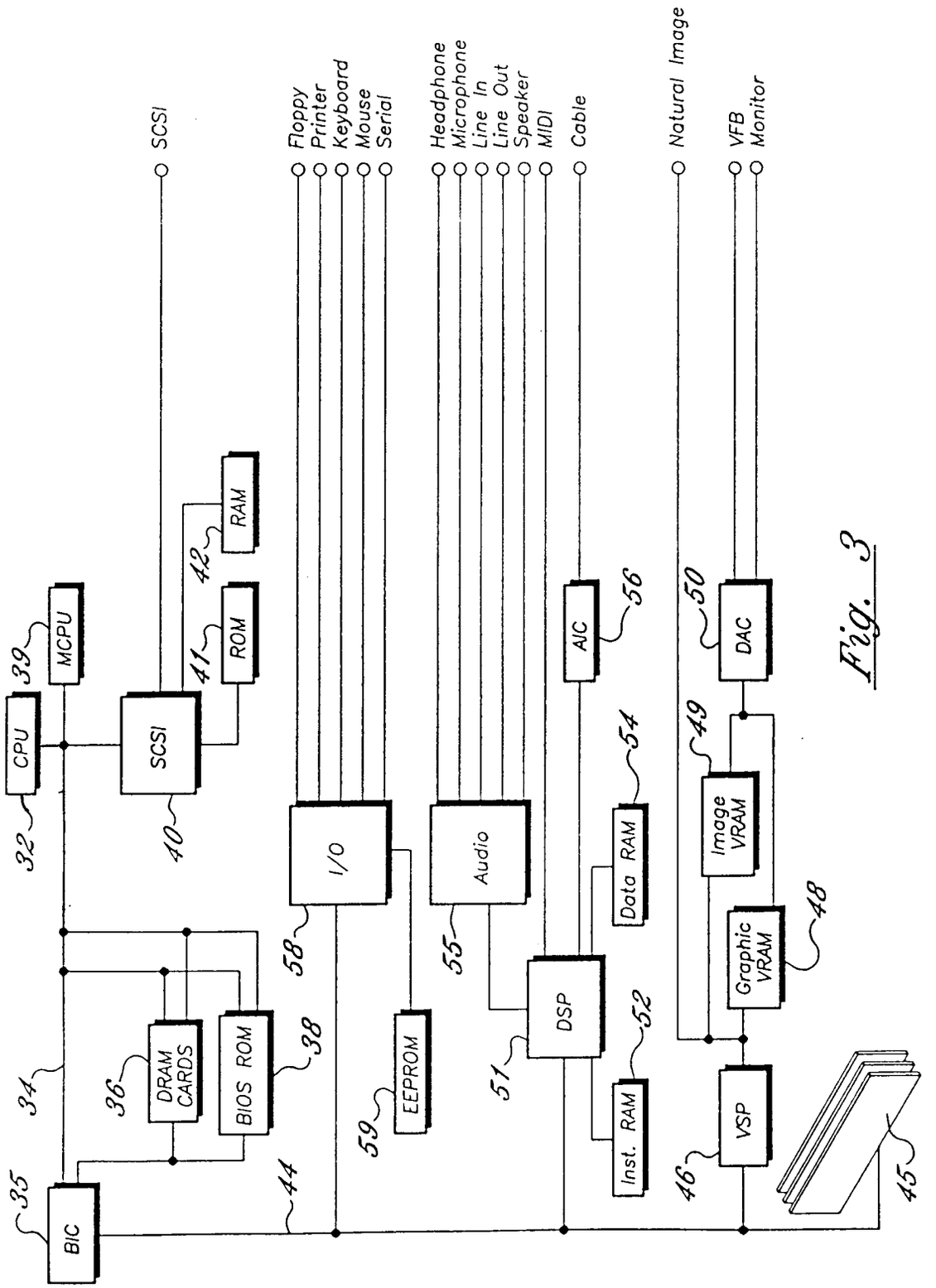


Fig. 2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Floppy
Printer
Keyboard
Mouse
Serial
Headphone
Microphone
Line In
Line Out
Speaker
MIDI
Cable
Natural Image
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MCPU
CPU
SCSI
RAM
ROM
I/O
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AIC
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Fig. 3

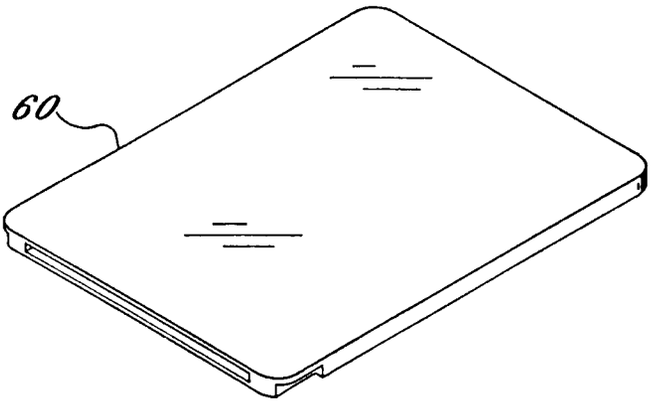
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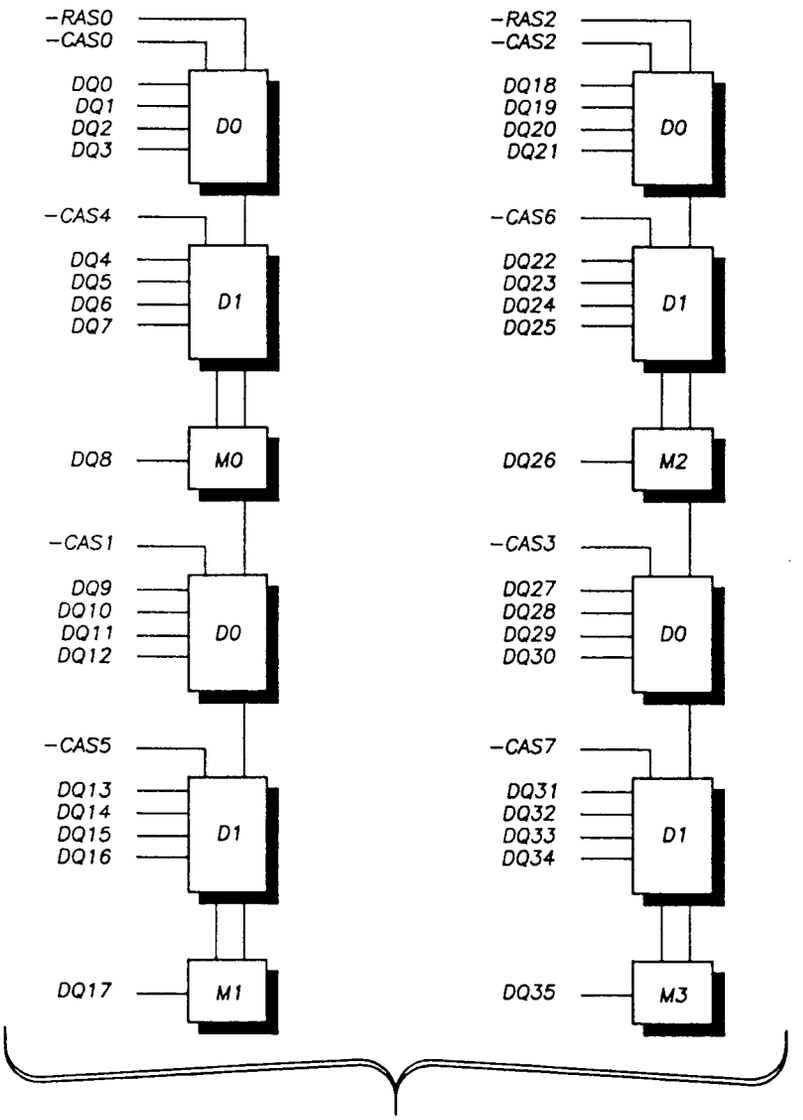
Fig. 4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D0
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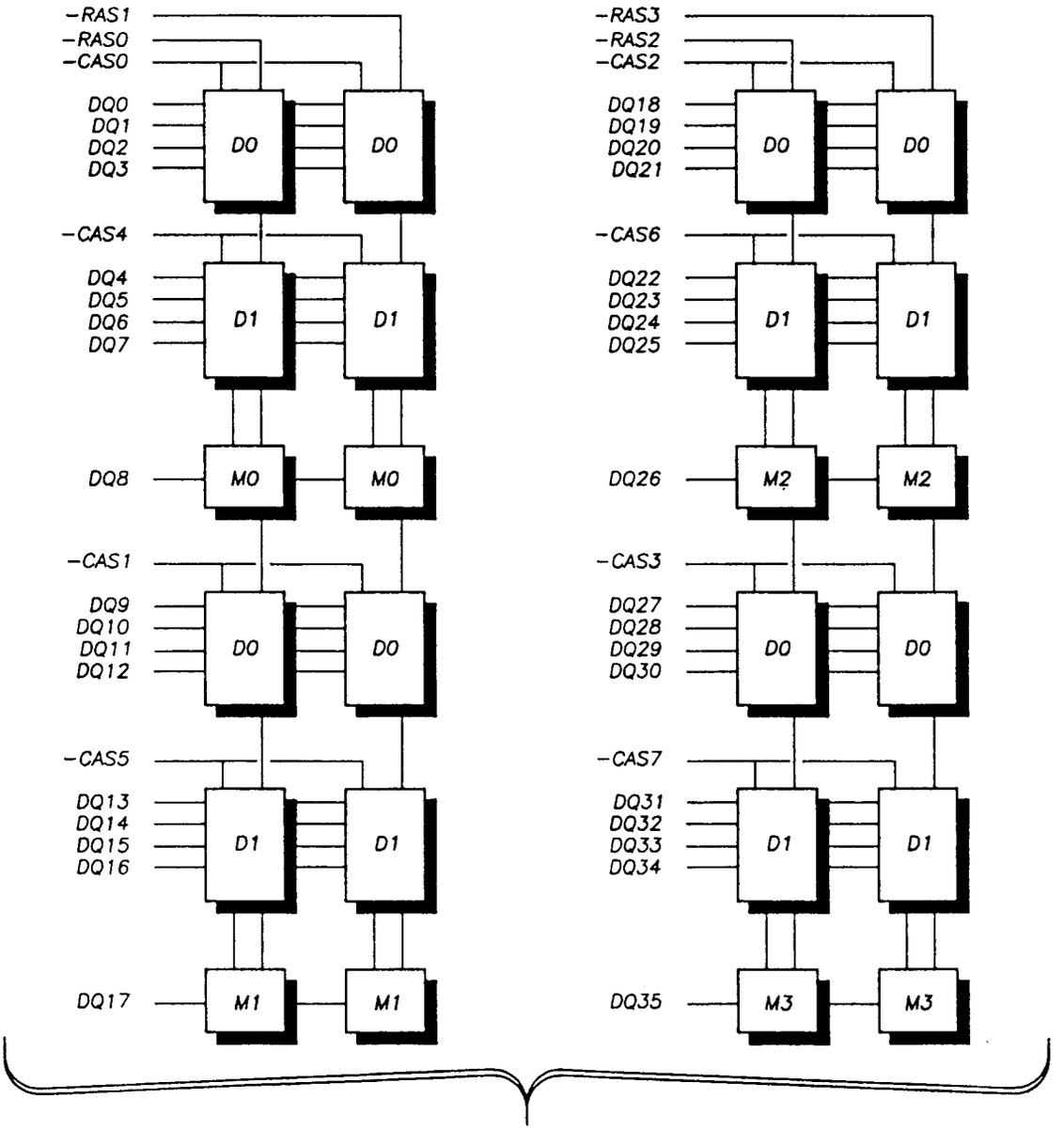
Fig. 5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DQ16
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Fig. 6

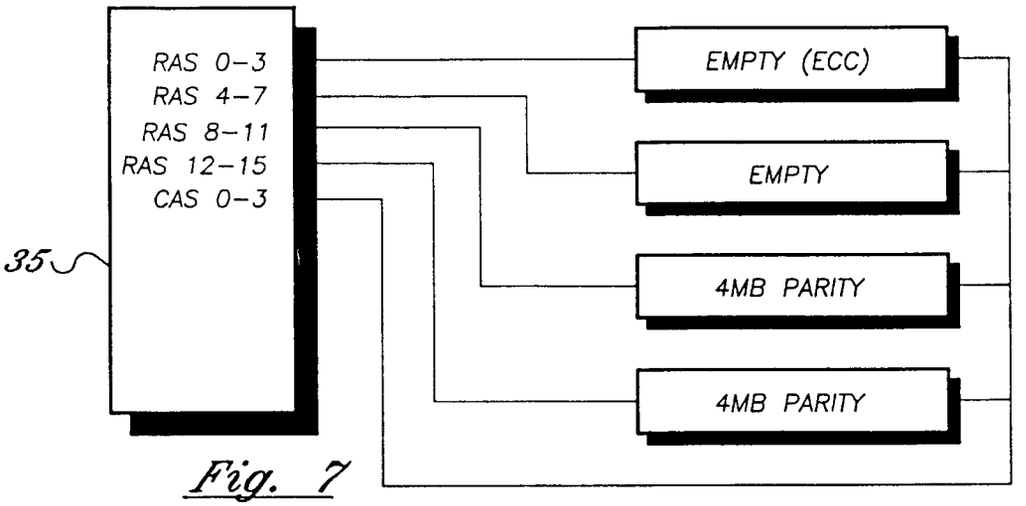


Fig. 7

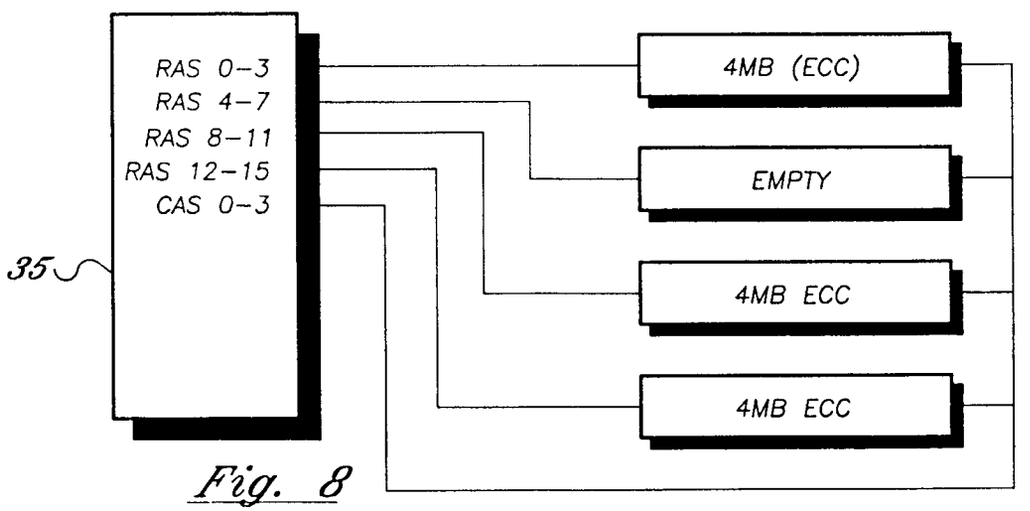


Fig. 8

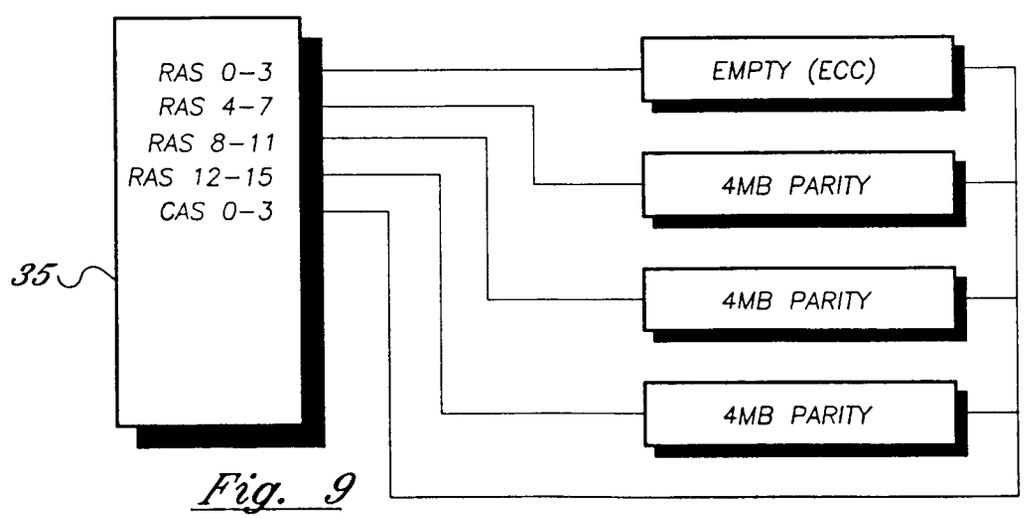


Fig. 9

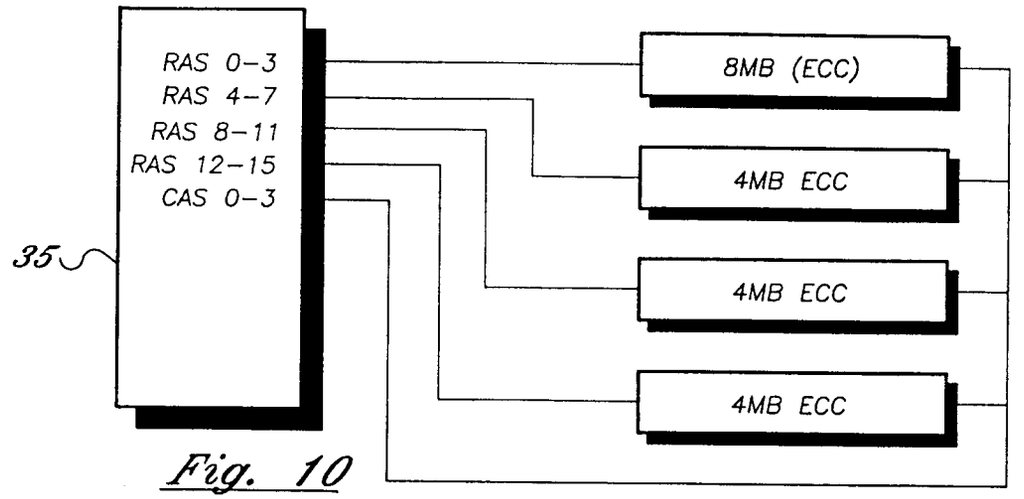


Fig. 10

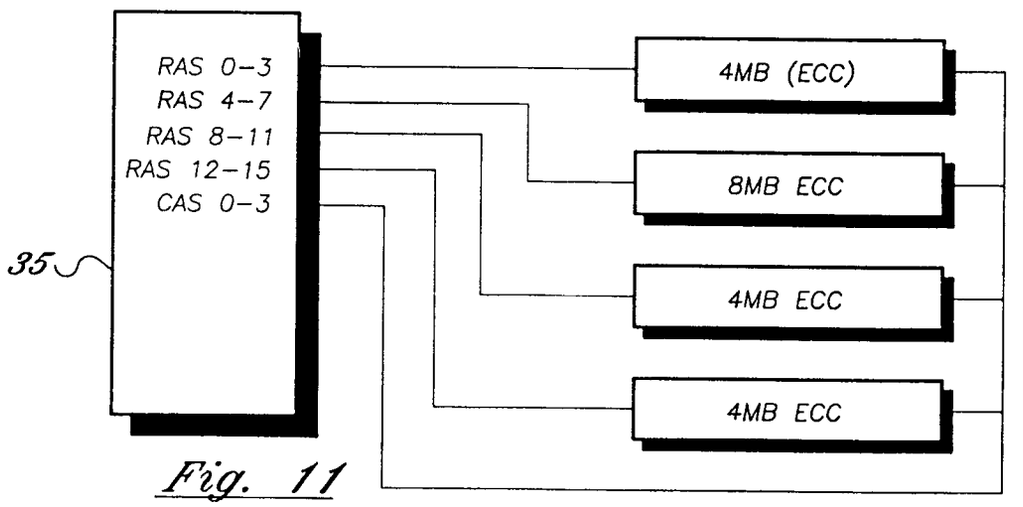


Fig. 11

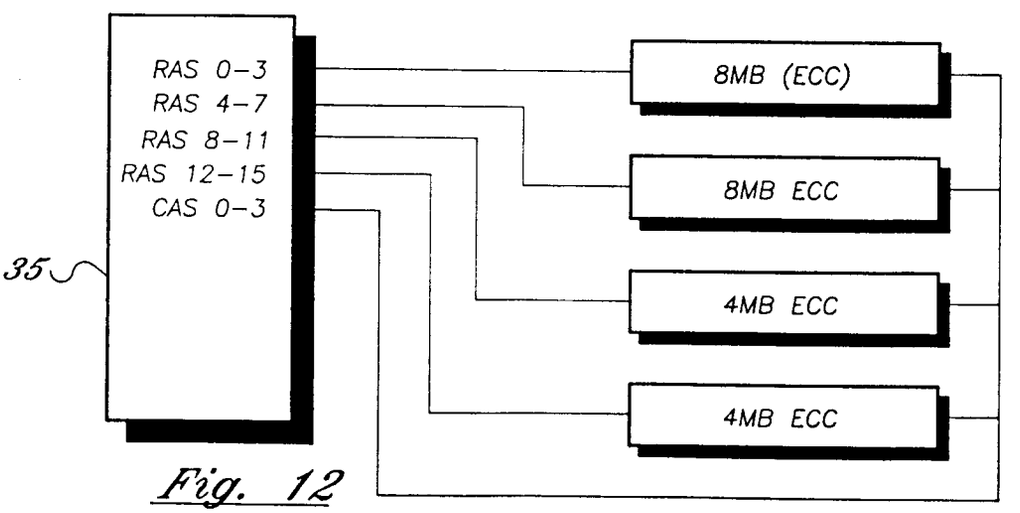


Fig. 12

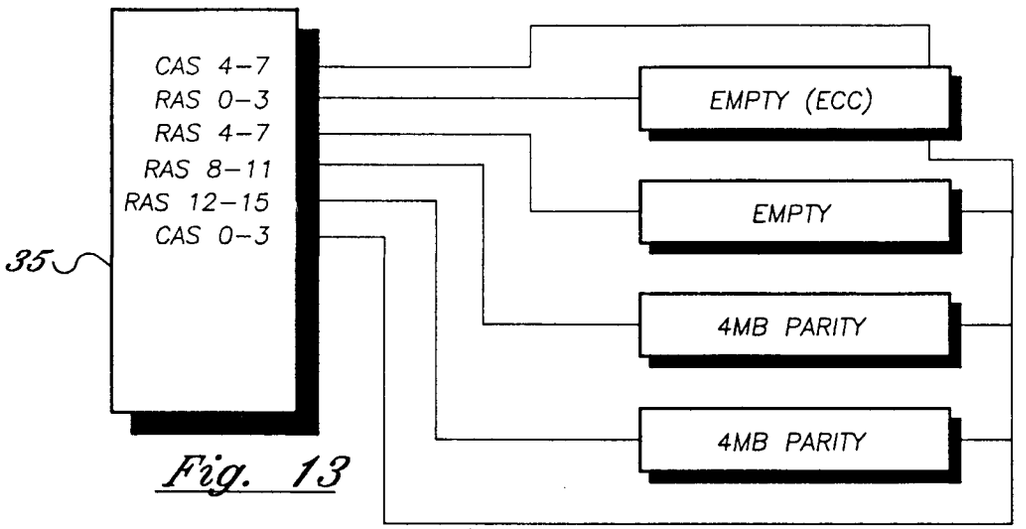


Fig. 13

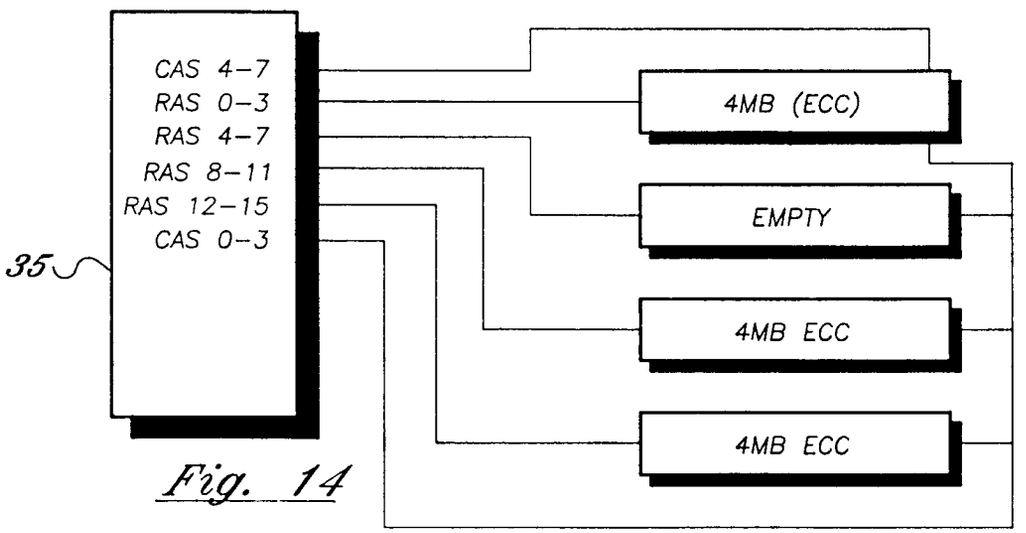


Fig. 14

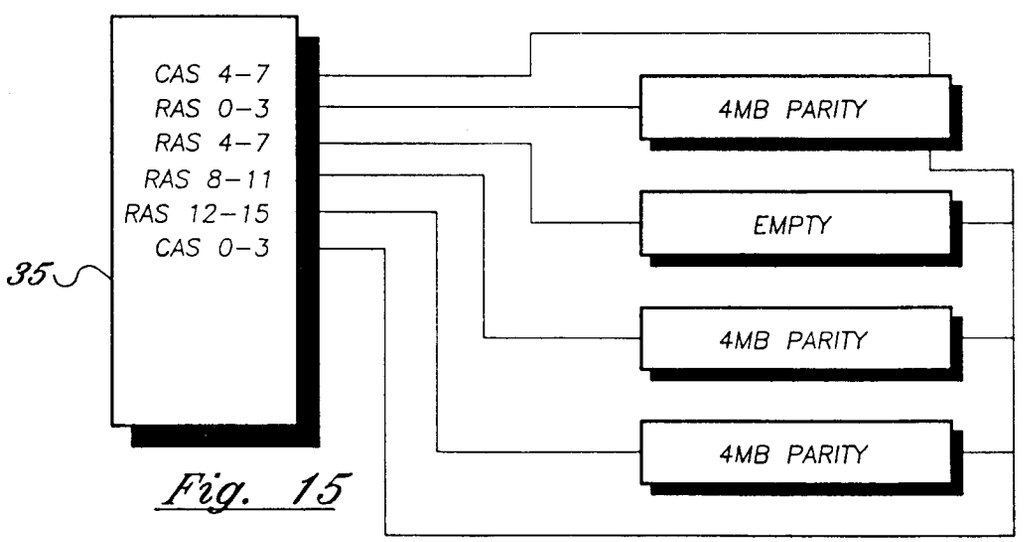
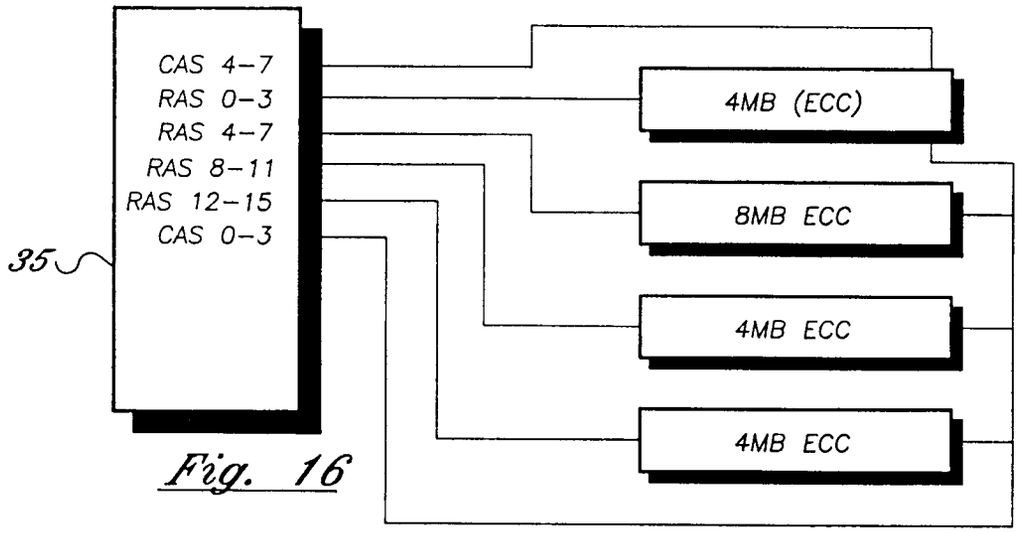


Fig. 15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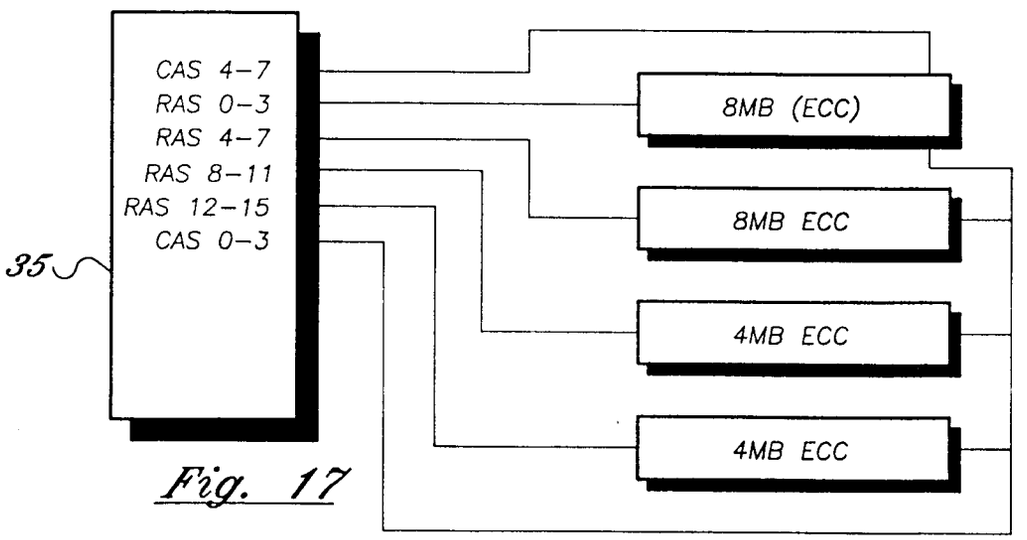
8MB ECC
4MB ECC
4MB ECC

Fig. 16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8MB (ECC)
8MB ECC
4MB ECC
4MB ECC

Fig. 17