WD90C26

VGA Flat Panel

Display Controller

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1.0 INTRODUCTION

This introduction contains the following information:

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1.1 SCOPE

The WD90C26 VGA Laptop Display Controller allows control of a flat-panel display, along with simultaneous display on a traditional CRT. The WD90C26 supports all of today's mono and color flat-panel technologies.

The WD90C26 has improved power management capabilities and a performance-scaling capability that makes it an ideal video solution for low battery drain portable computer applications.

1.2 FEATURES

- True 64-gray scale in including 640 by 480 by 256 mode
- Simultaneous display (with all types of flat-panels)*
- 'WD90C26LV' low voltage version available
- On-board VGA compatible RAMDAC
- Zero wait-state performance
- Adjustable video FIFO depth and fast page mode memory timing
- System interface write buffering
- Flexible display memory configuration (2, 3 or four 256K by 4 DRAMs or one 256K by 16 DRAM)
- 8- or 16-bit I/O and memory interface
- True 16-bit CPU to display memory data transfer in all modes
- 27K colors on 9-bit TFT color LCD panel, 256K colors on 9-bit STN LCD panel, and 4K undithered direct colors on 12-bit TFT color LCD panel
- Full screen presentation in simultaneous display mode
- Hardware auto-centering and vertical expansion
- Up to 16 loadable fonts
- Supports 800 by 600 by 256 and 1024 by 768 by 16 non-interlaced modes on CRT display
- Hidden register support for 100% hardware compatibility with IBM's VGA standards
- 100% compatibility with CGA, MDA, Hercules Graphics
- Typical power dissipation of 450 mW at 5V operation
- Up to 65 MHz maximum video clock rate on CRT display
- Up to 45 MHz maximum video clock rate on LCD display
- Up to 45 MHz maximum memory clock rate
- On-chip 8/16-bit ISA Bus (AT bus) interface
- On-chip 8- or 16-bit Micro Channel interface
- I/O mapping improves board level testability
- Enhanced power down management modes
- 144-pin EIAJ package
- Compatible with WD90C55 color STN LCD interface

* Patent pending

1.3 GENERAL DESCRIPTION

The Western Digital WD90C26 is a 0.9 micron CMOS VGA controller designed to simultaneously drive a flat-panel display and the traditional analog CRT with a minimum of external components. The only additional components required for a complete flat-panel VGA subsystem are 1, 2, 3, or 4 DRAMs and video/memory clock sources. Contained on-board are a RAMDAC and a flat-panel interface. The full-featured RAMDAC is capable of directly driving P/S2 style analog color or monochrome

monitors. The full-featured flat-panel interface is capable of supporting LCD, plasma, and EL and other flat-panel technologies.

The WD90C26's scalable architecture allows it to be used with either 2, 3, or 4 external 256K by 4 DRAMs or one 256K by 16 DRAM. Basic VGA performance is available with the minimum 2 DRAM configuration or the single 256K by 16 DRAM con-fig-uration. Added panel support and enhanced VGA modes are available using 3 or 4 256K by 4 DRAMs. 16-bit video memory performance is also available using the 4 256K by 4 DRAM configuration or the single 256K by 16 DRAM configuration. DRAM utilization is firmware controllable, allowing the scaling of DRAM power consumption or increasing performance.

Western Digital's superior orthogonal 64-gray scale to 64-gray scale mapping technology allows system developers to 'hand tune' each of the shades in the 64-gray scale to provide the most realistic linear gray scale shading for a particular panel. This is achieved through use of a firmware programmable 64-word gray scale lookup table on-board the WD90C26.

As with all Western Digital VGA offerings, the WD90C26 is 100% compatible with IBM VGA, CGA, MDA, and Hercules video systems. Through the use of its hidden, or 'shadow' registers, the WD90C26 can be programmed to support fixed-LCD screen sizes, yet appear to the host as capable of displaying the variety of screen pitches available with analog monitors. System routine modifications to video system registers, thus shadowed or hidden, do not destroy the WD90C26's ability to display the desired information on a flat-panel display as well.

The WD90C26's auto-centering and vertical expansion features provide full-screen flat-panel displays even in video modes with lower resolutions than those of the panel. A unique expansion algorithm provides for realistic appearance of both text and graphics on expanded displays, without requiring the use of special expanded display fonts.

Advanced power management features include:

- Separate supply pins for certain functions so that parts of the chip may be externally powered off
- The capability to slow down internal clocks to conserve power and to deactivate or tri-state I/O pins during power-down and reset modes
- Power sequencing that can be used to control power supply and interface signals, and to prevent panel burnout

Also included in the WD90C26 is an advanced TFT support circuit that allows display from a palette of 27K colors on 9-bit interface color panels.

The WD90C26 directly supports TFT displays with 12-bit interfaces with undithered 12-bit direct colors from a 4K palette for optimum 12-bit display performance.

2.0 ARCHITECTURE

This section describes the architecture of the WD90C26. A block diagram of the architecture is shown in Figure 2-1. The components described are:

- System Interface Logic
- CRT Controller
- Video Sequencer
- Video Graphics Controller
- Video Attribute Controller
- RAMDAC
- Flat Panel Adapter
- Display Memory Interface
- Power-Down Control

2.1 SYSTEM INTERFACE LOGIC

The WD90C26 includes a host system interface for direct connection to an ISA standard bus or IBM compatible Micro Channel. The interface allows the following features:

- Full 16-bit I/O and memory cycles
- Zero wait-state performance capability
- 16-bit to 8-bit data path conversion
- Full decoding of 16 MBytes of memory space for mapping of video memory, without requiring external decode logic
- Internal buffering of system operations to speed performance
- External video BIOS ROM

2.2 CRT CONTROLLER

A VGA-compatible CRT controller includes the following functions:

- Generates video buffer addresses for screen refresh operations
- Generates monitor synchronization signals
- Controls an alpha-numeric cursor
- May be set with remapped register locations to operate as a CGA, MDA, or Hercules
- Register shadowing

2.3 VIDEO SEQUENCER

The VGA compatible video sequencer is the central timing and memory control section of the WD90C26. Its functions include the following:

- Generation of memory handshake signals
- Control of CRT controller timings
- Provision of general interface timing and control signals to the balance of the WD90C26

2.4 VIDEO GRAPHICS CONTROLLER

The VGA video graphics controller performs VGA graphics operations on video data such as AND, OR, XOR, rotate, and color comparison functions.

2.5 VIDEO ATTRIBUTE CONTROLLER

The WD90C26's video attributes are added to display data by the Video Attribute Controller. Data added includes:

- Standard text attributes
- VGA graphics mode attributes
- Cursor display
- Screen border color

The Video Attribute Controller also performs data conversion from modes like packed pixel, planar, or text mode into video data to be presented to the RAMDAC.

2.6 RAMDAC

Integrated into the WD90C26 is a fully VGA-compatible high-speed 18-bit RAMDAC. This RAMDAC directly drives VGA and super-VGA color or monochrome analog monitors.

2.7 FLAT-PANEL ADAPTER

The flat-panel adapter takes video information from the WD90C26's internal RAMDAC color palette RAM and converts it into the format appropriate for the type of panel to be attached.

The following functions occur in the flat-panel adapter:

- "Digital DAC" color to monochrome gray scale conversion
- Gray scale mapping
- Gray shade dithering
- Color STN LCD panel dithering circuitry
- Row buffering
- Frame buffering
- Panel format conversion

2.7.1 Color to Gray Scale Conversion

For monochrome flat-panel display of what normally would be a color analog video output, a digital equivalent of the RAMDAC function is required to sum color information together into video signals. This function is accomplished through use of a digital equivalent of the DAC function, which takes the RGB color to gray scale weighting color palette RAM outputs and converts them to their digitally weighted monochrome equivalent. Weighting is performed using NTSC standard algorithms, and may be disabled for Monochrome Display Adapter emulation applications.

2.7.2 Gray Scale Mapping

The WD90C26's flat-panel adapter circuitry incorporates an orthogonal 64-word by 64 gray-scale to gray-shade mapping RAM. This mapping RAM serves as a firmware-programmable lookup table that may be configured to map gray scale value from color-to-gray scale conversion into the dithered gray-scale shades best suited to a particular panel model.

Maximum flexibility in 'tuning' the WD90C26 to work with a particular panel model's characteristics is possible via this mapping RAM. Its size also allows finer control when selecting dithering patterns from the 64-shade monochrome dithering circuitry, allowing any monochrome panel to perform to its best in displaying visually accurate gray scales.

Control of gray scale selection is facilitated by the WD OEM User Utility. Please refer to the application note for details.

2.7.3 Gray Shade Dithering

Monochrome gray shade dithering circuitry provides a total of 64 shades of gray on monochrome flat-panel displays. All 64 shades may be simultaneously displayed. Simultaneous display of 64 shades in VGA modes is possible in 256 color modes only.

2.7.4 Color STN Dithering

For color 4-bit interface STN panels, the WD90C26 dithering circuitry supports color display from the full 256K VGA palette.

2.7.5 Color TFT Panel Dithering Circuitry

For Color TFT panels, dithering circuitry supports a total of 27K colors 9-bit interface panels.

2.7.6 Direct 12-bit TFT Panel Support

The WD90C26 drives 12-bit TFT panels with direct undithered color for a palette of 4K colors.

2.7.7 Row Buffering

Monochrome dual-panel displays (most monochrome LCDs) can be directly supported by the WD90C26 due to its capability to internally buffer alternate panel rows.

When simultaneous display on CRT and monochrome dual panel displays is not required, no external frame buffer memory is needed to support a monochrome dual-panel style LCD.

2.7.8 Frame Buffering

The WD90C26 includes a frame buffering capability that allows simultaneous display on a CRT and on a dual-panel monochrome display. This function requires that a 256K by 4 DRAM be attached to the Bank B memory interface.

When simultaneous display is not required, the WD90C26's internal row buffering provides all the required support for a dual-panel display.

2.7.9 Panel Format Conversion

The internal panel format conversion circuit provides the flexibility to reformat color or monochrome panel data into the particular pixel grouping required.

2.8 DISPLAY MEMORY INTERFACE

The display memory interface that maps videomemory DRAM is controlled by two separate external memory buses. These buses allow the accommodation of the changing needs of peformance, support feature, and power conservation. Descriptions of these buses follow.

The Bank A bus is used for interfacing to 8-bit video memory configurations, or as the lower byte 16-bit video memory configurations.

The Bank B bus is used as the frame buffer interface when simultaneous display on a CRT and a dual-panel display is desired.

When simultaneous display with a dual-panel display is not required, the Bank B bus can either be used to access the upper byte of a 16-bit video memory, or shut down to conserve power.

2.9 POWER-DOWN CONTROL

The WD90C26's ability to control power consumption allows it to work successfully in portable applications. Power consumption is managed by the power-down control block, which performs the following functions:

- Turns off clocks to unused portions of the WD90C26
- Provides refresh signals to video memory when normal refresh functions are shut down
- Controls wakeup/sleep cycling
- Reduces chip power during power-down mode
- Sequences chip reset operations

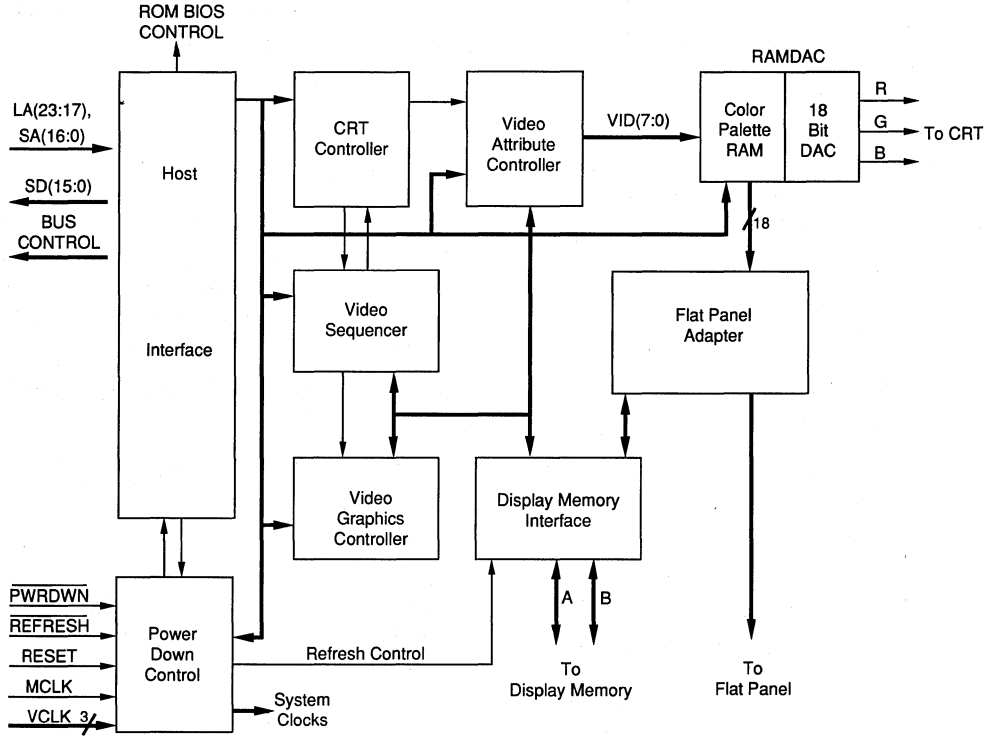

FIGURE 2-1. WD90C26 BLOCK DIAGRAM

3.0 INTERFACES

3.1 INTRODUCTION

This section describes the following WD90C26 interfaces:

- System Interface - Allows the WD90C26 to directly interface to ISA bus-based systems or to Micro Channel-based systems
- BIOS Support Interface - Allows the WD90C26 to provide an enable output for external video BIOS memory
- Video Memory Interface - Allows connection of either 2, 3, or 4 256K by 4 DRAMS or one 256K by 16 DRAM
- Video Interface - Alllows direct connection to most PC-compatible CRTs and to a wide range of industry-standard flat-panel types
- Clock Interface - Controls clock oscillators or allows up to four separate frequency inputs
- Power Management Interface - Allows control of chip power consumption

3.2 SYSTEM INTERFACE

The WD90C26 is designed to directly interface to ISA bus based systems or to Micro Channel based systems.

System interface selection is done by pulling high or low a video memory data line at time of chip reset.

For both Micro Channel and ISA Bus operations, the WD90C26 is mapped into the system I/O address space as the standard set of video I/O registers for the particular video system being emulated.

Four extensively indexed registers at locations 3B5h/3D5h and 3C5h and 3CFh are used to control the vast amount of features beyond those of standard VGA operation.

The WD90C26 has a 1-1/2 word write buffer which operates as a 2-cycle write buffer. This allows the WD90C26 to operate with a very high percentage of true zero wait state performance.

The WD90C26 is designed to be a portable computing device where driving a large capacitive bus, such as found in traditional PCs, is not a factor. To reduce power consumption, the WD90C26's system interface has been designed to drive typical loadings found in laptop applications where bus devices are few and closely grouped.

3.2.1 ISA Bus Interface

The WD90C26 interfaces to an ISA bus at bus clock rates of up to 12.5 MHz. The WD90C26 supports full 16-bit memory and I/O transfers. Support of 16-bit memory transfers is independent of whether the WD90C26 has an 8-bit or 16-bit video memory path, although increased performance occurs when a 16-bit video memory is available.

The following ISA Bus signals are directly supported by the WD90C26:

LA[23:17]	$\overline{\text{IOW}}$
SA [16:0]	$\overline{\text{MEMCS16}}$
$\overline{\text{BALE}}$	IOCS16
$\overline{\text{SBHE}}$	IOCHRDY
AEN	$\overline{\text{SRDY (OWS)}}$
$\overline{\text{SD[15:0]}}$	REFRESH
$\overline{\text{MEMR}}$	RESET
$\overline{\text{MEMW}}$	IRQ
$\overline{\text{IOR}}$	

LA addresses are latched internal to the WD90C26 by the ALE signal to eliminate bus timing problems in some common system implementations.

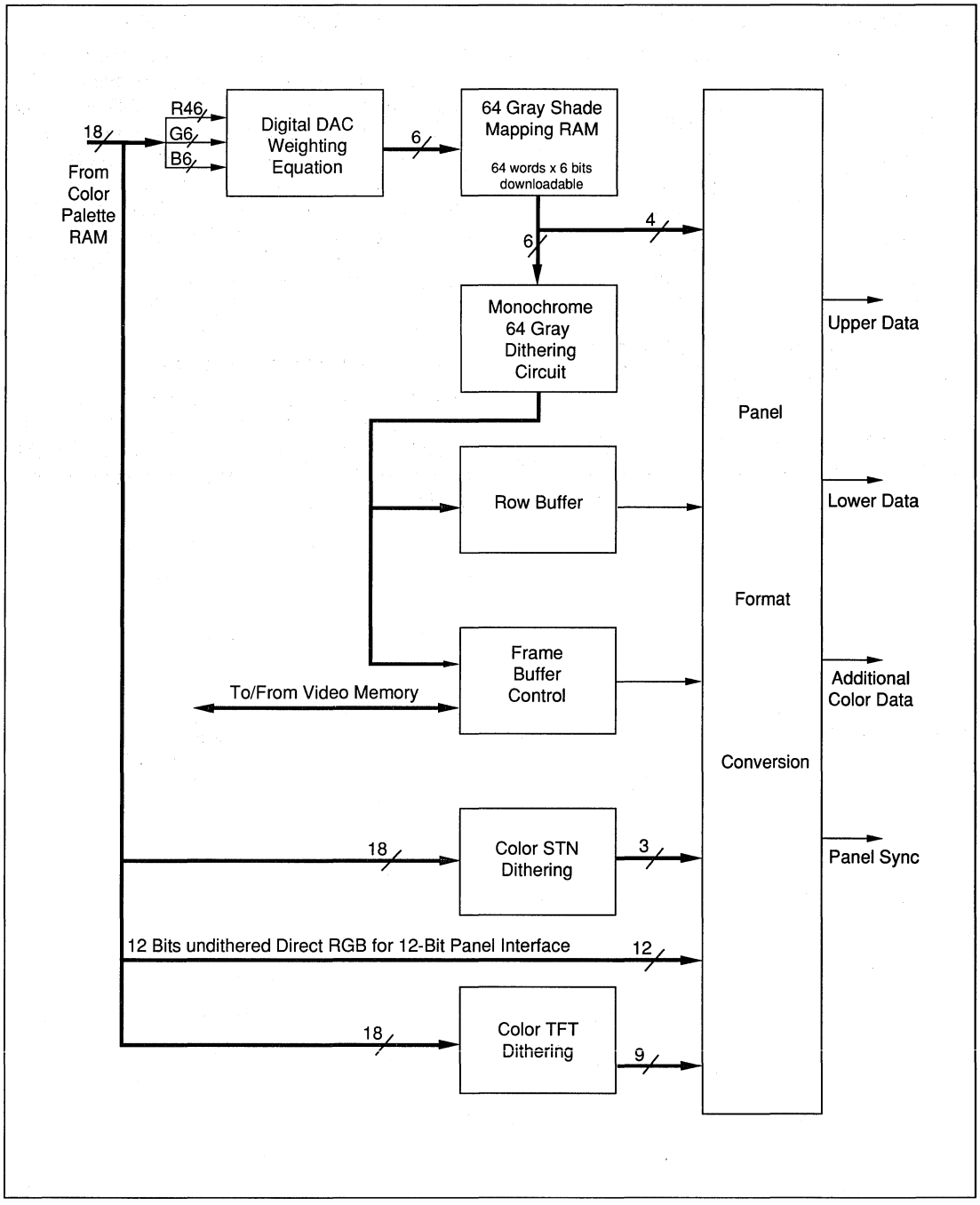

FIGURE 2-2. 90C26 BLOCK DIAGRAM, FLAT PANEL ADAPTER SECTION

3.3 MICROCHANNEL INTERFACE

The WD90C26 directly supports the following Micro Channel interface signals:

A[23:0]	SBHE
ADL	S0
CDSFDBK	S1
M/IO	IRQ
D[15:0]	CDSETUP
CDDS16	CHRESET
CDCHRDY	REFRESH
CMD	MADE24

In addition, the WD90C26 supports both an internal and external decode of I/O address 3C3 bit 0 as a video memory and I/O decode enable.

For full Micro Channel compatibility, only the lower 16 bits of system address bus are decoded for I/O accesses.

3.4 BIOS SUPPORT INTERFACE

The WD90C26 can be configured to provide an enable output for external video BIOS memory. The WD90C26 can support 8- or 16-bit BIOS widths and can be configured to automatically map this external BIOS in to the system memory map at time of reset, and then selectively map it in or out thereafter. Decodes of the 32K of VGA video BIOS address space as defined in the VGA architecture are provided, with an ability to dynamically map out the highest 2K of the 32K space.

3.5 VIDEO MEMORY INTERFACE

The WD90C26 is designed to operate with either 2, 3, or 4 256K by 4 DRAMs or a single 256K by 16 DRAM, with a variety of performance available at each step. The figure on the next page illustrates this implementation.

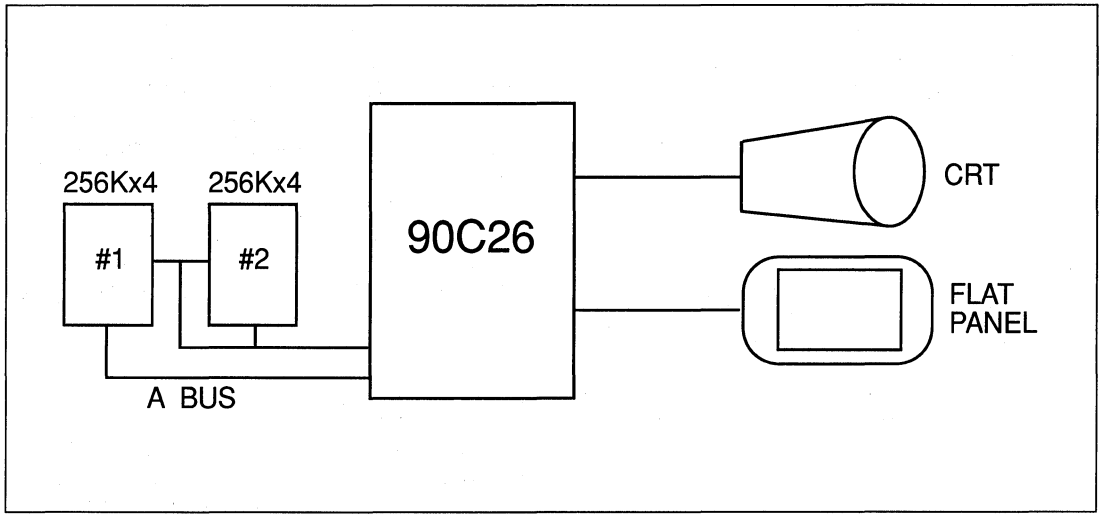

FIGURE 3-1. 2 DRAM IMPLEMENTATION

3.5.1 2 DRAM Implementation

In this implementation, the WD90C26 can support the following:

- simultaneous display on a CRT and any non-dual-panel flat-panel display such as active matrix (TFT), multiplexed (STN) color, plasma, and EL.
- non-simultaneous display with a dual-panel multiplexed (STN) LCD or mono.
- 256 color mode in a 640 by 400 resolution display.

This memory configuration provides for the lowest active power utilization since only two external DRAMs are active. During this time, Bus B memory connections are held static or tri-stated for minimum power dissipation.

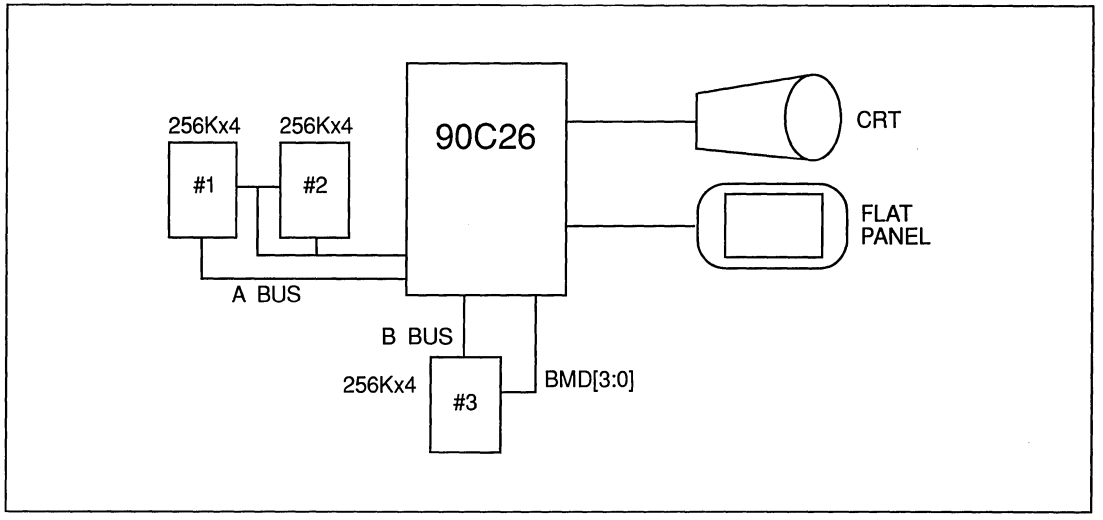

FIGURE 3-2. 3 DRAM IMPLEMENTATION

3.5.2 3 DRAM Implementation

When 3 DRAMs are used, the WD90C26 can additionally support the following:

- simultaneous display of a CRT and a dual-panel multiplexed(STN) LCD display.

The upper nibble of the B bus memory data BMD[7:4] remains tri-stated during the three DRAM mode.

DRAM #3 may be disabled under firmware control when this simultaneous display feature is not needed, allowing power savings when the two displays are not simultaneously connected or when the flat-panel is not a dual-panel type.

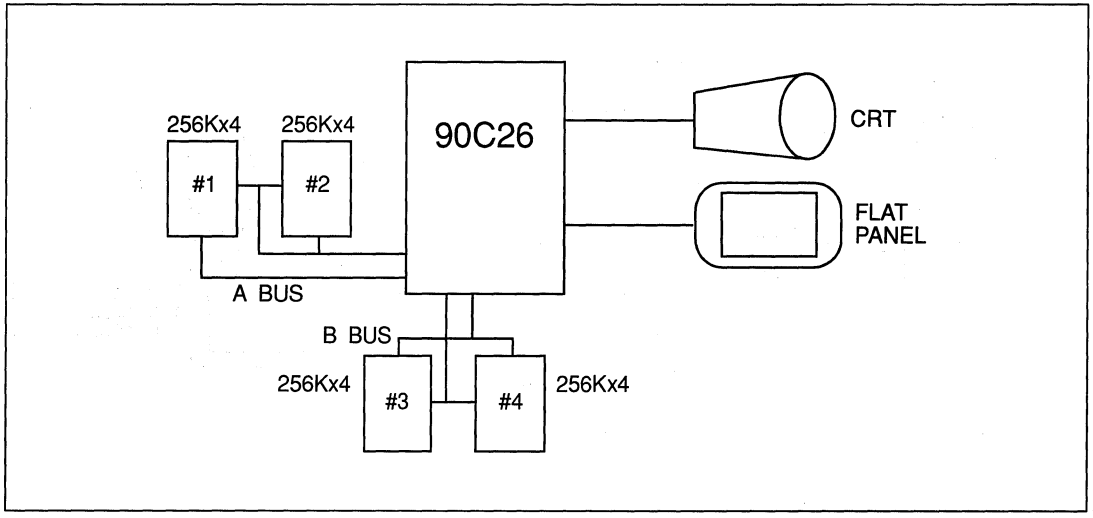

FIGURE 3-3. 4 DRAM IMPLEMENTATION

3.5.3 4 DRAM Implementation

In addition to the features of the 2 DRAM and 3 DRAM modes, the following feature is supported:

- the ability to use 16-bit 512K video RAM except in those occasional times when a dual panel multiplexed display and a CRT are used simultaneously.

Bank B of DRAM may also be disabled by firmware for power reduction, and as before DRAM #3 may be used alone for simultaneous display support of a dual panel display and CRT, while DRAM #4 is disabled.

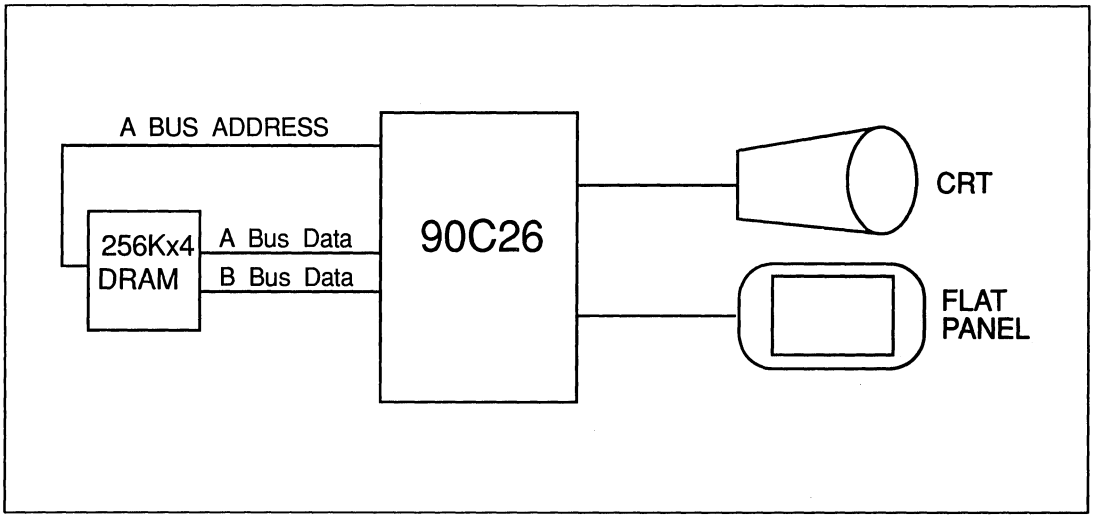

FIGURE 3-4. SINGLE 256K BY 16 IMPLEMENTATION

3.5.4 Single 256K by 16 DRAM Implementation

The WD90C26 may be used with a single 2 CAS 256K by 16 DRAM, providing 512K of video memory and 16-bit memory performance. Simultaneous display operation with all flat-panel types except dual-panel LCD's Is allowed.

3.6 VIDEO INTERFACE

The WD90C26 supports a number of video interfaces allowing it to directly connect to most PC compatible CRTs and to a wide range of industry-standard flat-panel types. This support is achieved through configurable CRT and flat-panel interfaces.

3.6.1 Flat Panel Interface

One of the key features of the WD90C26 is a configurable video output port designed for support of a number of flat-panel technologies. This port is designed to directly support the following flat-panel types without requiring external interface formatting circuitry:

- Monochrome STN multiplexed dual panel LCD displays with one upper panel pixel and one lower panel pixel per clock, one bit per pixel interfaces.
- Monochrome plasma panel displays with one pixel per clock, 4 bits per pixel interfaces.
- Monochrome EL panel displays with one pixel per clock, 4 bits per pixel interfaces.
- Monochrome TFT panel displays with one pixel per clock, 4 bits per pixel interfaces
- Color STN single panel multiplexed LCD displays with one pixel triad per clock, 3 bits per pixel triad (one red, one green, one blue) interfaces.
- Color single panel active matrix TFT LCD displays with one pixel per clock, 3 bits per pixel interfaces.
- Color single panel active matrix TFT LCD displays with one pixel per clock, 4 bits per pixel interfaces.

Programmable flat-panel timing signals allow wide degrees of flexibility in configuring panel interfaces, making the WD90C26 usable with most popular flat-panel designs for PC applications.

For flat panel designs with more unique timing requirements, the WD90C26 is designed to directly interface with the WD90C55 Color Interface Device.

3.6.2 Analog CRT Interface

The WD90C26 includes a complete VGA compatible CRT interface with on-board 256 by 18-bit RAMDAC, which can directly drive analog VGA compatible color or monochrome displays.The interface is also capable of driving older EGA or monochrome compatible displays.

3.6.3 External RAMDAC Interface

For applications where use of an external RAMDAC or equivalent external function is desired, the WD90C26's flat-panel interface can be configured as an industry-standard RAMDAC interface instead of flat-panel pixel data. This allows the WD90C26 to be used in applications where a 24-bit RAMDAC is needed or where special panel pixelization techniques are required.

3.7 CLOCK INTERFACE

The WD90C26 has four clock input signal pins:

- VCLK0
- VCLK1
- VCLK2
- VCLK3

Three of these (VCLK 2, 1, and 0) are normally connected to oscillators. VCLK1 and VCLK2 may be configured to control an external clock multiplexor or clock generator. In this configuration, VCLK0 becomes the clock input while VCLK1 and VCLK2 become outputs used to drive the multiplexor select inputs.

The memory clock input, MCLK, is used by the internal logic to generate all memory timing and may be up to 45 MHz for 70nsec DRAMs.

3.8 POWER MANAGEMENT INTERFACE

The WD90C26's power management interface controls power-down mode operations including DRAM refresh modes and four power reduction modes are available providing a range of function and power savings.

4.0 SIGNAL DESCRIPTIONS

4.1 INTRODUCTION

This section contains a pin diagram, a pin table, and a signal description summary for the following groups of pins:

System Interface Pins

EBROM	SD[15:8]
MEMW/S0	MEMR/M/IO
IOCS16/CDSETUP	MEMCS16/CDDS16
SBHE	BALE/MADE24
IRQ/IRQ	IOR/S1
IOW/CMD	AEN/3C3D0
SD[7:0]	OWS/CDSFBK
IOCHRDY/CDCHRDY	LA[19:17]
SA[16:0]	LA22/R3
LA23/BLW1M	LA20/B3
LA21/G3	IRQ/IRQ

Display Buffer Memory Interface Pins

BMA[8:0]	BRAS
BWE	ACAS
AOE	AMA[8:0]
ARAS	BCAS
AWE	BOE

Internal DAC Analog Interface

ANARED	ANAGRN
ANABLU	PNLOFF/WPLT
FSADJ/MDET	VREF/DACDISA

Clock Generation Interface

VCLK0/VCKIN
VCLK1/VCSLD/VCSEL1
MCLK
VCLK2/VCSEL/VCSELH

Panel Interface

HSYNC	VSYNC
FR/BLANK	XSCLK
ENDATA	LP
FP	PNLENA

Power Down Control Pins

PWRDWN	RESET
REFRESH	

Power Pins

VDD	VSS
PVDD	BVDD
AVDD	AVSS
RVDD	RVSS
BVDD	BVSS

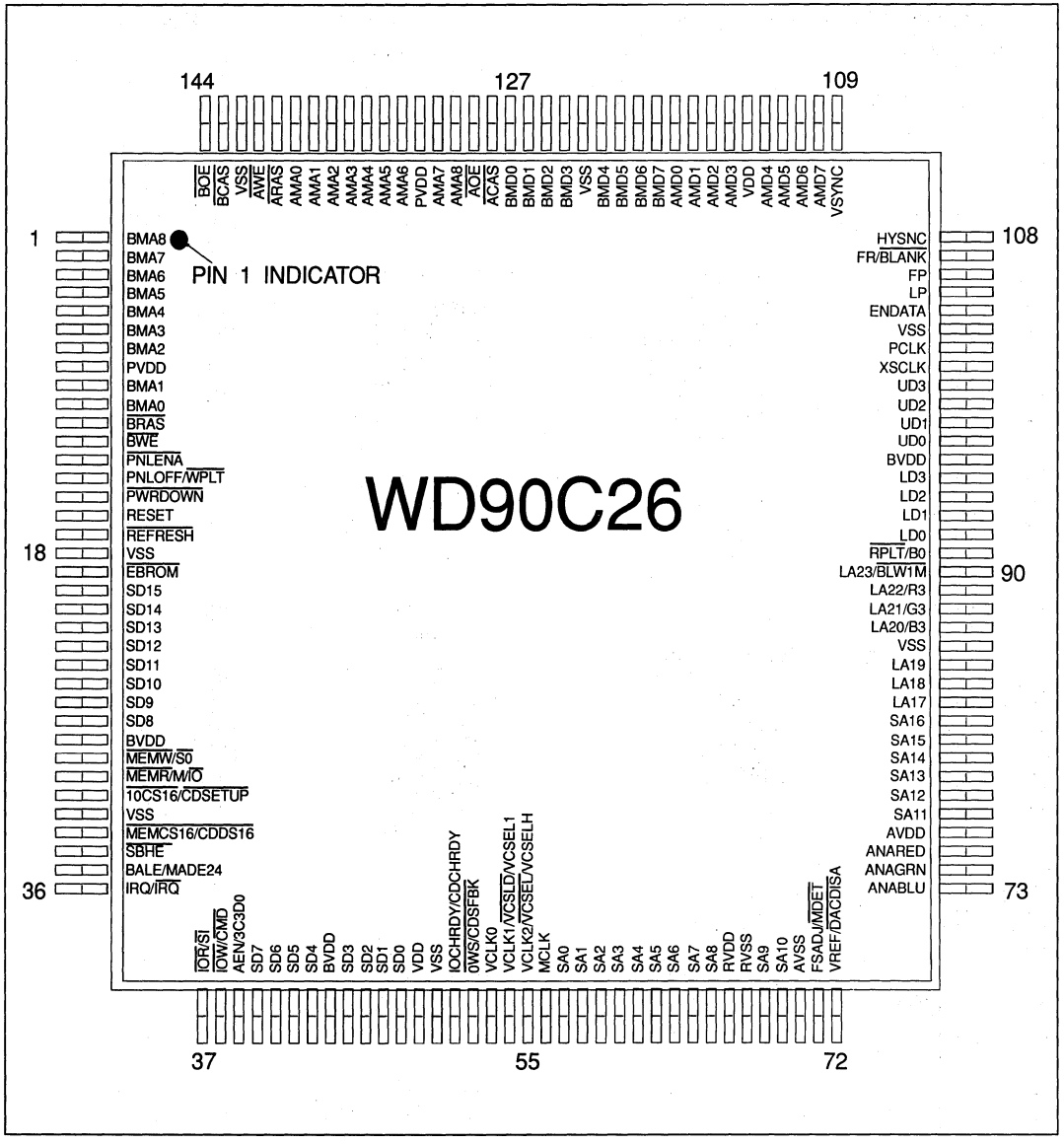

FIGURE 4-1. WD90C26 PIN DIAGRAM, 144-PIN JEDEC PQFP PACKAGE

PIN - NAME	PIN - NAME	PIN - NAME	PIN - NAME
1 - BMA8	38 - IOW/CMD	75 - ANARED	112 - AMD5
2 - BMA7	39 - AEN/3C3D0	76 - AVDD	113 - AMD4
3 - BMA6	40 - SD7	77 - SA11	114 - VDD
4 - BMA5	41 - SD6	78 - SA12	115 - AMD3
5 - BMA4	42 - SD5	79 - SA13	116 - AMD2
6 - BMA3	43 - SD4	80 - SA14	117 - AMD1
7 - BMA2	44 - BVDD	81 - SA15	118 - AMD0
8 - PVDD	45 - SE3	82 - SA16	119 - BMD7
9 - BMA1	46 - SD2	83 - LA17	120 - BMD6
10 - BMA0	47 - SD1	84 - LA18	121 - BMD5
11 - BRAS	48 - SD0	85 - LA19	122 - BMD4
12 - BWE	49 - VDD	86 - VSS	123 - VSS
13 - PNLENA	50 - VSS	87 - LA20/B3	124 - BMD3
14 - PNLOFF/WPLT	51 - IOCHRDY/ CDCHRDY	88 - LA21/G3	125 - BMD2
15 - PWRDOWN	52 - OWS/CDSBFK	89 - LA22/R3	126 - BMD1
16 - RESET	53 - VCLK0	90 - LA23/BLW1M	127 - BMD0
17 - REFRESH	54 - VCLK1/ VCSLD/ VCSEL1	91 - RPLT/B0	128 - ACAS
18 - VSS	55 - VCLK2/ VCEL/ VCSELH	92 - LD0	129 - AOE
19 - EBROM	56 - MCLK	93 - LD1	130 - AMA8
20 - SD15	57 - SA0	94 - LD2	131 - AMA7
21 - SD14	58 - SA1	95 - LD3	132 - PVDD
22 - SD13	59 - SA2	96 - BVDD	133 - AMA6
23 - SD12	60 - SA3	97 - UD0	134 - AMA5
24 - SD11	61 - SA4	98 - UD1	135 - AMA4
25 - SD10	62 - SA5	99 - UD2	136 - AMA3
26 - SD9	63 - SA6	100 - UD3	137 - AMA2
27 - SD8	64 - SA7	101 - XSCLK	138 - AMA1
28 - BVDD	65 - SA8	102 - PCLK	139 - AMA0
29 - MEMW/SO	66 - RVDD	103 - VSS	140 - ARAS
30 - MEMR/M/IO	67 - RVSS	104 - ENDATA	141 - AWE
31 - IOCS16/ CDSETUP	68 - SA9	105 - LP	142 - VSS
32 - VSS	69 - SA10	106 - FP	143 - BCAS
33 - MEMCS16/ CDDS16	70 - AVSS	107 - FR/BLANK	144 - BOE
34 - SBHE	71 - FSADJ/MDET	108 - HSYNC	145 - N/A
35 - BALE/MADE24	72 - VREF/DACDISA	109 - VSYNC	
36 - IRQ/IRQ	73 - ANABLU	110 - AMD7	
37 - IOR/S1	74 - ANAGRN	111 - AMD6	

TABLE 4-1. PIN ASSIGNMENTS

4.2 SYSTEM INTERFACE PINS

The following table describes each System Interface pin on the WD90C26. The WD90C26 system interface can be configured for either ISA bus or Micro Channel interface support by setting DCONF/2 high or low by pulling high or low the AMD2 pin at reset. Other configuration options may also be selected by setting configuration bits high or low at reset through pulling memory data lines high or low.

PIN	MNEMONIC	I/O	DESCRIPTION
16	RESET	I	**WD90C26's Initialization Signal** Typical usage in ISA Bus based system: connected to ISA Bus RESET signal.Typical usage in Micro Channel based system: connected to Micro Channel RESETDRV signal.
17	$\overline{\text{REFRESH}}$	I	**Input Active Low DRAM Refresh** The WD90C26 uses this input to initiate refresh operations to its video buffer memory. It also uses this signal as a negative qualifier for memory read operations.
19	$\overline{\text{EBROM}}$	O	**Enable BIOS ROM** In BIOS ROM Map-in mode, where CONF(0)=0 the WD90C26 drives this output low when it decodes system accesses to video BIOS ROM and a memory read operation is requested from an address range identified within the WD90C26 as a video BIOS ROM address. If CONF(0)=1 this pin remains inactive high.
29	$\overline{\text{MEMW}}$/$\overline{\text{S0}}$	I	**Memory Write** $\overline{\text{MEMW}}$ if CONF(2)=1 (ISA Bus Mode). Memory write input from ISA bus. **Decode MicroChannel Bus Cycles** $\overline{\text{S0}}$ if CONF(2)=0 (Micro Channel Mode). When the WD90C26 is in ISA Bus mode. This pin is the industry standard $\overline{\text{MEMW}}$ bus signal, and indicates to the WD90C26 that a memory write bus cycle is occurring. When the WD90C26 is in Micro Channel mode, this pin is the Micro Channel $\overline{\text{S0}}$ channel status input, which the WD90C26 uses, along with S1, M/$\overline{\text{IO}}$, and $\overline{\text{CMD}}$, to decode Micro Channel bus cycles.

TABLE 4-2. SYSTEM INTERFACE PINS

PIN	MNEMONIC	I/O	DESCRIPTION
30	MEMR/M/IO	I	**Memory Read** MEMR if CONF(2)=1 (ISA Bus Mode). When the WD90C26 is in ISA Bus mode, this pin is the industry-standard MEMR bus signal. This indicates to the WD90C26 that a memory read bus cycle is occurring. Because MEMR may also be active during refresh cycles, the WD90C26 internally gates MEMR with REFRESH. **Memory/IO Cycle** M/IO if CONF(2)=0 (Micro Channel Mode) When the WD90C26 is in Micro Channel mode, this pin is the M/IO signal from the Micro Channel bus. A high input at this pin is interpreted by the WD90C26 as a Micro Channel Bus Memory cycle. A signal at this pin indicates a Micro Channel Bus I/O cycle to the WD90C26.
31	IOCS16/CDSETUP	I/O O.C.	**I/O Chip Select 16** IOCS16 if CONF(2)=1 (ISA Bus Mode). Open collector Indicates the WD90C26 supports 16-bit I/O operations at the "current"I/O address. In ISA Bus mode, pin 31 becoming active low is an indication to the ISA Bus that it supports 20-bit I/O transfers at the 16-bit I/O address being presented to it. Otherwise this pin is in a high-impedance state. IOCS16 is not gated by any other signals. Its function is independent of other bus control lines, bus modes, or register settings. IOCS16 is not affected by AEN. **Card Setup** CDSETUP if CONF(2)=0 (Micro Channel Mode). In Micro Channel mode, this pin is the card setup input indicating to the WD90C26 to perform setup functions.

TABLE 4-2. SYSTEM INTERFACE PINS (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
33	MEMCS16/ CDDS16	O O.C.	**Memory Chip Select 16** MEMCS16 if CONF(2)=1 (ISA Bus Mode). In ISA bus mode, pin 33 is an indication to the system that the WD90C26 supports 16-bit memory transfers at the system address being presented. In ISA Bus applications, pin 33 is typically connected to the ISA Bus MEMCS16 signal. **Card Data Size 16** CDDS16 if CONF(2)=0 (Micro Channel Mode) In Micro Channel applications pin 33 indicates a 16-bit resource available at the address.
34	SBHE	I	**System Byte Hi Enable** SBHE indicates to the WD90C26 the mapping of bytes into high or low registers on write operations and the ordering of high and low bytes during read operations.
35	BALE/MADE24	I	**Address Latch Enable** BALE if CONF(2)=1 (ISA Bus Mode) Typical usage in ISA Bus based system: connected to ISA Bus BALE signal. When the WD90C26 is in ISA Bus mode this pin is the industry standard BALE signal input to the WD90C26. A high level is interpreted by the WD90C26 as an indication that the system address is setting up on its SA bus inputs to be latched on the falling edge of this signal. To ensure compatibility across a variety of platforms, the WD90C26 latches LA17-LA23 with the fall of BALE. **Memory Address Enable 24** MADE24 if CONF(2)=0 (Micro Channel Mode). When the WD90C26 is in Micro Channel mode, this pin is the Micro Channel MADE24 input to the WD90C26 and is used by the WD90C26 as an indication that the system address is in the below-16 MByte range.

TABLE 4-2. SYSTEM INTERFACE PINS (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
36	IRQ/$\overline{IRQ}$	O	**Interrupt Request** Active high if CONF(2)=1 (ISA Bus Mode), Active Low if in Micro Channel mode. Open Collector in Micro Channel mode. Description of function of IRQ in both ISA and Micro Channel Modes is as follows: When bit 5 of the VGA Vertical Retrace End Register (I/O Address 3?5h index 11) is set to 0, this signal is set active at the occurrence of the end of vertical display of a frame of active video. IRQ stays active until cleared by momentarily setting bit 4 of the Vertical Retrace End Register to 0 and then back to 1. When bit 5 of the VGA Vertical Retrace End Register is set to 0 the activation of this pin is disabled, forcing its output to be low in ISA bus mode or high impedance in Micro Channel mode. NOTE: This pin can only be configured or the interrupt cleared if the Vertical Retrace End Register is unlocked by setting PR3 bit 0 high.
37	$\overline{IOR}$/$\overline{S1}$	I	**$\overline{I/O}$ Read** $\overline{IOR}$ if CONF(2)=1 (ISA Bus Mode). When the WD90C26 is in ISA Bus Mode, this pin indicates to the WD90C26 that an I/O read bus cycle is to occur. $\overline{IOR}$ may also be active during DMA cycles and is therefore internally qualified by AEN. **$\overline{S1}$ Cycle Decode** $\overline{S1}$ if CONF(2)=0(Micro Channel Mode). When the WD90C26 is in Micro Channel mode (AMD2 low at reset), this pin is the Micro Channel $\overline{S1}$ channel status input, which the WD90C26 uses, along with $\overline{S0}$, M/$\overline{IO}$, and $\overline{CMD}$, to decode Micro Channel bus cycles.
38	$\overline{IOW}$/$\overline{CMD}$	I	**$\overline{I/O}$ Write** $\overline{IOW}$ if CONF(2)=1 (ISA Bus Mode). When the WD90C26 is in ISA Bus mode, this pin indicates to the WD90C26 that an I/O read bus cycle is to occur. The WD90C26 internally qualifies $\overline{IOW}$ write requests with AEN. **$\overline{Command}$** $\overline{CMD}$ if CONF(2)=0 (Micro Channel Mode) When the WD90C26 is in Micro Channel mode, this pin is interpreted by the WD90C26 as the $\overline{CMD}$ signal from a Micro Channel bus. The WD90C26 uses this signal to properly decode cycle types.

TABLE 4-2. SYSTEM INTERFACE PINS (Continued)

16

PIN	MNEMONIC	I/O	DESCRIPTION
39	AEN/3C3D0	I	**Address Enable** AEN if CONF(2)=1 (ISA Bus Mode). When active high, this signal disables the WD90C26 from performing ISA bus read or write accesses. When low, system accesses to the WD90C26 are enabled. **Video Subsystem Enable Port, Data Bit 0 Input** 3C3D0 if CONF(2)=0 (Micro Channel Mode). This signal typically comes from bit 0 of I/O port 3C3h. A high input at this pin enables the WD90C26's ability to respond to Micro Channel bus accesses. In Micro Channel mode, I/O writes to the WD90C26 of a '1' to I/O port 3C3 bit 0 also enables the WD90C26.
51	IOCHRDY/ CDCHRDY	O O.C.	**I/O Channel Ready Status** IOCHRDY if CONF(2)=1 (ISA Bus Mode). I/O Channel Ready status when active high. When the WD90C26 is in ISA Bus Mode (see section on configuration bits for description of use of AMD2 as a mode configuration pin), pin 51 is the industry-standard IOCHRDY bus signal, and indicates readiness of the WD90C26 in responding to ISA bus read and write cycles. When the WD90C26 cannot complete the desired bus cycle within the standard or 0 wait cycle times, it will de-assert IOCHRDY until it is ready to complete the transfer. **Channel Ready** CDCHRDY if CONF(2)=1 (Micro Channel Mode). When the WD90C26 is in Micro Channel Mode, CONF(2)=0), pin 51 is the CDCHRDY signal to a Micro Channel bus. The WD90C26 drives this pin low when additional cycle time is required. In Micro Channel mode, CDCHRDY is brought to its high-impedance inactive state by the rising edge of the signal to pin 48, $\overline{CMD}$. Under typical conditions of video memory speeds and bus rates, the WD90C26 does not cause IOCHRDY or CDCHRDY to go inactive low or cause CDCHRDY to occur later than the minimum requirement, except in certain instances when a write operation results in an internal write data buffer overflow.

TABLE 4-2. SYSTEM INTERFACE PINS (Continued)

PIN	MNEMONIC	I/O	DESCRIPTION
52	$\overline{0WS}$ $\overline{CDSFBK}$	O O.C.	**$\overline{Zero}$ Wait State** $\overline{0WS}$ if ISA Bus Mode CONF(2)=1 (ISA Bus Mode). This pin is the WD90C26's indication of readiness to support zero wait state option. The description of PR32 includes information on how to configure the WD90C26's support of $\overline{0WS}$. The WD90C26 drives this signal low when 0 wait cycles can be supported. Otherwise this signal is tri-stated. **$\overline{Card\ Selected}$ Feedback** $\overline{CDSFBK}$ if CONF(2)=1 (Micro Channel Mode). Feedback to the Micro Channel interface of CD status. Driven active low by the WD90C26 as an acknowledgment of its selection. Does not go active if $\overline{CDSETUP}$ is active low. It is tri-stated when not being driven active low.

TABLE 4-2. SYSTEM INTERFACE PINS (Continued)

4.2.1 System Interface Data Signals

PIN	MNEMONIC	I/O	DESCRIPTION
SD15 is the MSB and SD0 is the LSB of the 16-bit system data bus in ISA bus and Micro Channel bus architectures. The WD90C26's system data signals may be directly connected to the host system data bus, provided the WD90C26 drivers are adequate when host system data bus loading considerations are made. The full data sheet provides specifics about bus drive capabilities.			
20	SD15	I/O	System Data 15
21	SD14	I/O	System Data 14
22	SD13	I/O	System Data 13
23	SD12	I/O	System Data 12
24	SD11	I/O	System Data 11
25	SD10	I/O	System Data 10
26	SD9	I/O	System Data 9
27	SD8	I/O	System Data 8
40	SD7	I/O	System Data 7
41	SD6	I/O	System Data 6
42	SD5	I/O	System Data 5
43	SD4	I/O	System Data 4
45	SD3	I/O	System Data 3
46	SD2	I/O	System Data 2
47	SD1	I/O	System Data 1
48	SD1	I/O	System Data 0

TABLE 4-3. SYSTEM INTERFACE DATA SIGNALS

4.2.2 System Interface Address Signals

PIN	MNEMONIC	I/O	DESCRIPTION
SA9-SA0 are used by the WD90C26 as the I/O address during ISA bus or Micro Channel I/O cycles. SA16-SA0 are used as the lower 17 bits of the WD90C26's 24-bit memory address during ISA bus or Micro Channel memory cycles. SA16 is the MSB and SA0 is the LSB of the 17-bit system address bus.			
57	SA0	I	System Address 0
58	SA1	I	System Address 1
59	SA2	I	System Address 2
60	SA3	I	System Address 3
61	SA4	I	System Address 4
62	SA5	I	System Address 5
63	SA6	I	System Address 6
64	SA7	I	System Address 7
65	SA8	I	System Address 8
68	SA9	I	System Address 9
69	SA10	I	System Address 10
77	SA11	I	System Address 11
78	SA12	I	System Address 12
79	SA13	I	System Address 13
80	SA14	I	System Address 14
81	SA15	I	System Address 15
82	SA16	I	System Address 16
LA19-LA17 are additional latchable system address signals. LA19 is the MSB of the 20 bit below-1-megabyte memory address bus in ISA bus and Micro Channel bus architectures, formed by using LA19-LA17 and SA16-SA0. The WD90C26 uses the resulting memory address, along with either the BLW1M signal or decodes of LA23-LA20, for accesses to its video memory buffer DRAM. In certain other modes, the WD90C26 uses the address formed by LA19-SA0, along with a 1MB block decode from LA23-LA20, to access the WD90C26's DRAM video buffer as above-1-megabyte memory. In ISA bus mode CONF(2)=1), LA19-LA17 are inputs to a transparent latch internal to the WD90C26 that allows LA19-LA17 to propagate in, while BALE is active high. LA19-LA17 are then captured when BALE goes inactive low. In Micro Channel Mode CONF(2)=0), LA19-LA17 are also address inputs.			

TABLE 4-4. SYSTEM INTERFACE ADDRESS SIGNALS

PIN	MNEMONIC	I/O	DESCRIPTION
83	LA17	I	Latchable System Address 17
84	LA18	I	Latchable System Address 18
85	LA19	I	Latchable System Address 19
87	LA20/B3	I/O	**Latchable System Address Bit 20** LA20 if pull-up on MD 7 (Full Decode Mode). Blue MSB for 12-bit panel interface. B3 if pull-down on MD7 and in 12-bit panel mode.
88	LA21/G3	I/O	**Latchable System Address Bit 21** LA21 if pull-up on MD 7 (Full Decode Mode). Green MSB for 12-bit panel interface. G3 if pull-down on MD7 and in 12-bit panel mode.
89	LA22/R3	I/O	**Latchable System Address Bit 22** LA22 if CONF(7)=1 (Full Decode Mode). Red MSB for 12-bit panel interface. R3 if pull-down on MD7 and in 12-bit panel mode.
90	LA23/$\overline{\text{BLW1M}}$	I	**Latchable System Address Bit 23** LA23 if MSB of the 24-bit system address formed by LA(23:17) and SA(16:0). **Below 1 megabyte Address Decode** $\overline{\text{BLWIM}}$ if CONF(7)=1 (12-bit I/F mode). Active low input from external decode indicating that the system address is in the below-1-megabyte address range of 000000h to FFFFFFh.

TABLE 4-4. SYSTEM INTERFACE ADDRESS SIGNALS (Continued)

4.3 DISPLAY BUFFER MEMORY INTERFACE PINS

The display memory interface is designed for connection of up to four 256K by 4 or one 256K by 16 fast-page-mode DRAMs. This section is divided into the following subsections, which provide tables describing the data signals below:

- Bank A Video Memory Data Bus Signals
- Bank B Video Memory Data Bus Signals

4.3.1 Bank A Video Memory Signals

PIN	MNEMONIC	I/O	DESCRIPTION
		BANK A VIDEO MEMORY DATA BITS	
110	AMD7	I/O	Bank A Memory Data Bit 7
111	AMD6	I/O	Bank A Memory Data Bit 6
112	AMD5	I/O	Bank A Memory Data Bit 5
113	AMD4	I/O	Bank A Memory Data Bit 4
115	AMD3	I/O	Bank A Memory Data Bit 3
116	AMD2	I/O	Bank A Memory Data Bit 2
117	AMD1	I/O	Bank A Memory Data Bit 1
118	AMD0	I/O	Bank A Memory Data Bit 0
		BANK A VIDEO MEMORY ADDRESS BITS	
130	AMA8	O	Bank A Memory Address Bit 8
131	AMA7	O	Bank A Memory Address Bit 7
133	AMA6	O	Bank A Memory Address Bit 6
134	AMA5	O	Bank A Memory Address Bit 5
135	AMA4	O	Bank A Memory Address Bit 4
136	AMA3	O	Bank A Memory Address Bit 3
137	AMA2	O	Bank A Memory Address Bit 2
138	AMA1	O	Bank A Memory Address Bit 1
138	AMA0	O	Bank A Memory Address Bit 0
Primary 9-bit video buffer DRAM address bus. AMA8 is the MSB and AMA0 the LSB.			
128	$\overline{\text{ACAS}}$	O	**CAS Bank A** Column address strobe for video memory buffer DRAM bank A, consisting of 256K by 4 DRAMs #1 and #2. When 256K by 16 DRAM is used, this is the lower CAS strobe output and the BCAS signal is the upper CAS strobe input.
129	$\overline{\text{AOE}}$	O	**Output Enable Bank A** Output Enable control for video memory buffer DRAM bank A. When 256K by 16 DRAM is used, this is the DRAM output enable strobe.

TABLE 4-5. BANK A VIDEO MEMORY SIGNALS

PIN	MNEMONIC	I/O	DESCRIPTION
140	$\overline{\text{ARAS}}$	O	**RAS Bank A** Row address strobe for video memory buffer DRAM banks A, consisting of 256K by 4 DRAMs #1 and #2. When a 256K by 16 DRAM is used, this is the DRAM $\overline{\text{RAS}}$ strobe output.
141	$\overline{\text{AWE}}$	O	**Write Enable Bank A** Write Enable control for video memory buffer DRAM bank A. When a 256K by 16 DRAM is used this is the DRAM write enable output.

TABLE 4-5. BANK A VIDEO MEMORY SIGNALS (Continued)

4.3.2 Bank B Video Memory Signals

PIN	MNEMONIC	I/O	DESCRIPTION
BANK B VIDEO MEMORY DATA BITS			
119	BMD	I/O	Bank B Memory Data Bit 7
120	BMD	I/O	Bank B Memory Data Bit 6
121	BMD	I/O	Bank B Memory Data Bit 5
122	BMD	I/O	Bank B Memory Data Bit 4
124	BMD	I/O	Bank B Memory Data Bit 3
125	BMD	I/O	Bank B Memory Data Bit 2
126	BMD	I/O	Bank B Memory Data Bit 1
127	BMD	I/O	Bank B Memory Data Bit 0
BANK B VIDEO MEMORY ADDRESS BITS			
1	BMA	O	Bank B Memory Address Bit 8
2	BMA	O	Bank B Memory Address Bit 7
3	BMA	O	Bank B Memory Address Bit 6
4	BMA	O	Bank B Memory Address Bit 5
5	BMA	O	Bank B Memory Address Bit 4
6	BMA	O	Bank B Memory Address Bit 3
7	BMA	O	Bank B Memory Address Bit 2
9	BMA	O	Bank B Memory Address Bit 1
10	BMA	O	Bank B Memory Address Bit 0
11	$\overline{\text{BRAS}}$	O	**RAS Bank B** Row address strobe for video memory buffer DRAM bank B, consisting of 256K by 4 DRAM #3 or 256K by 4 DRAMs #3 and #4.
12	$\overline{\text{BWE}}$	O	**Write Enable Bank B** Write Enable control for video memory buffer DRAM bank B.
143	$\overline{\text{BCAS}}$	O	**CAS Bank B** Column address strobe for video memory buffer DRAM bank B, consisting of 256K by 4 DRAM #3 or 256K by 4 DRAMs #3 and #4. When a 256K by 16 DRAM is used, this is the upper $\overline{\text{CAS}}$ strobe output.
144	$\overline{\text{BOE}}$	O	**Output Enable Bank B** Output Enable control for video memory buffer DRAM bank B.

TABLE 4-6. BANK B VIDEO MEMORY SIGNALS

4.4 CRT INTERFACE SIGNALS

Internal DAC analog interface pins are described in the following table.

PIN	MNEMONIC	I/O	DESCRIPTION
75	ANARED	O Analog	CRT Red Drive
74	ANAGRN	O Analog	CRT Green Drive
73	ANABLU	O Analog	CRT Blue Drive
72	VREF/ DACDISA	I	**Attach External Precision Reference Input** VREF if above Vss DAC reference voltage. The input for attachment of an external precision reference used by the WD90C26's internal DAC for regulation purposes. **Disable Internal DAC** DACDISA if tied to Vss. If the internal DAC is not needed to drive a CRT, this input may be grounded to disable the internal DAC.
71	FSADJ/ MDET	I A/D	**DAC Full-Scale Adjustment** FSADJUST if pin 72 is above Vss. **Monitor Detect Input** MDET if pin 72 is tied to Vss. If pin 72 is above Vss, this pin serves as the input for a DAC full-scale current adjust external resistor or potentiometer. If pin 72 is tied to Vss, this pin is a digital input to which may be connected an external monitor detect circuit as part of an external RAMDAC support. A low level at this pin causes bit 4 of the VGA input status register 0, at 3C2h as detection of monitor connection to the VGA subsystem.

TABLE 4-7. DAC ANALOG INTERFACE PINS

PIN	MNEMONIC	I/O	DESCRIPTION
91	$\overline{\text{RPLT}}$/B0	O	**Read Palette** If not configured for a color TFT interface, this pin is the active low read pulse to the external RAMDAC or equivalent circuit. **Blue Data Bit 0** If the WD90C26 has been configured for a 9- or 12-bit color TFT interface, this pin is the low-order blue video data output to a panel. This output is static low if the external panel is not enabled or if the panel is not a color interface. The setting of bit 2 determines whether the WD90C26 is configured for a TFT interface.
108	HSYNC	O	**CRT Horizontal Sync** HSYNC is the CRT horizontal sync control signal output. It may be directly attached to CRT monitor connections. Its active low or high level is programmable as is its position and duration. This pin is inactive when the WD90C26 is in power-down modes or CRT display is not enabled. Control of horizontal sync polarity is done by setting register bits in the VGA Miscellaneous Output Register and in PR3 and PR39.
109	VSYNC	O	**CRT Vertical Sync** VSYNC is the CRT vertical sync control signal output. It may be directly attached to CRT monitor connections. Its active low or high level is programmable. This pin is inactive when the WD90C26 is in power-down modes or CRT display is not enabled. Control of vertical sync polarity is done by setting register bits in the VGA Miscellaneous Output Register and in PR3 and PR39.

TABLE 4-7. DAC ANALOG INTERFACE PINS (Continued)

4.5 CLOCK GENERATION INTERFACE PINS

Clock generation interface pins are described in the following table.

PIN	MNEMONIC	I/O	DESCRIPTION
53	VCLK0/VCLKN	I	**Video Clock 0** VCLK0 if CONF(3)=1. The primary of four possible video clock inputs to the WD90C26. VCLK0 is the main video clock to the WD90C26. **Video Clock Input** VCLKN if CONF(3)=0 If AMD[3] is high while RESET is active, this pin is VCLKN, the video clock input from an external frequency source or multiplexer, whose frequency is controlled by Miscellaneous Write Register bit 2, and depending on PR15 bit 5, bit 3, of the Miscellaneous Write Register. Selection of the video shift clock is internally overridden if MCLK has been selected by the setting of PR15 bit 4.
54	VCLK1/ VCSLD/ VCSELL	I/ O/ O	**Video Clock 1** VCLK1 if f pulldown on AMD[3]. If AMD[3] is low while RESET is active, pin 54 is the VCLK1 signal, VCLK1 is the second of four possible video clock inputs to the WD90C26, which are internally selected to provide video shift clock rates for various screen formats and display types. **Video Clock Select Load** VCSLD if CONF(3)=0. This signal is typically used as a video clock select load control line to an external multiple video frequency source. **Video Clock Select Low** VCSELL if CONF(3)=0 and PR15(5)=1 The lower order signal of VCSELL. VCSELL are outputs used as select lines to an external video clock source multiplexer.

TABLE 4-8. CLOCK GENERATION INTERFACE PIN TABLE

PIN	MNEMONIC	I/O	DESCRIPTION
55	VCLK2/ VCSEL/ VCSELH	I/ O/ O	**Video Clock 2** VCLK2 if CONF(3)=1. The third of four possible video clock inputs to the WD90C26, which are internally selected to provide video shift clock rates for various screen formats and display types. **Video Clock Select** VCSEL if CONF(3)=0 and PR15(5)=0. VCSEL is typically used as a video clock select control link to an external multiple video frequency source. Its output follows the setting of WD90C26 register PR2 bit 1. **Video Clock Select High** VCSELH if CONF(3)=0 and PR15(5)-1. The higher order signal of VCSELH, VCSELL, which are outputs used as select lines to an external video clock source multiplexer.
56	MCLK	I	**Memory Timing Clock Input** This signal is the memory timing clock input to the WD90C26. Its speed dictates video memory access timing and speeds as well as system I/O timing. MCLK may also serve as one of four possible sources of video shift clock.

TABLE 4-8. CLOCK GENERATION INTERFACE PIN TABLE (Continued)

4.6 PANEL INTERFACE PINS

PIN	MNEMONIC	I/O	DESCRIPTION
13	$\overline{\text{PNLENA}}$	O	**LCD Enable** $\overline{\text{PNLENA}}$ is intended to be used to control the attached panel's power supply.
14	PNLOFF/$\overline{\text{WPLT}}$	O	**Panel Power Off** PNLOFF if PR57 bit 2 is '0'. The Power-Off active high signal to an LCD panel's bias supply circuit. The PNLOFF signal is used as a power enable/disable to a control panel, and is tied to the WD90C26's power management circuitry. The WD90C26 sequences this signal as part of the panel power/power-down procedures designed to protect panel circuitry. A high at this output indicates power-off to the panel and a low power-on. **Write Palette** $\overline{\text{WPLT}}$ if PR57 bit 2 is '1'. If the WD90C26 has been configured for external DAC mode, $\overline{\text{WPLT}}$ is the write pulse to the external RAMDAC or equivalent circuit.
102	PCLK	O	**Pixel Clock** This pin serves as a pixel clock output which may be used to latch pixel data from the WD90C26's video output bus into an external RAMDAC. Pixel data from the WD90C26 changes on the rising edge of PCLK and is intended to be latched into an external RAMDAC by the falling edge of PCLK.
107	FR/$\overline{\text{BLANK}}$	O	**Frame Rate Signal** FR if operation in any LCD modes. FR is a free-running clock which is intended to be connected to FR frame rate inputs on some LCD panels. Frequency of its signal is programmable. **Blanking Control Signal** $\overline{\text{BLANK}}$ is the standard analog VGA RAMDAC blanking signal. Output when the WD90C26 is not operating in any ICD modes.

TABLE 4-9. PANEL INTERFACE PINS

PIN	MNEMONIC	I/O	DESCRIPTION
100 99 98 97	UD3 UD2 UD1 UD0	O	**Upper Panel Data Bit 3 to Bit 0** In an LCD interface, these signals are used for the upper panel data bus. In a plasma interface, they provide the pure 4-bit video data interface. In a CRT interface, they are the upper four bits pixel video outputs to the RAMDAC.
95 94 93 92	LD3 LD2 LD1 LD0	O	**Lower Panel Data Bit 3 to Bit 0** In an LCD interface, these signals are used for the lower panel data bus. In a plasma interface, they are reserved. In a CRT interface, they are the lower four bits pixel video outputs to the RAMDAC.
101	XSCLK	O	**X Driver Shift Clock** In a dual panel interface, this signal is used to shift the upper and lower panel's data into the X-driver.
104	ENDATA	O	**Weight Control Clock** In an LCD interface, this signal is required to generate a gray scale in panels using pulse width modulation. In a Plasma interface, it is an "enable video" signal.
106	FP	O	**Frame Pulse** FP is used as an indication to attached panels that a new frame has begun.
105	LP	O	**Latch Pulse** The LP output is intended to be used to latch all the current panel data into the current scan line of the panel.

TABLE 4-9. PANEL INTERFACE PINS (Continued)

4.7 POWER-DOWN CONTROL PINS

PIN	MNEMONIC	I/O	DESCRIPTION
15	PWRDWN	I	**Input Active Low Power Down Control** When active low, this pin causes flat-panel and CRT display update circuitry to halt. PNLENA goes inactive, PNLOFF goes active, and BLANK goes active. The internal RAMDAC's outputs are shut off. Flat-panel and CRT timing signals are halted. Video buffer memory and WD90C26 registers are still accessible when PWRDWN is active.

TABLE 4-10. POWER-DOWN CONTROL PINS

4.8 POWER PINS

PIN	MNEMONIC	I/O	DESCRIPTION
8, 132	PVDD	Power	Power-down section V_{DD} supply.
18, 32, 50, 86, 103, 123, 142	VSS	Ground	Ground V_{SS} = 0V.
28, 44, 90	BVDD	Power	Bus interface V_{DD} supply for system bus, panel, CRT, and clock interfaces.
49, 114	VDD	Power	WD90C26 main V_{DD} supply to core and memory data buses.
66	RVDD	Power	RAM filtered palette V_{DD} supply.
67	RVSS	Ground	RAM palette V_{SS} connection.
70	AVSS	Ground	Internal DAC V_{SS} connection.
77	AVDD	Power	Filtered internal DAC V_{DD} power connection.

TABLE 4-11. POWER PINS