1.0 INTRODUCTION

This data sheet applies to both the WD90C20, and WD90C20A. The WD90C20A is a 0.9 micron version of the WD90C20 VGA controller chip.

For convenience all references to these two devices will be referred to as the WD90C20. When a particular feature is available only on one of these devices, it is called out in the text.

See Appendix F for a detailed explanation of the differences between the WD90C20 and the WD90C20A.

1.1 DESCRIPTION

The WD90C20 is a VGA display controller that has been optimized for applications that require flat panel display support. It is an extension of the WD90C00 and as such supports all of the WD90C00's features and modes when driving a standard CRT. The WD90C20's highly integrated design includes a complete Micro Channel or AT compatible bus interface, as well as an on-chip PS/2 compatible RAMDAC with integral monitor detection logic.

The WD90C20 is a VGA controller for up to 640 by 480 plasma and LCD display applications. It provides complete flat panel display subsystems for Micro Channel and AT compatible interfaces and has expanded Micro Channel compatibility.

The WD90C20 is 1.25 micron device and the WD90C20A is a 0.9 micron CMOS device.

1.2 FEATURES

- On-chip Micro Channel interface
- On-chip 8- or 16-bit AT bus interface
- Direct interface with CRT and flat panel displays (monochrome and color TFT LCD)
- On-chip frame rate modulation logic
- Supports all functions of WD90C00 VGA chip in CRT mode
- 32-shade gray scale mapping
- Software-selectable vertical screen centering
- Hardware vertical expansion(WD90C20A)*
- On-chip PS/2 compatible RAMDAC*
- On-chip monitor detection logic
- 32 MHz maximum LCD video clock (WD90C20)
  36 MHz maximum LCD video clock (WD90C20A)
- 45 MHz maximum CRT video clock
- Flexible power management features *
- Vcc may be removed in powered system
- 256 out of 512 color support for DSTN color LCD(WD90C20)
  256 out of 4K color support for DSTN color LCD (WD90C20A)
  8 or 512 color support for TFT color LCD
- Four powerdown modes

* Patent pending

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2.0 THEORY OF OPERATION

The WD90C20 contains six major functional modules. In addition to the CRT controller, there is a sequencer, a graphics controller, an attribute controller, a flat panel interface, and a RAMDAC. The WD90C20 handles all display buffer management functions, including display refresh cycles, memory refresh cycles, and the arbitration and sequencing of host access cycles.

- **Sequencer**

The sequencer provides the display memory control signals and timing. It also provides the synchronization between the CRT controller and the attribute controller. The sequencer controls the arbitration between the CPU cycle and the CRT cycle, or the CPU cycle and the memory refresh cycle.

- **Graphics Controller**

The graphics controller manages data flow between video memory and the attribute controller during active display (non-blanked) periods. It also controls system microprocessor reads from and writes to the video memory, using the time slots defined by the sequencer.

- **Attribute Controller**

The attribute controller modifies the CRT display data stream in graphics and character modes. It controls display attributes such as blinking, underlining, cursor, scrolling, reverse video (as well as background or foreground video) in VGA and enhanced VGA BIOS modes.

- **Flat Panel Adapter**

The flat panel adapter section includes color-to-gray scale mapping*, a dithering mapping RAM, a dithering engine, a row buffer*, shading control*, and panel interface logic.
* Patent pending.

- **RAMDAC**

The WD90C20's on-board RAMDAC is a low power, PS/2-compatible device with special power-down modes and PS/2 monitor detection logic.
The RAMDAC's 256 by 18 color look-up table has triple 6-bit D/A converters, a pixel mask register, and composite blank generation on the three channels. It also supports the use of an external voltage reference. Without external buffering the RAMDAC will generate RS-343A-compatible video signals into a doubly terminated 75 ohm load or a 50 ohm load. Integral and differential linearity errors are a maximum of ± 1/2 LSB.

2.1 WD90C20 INTERFACES

The WD90C20 has five main system interfaces: the CPU, a display memory, a RAMDAC/CRT, a clock, and a flat panel display. In most implementations, these interfaces eliminate the need for glue logic.

- **CPU Interface**

The WD90C20 host interface supports both the AT and Micro Channel buses with both 8- and 16-bit data path widths. The WD90C20 may also be directly connected to the bus if drive requirements permit. The bus mode is determined by the status of the configuration register bit, CNF(2), which is loaded by the de-assertion of reset. The value that is loaded reflects the status of one of the memory data pins at reset.
I/O transfers to and from the device are 8-bits wide, and display memory transfers are 8- or 16-bits wide, depending on the video mode selected. Because of their architecture, EGA type planar modes are restricted to 8-bit display data transfers. Text and 256 color extended modes allow 16-bit transfers on a 16-bit bus.

The controller generates wait states as required during display memory accesses. Wait states are not generated for I/O or video BIOS ROM accesses. Special I/O ports, such as 46E8H (when in AT bus mode) for setup, and 102H for VGA enable, are internally implemented.

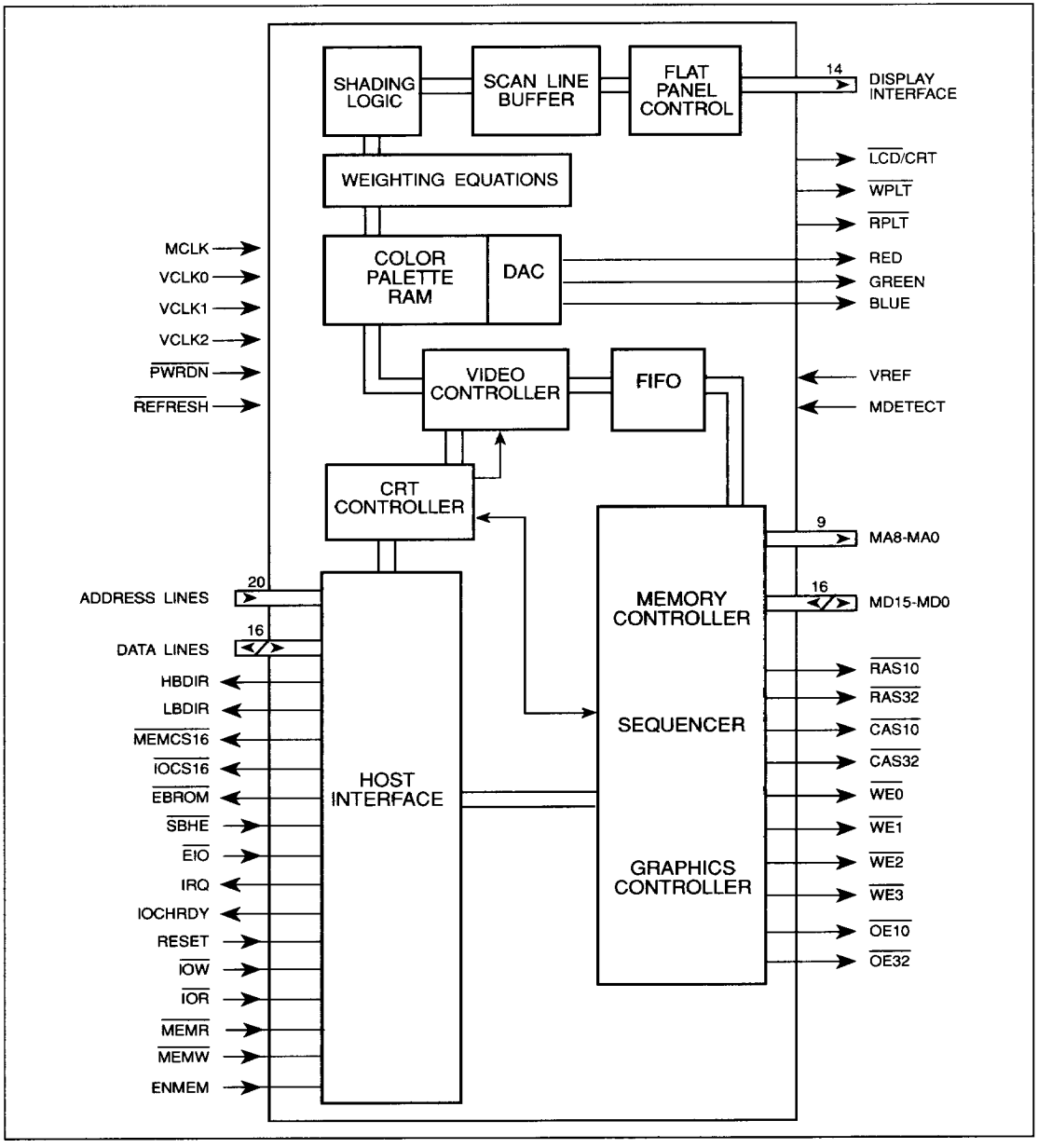

FIGURE 2-1. WD90C20 BLOCK DIAGRAM

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- **Display Memory Interface**

The WD90C20 generates all signals and memory timing required to operate the display memory. It directly controls three display memory sizes, 256 Kbyte, 512 Kbyte, and 1 Mbyte, as follows:

MEMORY SIZE	NUMBER AND TYPE OF DRAM REQUIRED
256 Kbytes	8 64 Kbyte by 4 DRAMs, or 2 64 Kbyte by 16 DRAMs
512 Kbytes	16 64 Kbyte by 4 DRAMs*, or 4 64 Kbyte by 16 DRAMs
1 Mbyte*	8 64 Kbyte by 16 DRAMs, or 8 256 Kbyte by 4 DRAMs

* Requires minimal support logic.

Page mode memories are required for all configurations. With a 36 MHz memory clock (MCLK), 120 ns devices may be used. If 256 color CRT modes are to be supported, 100 ns DRAMs and a 45 MHz MCLK are required. The WD90C20 includes special offset registers that allow the host to address up to 1 Mbyte of display memory.

- **CRT/RAMDAC Interface**

In addition to its internal RAMDAC, the WD90C20 allows the use of an external RAMDAC. This is helpful in specialized applications where a 24-bit wide color lookup table or pixel demultiplexing (to obtain higher video rates) is required. The external RAMDAC interface will support any Bt471/478/476 compatible device.

- **Clock Interface**

The WD90C20 has four clock input signal pins. Three of these (VCLK0, VCLK1, and VCLK2) are normally connected to oscillators. VCLK1 and VCLK2 may be configured to control an external clock multiplexor or clock generator, such as the WD90C61. In this configuration, VCLK0 becomes the clock input while VCLK1 and VCLK2 become outputs used to drive the multiplexor select inputs.

The memory clock input, MCLK, is used by the internal logic to generate all memory timing and may be up to 36 MHz for 120 ns DRAMs or 45 MHz for 100 ns DRAMs.

- **Flat Panel Interface**

The WD90C20 is designed to interface with 640 by 480 LCD or plasma panels. The flat panel interface lines change function to support the specific panel type chosen. Table 2-1 summarizes their use for each mode of operation.

When in LCD mode, with frame rate modulation selected, the controller supplies eight pixels per shift clock (four for the upper panel, and four for the lower). If pulse width modulation is selected, the controller provides two pixels per shift clock (one 4-bit pixel for the upper screen, and one 4-bit pixel for the lower screen).

When in Plasma mode, pulse width modulation is used to provide shading, while the controller supplies one pixel (four bits per pixel) per clock.

When in color STN LCD mode, the controller supplies two pixels per shift clock and uses hardware dithering. Each pixel (three bits, one each for R, G, and B), with dithering, provides 16 colors. The user can select:

– 256 out of 512 colors (WD90C20)
– 256 out of 4K colors (WD90C20A)

LCD	PLASMA	CRT
UD (3:0)	VD (3:0)	P (7:4)
LD (3:0)	Reserved	P (3:0)
FR	Reserved	BLANK
FP	VS	VSYNC
LP	HS	HSYNC
XSCLK	XSCLK	Reserved
WGTCLK	ENABLE	Reserved
Reserved	Reserved	PCLK

TABLE 2-1. DISPLAY INTERFACE OUTPUT FUNCTIONS

MONOCHROME LCD	COLOR LCD Device
UD (3)	R1
UD (2)	G1
UD (1)	B1
UD (0)	Border Information
LD (3)	R2
LD (2)	G2
LD (1)	B2
LD (0)	Reserved

TABLE 2-2. LCD DATA BIT ASSIGNMENTS

- **Powerup Configuration**

An internal 8-bit configuration register, CNF, controls the behavior of the major interfaces. Its bits are loaded with the inverted state of memory data lines 0 through 7 at the time RESET is deasserted. Pullup or pulldown resistors on the MD lines are used to set the configuration.

3.0 FLAT PANEL SUPPORT CONSIDERATIONS

Supporting VGA compatible graphics on flat panel displays involves several non-trivial issues, including:

- Display Timing Differences
- Screen Size Mapping
- Color-to-Gray Scale Mapping
- Shading Mechanics
- Split Screen Refresh

The following paragraphs address each of these issues.

• Display Timing Differences

Typically, flat panel displays have different timing requirements from a CRT. To overcome this problem, the WD90C20 provides a set of hidden display timing registers, which are read/write protected in locked mode.

• Screen Size Mapping

Unlike those of a CRT, the pixels on a flat panel display are real, discrete entities of a fixed size. This can result in problems when different display modes are mapped onto a single panel. The WD90C20 has been designed to support VGA and various backward compatible display modes on a 640 by 480 dot flat panel and it provides integral hardware support to deal with screen size incompatibilities.

In case of backward compatible display modes, such as EGA, which has a maximum resolution of 640 by 350, the vertical resolution of the mode is less than the number of dots of vertical resolution of the panel. This results in an active display area that is smaller than that of the panel and shifted up on the display, as shown in Figure 3-1(A). There are two ways to enhance screen size mapping as described below.

The simplest approach, supported by the WD90C20 is to keep the vertical resolution of the display mode constant but center the active display area vertically on the panel. In the case of an EGA 350 line mode being displayed on a 480 line panel, this would involve shifting the active display area down 65 lines (that is, 480 minus 350, the quantity divided by two). The effect of such a mapping is shown in Figure 3-1(B).

If the goal is to have the active display area fill the panel in all modes, then the active display area can be expanded by double scanning a portion of the active scan lines. Previously available controllers simply double scan lines at regular intervals, every third line in the case of EGA 350 line modes.

The WD90C20A uses an advanced proprietary algorithm that automatically expands to fill all 480 lines*. This algorithm can be used to support better "screen scrolling" when in 350 line modes.

* Patent pending on Hardware Vertical Expansion.

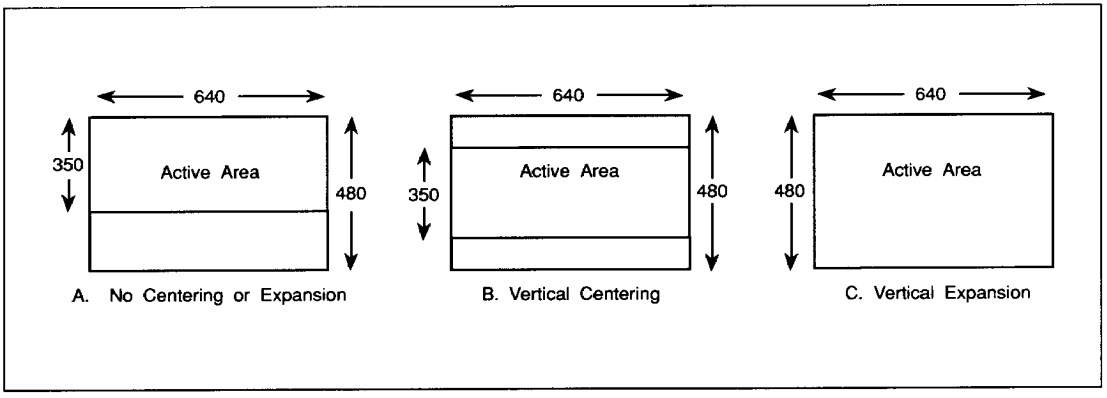

FIGURE 3-1. EXAMPLE OF SCREEN SIZE MAPPING

Under certain display conditions, any expansion scheme can result in undesirable aliasing effects of the displayed data. For this reason the WD90C20A allows the system designer flexibility to choose between vertical expansion or centering as shown below.

	CENTERING	VERTICAL EXPANSION
WD90C20	Y	N
WD90C20A	Y	Y

Horizontal resolution issues involve 720 dot modes such as VGA text and Hercules graphics. In VGA text mode, the 9th dot in each character box is dropped. The net effect is a slight compression in the spacing between characters. Alternatively, a different font may be loaded, although a nonstandard font size may not be fully compatible.

- **Color-to-Gray Scale Mapping**

The VGA standard defines how colors are mapped to 64 gray scale values on monochrome monitors. The mapping is based on the following RGB weighting equation:

$$I = .30R + .59G + .11B$$

Unfortunately, many of the currently available panels support at most sixteen shades and some only support two. In order to provide faithful support of all of the standard VGA modes on a flat panel, the WD90C20 provides a range of features to map colors to intensities and control panel shading. Foremost among these is sophisticated logic that converts gray scale values into dithering patterns. Additionally, the device allows software modification of the weighting values used in the gray scale mapping equation. Figure 3-2 gives an overview of the color-to-gray scale support provided by the WD90C20.

- **Shading Mechanics**

The WD90C20 supports shading via either frame rate or pulse width modulation. Pulse width modulation is handled via the display panel. The controller transfers 2, 3, or 4 bits per pixel to the driver logic on the panel, along with a high speed clock signal used to sequence the shading logic. Frame rate modulation, on the other hand, must be implemented in the display controller. The WD90C20 provides support for 2, 4, 8, 16, or 32 shade frame rate modulation with its integrated dithering controller. Any combination of dithering patterns can be selected via the dithering controller's mapping RAM. This design allows the WD90C20 to provide flicker-free frame rate modulation with frame rates as low as 70 Hz.

- **Split Screen Refresh**

The WD90C20 provides support for panels that are split into upper and lower panels requiring simultaneous refresh. This type of refresh is typically used by non-active matrix LCDs.

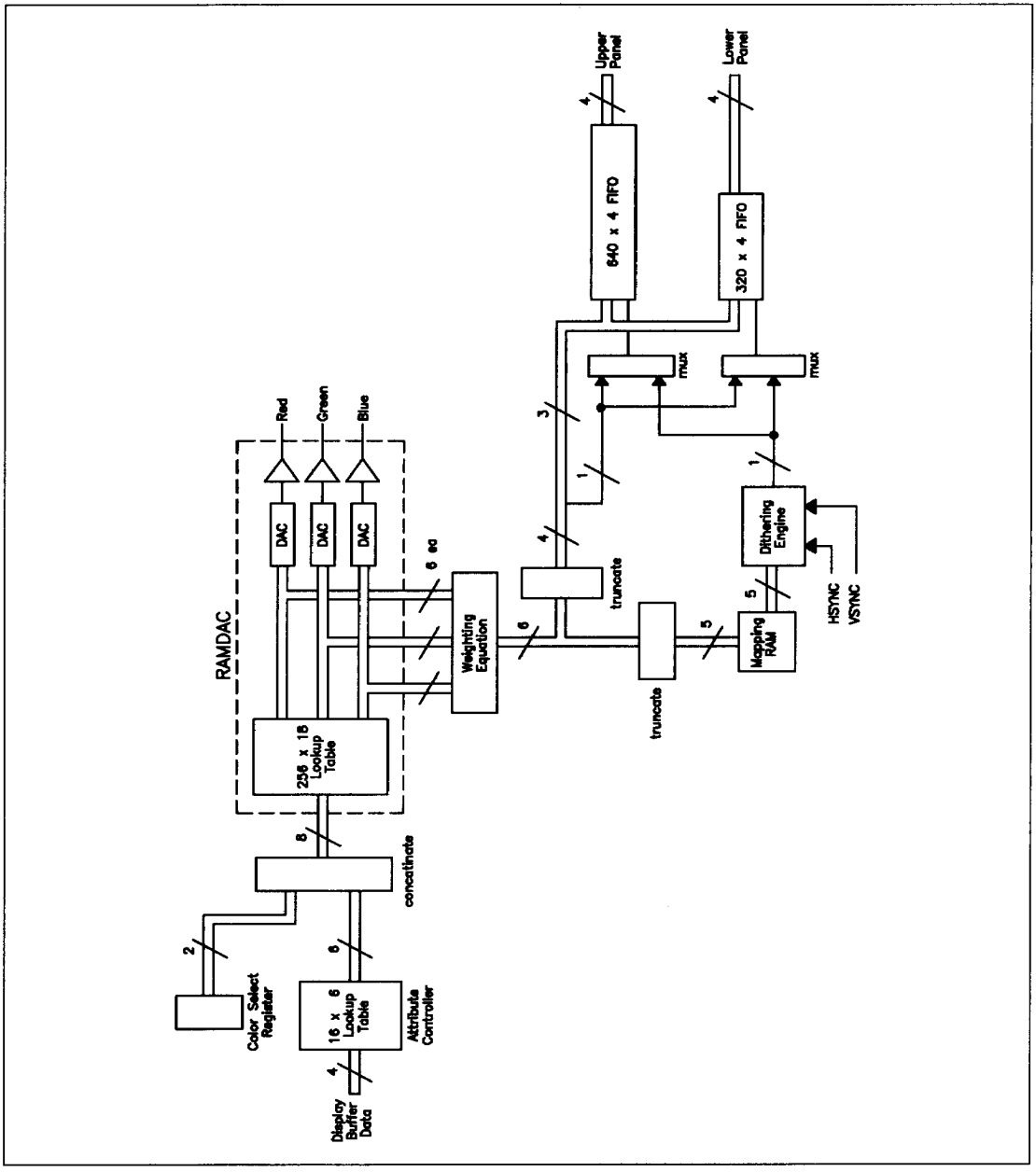

FIGURE 3-2. WD90C20 COLOR MAPPING

4.0 SIGNAL DESCRIPTION

Figure 4-1 illustrates the 132 plastic flat pack (PFP).

Table 4-1 lists all pins referenced in Figure 4-1 and provides a detailed description of each signal.

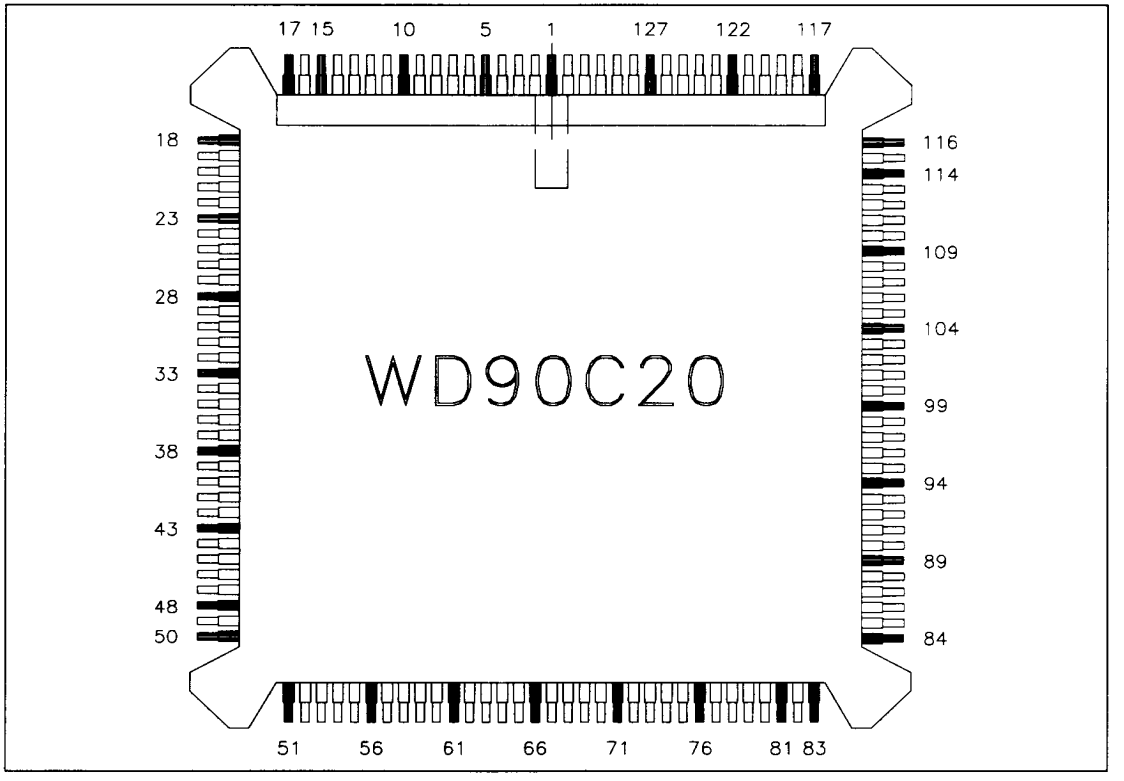

FIGURE 4-1. 132-PIN PFP (TOP VIEW)

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PIN	MNEMONIC	I/O	DESCRIPTION
			POWERON
42	RESET	I	**Reset** This signal input will reset the WD90C20. MCLK and VCLK0 should be connected to the WD90C20 in order for the WD90C20 to initialize during reset. Western Digital Imaging Registers, PR1 and CNF, are initialized at powerup reset based on the logic level on the MD15-0 bus as determined by pullup/ pulldown resistors. The reset pulse width should be at least ten MCLK clock periods.
			CLOCK SELECTION
96	VCLK2	I/O	**Video Clock 2** This pin can be a third video display clock input or an output to the external clock selection module. Pin direction is programmed simultaneously with that of VCLK1. It acts as either a user-defined external clock input, or as an output reflecting the content of bit PR2(1) if CNF (3) is set to 1. Refer to the Configuration Register description. MCLK should be greater than or equal to selected VCLK.
97	VCLK1	I/O	**Video Clock 1** This pin can be a second video display clock input or an output to the external clock selection module. Pin direction is determined on reset by a pullup/down resistor on pin MD3. A VCLK1 input frequency of 28.322 MHz is used to display 720 pixels per horizontal line. When it is an output, VCLK1 is an active low pulse during I/O writes to port 3C2H. Refer to the Configuration Register description. MCLK should be greater than or equal to selected VCLK.
98	MCLK	I	**Memory Clock** This clock signal determines the VGA graphics mode video DRAM read/write access timing as well as system micro-processor I/O and memory timing. MCLK should be approximately 36 MHz for 120 ns DRAMS, and 45.0 MHz for 100 ns DRAMS.
99	VCLK0	I	**Video Clock 0** This input is the video display clock for alphanumeric and graphics display modes. Typically, VCLK0 is 25.175 MHz to display 640 pixels per horizontal display line. MCLK should be greater than or equal to VCLK0. The Miscellaneous Output Register bits 2 and 3, both set to 0, will select this clock if VCLK1 and VCLK2 are used as inputs.
			HOST INTERFACE
1 - 2 117 - 122 124 - 132	SA15 - SA16 SA0 - SA5 SA6 - SA14	I	**Address Bus (SA16-SA0)** These active high inputs form the lower order 17 bits of video memory address. These inputs are directly connected to the system bus.

TABLE 4-1. SIGNAL DESCRIPTION

PIN	MNEMONIC	I/O	DESCRIPTION
			HOST INTERFACE
3 - 5	LA17 - LA19	I	**Unlatched Address Bus (LA19 -LA17)** These active high inputs form the high-order three bits of video memory address. These addresses are not decoded during I/O accesses in AT or Micro Channel modes. These inputs are directly connected to the system bus.
6	SBHE	I	**System Byte High Enable** If SA0 is "0", this signal is used to enable 16-bit data transfer mode when SBHE is "0". With SA0, this signal is also used to select high byte data (SD[15:8]) or low byte data (SD[7:0]).
7	ENMEM	I	**Enable Memory** This line is driven by external decode logic. In AT mode, this signal is decoded by LA23 - LA20 and REFRESH. In Micro Channel mode, this signal is decoded by LA23 - LA20 and MADE24 ("1" = enable).
8	EIO/3C3D0	I	**Enable I/O** In AT mode, this active low signal is used to enable I/O address decoding and is connected directly to the system bus signal AEN (address enable). In Micro Channel mode, this line is from I/O port 3C3 bit 0, and enables video subsystem memory and I/O address decoding ("1" = enable).
11	ALE CDSETUP	I	**ALE** In AT mode, this line is ALE; in Micro Channel mode, it is driven by the host to individually select channel connector slots during system configuration and error recovery procedures.
12	IRQ/IRQ	O	**Interrupt Request** Programmable processor interrupt request. It is enabled via Bit 5 in the Vertical Retrace End register. It is active high in AT mode and active low in Micro Channel mode. When the end of the vertical display occurs, this signal goes active, causing an interrupt. It will stay latched until CRTC11 Bit 4 clears it. In an AT system IRQ is not connected, although you may connect it if you desire. IRQ9 is used to generate an interrupt in Micro Channel mode. For further details, see the reference literature.
13	EBROM CDSFDBK	O	**Enable BIOS ROM** In AT mode, this is an active low signal to enable BIOS ROM (C0000H - C7FFFH) if enabled by PR1(0). It is not active for access to addresses in the range C60000H-C67FFH, but this address range may be mapped-in by setting PR17 (0) = 0. A write to the WD90C20 internal I/O port address, 46E8H, causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping. In Micro Channel mode, this signal is used as Card Selected Feedback to provide positive acknowledgement of its presence at the addresses specified by the host.

TABLE 4-1. SIGNAL DESCRIPTION (CONTINUED)

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PIN	MNEMONIC	I/O	DESCRIPTION
14	$\overline{\text{MEMCS16}}$/ $\overline{\text{CDDS16}}$	O	**Memory Chip Select 16 Bits** In AT mode, this line is used to respond to the host to enable a 16-bit video memory data transfer. In Micro Channel mode, this line provides $\overline{\text{CDDS16}}$ for 16-bit video memory or I/O access. (For WD90C20 only, this line must be inverted to provide $\overline{\text{CDDS16}}$).
15	IOCHRDY/ CDCHRDY	O	**Ready** An active high output which signals to the system processor that a memory access is complete. This signal is used only to add wait states to the bus cycles during video memory accesses. It is pulled inactive by the WD90C20 to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM. For further details, refer to the reference literature.
16	HBDIR/ HSYNC	O	**High Byte Direction** This line is used to control the data direction of an external high byte data buffer if the external data buffer is necessary for the implementation. This line will be driven "LOW" only in memory READ or I/O READ cycles. (For the WD90C20A only simultaneous display mode, the HBDIR pin can be programmed to output CRT HSYNC.)
17	LBDIR/ VSYNC	O	**Low Byte Direction** This line is used to control the data direction of an external low byte data buffer if the external data buffer is necessary for the implementation. This line will be driven "LOW" only in memory READ or I/O READ cycles. (For the WD90C20A only simultaneous display mode, the LBDIR pin can be programmed to output CRT VSYNC.)
19 - 26 29 - 36	SD15 - SD8 SD7 - SD0	I/O	**Data Bus (SD15 - SD0)** These bidirectional signals may either be connected directly to a local data bus requiring less than 8 ma. of source/sink, or may be connected through two external bus buffers.
38	$\overline{\text{MEMR}}$/ M/$\overline{\text{IO}}$	I	**Memory Read** In AT mode, this signal is called $\overline{\text{SMEMR}}$ and is an active low memory read strobe. It is asserted in 8-/16-bit memory read cycles. In Micro Channel mode, the signal is called M/$\overline{\text{IO}}$. It distinguishes between memory and I/O cycles. When (M/$\overline{\text{IO}}$) is high, a memory cycle is in process. A low on (M/$\overline{\text{IO}}$) shows that an I/O cycle is in process. For further details, refer to the reference literature.
39	$\overline{\text{MEMW}}$/ $\overline{\text{S0}}$	I	**Memory Write** The active low memory write strobe in AT mode for 8-/16-bit data transfers. In Micro Channel mode, it becomes $\overline{\text{S0}}$ and is the channel status signal which indicates the start and type of a channel cycle. Along with the $\overline{\text{S1}}$, M/$\overline{\text{IO}}$ and $\overline{\text{CMD}}$ signals, it is decoded to interpret I/O and memory commands. For further details, refer to the reference literature.

TABLE 4-1. SIGNAL DESCRIPTION (CONTINUED)

PIN	MNEMONIC	I/O	DESCRIPTION
43	$\overline{\text{REFRESH}}$	I	**Refresh** This active low input pin is connected to the system $\overline{\text{REFRESH}}$ signal from the I/O bus.
40	$\overline{\text{IOR}}$/ $\overline{\text{S1}}$	I	**I/O Read** Active low I/O read strobe in AT mode. It is asserted in 8-/16-bit I/O read bus cycles. $\overline{\text{S1}}$ is the alternate mnemonic used in Micro Channel mode to indicate the start and type of a channel cycle. For further details, refer to the reference literature.
41	$\overline{\text{IOW}}$/ $\overline{\text{CMD}}$	I	**I/O Write** Active low strobe. In AT mode, the strobe signals an I/O write for 8-/16-bit I/O write cycles. In Micro Channel mode it is synonymous with $\overline{\text{CMD}}$; address bus validity is signaled by $\overline{\text{CMD}}$ going low while the rising edge of $\overline{\text{CMD}}$ indicates the end of a Micro Channel bus cycle. For further details, refer to the reference literature.
DISPLAY MEMORY INTERFACE			
45 - 52 55	MA0 - MA7 MA8	O	**Memory Address (MA0 - MA8)** Display memory DRAM address.
56	$\overline{\text{RAS10}}$	O	**Row Address Strobe** Active low Memory Maps 1 and 0 RAS output signal.
57	$\overline{\text{RAS32}}$	O	**Row Address Strobe** Active low Memory Maps 3 and 2 RAS output signal.
58	$\overline{\text{CAS10}}$	O	**Column Address Strobe** Active low Memory Maps 1 and 0 CAS output signal.
59	$\overline{\text{CAS32}}$	O	**Column Address Strobe** Active low Memory Maps 3 and 2 CAS output signal.
60	$\overline{\text{WE0}}$	O	**Write Enable** Active low Memory Map 0 DRAM write enable signal.
61	$\overline{\text{WE1}}$	O	**Write Enable** Active low Memory Map 1 DRAM write enable signal.
62	$\overline{\text{WE2}}$	O	**Write Enable** Active low, Memory Map 2 write enable signal.
63	$\overline{\text{WE3}}$	O	**Write Enable** Active low, Memory Map 3 write enable signal.
64	$\overline{\text{OE10}}$	O	**Output Enable** Active low, Memory Maps 1 and 0 output enable signal.
65	$\overline{\text{OE32}}$	O	**Output Enable** Active low, Memory Maps 3 and 2 output enable signal.
68-75 77-84	MD15 - MD8 MD7 - MD0	I/O	**Data Lines** Lines MD15 through MD0 are the data bus to the video display DRAMS. Data lines MD0 through MD15 are pulled up or down with resistors to provide setup information on power-up (reset) as shown in Table 4-2.

TABLE 4-1. SIGNAL DESCRIPTION (CONTINUED)

PIN	MNEMONIC	I/O	DESCRIPTION
			MISCELLANEOUS
44	$\overline{\text{PWRDN}}$	I	**Power Down Selected** This active low input signal is used to disable screen refresh cycle.
110	$\overline{\text{LCD}}$/CRT	O	**LCD or CRT Selected** This active high output is used to power down an external RAM-DAC chip whenever the WD90C20 operates in LCD mode. "1" is CRT mode, and "0" is LCD mode.
			*DISPLAY INTERFACE**
86	PCLK	O	**Pixel Clock** This line is used to clock the video outputs into a RAMDAC in a CRT interface.
87	XSCLK	O	**Shift Clock** In an LCD interface, this signal is used to shift the upper and lower panel's data into the X-driver. In a Plasma interface, this signal is also used as shift clock.
88	WGTCLK	O	**Weight Control Clock** In an LCD interface, this signal is required to generate a gray scale in panels using pulse width modulation. In a Plasma interface, it is an "ENABLE VIDEO" signal.
89	LP/HSYNC	O	**Latch Pulse** In an LCD interface, this signal is used to latch all the data in the current scan line. In either a Plasma or a CRT interface, this signal is used for horizontal sync.
90	FP/VSYNC	O	**Frame Pulse** This signal is used to indicate the start of scanning to the Y-driver in an LCD interface. In either a Plasma or a CRT interface, this signal is used for vertical sync.
91	FR/BLANK	O	**Frame Control** In an LCD interface, it is an AC signal which is toggled every frame. In a CRT interface, it is the $\overline{\text{BLANK}}$ signal. Some panels call this signal "M."
103 - 100	LD3 - LD0	O	**Lower Panel Data Bit 3 to Bit 0** In an LCD interface, these signals are used for the lower panel data bus. In a Plasma interface, they are reserved. In a CRT interface, they are the lower four bits pixel video outputs to the RAM-DAC.
107 - 104	UD3 - UD0	O	**Upper Panel Data Bit 3 to Bit 0** In an LCD interface, these signals are used for the upper panel data bus. In a Plasma interface, they provide the pure 4-bit video data interface. In a CRT interface, they are the upper four bits pixel video outputs to the RAMDAC.

TABLE 4-1. SIGNAL DESCRIPTION (CONTINUED)

*The display interface functions are redefined for each display mode – see Table 2-1 on page 4 for details.

PIN	MNEMONIC	I/O	DESCRIPTION
			RAMDAC INTERFACE
92	$\overline{\text{RPLT}}$ /	O	**Read Palette** Video DAC register and color palette read signal. Active low during an I/O read of addresses 3C6H, 3C8H, and 3C9H. This line is active in both internal and external RAMDAC configurations.
	VD9		**Video Data Bit 9** In color TFT mode, this is the ninth data bit of the LCD interface.
93	$\overline{\text{WPLT}}$	O	**$\overline{\text{Write Palette}}$** Video DAC register and color palette write signal. Active low during an I/O write to addresses 3C6H-3C9H. This line is active in both internal and external RAMDAC configurations.
111	VREF	I	**Voltage Reference Input** An external voltage reference of 1.2V is connected to this input for normal operation of the internal RAMDAC. Grounding this pin changes the function of pin 112 and disables the internal RAMDAC so that the WD90C20 can be used with an external RAMDAC.
112	MDETECT/	I	**Monitor Detect** When pin 111 is grounded, this pin is used as a monitor detect input. The result of this input is read from 3C2H Bit 4.
	FSADJUST		**Full Scale Adjust** A resistor (RSET) on this pin sets the full scale output current of the RED, GREEN, and BLUE DAC's.
114	BLUE	O	**Blue Current Output** High impedance current source can directly drive a doubly-terminated 75 ohm coaxial cable.
115	GREEN	O	**Green Current Output** High impedance current source can directly drive a doubly-terminated 75 ohm coaxial cable.
116	RED	O	**Red Current Output** High impedance current source can directly drive a doubly-terminated 75 ohm coaxial cable.
			POWER AND GROUND
9,28, 53, 67, 94	Vcc	-	**Power**
10,18, 27,37,54, 66,76,85, 95	GND	-	**Ground**
123	AVcc	-	**+ 5VDC** - ANALOG (See Figure 4-2)
113	AGND	-	**Ground** - ANALOG (See Figure 4-2)
108	RVcc	-	**RAMDAC power** (See Figure 4-2)
	RGND	-	**RAMDAC ground** (See Figure 4-2)

TABLE 4-1. SIGNAL DESCRIPTION (CONTINUED)

14

PIN	WD90C20	WD90C20A
	Pullup/Pulldown Type	Pullup/Pulldown Type
SD [15:0]	PU	
LA [19:17]	PD	
SA [16:0]	PD	PD
MEMEN	PD	PD

PU = 100K Ohm Nominal, PD = 200K Ohm Nominal

MEMORY DATA LINE	POWERUP FUNCTION	DATA STORED AT NAME	PORT
MD15	EGA SW4 / LCD Select*	PR11(7)**	3?5.2A.7
MD14	EGA SW3	PR11(6)**	3?5.2A.6
MD13	EGA SW2	PR11(5)**	3?5.2A.5
MD12	EGA SW1	PR11(4)**	3?5.2A.4
MD11	ANALOG/TTL Display	PR5(3)**	3CF.0F.3
MD10	–	–	–
MD9	Panel Select Bit 1	PR18(1)**	3?5.31.1
MD8	Panel Select Bit 0	PR18(0)**	3?5.31.0
MD7	General Purpose	PR5(7)***	3CF.0F.7
MD6	General Purpose	PR5(6)***	3CF.0F.6
MD5	General Purpose	PR5(5)***	3CF.0F.5
MD4	General Purpose	PR5(4)***	3CF.0F.4
MD3	VCLK1,2 (I/O)	None**	–
MD2	AT/Micro Channel Mode	None**	–
MD1	–	PR1(1)***	3CF.0B.1
MD0	BIOS ROM Mapping	PR1(0)***	3CF.0B.0

TABLE 4-2. PR REGISTER FUNCTIONS

NOTES:
Data lines MD0 - MD15 are pulled up or down with resistors to provide setup information on powerup (reset) as shown above.

* PR11(7) = 0 : mono LCD, PR11(7) = 1 : color LCD.
** Pullup resistor sets these bits to logic 1.
*** Pulldown resistor sets these bits to logic 1.

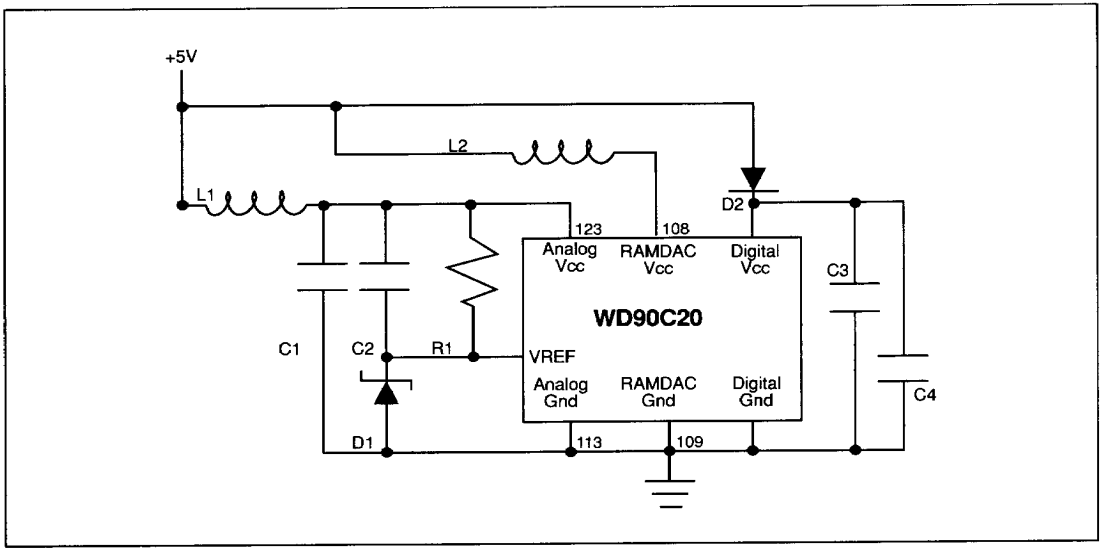

FIGURE 4-2. POWER DISTRIBUTION FOR WD90C20

COMPONENT	RECOMMENDED COMPONENT VALUE	SUGGESTED PART NUMBER/ COMMENTS
C1	0.1 UF	Reduces noise in analog portion of chip.
C2	0.1 UF	Stablizes VREF voltage.
C3	5 by 0.1 UF One each for Pins 9, 28, 53, 67, 94	Reduces noise to the VGA core.
C4	22 UF	Bulk decoupling.
D1	LM385	1.2 volt voltage reference.
D2	MBR150 (MBRL040-SMT) MBR160, or 2 1N5817s in series	Reduces voltage to digital portion of chip (40-50 mA reduction in current)
L1	TDK CB70-453215 FERRITE BEAD	Provides noise immunity to analog portions of WD90C20.
L2	TDK CB70-453215 FERRITE BEAD	Provides noise immunity to RAMDAC. No decoupling capacitor is to be used at Pin 108.

TABLE 4-3. RECOMMENDED COMPONENT VALUE

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5.0 WD90C20 REGISTERS

All standard IBM registers incorporated in the WD90C20 are functionally equivalent to the VGA implementation, while additional PR registers enhance the video subsystem. Compatibility registers provide functional equivalence for AT&T, Hercules, MDA, and CGA standards using the 6845 CRT Controller. This section describes the VGA registers (and the differences between VGA and EGA), as well as the PR registers.

5.1 VGA REGISTERS SUMMARY

REGISTERS	RW	MONO	COLOR	EITHER
GENERAL REGISTERS				
Miscellaneous Output Reg	W			3C2
	R			3CC
Input Status Reg 0	RO			3C2
Input Status Reg 1	RO	3BA	3DA	
Feature Control Reg	W	3BA	3DA	
	R			3CA
*Video Subsystem Enable	RW			3C3
NOTE: *Video Subsystem Enable Register 3C3H needs to be implemented externally in a Micro Channel configuration.				
SEQUENCER REGISTERS				
Sequencer Index Reg	RW			3C4
Sequencer Data Reg	RW			3C5
CRT CONTROLLER REGISTERS				
Index Reg	RW	3B4	3D4	
CRT Controller Data Reg	RW	3B5	3D5	
GRAPHICS CONTROLLER REGISTERS				
Index Reg	RW			3CE
Other Graphics Reg	RW			3CF
ATTRIBUTE CONTROLLER REGISTERS				
Index Reg	RW			3C0
Attribute Controller Data Reg	W			3C0
	R			3C1
VIDEO DAC PALETTE REGISTERS				
Write Address	RW			3C8
Red Address	W			3C7
DAC State	R			3C7
Data	RW			3C9
Pel Mask	RW			3C6

TABLE 5-1. VGA REGISTERS SUMMARY

5.2 COMPATIBILITY REGISTERS

FUNCTIONS	RW[1]	MDA[2]	CGA[2]	AT&T[2]	HERCULES[2]
Mode Control Reg	WO	3B8	3D8	3D8	3B8
Color Select Reg	WO		3D9	3D9	
Status Reg	RO	3BA	3DA	3DA	3BA
Preset Light Pen Latch	WO	3B9	3DC	3DC	
Clear Light Pen Latch	WO	3BB	3DB	3DB	
AT&T/M24 Reg	WO			3DE	
Hercules Reg	WO				3BF
CRTC[3]	RW	3B0-3B7	3D0-3D7	3D0-3D7	3B0-3B7

TABLE 5-2. COMPATIBILITY REGISTERS SUMMARY

NOTES:

1. RO = Read-Only, WO = Write-Only, RW = Read/Write.
2. All Register addresses are in hex.
3. 6845 Mode Registers.

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5.3 VGA REGISTERS

This section describes the VGA registers.

5.4 GENERAL REGISTERS

NAME	READ PORT	WRITE PORT
Miscellaneous Output	3CC	3C2
Input Status Register 0	3C2	---
Input Status Register 1	3?A	---
Feature Control	3CA	3?A

NOTES:
1. Reserved bits should be set to zero.
2. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

   0 = B in Monochrome Modes
   1 = D in Color Modes

5.4.1 Miscellaneous Output Register, Read Port = 3CC, Write Port = 3C2

BIT	FUNCTION
7	Vertical Sync Polarity Select
6	Horizontal Sync Polarity Select
5	Odd/Even Memory Page Select
4	Reserved
3	Clock Select 1
2	Clock Select 0
1	Enable Video RAM
0	I/O Address Select

Bit 7 *

Vertical Sync Polarity Selection.
0 = Positive vertical sync polarity.
1 = Negative vertical sync polarity.

Bit 6 *

Horizontal Sync Polarity Selection.
0 = Positive horizontal sync polarity.
1 = Negative horizontal sync polarity.

* These bits determine the vertical size of the vertical frame by the monitor. Their encoding is shown below:

BIT 7	BIT 6	VERTICAL FRAME
0	0	Reserved
0	1	400 lines/scan
1	0	350 lines/scan
1	1	480 lines/scan

Bit 5

Odd or Even Memory Page Select.
When in modes 0 through 5, one memory page is selected from the two 64 Kbyte pages.
0 = Lower page is selected.
1 = Upper page is selected.

Bit 4

Reserved in VGA.

Bit(3:2) Clock Select 1,0.

BIT 3	BIT 2	FUNCTION
0	0	Selects VCLK0 for VGA applications. Can be connected to allow 640 dots/line (25.175 MHz in CRT mode).
0	1	Selects VCLK1 for VGA applications. Can be connected to allow 720 dots/line (28.322 MHz in CRT mode) if Configuration Register bit 3 = 0.
1	0	Selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.
1	1	Reserved. Also selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.

Bit 1

System Processor Video RAM Access Enable.
0 = CPU access disabled.
1 = CPU access enabled.

Bit 0

CRT Controller I/O Address Range Selection. Selection for Monochrome (3B4 and 3B5), or Color (3D4 and 3D5) mode. Bit 0 also maps Input Status Register 1 at MDA (3BA) or CGA (3DA).

0 = CRTC and status addresses for MDA mode (3BX).
1 = CRTC and status addresses for CGA mode (3DX).

5.4.2 Input Status Register 0, Read Only Port = 3C2

BIT	FUNCTION
7	CRT Interrupt
6, 5	Reserved
4	Monitor Detect Bit for Color/ Monochrome Display
3: 0	Reserved

Bit 7

CRT Vertical Retrace Interrupt Pending or Cleared.
0 = Vertical retrace interrupt cleared.
1 = Vertical retrace interrupt pending.

Bit(6:5)

Reserved in VGA.

Bit 4

The DAC output currents, I_{RED}, I_{GREEN}, and I_{BLUE}, develop a voltage across the load resistances R_{LD}. These voltages are sent to comparitors against a voltage derived from the external voltage reference V_{REF}. For the WD90C20, the output current is determined by the formula:

$$I = \frac{code \times 0.04 \times V_{REF}}{R_{SET}}$$

where the codes range from 0 to 63 (0H to 3FH) for a 6-bit DAC.

For the WD90C20A, the output current is determined by the formula:

$$I = \frac{code \times V_{REF} \times 1.036}{R_{SET}}$$

The results of the monitor detection circuitry is readable at port 3C2H Bit 4. (See Figure B-1) It is important that this output signal be read during active video ouput, not during retrace or any other blanking period.

Bit(3:0)

Reserved.

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5.4.3 Input Status Register 1, Read Only Port = 3?A

BIT	FUNCTION
7, 6	Reserved
5	Diagnostic 0
4	Diagnostic 1
3	Vertical Retrace
2, 1	Reserved
0	Display Enable

Bit(7:6)

Reserved.

Bit(5:4)

Color Plane Diagnostics.
These bits allow the processor to set two out of eight colors by activating the Attribute Controller's Color Plane Enable Register Bits 4 and 5. Their status is defined in the following table:

COLOR PLANE ENABLE REGISTER		INPUT STATUS REGISTER 1	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit 3

Vertical Retrace Status.
0 = Vertical frame is displayed.
1 = Vertical retrace is active.

Bit(2:1)

Reserved.

Bit 0

Display Enable Status.
0 = CRT screen display in process.
1 = CRT screen display disabled for horizontal or vertical retrace interval.

5.4.4 Feature Control Register, Read Port = 3CA, Write Port = 3?A

BIT	FUNCTION
7 - 4	Reserved
3	Vertical Sync Control
2 - 0	Reserved

Bits(7:4)

Reserved

Bit 3

Vertical Sync Control.
0 = Vsync output enabled.
1 = Vsync output is logical "OR" of Vsync and Vertical Display Enable.

Bit(2:0)

Reserved.

5.5 SEQUENCER REGISTERS

PORT	INDEX	NAME
3C4	---	Sequencer Index
3C5	00	Reset
3C5	01	Clocking Mode
3C5	02	Map Mask
3C5	03	Character Map Select
3C5	04	Memory Mode

NOTE: Reserved bits should be set to 0.

5.5.1 Sequencer Index Register, Read/Write Port = 3C4

BIT	FUNCTION
7 - 3	Reserved
2 - 0	Sequencer Address/Index Bits

Bit(7:3)

Reserved.

Bit(2:0)

Sequencer Address/Index.
The Sequencer Address Register is written with the index value (00H-04H) of the Sequencer register to be accessed.

5.5.2 Reset Register, Read/Write Port = 3C5, Index = 00H

BIT	FUNCTION
7 - 2	Reserved
1	Synchronous Reset
0	Asynchronous Reset

Bit(7:2)

Reserved.

Bit 1

Synchronous Reset.
0 = Sequencer is cleared and halted synchronously.
1 = Operational mode (Bit 0 = 1).

Bit 0

Asynchronous Reset.
0 = Sequencer is cleared and halted asynchronously.
1 = Operational mode (Bit 1 = 1).

5.5.3 Clocking Mode Register, Read/Write Port = 3C5, Index = 01H

BIT	FUNCTION
7, 6	Reserved
5	Screen Off
4	Shift 4
3	Dot Clock
2	Shift Load if Bit 4 = 0
1	Reserved
0	8/9 Dot Clocks

Bit(7:6)

Reserved.

Bit 5

Screen Off.
0 = Normal screen operation.
1 = Screen turned off. SYNC signals are active and this bit may be used for quick full screen updates.

Bit 4

Video Serial Shift Register Loading.
0 = Serial shift registers loaded every character or every other character clock depending on Bit 2.
1 = Serial shift registers loaded every 4th character clock (32 bit fetches).

Bit 3

Dot Clock Selection.
0 = Normal dot clock selected by VCLK input frequency.
1 = Dot Clock divided by 2 (320/360 pixels wide).

Bit 2

Shift Load. Effective only if Bit 4=0.
0 = Video serializers will be loaded every character clock.
1 = Video serializers are loaded every other character clock.

Bit 1

Reserved.

Bit 0

8/9 Dot Clock.
Commands Sequencer to generate 8 or 9 dot wide character clock.
0 = 9 dot wide character clock.
1 = 8 dot wide character clock.

5.5.4 Map Mask Register, Read/Write Port = 3C5, Index = 02

BIT	FUNCTION
7 - 4	Reserved
3	Map 3 Enable
2	Map 2 Enable
1	Map 1 Enable
0	Map 0 Enable

Bit(7:4)

Reserved.

Bit(3:0)

Controls Writing to Memory Maps (0-3), respectively.
0 = Writing to maps (0-3) disallowed.
1 = Maps (0-3) accessible.

5.5.5 Character Map Select Register, Read/Write Port = 3C5, Index = 03H

BIT	FUNCTION
7, 6	Reserved
5	Character Map Select A Bit 2
4	Character Map Select B Bit 2
3	Character Map Select A Bit 1
2	Character Map Select A Bit 0
1	Character Map Select B Bit 1
0	Character Map Select B Bit 0

If Sequencer Register 4 Bit 1 is 1, then the attribute byte Bit 3 in text modes is redefined to control switching between character sets. "0" selects character map B. "1" selects character map A. Character Map selection from either plane 2 or plane 3 is determined by PR2(2), PR2(5), and Bit 4 of the attribute code.

Bit(7:6)

Reserved.

Bit 5

Character Map A MSB Select.
The Most Significant Bit (MSB) of character map A, along with Bits 3 and 2, select the location of character map A as shown below.

BITS 5 3 2	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 Kbyte
0 0 1	1	3rd 8 Kbyte
0 1 0	2	5th 8 Kbyte
0 1 1	3	7th 8 Kbyte
1 0 0	4	2nd 8 Kbyte
1 0 1	5	4th 8 Kbyte
1 1 0	6	6th 8 Kbyte
1 1 1	7	8th 8 Kbyte

Bit 4

Character Map B MSB Select.
The MSB of character map B, along with Bits 1 and 0, select the location of character map B as shown below.

BITS 4 1 0	MAP SELECTED	FONT/PLANE 2 OR 3 LOCATION
0 0 0	0	1st 8 Kbyte
0 0 1	1	3rd 8 Kbyte
0 1 0	2	5th 8 Kbyte
0 1 1	3	7th 8 Kbyte
1 0 0	4	2nd 8 Kbyte
1 0 1	5	4th 8 Kbyte
1 1 0	6	6th 8 Kbyte
1 1 1	7	8th 8 Kbyte

Bit(3:2)

Character Map Select A.
Refer to Bit 5 table.

Bit(1:0)

Character Map Select B.
Refer to Bit 4 table.

5.5.6 Memory Mode Register, Read/Write Port = 3C5, Index = 04H

BIT	FUNCTION
7 - 4	Reserved
3	Chain 4
2	Odd/Even
1	Extended Memory
0	Reserved

Bit(7:4)

Reserved.

Bit 3

Chains 4 Maps.
0 = Processor sequentially accesses data using map mask register.
1 = Directs the two lower order video memory address pins (MA0,MA1) to select the map to be addressed. The map selection table is shown below:

MA1	MA0	MAP SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2

Odd/Even Map Selection.
0 = Even processor addresses to access maps 0 and 2. Odd processor addresses to access maps 1 and 3.
1 = Sequential processor access as defined by map mask register.

Bit 1

Extended Video Memory.
0 = 64 Kbyte of video memory.
1 = Greater than 64 Kbyte of memory for VGA/EGA modes.

Bit 0

Reserved.

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5.6 CRT CONTROLLER REGISTERS

PORT[1]	INDEX	VGA REGISTER NAME	6845 REG NAME[2]
3?4	---	CRT Controller Address Reg.	CRTC Address Reg
3?5	00	Horizontal Total	Hor. Total
3?5	01	Horizontal Display Enable End	Hor. Disp
3?5	02	Start Horizontal Blanking	See note 3.
3?5	03	End Horizontal Blanking	See note 3.
3?5	04	Start Horizontal Retrace	See note 3.
3?5	05	End Horizontal Retrace	See note 3.
3?5	06	Vertical Total	Vert. Disp.
3?5	07	Overflow	See note 3.
3?5	08	Preset Row Scan	See note 3.
3?5	09	Maximum Scan Line/Others	Max. Scan Line Add.
3?5	0A	Cursor Start	Cursor Start
3?5	0B	Cursor End	Cursor End
3?5	0C	Start Address High	Start Add. High
3?5	0D	Start Address Low	Start Add. Low
3?5	0E	Cursor Location High	Cursor Loc. High
3?5	0F	Cursor Location Low	Cursor Loc. Low
3?5	10	Vertical Retrace Start	Light Pen High Read
3?5	11	Vertical Retrace End	Light Pen Low Read
3?5	12	Vertical Display Enable End	
3?5	13	Offset	See note 3.
3?5	14	Underline Location	See note 3.
3?5	15	Start Vertical Blank	See note 3.
3?5	16	End Vertical Blank	See note 3.
3?5	17	CRTC Mode Control	See note 3.
3?5	18	Line Compare	See note 3.

TABLE 5-3. CRT CONTROLLER REGISTERS

NOTES:

1. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:
   ?= B in monochrome modes.
   ?= D in color modes.
2. 6845 Mode Registers are defined and explained in greater in the reference literature.
3. This register can be programmed in VGA mode only. It is not applicable in 6845 mode.
4. Reserved bits should be set to zero.

5.6.1 CRT Address Register, Read/Write Port = 3?4

BIT	FUNCTION
7 - 5	Reserved
4 - 0	Index bits

Bit(7:5)

Reserved.

Bit(4:0)

Index Register Bits.
CRT Controller index pointer bits to specify the register to be addressed. Its value is programmed hex.

5.6.2 Horizontal Total Register, Read/Write Port = 3?5, Index=00H

BIT	FUNCTION
7 - 0	Horizontal Total Period

Bit(7:0)

Count Plus Retrace Less 5.
In VGA mode, the horizontal total period is the total of the character count in the active display plus the character count in the retrace time less 5, per horizontal scan line.

5.6.3 Horizontal Display Enable End Register Read/Write Port = 3?5, Index 01H

BIT	FUNCTION
7 - 0	Displayed Characters per scan line

Bit(7:0)

The total number of displayed characters less one is programmed into this register.

Horizontal overscan begins when the horizontal character counter reaches this character clock value.

5.6.4 Start Horizontal Blanking Register, Read/Write Port = 3?5, Index = 02H

BIT	FUNCTION
7 - 0	Start Horizontal Blanking

Horizontal blanking begins when the horizontal character counter reaches the hexidecimal value in the character clocks in this register. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

5.6.5 End Horizontal Blanking, Read/Write Port = 3?5, Index = 03H

BIT	FUNCTION
7	Reserved
6, 5	Display Enable Signal Skew Control
4 - 0	End Horizontal Blanking (lower 5 bits)

This register is locked if the PR Register PR3(5) = 1 OR the Vertical Retrace End Register Bit 7 = 1.

Bit 7

Reserved.

Bit(6:5)

Display Enable Signal Skew Control.
These bits define the display enable signal skew time in relation to horizontal synchronization pulses. The skew table is shown below:

BIT 6	BIT 5	SKEW IN CHARACTER CLOCKS
0	0	0
0	1	1
1	0	2
1	1	3

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Bit (4:0)

End Horizontal Blanking.
To determine the value to be programmed into this register, first add the value in the register Start Horizontal Blanking and the desired width of the horizontal blanking in character clocks. The least significant five bits are programmed into this register, while the sixth most significant bit is the End Horizontal Retrace register (index 05H) Bit 7. When the least significant six bits of the horizontal character counter match these six bits, the horizontal blanking is ended.

5.6.6 Start Horizontal Retrace Pulse Register Read/Write Port = 3?5, Index = 04H

BIT	FUNCTION
7 - 0	Start Horizontal Retrace Character Count

Bit(7:0)

Start Horizontal Retrace Character Count.
Hex value in character count at which horizontal retrace output pulse becomes active. This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

5.6.7 End Horizontal Retrace Register, Read/Write Port = 3?5, Index = 05H

BIT	FUNCTION
7	End Horizontal Blank bit 6
6, 5	Horizontal Retrace Delay
4 - 0	End Horizontal Retrace

This register is locked if the PR Register PR3 (5) = 1 or the Vertical Retrace End Register Bit 7 = 1.

Bit 7

MSB (sixth bit) of the End Horizontal Blanking register.

Bit(6:5)

Horizontal Retrace Delay.
These bits define horizontal retrace signal delay. See the following table for details:

BIT 6	BIT 5	CHARACTER CLOCK DELAY
0	0	0
0	1	1
1	0	2
1	1	3

Bit(4:0)

End Horizontal Retrace.
To determine the value to be programmed into this register, first add the value in the register Start Horizontal Retrace and the desired width of the horizontal retrace in character clocks. The least significant five bits are programmed into this register. When the least significant five bits of the horizontal character counter match these five bits, the horizontal retrace signal is turned off.

5.6.8 Vertical Total Register, Read/Write Port = 3?5,Index = 06H

BIT	FUNCTION
7 - 0	Vertical Total

Bit(7:0)

Raster Scan Line Total Less 2.
The least significant 8 bits of a 10-bit count of raster scan lines for a display frame. The loaded value includes vertical total scan lines minus 2. Time for vertical retrace, and vertical sync are also included. The ninth and tenth bits of this count are loaded into the Vertical Overflow Register (index = 07H) Bit 0 and Bit 5, respectively. In 6845 modes, total vertical display time in rows is programmed into Bit 6 through Bit 0, while Bit 7 is reserved. Scan count reduction is not necessary. The number of scan lines in a row is determined by the maximum Scan Line Register (index 09H Bits 0 through 4). This register is locked if the PR Register PR3 (0) = 1 or the Vertical Retrace End Register Bit 7 = 1.

5.6.9 Overflow Vertical Register Read/Write Port = 3?5, Index = 07H

BIT	FUNCTION
7	Vertical Retrace Start Bit 9
6	Vertical Display Enable End Bit 9
5	Vertical Total Bit 9
4	Line Compare Bit 8
3	Start Vertical Blank Bit 8
2	Vertical Retrace Start Bit 8
1	Vertical Display Enable End Bit 8
0	Vertical Total Bit 8

++Bit 7

Vertical Retrace Start Bit 9 (index = 10H).

****Bit 6**

Vertical Display Enable End Bit 9 (index = 12H).

++Bit 5

Vertical Total Bit 9 (index = 06H).

Bit 4

Line Compare Bit 8 (index = 18H).

++Bit 3

Start Vertical Blank Bit 8 (index =15H).

++Bit 2

Vertical Retrace Start Bit 8 (index = 10H).

****Bit 1**

Vertical Display Enable End Bit 8 (index = 12H).

++Bit 0

Vertical Total Bit 8 (index = 06H).

NOTES:

** This register is locked if the PR Register PR3(1)=0 AND the Vertical Retrace End Register Bit 7 = 1.

++ This register is locked if the PR Register PR3(0) = 1 OR the Vertical Retrace End Register Bit 7 = 1.

5.6.10 Preset Row Scan Register, Read/Write Port = 3?5, Index = 08H

BIT	FUNCTION
7	Reserved
6, 5	Byte Panning Control
4 - 0	Preset Row Scan Count

Bit 7

Reserved.

Bit(6:5)

Byte Panning Control.
These bits allow up to 3 bytes to be panned in modes programmed as multiple shift modes.

BIT 6	BIT 5	OPERATION
0	0	Normal
0	1	1 Byte Left Shift
1	0	2 Bytes Left Shift
1	1	3 Bytes Left Shift

Bit(4:0)

Preset Row Scan Count.
These bits preset the vertical row scan counter once after each vertical retrace. This counter is incremented after each horizontal retrace period, until the maximum row scan count is reached. When maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scrolling of text.

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5.6.11 Maximum Scan Line Register, Read/Write Port=3?5, Index=09H

BIT	FUNCTION
7	200 to 400 Line Conversion
6	Line Compare Bit 9
5	Start Vertical Blank Bit 9
4 - 0	Maximum Scan Line

Bit 7

200 to 400 Line Conversion.
0 = Normal operation.
1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes display 400 scan lines (each line is double scanned).

Bit 6

Line Compare.
This is Bit 9 of the Line Compare Register (index = 18H).

Bit 5

Start Vertical Blank.
This is bit 9 of the Start Vertical Blank Register (index = 15H). This register is locked if the PR Register PR3 (0) = 1.

Bit(4:0)

Maximum Scan Line.
Maximum number of scanned lines for each row of characters. The value programmed is the maximum number of scanned rows per character minus 1. In 6845 mode, Bits 5 through 7 are reserved, and Bits 4 through 0 are programmed with the maximum scan line count less 1 for non-interlace mode. Interlaced mode is not supported.

5.6.12 Cursor Start Register, Read/Write Port = 3?5, Index = 0AH

BIT	FUNCTION
7, 6	Reserved
5	Cursor Control
4 - 0	Cursor Start Scan Line

Bit(7:6)

Reserved.

Bit 5

Cursor Control.
0 = Cursor on.
1 = Cursor off.

Bit(4:0)

These bits specify the row scan counter value within the character box where the cursor begins. They contain the value of the character row less 1. If this value is programmed with a value greater than the Cursor End Register (index = 0BH), no cursor is generated. For 6845 modes, Bit 7 is reserved. Bit 5 controls the cursor operation and Bits 4 through 0 contain the cursor start value. Bit 6 is not used.

5.6.13 Cursor End Register, Read/Write, Port = 3?5h, Index = 0BH

BIT	FUNCTION
7	Reserved
6, 5	Cursor Skew
4 - 0	Cursor End Scan Line

Bit 7

Reserved.

Bit(6:5)

Cursor Skew Bits.
Delays the displayed cursor to the right by the skew value in character clocks; e.g., 1 character clock skew moves the cursor right by 1 position on the screen. Refer to the table below.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bit (4:0)

These bits specify the last row scan counter value within the character box during which the cursor is active. If this value is less than the cursor start value, no cursor is displayed. In 6845 mode, Bits 7 through 5 are reserved and Bits 4 through 0 contain the row value of the cursor end.

NOTE: There are three types of cursors generated, depending upon the mode; i.e, EGA, VGA, or 6845 (non-VGA). The above description refers to the VGA cursor only.

5.6.14 Start Address High Register, Read/Write Port 3?5H, Index = 0CH

BIT	FUNCTION
7 - 0	Start Address High Byte

Bit(7:0)

Display Screen Start Address Upper Byte Bits.
Eight high order bits of the 16-bit video memory address used for screen refresh. The low order 8-bit register is at index 0DH. The PR Register PR3 Bits 3 and 4 extend this video memory start register to 18 bits. In 6845 modes Bits 6 and 7 are forced to "0" regardless of this register's contents, while the lower order 8 bits are at index register 0DH.

5.6.15 Start Address Low Register, Read/Write Port = 3?5H, Index = 0DH

BIT	FUNCTION
7 - 0	Start Address Low Byte

Bit(7:0)

The lower order eight bits of the 16-bit video memory address in VGA or 6845 modes.

5.6.16 Cursor Location High Register, Read/Write Port = 3?5h, Index = 0Eh

BIT	FUNCTION
7 - 0	Cursor Location High Byte

Bit(7:0)

Cursor Address Upper Byte Bits.
The eight higher order bits of 16-bit cursor location in VGA mode. For the lower order eight bits, see the Cursor Location Low Register at index 0FH. In VGA mode, the PR Register PR3 bits 3 and 4 extend the cursor location High Register to 18 bits. For 6845 modes, Bits 6 and 7 are reserved, while Bits 5 through 0 are the high order bits of the cursor.

5.6.17 Cursor Location Low Register, Read/Write Port = 3?5, Index = 0FH

BIT	FUNCTION
7 - 0	Cursor Location Low Byte

Bit(7:0)

Cursor Address Lower Byte Bits.

The lower order eight bits of the 16-bit video memory address in VGA or 6845 mode.

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5.6.18 Vertical Retrace Start Register, Read/Write Port = 3?5, Index=10H

BIT	FUNCTION
7 - 0	Vertical Retrace Start (Lower eight bits)

Bit(7:0)

Vertical Retrace Start Pulse Lower Eight Bits.
The lower eight bits of the 10-bit vertical retrace start register. Bits 8 and 9 are located in the Overflow Register (index = 07H). In 6845 compatible mode, this register shows the high order six bits in positions 5 through 0 as the light pen read back value, and Bits 6 and 7 are reserved. The lower order eight bits of the light pen read back register are at the index 11H. In EGA compatible mode this register shows the high order eight bits as the light pen value. This register is locked if PR register PR3 (0) = 1.

5.6.19 Vertical Retrace End Register, Read/Write Port = 3?5, Index = 11H

BIT	FUNCTION
7	CRTC 0-7 Write Protect
6	Select 3/5 DRAM Refresh
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
3 - 0	Vertical Retrace End

This register is locked if the PR Register PR3(0)=1.

Bit 7

CRTC Registers Write Protect.
0 = Enables writes to CRT index registers 00H-07H.
1 = Write protects CRT Controller index registers in the range of index 00H-07H. The line compare Bit 4 in the Overflow Register (07H) is not protected.

Bit 6

DRAM Refresh/Horizontal Scan Line.
Selects DRAM refresh cycles per horizontal scan line.
0 = Generates 3 refresh cycles for each horizontal scan line for normal VGA operation.
1 = Generates 5 DRAM refresh cycles per horizontal scan line.

Bit 5

Enable Vertical Retrace Interrupt.
0 = Enables vertical retrace interrupt.
1 = Disable vertical retrace interrupt.

Bit 4

Clear Vertical Retrace Interrupt.
0 = Clears vertical retrace interrupt by resetting (writing a 0 to) and internal flip flop.
1 = Vertical retrace interrupt. Allows an interrupt to be generated after the last displayed scan of the frame has occurred (i.e., the start of the bottom border).

Bit(3:0)

Vertical Retrace End.
These bits specify scan count at which vertical sync becomes inactive. For retrace signal pulse width "W", add the number of scan count for "W" to the value of the Vertical Retrace Start register. The least significant four bits of the result are written in the Vertical Retrace End register. When the least significant four bits of the vertical scan line counter match these four bits, the vertical retrace signal is turned off.

5.6.20 Vertical Display Enable End Register, Read/Write Port = 3?5, Index = 12H

BIT	FUNCTION
7 - 0	Vertical Display Enable End (Lower 8 bits)

Bit(7:0)

Vertical Display Enable End Lower 8 Bits.
The lower eight bits of 10-bit register that defines where the active display frame ends.

The programmed count is in scan lines minus 1. Bits 8 and 9 are in the Overflow Register (index 07H) at positions 1 and 6, respectively.

5.6.21 Offset Register, Read/Write Port = 3?5, Index = 13H

BIT	FUNCTION
7 - 0	Logical Line Screen Width

Bit(7:0)

Logical Line Screen Width.
This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or doubleword display memory access. It is calculated as follows:

Next Row Scan Start Address = Current Row Scan Start Address + (K * value in Offset Register), where K=2 in byte mode and K=4 in word mode.

5.6.22 Underline Location Register, Read/Write Port = 3?5, Index = 14H

BIT	FUNCTION
7	Reserved
6	Doubleword Mode
5	Count by 4
4 - 0	Underline Location

Bit 7

Reserved.

Bit 6

Doubleword Mode.
0 = Display memory addressed for byte or word access.
1 = Display memory addressed for double word access.

Bit 5

Count By 4 For Double Word Access
0 = Memory address counter clocked for byte or word access.
1 = Memory address counter is clocked at the character clock rate divided by 4.

Bit(4:0)

Underline Location.
These bits specify the row scan counter value within a character matrix where under line is to be displayed. Load a value 1 less than the desired scan line number.

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5.6.23 Start Vertical Blank Register, Read/Write Port = 3?5, Index =15H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	Start Vertical Blank (Lower eight bits)

Bit(7:0)

Start Vertical Blank Lower Eight Bits.
The lower eight bits of the 10-bit Start Vertical Blank Register. Bit 8 is in the Overflow Register (index = 07H) and Bit 9 is in the Maximum Scan Line Register (index = 09H). The 10-bit value is reduced by 1 from the desired scan line count where the vertical blanking signal starts.

5.6.24 End Vertical Blank Register, Read/write Port=3?5, Index=16H

This register is locked if the PR Register PR3(0)=1.

BIT	FUNCTION
7 - 0	End Vertical Blank

Bit(7:0)

Vertical Blank Inactive Count.
End Vertical Blank is an 8-bit value calculated as follows:

8-bit End Vertical Blank value =
(value of Start Vertical Blank minus 1) +
(value of vertical blank signal width in scan lines).

When the least significant eight bits of the vertical scan line counter match these eight bits, the vertical blank signal is turned off.

5.6.25 CRT Mode Control Register, Read/Write Port = 3?5, Index = 17H

This register is locked if PR Register PR3(5) = 1.

BIT	FUNCTION
7	Hardware Reset
6	Word or Byte Mode
5	Address Wrap
4	Reserved
3	Count by 2
2	Horizontal Retrace Select
1	Select Row Scan Counter
0	CGA Compatibility

Bit 7

Hardware Reset.
0 = Horizontal and vertical retrace outputs to be inactive.
1 = Horizontal and vertical retrace outputs enabled.

Bit 6

Word Or Byte Mode.
0 = Word address mode. All memory address counter bits shift down by 1-bit and the MSB of the address counter appears on the LSB. See the table on the next page.
1 = Byte address mode.

MEMORY ADDRESS	BYTE ADDRESS MODE	WORD ADDRESS MODE	DOUBLEWORD ADDRESS MODE
MA0/RF0	MA0	*MA15 OR MA13	MA12
MA1/RF1	1	0	MA13
MA2/RF2	2	1	0
MA3/RF3	3	2	1
MA4/RF4	4	3	2
MA5/RF5	5	4	3
MA6/RF6	6	5	4
MA7/RF7	7	6	5
MA8/RF8	8	7	6
MA9	9	8	7
MA10	10	9	8
MA11	11	10	9
MA12	12	11	10
MA13	13	12	11
MA14	14	13	12
MA15	15	14	13

* See Bit 5, defining address wrap. This table is applicable only when PR Register PR1 Bits 7 and 6 equal 0, or PR16 Bit 1 equals one.

The CRT Underline Location Register (index = 14H) bit 6 also controls addressing. However, when CRT14H(6) = 0, only the CRT Mode Control Register (index 17H) Bit 6 controls addressing. See the following table.

CRT14H	CRT17H	ADDRESS
Bit 6	Bit 6	Mode
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5

Address Wrap.

0 = In word address mode, this bit enables Bit 13 to appear at MA0, otherwise Bit 0 appears on MAO.

1 = Select MA15 for odd/even mode when 256 Kbyte of video memory is used on the system board.

Bit 4

Reserved.

Bit 3

Count by 2.

0 = Character clock increments memory address counter.

1 = Character clock divided by 2 increments the address counter.

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Bit 2

Horizontal Retrace Clock Rate Select for Vertical Timing Counter.

0 = Selects horizontal retrace clock rate.

1 = Selects horizontal retrace clock rate divided by 2.

Bit 1

Select Row Scan Counter.

0 = Selects row scan counter Bit 1 as output at MA14 address pin.

1 = Selects Bit 14 of the CRTC address counter as output at MA14 pin.

Bit 0

6845 CRT Controller Compatibility Mode Support for CGA Operation.

0 = Row scan address Bit 0 is substituted for memory address Bit 13 at MA13 output pin during active display time.

1 = Enable memory address pin 13 to be output at MA13 address pin.

5.6.26 Line Compare Register, Read/Write Port = 3?5, Index = 18H

BIT	FUNCTION
7 - 0	Line Compare (lower eight bits)

Bit(7:0)

Line Compare Lower 8 Bits.
Lower 8 bits of the 10-bit Scan Line Compare Register. Bit 8 is in the Overflow Register (index = 07H) and Bit 9 is in the Maximum Scan Line Register (index = 09H). When the vertical counter reaches this value, the internal start of the line counter is cleared.

5.7 GRAPHICS CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3CE	—	Graphics Index Register
3CF	00	Set/Reset
3CF	01	Enable Set/Reset
3CF	02	Color Compare
3CF	03	Data Rotate
3CF	04	Read Map Select
3CF	05	Graphics Mode
3CF	06	Miscellaneous
3CF	07	Color Don't Care
3CF	08	Bit Mask

NOTE: Reserved bits should be set to 0.

5.7.1 Graphics Index Register, Read/Write Port = 3CE

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Graphics Address Bits

Bit(7:4)

Reserved.

Bit(3:0)

Graphics Controller Register Index Pointer Bits. Note that some of the PR registers reside with the index pointer extension beyond the standard VGA Graphics Controller registers.

5.7.2 Set/Reset Register, Read/Write Port 3CF, Index = 00H

BIT	FUNCTION
7 - 4	Reserved
3	Set/Reset Map 3
2	Set/Reset Map 2
1	Set/Reset Map 1
0	Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Set/Reset Map.
When the CPU executes display memory write with Write Mode 0* selected and the Enable Set/Reset Register (index = 01H) activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are written to the corresponding display memory map. It is an eight bit fill operation. The map designations are defined below:

0 = Reset.
1 = Set.

BIT	SET/RESET
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE: The selection of Write Mode 0 is determined by the Graphics Mode Register (index = 05H) Bit 1 and Bit 0.

5.7.3 Enable Set/Reset Register, Read/Write Port = 3CF, Index = 01H

BIT	FUNCTION
7 - 4	Reserved
3	Enable Set/Reset Map 3
2	Enable Set/Reset Map 2
1	Enable Set/Reset Map 1
0	Enable Set/Reset Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Enable Set/Reset Register (Index 00H).
0 = When Write Mode 0 is selected, these bits, set to 0, disable the Set/Reset Register (index = 00H) memory map access and the map is written with the rotated 8-bit data from the system microprocessor as defined by the Data Rotate Register.
1 = When Write Mode 0 is selected, these bits enable memory map access defined by the Set/Reset Register (index = 00H), and the respective memory map is written with the Set/Reset Register value.

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5.7.4 Color Compare Register, Read/Write PORT 3CF, Index = 02H

BIT	FUNCTION
7 - 4	Reserved
3	Color Compare Map 3
2	Color Compare Map 2
1	Color Compare Map 1
0	Color Compare Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Color Compare.
The color compare bit contains the value to which all 8 bits of the corresponding memory map are compared. This comparison also occurs across all four maps, and a "1" is returned for the map positions where the bits of all four maps equal the Color Compare Register. If a system read is done with bit 3 = 0 for the Graphics Mode Register (index = 05H), data is returned without comparison. Color compare map coding is shown below.

BIT	COLOR COMPARE
3	Map 3
2	Map 2
1	Map 1
0	Map 0

5.7.5 Data Rotate Register, Read/Write Port = 3CF, Index = 03H

BIT	FUNCTION
7 - 5	Reserved
4	Function Select 1
3	Function Select 0
2	Rotate Count 2 Bit 2
1	Rotate Count 1 Bit 1
0	Rotate Count 0 Bit 0

Bit(7:5)

Reserved.

Bit(4:3)

Function Select.
Function select for any of the write mode operations defined in the Graphics Mode Register (index = 05H) is defined as follows.

BIT 4	BIT 3	FUNCTION
0	0	Video memory data unmodified
0	1	Video memory data ANDed with system data in the latches
1	0	Video memory data ORed with system data in the latches
1	1	Video memory data XORed with system data in the latches

Bit(2:0)

Rotate Count.
This specifies number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register (index = 05H).

5.7.6 Read Map Select Register, Read/Write Port = 3CF, Index = 04H

BIT	FUNCTION
7 - 2	Reserved
1	Map Select 1
0	Map Select 0

Bit(7:2)

Reserved.

Bit(1:0)

Map Select.

These bits select memory map in system read operations. This operation has no effect on color compare read mode. In odd/even modes, the value can be 00b or 01b to select chained maps 0 and 1 or value 10b or 11 to select the chained maps 2 and 3. Map read is defined as shown below.

BIT 1	BIT 0	READ MAP
0	0	0
0	1	1
1	0	2
1	1	3

5.7.7 Graphics Mode Register, Read/Write Port = 3CF, Index = 05H

BIT	FUNCTION
7	Reserved
6	256 Color Mode
5	Shift Register
4	CGA Odd/Even
3	Read Type
2	Reserved
1	Write Mode Bit 1
0	Write Mode Bit 0

Bit 7

Reserved.

Bit 6

256 Color Mode.

0 = Enables Bit 5 of this register to control loading of the shift registers. Four bit pixel is expanded to 6 bits through internal palette and is sent out on the lower 6-bit pins (VID5 - VID0) every dot clock. The remaining two video outputs (VID6, VID7) are determined by Bits 2 and 3 of the Color Select Register located at index = 14H within the Attribute Controller.

1 = Load video shift registers to support 256 color mode.

Bit 5

Shift Register.

Shift register load controls the way in which memory data is formatted in the four video shift registers. MSB is shifted out in all cases.

0 = Map 0 – Map 3 data is placed into shift registers for normal operations.

1 = For CGA graphics mode compatibility, even numbered shift registers, and odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4

Odd/Even Mode.

0 = Normal

1 = CGA compatible odd/even system access mode. Sequential addressing as defined by Bit 2 of the memory mode register (index = 04H) in the Sequencer Register. Even system addresses access maps 0 or 2 and odd system addresses access maps 1 or 3.

Bit 3

Read Mode.

0 = System reads data from memory maps selected by Read Map Select Register (index 04H). This setting will have no effect if Bit 3 of the Sequencer Memory Mode Register = 1.

1 = System reads the comparison of the memory maps and the Color Compare Register.

Bit 2

Reserved.

Bit(1:0)

Write Mode.

The table below defines the four write modes.

BIT 0	BIT 1	WRITE MODE
0	0	Write Mode 0. If the Set/Reset Register function is enabled for any of the maps, the 8 bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data which is right rotated by the number of bits defined in the Data Rotate Register, with the old LSB now the new MSB.
0	1	Write Mode 1. This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	Write Mode 2. Memory maps (3:0) are filled with the 8-bit value of the corresponding CPU data bits (3:0). The 32-bit output of the four memory maps is then operated on by the Bit Mask Register and the resulting data is written to the four memory maps.
1	1	Write Mode 3. Eight bits of the value contained in the Set/Reset Register (index = 00H) is written into the corresponding map, regardless of the Enable Set/Reset Register (index = 01H). The right rotated CPU data (see Write Mode 0) is ANDed with Bit Mask Register data to form an 8-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

5.7.8 Miscellaneous Register, Read/Write Port = 3CF, Index = 06H

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 1
2	Memory Map 0
1	Odd/Even
0	Graphics Mode

Bit(7:4)

Reserved.

Bit(3:2)

Memory Map 1, 0.
Display memory map control into the CPU address space is shown below:

BIT 3	BIT 2	CPU ADDRESS RANGE	LENGTH
0	0	A000:0H-BFFF:FH	128 Kbyte
0	1	A000:0H-AFFF:FH	64 Kbyte
1	0	B000:0H-B7FF:FH	32 Kbyte
1	1	B800:0H-BFFF:FH	32 Kbyte

Bit 1

Odd/Even Mode.
0 = CPU address bit A0 is the memory address bit MA0.
1 = CPU address bit A0 is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects map 0 or 2, while A0 = 1 selects map 1 or 3.

Bit 0

Graphics/Alphanumeric Mode.
This bit is programmed the same way as Bit 0 of the Attribute Mode Control Register.
0 = Alphanumeric mode selects.
1 = Graphics mode selected.

5.7.9 Color Don't Care Register, Read/Write Port 3CF, Index = 07H

BIT	FUNCTION
7 - 4	Reserved
3	Memory Map 3
2	Memory Map 2
1	Memory Map 1
0	Memory Map 0

Bit(7:4)

Reserved.

Bit(3:0)

Memory Map Color Compare Operation.
0 = Disable color compare operation.
1 = Enable color compare operation.

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5.7.10 Bit Mask Register, Read/Write Port = 3CF, Index = 08H

BIT	FUNCTION
7 - 0	Bit Mask

Bit(7:0)

The bit mask operation applies simultaneously to all four maps. In Write Modes 0 and 2, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation affects any data written by the processor.

0 = Bit position value is masked or is not changeable.
1 = Bit position value is unmasked and can be changed in the corresponding map.

5.8 ATTRIBUTE CONTROLLER REGISTERS

PORT (HEX)	INDEX (HEX)	NAME
3C0	——	Index Register
3C0	00-0F	Palette Registers
3C0	10	Attribute Mode Control Register
3C0	11	Overscan Control Register
3C0	12	Color Plane Enable Register
3C0	13	Horizontal PEL Panning Register
3C0	14	Color Select Register

NOTES:
1. Each attribute data register is written at 3C0 and register data is read from address 3C1.
2. Reserved bits should be set to zero.
3. ? " Value is controlled by Bit 0 of the Miscellaneous Output register and is programmed as shown below.

0 = B in Monochrome Modes.
1 = D in Color Modes.

5.8.1 Attribute Index Register, Read/Write Port = 3C0

BIT	FUNCTION
7 - 6	Reserved
5	Palette Address Source
4 - 0	Attribute Address Bits

Bit(7:6)

Reserved.

Bit 5

Palette Address Source.
0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers (index 00 - 0FH).
1 = Enable internal color palette and normal video translation.

Bit(4:0)

Attribute Controller Index Register Address Bits.

NOTE: The Attribute Index Register has an internal flip-flop, rather than an input bit, which controls the selection of the Address and Data Registers. Reading the Input Status Register 1 (port = 3?A) clears the flip-flop and selects the Address Register, which is read through address 3C1 and written at address 3C0. Once the Address Register has been loaded with an index, the next write operation to 3C0 will load the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address 3C0, but does not toggle for reads to address 3C1.

5.8.2 Palette Registers (00-0F Hex), Read Port 3C1/Write Port 3C0

BIT	FUNCTION
7 - 6	Reserved
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:6)

Reserved.

Bit(5:0)

Palette Pixel Colors.
They are defined as follows:
0 = Current pixel color deselected.
1 = Enable corresponding pixel color per the table below.

BIT	FUNCTION
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

5.8.3 Attribute Mode Control Register, Read Port 3C1/Write Port 3C0, Index = 10H

BIT	FUNCTION
7	VID5, VID4 Select
6	PEL Width
5	PEL Panning Compatibility
4	Reserved
3	Enable Blink/Select Background Intensity
2	Enable Line Graphics Character Code
1	Mono-Emulation
0	Graphics/Alphanumeric Mode

Bit 7

VID5, VID4 Select.
0 = VID5 and VID4 palette register outputs are selected.
1 = Color Select Register (index 14H) Bits 1 and 0 are selected for outputs at VID5 and VID4 pins.

Bit 6

Pixel Width.
0 = Disable 256 color mode pixel width. The PCLK output is the same as the internal dot clock rate.
1 = Enable pixel width for 256 color mode. The PCLK output is the internal dot clock divided by two.

Bit 5

PEL Panning Compatibility.
Line Compare in the CRT Controller.
0 = A Line Compare will have no effect on the PEL Panning Register.
1 = Allows a successful Line Compare to disable the PEL Panning Register and also Bits 5 and 6 of the CRT Controller Register 08 until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

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Bit 4

Reserved.

Bit 3

Background Intensity/Blink Selection.
0 = Selects background intensity from the MSB of the attribute byte.
1 = Selects blink attribute.

Bit 2

Enable Line Graphics Character Code.
Set this bit to 0 for character fonts that do not utilize line graphics character codes.
0 = Forces ninth dot to be the same color as background in line graphics character codes.
1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1

Mono/Color Emulation.
0 = Color display attributes.
1 = MDA attributes.

Bit 0

Graphics/Alphanumeric Mode Enable.
0 = Alphanumeric mode.
1 = Graphics mode.

5.8.4 Overscan Color Register, Read Port 3C1/Write Port 3C0, Index = 11H

BIT	FUNCTION
7	VID7
6	VID6
5	VID5
4	VID4
3	VID3
2	VID2
1	VID1
0	VID0

Bit(7:0)

Overscan/Border Color.
These bits determine the overscan or border color. For monochrome display, this register is set to 0. Border colors are set as shown above.

5.8.5 Color Plane Enable Register, Read Port 3C1/Write Port 3C0, Index = 12H

BIT	FUNCTION
7 - 6	Reserved
5	Video Status MUX1
4	Video Status MUX0
3 - 0	Enable Color Plane

Bit(7:6)

Reserved.

Bit(5:4)

Video Status Control.
These bits select two out of eight color outputs which can be read by the Input Status Register 1 (port = 03?A) Bits 4 and 5.

COLOR PLANE		INPUT STATUS REGISTER	
BIT 5	BIT 4	BIT 5	BIT 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit(3:0)

Color Plane Enable.
0 = Disables respective color planes. Forces pixel bit to 0 before it addresses palette.
1 = Enables the respective display memory color plane.

5.8.6 Horizontal PEL Panning Register, Read Port 3C1/Write Port 3C0, Index = 13H

BIT	FUNCTION
7 - 4	Reserved
3 - 0	Horizontal PEL Panning

Bit(7:4)

Reserved.

Bit(3:0)

Horizontal Pixel Panning.
It is available in text or graphics modes. These bits select pixel shift to the left horizontally. For 9 dots/character modes, up to 8 pixels can be shifted horizontally to the left. Likewise, for 8 dots/character up to 7 pixels can be shifted horizontally to the left. For 256 color, up to 3 position pixel shift can occur. The following table defines the shift in different modes.

LEFT SHIFT PIXEL VALUE			
Register Value	9 Dots Character	8 Dots Character	256 Color Mode
0	1	0	0
1	2	1	--
2	3	2	1
3	4	3	--
4	5	4	2
5	6	5	--
6	7	6	3
7	8	7	--
8	0	--	--

5.8.7 Color Select Register, Read Port 3C1/Write Port 3C0, Index = 14H

BIT	FUNCTION
7 - 4	Reserved
3	S_Color 7
2	S_Color 6
1	S_Color 5
0	S_Color 4

Bit(7:4)

Reserved.

Bit(3:2)

Color Value MSB.
Two most two significant bits of the eight digit color value for the video DAC. They are normally used in all modes except 256 color graphics.
Bit 3 = Set color bit VID7.
Bit 2 = Set color bit VID6

Bit(1:0)

Substituted Color Value Bits.
These bits can be substituted for VID5 and VID4 output by the Attribute Controller palette registers to create 8-bit color value. They are selected by the Attribute Controller Mode Control Register (index = 10H).

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5.9 COMPATIBILITY REGISTERS

NAME	PORT (HEX)
Mode Control Register	3?8
Color Select Register	3D9
Status Register	3?A
AT&T/M24 Register	3DE
Hercules Register	3BF
Preset Light Pen Latch	3B9 (Mono) 3DC (CGA)
Clear Light Pen Latch	3?B

NOTES:

1. The Compatibility Registers are available only in 6845 mode (non-VGA), which is enabled by setting PR Register PR2(6) = 1.

2. The AT&T/M24 Register also requires that M24 mode be enabled. This is done by setting PR Register PR2(7) = 1.

3. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

   0 = B in Monochrome Modes
   1 = D in Color Modes

5.9.1 Hercules/MDA Mode Control Register, MDA Operation Write Only Port = 3B8H

BIT	FUNCTION
7	Reserved/Display Memory Page Select
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Reserved/ Port 3BFH Enable
0	High Resolution Mode

Bit 7

Reserved in MDA mode. If Bit 1=1 and Port 3BFH bit 0 = 1, then this bit in Hercules Graphics mode selects the Display Memory Page.

0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit 6

Reserved.

Bit 5

Enable Blink.
0 = Disable blinking.
1 = Enable blinking.

Bit 4

Reserved.

Bit 3

Video Enable.
0 = Video disable.
1 = Video activated.

Bit 2

Reserved.

Bit 1

Port 3BFH Enable.
0 = Prevents setting of Port 3BF Bit 1:0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BFh Bit 1:0 to switch for the alpha or graphics mode selection.

Bit 0

High Resolution Mode (should be 1).
0 = High resolution disabled.
1 = High resolution is enabled.

5.9.2 Hercules Registers

The Hercules Mode Register is a 2-bit write only register located at I/O port address 3BF. It affects the device operation only in the 6845 mode. The enable mode register located at the address 3B8 overrides the write port 3BF functions defined by its Bits 0 and 1.

5.9.3 Enable Mode Register 3B8

BIT	FUNCTION
7	Display Memory Page Address Graphics Mode
6	Reserved
5	Enable Blink
4	Reserved
3	Video Enable
2	Reserved
1	Port 3BF Bit 0 Override
0	High Resolution Mode = 1

Bit 7

Display Memory Page Address In Graphics Mode.
0 = Display memory page address starts at B000:0H.
1 = Display memory page address starts at B800:0H.

Bit (6,4,2)

Reserved.

Bit 1

Port 3BF Bit 0 Override.
0 = Prevents setting of Port 3BF Bit 0, thereby forcing the alpha mode operation.
1 = Allows the Port 3BF Bit 0 to switch for the alpha or graphics mode selection.

Bit 5

Enable Blink.
0 = Disable blinking.
1 = Enable blinking.

Bit 3

Video Enable.
0 = Video disable.
1 = Video enable.

Bit 0

High Resolution (should be 1).
0 = High resolution disabled.
1 = High resolution enabled.

5.9.4 Hercules Compatibility Register, Write Only Port = 3BFH

BIT	FUNCTION
7 - 2	Reserved
1	Upper Memory Page Address
0	Enable Graphics

Bits (7:2)

Reserved.

Bit 1

Upper Memory Page Address.
Enable Mode Control Register (3B8) Bit 7 selects the displayed memory page address in the graphics mode. When it is reset, Bit 1 prevents access to the second memory page, located at B800:0H for the 32 Kbyte memory space.
0 = Upper memory page is mapped out.
1 = Upper memory page is accessible.

Bit 0

Enable Graphics.
Allows the Enable Mode Register (3B8) Bit 1 to override.
0 = Alpha mode display.
1 = Graphics modes may be displayed.

5.9.5 Color CGA Operation Register, Write Only Port = 3D8

BIT	FUNCTION
7, 6	Reserved
5	Enable Blink
4	B/W Graphics Mode
3	Enable Video
2	B/W/Color Mode Select
1	Graphics/Alpha Mode Select
0	Alpha Mode

Bit (7:6)

Reserved.

Bit 5

Enable Blink Function.
0 = Disables blinking function.
1 = For normal operation, set this bit to allow blinking.

Bit 4

B/W Graphics Mode Enable.
0 = Deselect 640 by 200 B/W graphics mode.
1 = Enable 640 by 200 B/W graphics mode.

Bit 3

Activate Video Signal.
0 = Deactivates video signal. This is done during mode changes.
1 = B/W mode enabled.

Bit 1

Text or Graphics Mode Selection.
0 = Alpha mode enabled.
1 = Graphics mode (320 by 200) activated.

Bit 0

(40 by 25) or (80 by 25) Text Mode Selection.
0 = 40 by 25 alpha mode enabled.
1 = 80 by 25 alpha mode activated.

5.9.6 CGA Color Select Register, Write Only Port = 3D9

BIT	FUNCTION
7, 6	Reserved
5	Graphics Mode Color Set
4	Alternate Color Set
3	Border Intensity
2	Red Border
1	Green Border
0	Blue Border

Bit (7:6)

Reserved.

Bit 5

320 by 200 Color Set Select for the CGA 2 bits per pixel.
0 = Background, green, red, brown colors.
1 = Background, cyan, magenta, white colors.

Bit 4

Alternate Color Set Enable.
0 = Background color in alpha mode.
1 = Enable alternate color set in graphics mode.

Bit 3

Border Intensity.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric mode.
1 = Selects intensified border color.
320 by 200 Graphics Mode.
1 = Selects intensified background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects red foreground color.

Bit 1

Green Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.
1 = Selects green border color.
320 by 200 Graphics Mode.
1 = Selects green background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects green foreground color.

Bit 0

Blue Border/Background.
Border color select in text modes, and screen background color in 320 by 200 and 640 by 200 graphics mode.

Alphanumeric Mode.
1 = Selects blue border color.
320 by 200 Graphics Mode.
1 = Select blue background and border color (C0 - C1).
640 by 200 Graphics Mode.
1 = Selects blue foreground color.

5.9.7 CRT Status Register, MDA Operation, Read Only Port = 3BA

BIT	FUNCTION
7	VSYNC Inactive
6 - 4	Reserved
3	B/W Video Enabled
2 - 1	Reserved
0	Display Enable Inactive

Bit 7

Vertical Retrace.
0 = Indicates the raster is in vertical retrace mode.
1 = Indicates vertical retrace is inactive (inverted VSYNC if I/O is mapped into 3BX).

Bit (6:4)

Reserved.

Bit 3

B/W Video Status.
0 = B/W Video disabled.
1 = B/W Video enabled.

Bit 2 - Bit 1

Reserved.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking is active; Display Enable is inactive.

5.9.8 CRT Status Register, CGA Operation, Read Only Port = 3DA

BIT	FUNCTION
7 - 4	Reserved
3	VSYNC Active
2	Light Pen Switch Status
1	Light Pen Latch Set
0	Display Enable Inactive

Bit (7:4)

Reserved.

Bit 3

Vertical Retrace.
0 = Indicates vertical retrace is inactive.
1 = Indicates the raster is in vertical retrace mode.

Bit 2

Light Pen Switch Status.
0 = Light pen switch closed.
1 = Light pen switch open.

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Bit 1

Light Pen Latch.
0 = Light pen latch cleared.
1 = Light pen latch set.

Bit 0

Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking active; Display Enable is inactive.

5.9.9 AT&T/M24 Register, Write Only Port = 3DE

This is a write only, 8-bit register located at address 3DE. It is used to control the 640 by 400 AT&T graphics mode. All bits are set to 0 by reset. This register is enabled by setting Bit 7 in PR Register 2 (PR2).

BIT	FUNCTION
7	Reserved
6	White/Blue Underline
5, 4	Reserved
3	Memory Map Display
2	Character Set Select
1	Reserved
0	AT&T Mode Enable

Bit 7

Reserved.

Bit 6

White/Blue Underline.
Defines underline attribute according to the MDA display requirements.
0 = Underline attribute selects blue foreground in-color text modes.
1 = Underline attribute selects white underlined foreground.

Bit (5:4)

Reserved.

Bit 3

Page Select.
Selects between one or two 16 Kbyte RAM page for display in 200 line graphics mode.
0 = Display memory address starts at B800:0H (16 Kbyte length).
1 = Display memory address starts at BC00:0H (16 Kbyte length).

Bit 2

Character Set Select.
Selects between two character font planes.
0 = Standard character font from plane 2.
1 = Alternate character font from plane 3.

Bit 1

Reserved.

Bit 0

M24 or Non-IBM Graphics Mode. 400 line mode.
A 400 line monitor is required for this mode.
0 = 200 line graphics mode active, using paired lines.
1 = AT&T mode enabled for 400 line graphics.

5.10 WD90C20 PR REGISTERS

NAME	RW [1]	DESIGNATION[2]	I/O LOCATION[3]	SECTION
Address Offset A	RW	PR0A(6:0)	3CF.09	5.10.1
Alternate Address Offset B	RW	PR0B(6:0)	3CF.0A	5.10.1
Memory Size	RW	PR1(7:0)	3CF.0B	5.10.2
Video Select	RW	PR2(7:0)	3CF.0C	5.10.3
CRT Control and Group Locking	RW	PR3(7:0)	3CF.0D	5.10.4
Video Control	RW	PR4(7:0)	3CF.0E	5.10.5
Unlock PR0-PR4	RW	PR5(7:0)	3CF.0F	5.10.6
Unlock PR11 - PR17	RW	PR10(7:0)	3?5.29[4]	5.10.7
EGA Switches	RW	PR11(7:0)	3?5.2A	5.10.8
Scratch Pad	RW	PR12(7:0)	3?5.2B	5.10.9
Interlace H/2 Start	RW	PR13(7:0)	3?5.2C	5.10.10
Interlace H/2 End	RW	PR14(7:0)	3?5.2D	5.10.11
Miscellaneous Control 1	RW	PR15(7:0)	3?5.2E	5.10.12
Miscellaneous Control 2	RW	PR16(7:0)	3?5.2F	5.10.13
Miscellaneous Control 3	RW	PR17(1:0)	3?5.30	5.10.14
Flat Panel Status	RW[5,6]	PR18(7:0)	3?5.31	5.10.15
Flat Panel Control I	RW	PR19(7:0)	3?5.32	5.10.16
Flat Panel Control II	RW	PR1A(7:0)	3?5.33	5.10.17
Flat Panel Unlock	RW	PR1B(7:0)	3?5.34	5.10.18
Mapping RAM Unlock	RW	PR30(7:0)	3?5.35	5.10.19
Mapping RAM Address Counter	RW	PR33(7:0)	3?5.38	5.10.20
Mapping RAM Data	RW	PR34(7:0)	3?5.39	5.10.21
Mapping RAM Control	RW[6]	PR35(1:0)	3?5.3A	5.10.22
LCD Panel Height Select	RW	PR36(7:0)	3?5.3B	5.10.23
Flat Panel Blinking Control	RW	PR37(7:0)	3?5.3C	5.10.24
Color LCD Control	RW	PR39(7:0)	3?5.3E	5.10.25
Vertical Expansion Initial Value	RW	PR41(7:0)	3?5.37	5.10.26
PR43 Unlock Register	WO	PR42(7:0)	3C5.06	5.10.27
Paradise VGA Status	RW	PR43(7:0)	3C5.07	5.10.28
Power-Down Memory Refresh	RW	PR44(7:0)	3?5.3F	5.10.29
CNF Configuration	HARD[6]	–	–	5.13

TABLE 5-4. PR REGISTERS SUMMARY

NOTES:
1. RO = Read-Only, WO = Write-Only, RW = Read/Write.
2. In the PR register notation, XXX.YY, XXX is the data port address and YY is the register index.
3. All register addresses are in hex.
4. The designation 3?5 means that the register is mapped into either 3B5 in monochrome mode or 3D5 in color modes.
5. The register bits (1:0) are loaded as CNF (10:9) upon reset.
6. Not all bits are readable.

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The WD90C20 has additional features that enhance the performance and function of the Western Digital Imaging WD90C00 and basic VGA subsystem.

The registers are at the I/O locations unused by IBM. All registers are read/write, except where noted.

Registers PR0 through PR4 and PR11 through PR17 are normally locked. They are write-protected at power-up by the hardware reset. In order to load these registers, the appropriate unlock register, PR5 or PR10, must be loaded first with binary XXXXX101; the register remains unlocked until any other value is written to it. Registers PR0 through PR5 are readable only if PR4 Bit 1 = 0. Registers PR10 through PR17 are read protected at power-up by hardware reset. To read registers PR10 through PR17, load PR10 with 1XXX0XXX. The registers remain readable until any other value is written to PR10. When registers PR10 through PR17 are read protected, reading them shows data to be FFH. Setting PR4 Bit 1 to 1 does not read protect registers PR10 through PR17. All PR registers are set to 0 at power-on reset except where noted.

5.10.1 Address Offset Registers, PR0A & PR0B

PR0A - Address Offset Register A, Read/Write Port = 3CF, Index = 09

BIT	FUNCTION
7	Reserved
6 - 0	Primary Address Offset Bits

PR0B - Address Offset Register B, Read/Write Port = 3CF, Index = 0A

BIT	FUNCTION
7	Reserved
6 - 0	Alternate Address Offset Bits

The WD90C20 can control up to 1 Mbyte of video RAM. However, the memory map for IBM PC and compatibles assigns 128 Kbytes of the available 1 Mbyte total system space to the video controller. Therefore, the video memory space starts at A000:0H and ends at BFFF:FH. This space is further limited to a 64 Kbyte video memory partition to allow a second video card to co-exist.

The WD90C20 has two offset registers that help address 512 Kbytes of linear addressed memory. These are PR0A and PR0B. These registers contain an offset which gets added to the system address when accessing more than 64 Kbytes of video memory. Address offset register PR0A is the primary address offset register and is always enabled. Alternatively, Address offset register PR0B is enabled only if PR1 Bit 3 is set to 1. PR0A and PR0B provide a 7-bit offset that is added to address Bits A (18:12) of the system address to form a 20-bit address. The arrangement is similar to that of the segment register DS and ES of the 8088/80X86 architecture, with PR0A and PR0B providing 4 Kbyte segments.

In a 64 Kbyte VGA address space (as defined by Graphics Miscellaneous Register Bits 3 and 2), when PR0B is enabled by setting PR1 Bit 3 = 1, PR address offset registers, PR0A and Alternate Offset Address register (PR0B), may be used to access two 32 Kbyte video RAM windows. PR0A window is mapped from A800:0H–AFFF:FH while PR0B is mapped from A000:0H–A7FF:FH.

When there is a 128 Kbyte address space (as defined by Graphics Miscellaneous Register Bits 3 and 2) and the Alternate Offset register is enabled, PR0A is mapped from B000:0H-BFFF:FH, while PR0B is mapped from A000:0H-AFFF:FH.

5.10.2 PR1 - Memory Size, Read/write Port = 3CF, Index = 0BH

BIT	FUNCTION
7, 6	Memory Size Select
5, 4	Memory Map Select
3	Enable Alternate Address Offset Register PROB
2	16-Bit Video Memory
1	Reserved
0	BIOS ROM Map Out

This register is eight bits wide. Bits PR1 (1:0) are latched internally at power-on reset from the corresponding memory data bus pins MD(1:0), using either pull-up or pull-down external resistors. Pull-up resistors on MD(1:0) cause PR1(1:0) bits to be latched low.

Bits 7, 6
Memory Size.

256 Kbyte of available VGA video memory space is divided into four 64 Kbyte maps (0-3), each defining bit planes (0-3). In mode 13, the 4-bit planes are chained to form one large bit plane. The starting address of the 256 Kbyte video memory buffer can be configured to match other video adapters and/or application programs. WD90C20 enhances memory size capability when Bits 6 and 7 are programmed to extend video buffer size to 512 Kbyte or 1024 Kbyte.

DRAMS	MA8 PIN	VIDEO SPACE	MEMORY PLANES
64 Kbyte by 4	N/U	256 Kbyte	4 (64 Kbyte Per Plane)
64 Kbyte by 4	BANK SELECT	512 Kbyte	4 (128 Kbyte Per Plane)
256 Kbyte by 4	DRAM PIN A8	1024 Kbyte	4 (256 Kbyte Per Plane)

The DRAM organizations supported by the WD90C20 and its associated video space are shown in the table at the bottom of the page.

When video memory size is 512 Kbyte, and 64 Kbyte by 4 DRAMs are used, two banks of 64 Kbyte form 128 Kbyte per plane. MA8 provides the bank selection using an external multiplexer to access the appropriate bank in a plane by multiplexing the CAS10N and CAS32N signals. Four planes form the desired 512 Kbyte video memory space. For 1024 Kbyte video memory size, MA8 is directly connected to the A8 address pin of the 256 Kbyte by 4 DRAMS, and two DRAMS form a 256 Kbyte space per plane. Four planes make the desired 1024 Kbyte video memory space.

PR1 Bits 7 and 6 must be set to reflect the amount of memory installed. These bits in conjunction with PR16(1) also select the way memory is mapped into the system address space. If PR16(1) is set to 1, the memory mapping is the same as IBM VGA regardless of PR1 (6) and PR1(7)

BIT7	BIT6	PR16(1)	MEMORY SIZE	MAPPING
0	0	0	256 Kbyte Standard VGA	VGA*
0	1	0	256 Kbyte WDI VGA	PVGA**
1	0	0	512 Kbyte WDI VGA	PVGA
1	1	0	1024 Kbyte WDI VGA	PVGA
X	X	1	Any Of The Above	VGA*

NOTE:
* Only 64 Kbytes are accessible for chained 4 packed pixel mode.
**WDI extended modes can fully utilize up to 256 Kbytes.

RAM ADDRESSING:
PR1(7) PR1(6)
0 0 256 Kbyte Total; 64 Kbyte Plane; IBM VGA Memory Organization

VIDEO RAM ADDRESS BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	0	0	0	0	0	0
MA(16) *	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
–	–	–	–	–	–	–
–	–	–	–	–	–	–
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(15)	CA(13)
MA(0)	A(0)	CA(0)	A(16) or XRN(50)	CA(15) or CA(13)	A(14)	CA(12)

RAM ADDRESSING:
PR1(7) PR1(6)
0 1 256 Kbyte Total; 64 Kbyte Plane; WD90C20 Memory Organization

VIDEO RAM ADDRESS BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	0	0	0	0	0	0
MA(16) *	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
–	–	–	–	–	–	–
–	–	–	–	–	–	–
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

RAM ADDRESSING:
PR1(7) PR1(6)

1 0 512 Kbyte Total; 128 Kbyte/Plane; WD90C20 Memory Organization

VIDEO RAM ADDRESS BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	0	0	0	0	0	0
MA(16) *	A(16)*	CA(16)*	A(17)*	CA(16)*	A(18)*	CA(16)*
*						
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
–	–	–	–	–	–	–
–	–	–	–	–	–	–
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

RAM ADDRESSING:
PR1(7) PR1(6)

1 1 1024 Kbyte Total In 4 Planes; 256 Kbyte/Plane; WD90C20 Memory Organization

VIDEO RAM ADDRESS BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	A(17)	CA(17)	A(17)	CA(16)	A(17)	CA(15)
MA(16) *	A(16)	CA(16)	A(16)	CA(15)	A(16)	CA(14)
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
–	–	–	–	–	–	–
–	–	–	–	–	–	–
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(19)	CA(17)
MA(0)	A(0)	CA(0)	A(18)	CA(17)	A(18)	CA(16)

NOTES:
1. A(19:0) are WD90C00 internally modified system Addresses.
2. CA(17:0) are CRT Controller Character Address Counter Bits.
3. XRN(5) is Miscellaneous Output Register 3C2H, inverted bit 5. This bit selects the displayed page in chained modes. XRN(5) is selected as MA(0) if Graphics Register 6 Bit 3 or Bit 2 = 1.
4. CA(13) is selected as MA(0) if CRTC Mode Register 17 Bit 5 = 0.

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BIT 5	BIT 4	MEMORY MAP
0	0	VGA Mapping in 64 Kbyte space - A000:0H to BFFF:FH Address Range
0	1	First 256 Kbyte in 1 Mbyte space - 0000:0H to 3FFF:FH Address Range
1	0	First 512 Kbyte in 1 Mbyte space - 0000:0H to 7FFF:FH Address Range
1	1	First 1024 Kbyte in greater or equal to 1 Mbyte space - 0000:0H to FFFF:FH Address Range

Bit 3

Enable Alternate Address Offset Register PR0B.

Bit 2

Enable 16-Bit Bus for Video Memory.
When set to 1, DS16N will be active low in text modes and packed pixel modes such as mode 13h. Planar graphics modes will always have $\overline{DS16}$ inactive.

Bit 1

Reserved. Set to 0.

Bit 0

If set to 1 the BIOS ROM is mapped out. A pull-up resistor latches 0 after power-up. A pull-up on MD(0) sets this bit to 0 at power-on reset.

5.10.3 PR2-Video Select Register, Read/Write Port = 3CF, Index = 0CH

BIT	FUNCTION
7	AT&T/M24 Mode Enable
6	6845 Compatibility
5	Character Map Select
4, 3	Character Clock Period Control
2	Underline/Character Map
1	Third Clock Select Line VCLK2
0	Force VCLK (overrides SEQ1 bit 3)

Bit 7

Enable AT&T/M24 Register and Mode.

Bit 6

0: VGA or EGA mode.
1: Non-VGA (6845) mode.

Bit 5

Character Map Select.
The following functions are overridden by setting PR15(2). This bit, in conjunction with PR2(2) and Bit 3 of the attribute code, enables character maps from planes 2 or 3 to be selected according to the table below:

PR2(5)	PR2(2)	ATT(4)	PLANE SELECT
0	0	X	2
0	1	X	2
1	0	X	3
1	1	0	2
1	1	1	3

NOTE: Setting PR15(2) = 1, i.e., selecting "page mode addressing" overrides the "plane selected" table shown above.

Bit(4:3)

Character Clock Period Control.

0	0	IBM VGA character clock (8 or 9 dots)
0	1	7 dots (used for 132 character mode)
1	0	9 dots
1	1	10 dots

Selecting 10 dots per character modifies the function of the horizontal PEL Panning register (3C0.13). Pixel panning in the 10 dot-character modes is obtained by storing the following values into the horizontal PEL Panning register.

PEL PANNING REGISTER VALUE	PELS SHIFTED LEFT
09	0
08	1
00	2
01	3
02	4
03	5
04	6
05	7
06	8
07	9

NOTE: The character clock period control functions have no effect in graphics modes.

Bit 2

Underline and Character Map Select.
Setting this bit to 1 enables underline for all odd values of attribute codes, e.g., Programming 1 gives blue underline. It overrides the background color function of the attribute code Bit 3, which is forced to 0. Therefore, only eight choices of background colors are available. This function allows trading background colors for more character maps. In conjunction with PR2(5), this bit is also decoded to enable character maps from planes 2 or 3. See PR2(5) for details.

Bit 1

This bit is the third clock select line VCLK2 which is sent to the external clock chip if CNF(3) is set to 1. When CNF(3) is set to 0, setting this bit locks the internal video clock select multiplexer.

Bit 0

Forces horizontal sync timing clock of the CRTC to VCLK. Uses VCLK when sequencer register 1 bit 3 is set for VCLK/2. This is for compatibility modes that require locking the CRTC timing parameters.

5.10.4 PR3 - CRT Lock Control Register, Read/Write Port=3CF, Index = 0DH

BIT	FUNCTION
7	Lock VSYNC Polarity
6	Lock HSYNC Polarity
5	Lock Horizontal Timing
4	Bit 9 Control
3	Bit 8 Control
2	CRT Control
1	Lock Prevention
0	Lock Vertical Timing

Register locking is controlled by 4 bits. They are PR3 (5,1,0) and 3?5.11(7) (i.e., the IBM Vertical Retrace End Register Bit 7 controlled by index register 11). When Bit 7 is 1, CRT controller registers (R0-7) are write protected by VGA definition. Information on the five groups, and their locking schemes, is provided below.

- **Group 0**

These registers are locked if PR3(5)=1 OR 3?5.11(7)=1.
CRT Controller Register 00
–Horizontal Total Characters per scan
CRT Controller Register 01
–Horizontal Display Enable End
CRT Controller Register 02
–Start Horizontal Blanking
CRT Controller Register 03
–End Horizontal Blanking
CRT Controller Register 04
–Start Horizontal Retrace
CRT Controller Register 05
–End Horizontal Retrace

- **Group 1**

These registers are locked if PR3(1)=0 AND 3?5.11(7)=1.
CRT Controller Register 07(Bit6)
–Vert. Display Enable End bit 9
CRT Controller Register 07(Bit1)
–Vert. Display Enable End bit 8

- **Group 2**

These registers are locked if PR3(0)=1 OR 3?5.11(7)=1.
CRT Controller Register 06
– Vertical Total
CRT Controller Register 07(Bit7)
–Vertical Retrace Start bit 9
CRT Controller Register 07(Bit5)
–Vertical Total bit 9
CRT Controller Register 07(Bit3)
–Start Vertical Blank bit 8
CRT Controller Register 07(Bit2)
–Vertical Retrace Start bit 8
CRT Controller Register 07(Bit0)
–Vertical Total bit 8

- **Group 3**

These registers are locked if PR3(0)=1.
CRT Controller Register 09(Bit5)
–Start Vertical Blank bit 9
CRT Controller Register 10
–Vertical Retrace Start
CRT Controller Register 11 [Bits(3:0)]
–Vertical Retrace End
CRT Controller Register 15
–Start Vertical Blanking
CRT Controller Register 16
–End Vertical Blanking

- **Group 4**

This register is locked if PR3(5)=1.
CRTC mode Control Register 17(Bit2)
–Selects divide by two vertical timing

Bit7

Lock VSYNC polarity, as programmed in 3C2 Bit 7.

Bit 6

Lock HSYNC polarity, as programmed in 3C2 Bit 6.

Bit 5

Lock Horizontal Timing.
Locks CRTC registers of Group 0 and 4.
Prevents attempt by applications software to unlock Group 0 registers by setting 3?5.11 Bit 7=0

Bit 4

Bit 9 of CRT Controller Start Memory Address High Register 3?5.0C, and Bit 9 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (17).

Bit 3

Bit 8 of CRT Controller Start Memory Address High Register 3?5.0C, and Bit 8 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (16).

Bit 2

Cursor start, stop, preset row scan, and maximum scan line address register values multiplied by two.

Bit 1

1 = Prevents attempt by applications software to lock registers of Group 1 by its setting 3?5.11 Bit 7=1.

Bit 0

Lock Vertical Timing.
1 = Locks CRTC registers of Groups 2 and 3. Overrides attempt by applications software to unlock Group 2 registers by its setting 3?5.11 Bit 7=0.

5.10.5 PR4- Video Control Register, Read/Write Port=3CF, Index = 0EH

The video monitor output control register (PR4) can be programmed to tri-state the CRT display control outputs as well as video data for the RAM-DAC, and memory control outputs.

BIT	FUNCTION
7	$\overline{\text{BLNK}}$ / Display Enable
6	PCLK=VCLK
5	Tri-state Video Outputs
4	Tri-state Memory Control Outputs
3	Override CGA Enable Video Bit
2	Lock Internal Palette and Overscan Registers
1	EGA Compatibility
0	Ext 256 color Shift Register Control

Bit 7

This bit controls the output signal $\overline{\text{BLNK}}$.
Normally in the VGA mode, $\overline{\text{BLNK}}$ is used by the external video DAC to generate blanking. If this bit = 1, the $\overline{\text{BLNK}}$ output supplies a display enable signal. One of two types of display enable timings can be selected; the choice is determined by PR15(1).

Bit 6

Select PCLK Equal to VCLK.
0 = PCLK is the inverted internal video dot clock, or half the dot clock frequency, depending upon the video mode.
1 = PCLK is always the non-inverted VCLK input clock.

Bit 5

Tri-state the outputs VID(7:0), HSYNC, VSYNC, and $\overline{\text{BLNK}}$.

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Bit 4

Tri-state the Memory Control Outputs.
The memory address bus, MA(8:0), and all ten DRAM control signals, are tri-stated when this bit is set to 1.

Bit 3

Overrides the CGA "enable video" Bit 3 of mode register 3D8, only in 80 by 25 alpha CGA (Non-VGA) mode. Override effectively forces this bit to 1. Power-on-reset causes no override.

Bit 2

Lock Internal Palette and Overscan Registers.

Bit 1

EGA compatibility bit where 1 = EGA Compatible Mode. It disables reads to all registers which are write-only registers in the IBM EGA. Also, registers at 3CO/3C1 change to write-only mode if the EGA compatibility bit is set. In addition to selecting EGA compatibility bit, setting this bit to 1 disables reading PR0-PR5. In VGA mode (PR(4) Bit 1 is 0) 3C0 register is read/write while 3C1 register is read only, according to the Attribute Controller register definitions.

Bit 0

Shift Register Control.
This bit configures the video shift registers for 256-color mode.

5.10.6 PR5 - General Purpose Status Bits Read/Write Port=3CF, Index = 0FH

BIT	FUNCTION
7	Read CNF(7) Status
6	Read CNF(6) Status
5	Read CNF(5) Status
4	Read CNF(4) Status
3	Read CNF(8) Status
2	PR0-PR4 Unlock
1	PR0-PR4 Unlock
0	PR0-PR4 Unlock

Bits (2:0) are READ/WRITE bits and cleared to 0 by reset. They provide lock or unlock capability for PR registers PR0 through PR4 like the PVGA1A. The PR0 through PR4 registers are unlocked when "X5Hex" is written to PR5. They remain unlocked until any other value is written to PR5. This register also provides readable status for the configuration register Bits 4 through 8. Setting PR(4) Bit 1 to 1 read protects registers PR0 through PR5.

BIT	FUNCTION
7	CNF(7) [READ ONLY]
6	CNF(6) [READ ONLY]
5	CNF(5) [READ ONLY]
4	CNF(4) [READ ONLY]
3	CNF(8) [READ ONLY]

Bits (2:0)

READ/WRITE bits are cleared to 0 by reset. They control writing to PR registers PR0 through PR4 as follows:

2	1	0	PR0-PR4
0	X	X	Write Protected
X	1	X	Write Protected
X	X	0	Write Protected

5.10.7 PR10 Unlock PR11-PR17
Read/Write Port = 3?5, Index = 29H

This register is READ/WRITE and cleared to 0 by reset. PR10 can only be read if it has 1XXX0XXX. Bits (7,3), Bits (6:4), and Bits (2:0) control access to PR registers PR10 through PR17. Bits 7 and 3 enable register read operation for PR10 through PR17. Bits (6:4) may be used as scratch pad. Bits (2:0) enable register write operation for PR11 through PR17.

BIT	FUNCTION
7	PR10-PR17 - Read Enable Bit 1
6 - 4	PR10(6:4) - Scratch Pad
3	PR10-PR17 - Read Enable Bit 0
2 - 0	PR11-PR17 - Write Enable

BIT7	BIT3	PR10-PR17
0	X	Read protected, read back data FFH
X	1	Read protected, read back data FFH
1	0	Read Enabled

BIT2	BIT1	BIT0	PR11-PR17
0	X	X	Write Protected
X	1	X	Write Protected
X	X	0	Write Protected
1	0	1	Write Enabled

BIT6	BIT5	BIT4	PR10(6:4)
0	X	X	Scratch pad
X	1	X	Scratch pad
X	X	0	Scratch pad
1	0	1	Reserved for Manufacturing Test

5.10.8 PR11 EGA Switches
Read/Write Port = 3?5, Index = 2AH

The EGA switch configuration details are stored in the PR11 register bits.

BIT	FUNCTION
7	EGASW4
6	EGASW3
5	EGASW2
4	EGASW1
3	EGA Emulation on Analog Display
2	Lock Clock Select
1	Lock Graphics and Sequencer Screen Control
0	Lock 8/9 Character Clock

Bits (7:4)

EGA configuration switches SW4-SW1. These bits are READ/WRITE and latched internally at power-on-reset from corresponding memory data bus pins MD(15:12), provided with either pull-up or pull-down external resistors. PULLING UP MD(15:12) causes PR11(7:4) to be latched HIGH. These bits can be read as bit 4 of port 3C2 if the EGA compatibility bit [PR4(1)] has been set to 1. Selection of the bit to be read is determined by Bits 3 and 2 of the Miscellaneous Output Register 3C2, as follows.

WRITE 3C2 bit 3	WRITE 3C2 bit 2	READ 3C2 bit 4
0	0	PR11(7) [=EGA SW4]
0	1	PR11(6) [=EGA SW3]
1	0	PR11(5) [=EGA SW2]
1	1	PR11(4) [=EGA SW1]

PR11 Bits 3 through 0 are READ/WRITE and cleared to 0 at power on reset.

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Bit 3

Select EGA Emulation on a PS/2 (VGA-compatible analog) display.

Bit 2

Lock Clock Select.
This bit locks the internal video clock select multiplexer and disables loading of an external clock chip through VCLK1.

Bit 1

Lock Graphics Controller/Sequencer Screen Control. Setting PR11(1) to 1 prevents modification of the following bits in the Graphics controller and Sequencer:

Graphics controller	3CF.05 bits (6:5)
Sequencer	3C5.01 bits (5:2)
Sequencer	3C5.03 bits (5:0)

Although the internal functions selected by these graphics controller and sequencer bits are locked by setting PR11 bit 1 to 1, they appear unlocked to the system processor during a read operation.

Bit 0

Lock 8/9 Dots.
Setting this bit to 1 prevents modification of clocking mode sequencer register 3C5.01 Bit 0. Although 8 or 9 character timing is locked by setting PR11 Bit 0 to 1, the 3C5.01 Bit 0 appears unlocked to the system processor during reads.

5.10.9 PR12 Scratch Pad
Read/Write Port = 3?5, Index = 2BH

BIT	FUNCTION
7 - 0	Scratch Pad Bits (7:0)

The data in this register is unaffected by hardware reset and undefined at power-up.

5.10.10 PR13 Interlace H/2 Start
Read/Write Port = 3?5, Index = 2C

BIT	FUNCTION
7 - 0	Interlaced H/2 Start

The data in this register is unaffected by hardware reset and undefined at power-up. This register defines the starting horizontal character count at which vertical timing is clocked on alternate fields in interlaced operation. Interlaced operation is enabled by setting PR14(5) to 1. All other standard non-interlaced modes are unaffected by the contents of this register. This register must be programmed with a value derived from the values chosen to be programmed into the Horizontal Retrace Start Register (3?5.04) and Horizontal Total Register (3?5.00). The equation is as follows:

PR13(7:0) = [HORIZONTAL RETRACE START] - [(HORIZONTAL TOTAL + 5)/2] + HRD

NOTE: HRD = Horizontal Retrace Delay, determined by Bits 6 and 5 of the Horizontal Retrace End Register (3?5.05).

5.10.11 PR14 Interlace H/2 End Read/Write Port = 3?5, Index = 2DH

Bits 4 through 0 are unaffected by hardware reset and undefined at power-up. Bits 7 through 5 are cleared to 0 by reset.

BIT	FUNCTION
7	Enable IRQ
6	Vertical Double Scan for EGA on PS/2 Display
5	Enable Interlaced Mode
4 - 0	Interlaced H/2 Start

Bit 7

Enable IRQ.
This bit may be set to enable CRT interrupts to be generated when configured for AT BUS operation, allowing EGA compatibility support for interrupt-driven EGA applications. For VGA operation with an AT BUS, interrupts are not used, and this bit should be set to 0. This bit should not be set to 1 in Micro Channel operation.

Bit 6

Vertical Double Scan.
This bit should be set to 1 when emulating EGA on a PS/2 display. Setting this bit to 1 causes the CRTC's Vertical Displayed line counter and row scan counter to be clocked by divide-by-two horizontal timing if vertical sync polarity (3C2 Bit 7=0) is programmed to be positive. The relationship between the actual number of lines displayed [N] and the data [n] programmed into the Vertical Display Enable End register is as follows:

$$N=2(n+1)$$

Likewise, the relationship between the actual number of scan lines per character row [N] and the data [n] programmed in the maximum Scan Line register holds true.

Bit 5

Interlaced Mode.
Setting this bit to 1 selects interlaced mode. Interlaced mode can be used in video modes in which the data programmed into the Maximum Scan Line Address register [3?5.09] = 0XX00000.
Line compare and double scan are not supported.

Bits (4:0)

Interlaced H/2 End Bits (4:0).
Add the contents of the Interlaced H/2 Start Register PR(13) to the horizontal sync width (same as defined by 3X5.04,05). Program 5 LSB of the sum into these bit locations.

5.10.12 PR15 Miscellaneous Control 1 Read/Write Port = 3?5, Index = 2EH

BIT	FUNCTION
7	Read 46E8 Enable
6	Low VCLK
5	VCLK1,VCLK2 Latched Outputs
4	VCLK = MCLK
3	8514/A Interlaced Compatibility
2	Enable Page Mode
1	Select Display Enable
0	Disable Border

Bit 7

Enable Reading Port 46E8H.
This bit is functional only if AT BUS architecture [CNF(2)=1] is selected. Setting this bit to 1 enables I/O port 46E8H to be read, regardless of the state of its own bits 3 and 4 and of port 102 bit 0 (sleep bit). Only bits (4:0) of port 46E8H are readable; bits (7:5) are 0.

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Bit 6

Low VCLK.
Setting this bit to 1 adjusts the memory timing to allow use of a video clock (VCLK) frequency which is much lower than the memory clock (MCLK) frequency. This bit should be set to 1 if the following expression is satisfied:

(MCLK in MHZ) / (VCLK in MHZ) >2

Bit 5

Latched VCLK1 and VCLK2.
This bit is used only if CNF(3) = 1 (which configures the VCLK1 and VCLK2 pins as outputs). Setting this bit to 1 causes outputs VCLK1 and VCLK2 to equal Bits 2 and 3 of I/O write register (Miscellaneous output register) at 3C2H, respectively.

Bit 4

Select MCLK as Video Clock.
Setting this bit to 1 causes the MCLK input to be selected for the source of all video timing. The other three VCLK inputs cannot be selected when this bit is set.

Bit 3

Interlaced Compatibility.
This bit should be used only if interlaced mode is selected (see PR14). This bit should be set to 1 if exact timing emulation of the IBM 8514/A's interlaced video timing is required. Setting this bit to 1 causes vertical sync to be generated from the trailing edge of non-skewed horizontal sync, instead of leading edge, as generated for VGA timing.

Setting this bit to 1 also removes two VCLK delays from the default VGA video dot path delay chain.

Bit 2

Select Page Mode Addressing.
Setting this bit to 1 forces screen refresh memory read cycles to use page mode addressing in alpha modes. Page mode addressing is automatically used in the graphics modes. Page mode addressing requires less time than RAS-CAS addressing; therefore, selecting page mode addressing increases the bandwidth for the CPU to access video memory (by 30-40%). Set this bit to 1 if 132 character mode timing is selected (see description of PR2). Setting this bit to any alpha mode overrides the character map select functions of PR2(2) and PR2(5). When this bit is set to 1, it redefines the Character Map Select Register (3C5.03). One of eight, 8 Kbyte memory segments containing a pair of maps in Plane 2 or Plane 3 is addressed by bits (2:0) of this register, while the map selection is determined by the bits (4:3). A pair of adjacent 8 Kbyte character maps in planes 2 and 3 (adjacent in the sense that they have the same addressing), may be selected by Bit 3 of the attribute code.

The Character attribute Bit 3, in conjunction with bits 3 and 4 of the Character Map Select register (3C5.03), determine a character map from either Plane 2 or Plane 3 as shown by the table below.

3C5.03 BIT4	3C5.03 BIT 3	ATT BIT3	PLANE SELECT
0	0	X	2
1	1	X	3
1	0	0	2
1	0	1	3
0	1	0	3
0	1	1	2

NOTE: The above Character Map Select functions override the functions of PR2(5) and PR2(2).

This bit must be set to 1 before loading the character maps into the video DRAM, because the addressing of the page mode character maps differs from the addressing of the default, non-page mode. However, setting this bit to 1 internally redirects all necessary addressing to make loading the character maps the same, whether in page mode or non-page mode.

Bit 1

Display Enable Timing Select.
This bit is used to choose between two types of Display Enable timings available at output pin BLNKN if PR4(7)=1. If PR4(7)=0, this bit has no effect.

0= BLNKN supplies Pre-Display Enable. Pre-Display Enable timing precedes active video by one dot clock.

1 = BLNKN supplies Display Enable. The display enable timing coincides with active video timing.

Bit 0

Disable Border.
Setting this bit to 1 forces the video outputs to 0 during the interval when border (overscan) color would be active.

5.10.13 PR16 Miscellaneous Control 2 Read/Write Port = 3?5, Index = 2FH

BIT	FUNCTION
7	External Register 46E8H Lock
6	CRTC Address Count Width Bit 1
5	CRTC Address Count Width Bit 0
4	CRTC Address Counter Offset Bit 1
3	CRTC Address Counter Offset Bit 0
2	Enable Odd/Even Page Bit
1	VGA Mapping Enable
0	Lock RAMDAC Write Strobe

Bit (7)

Lock External 46E8H Register.
Setting this bit to 1 causes EBROMN output to be forced high (inactive) during I/O writes to port 46E8H. This bit has no effect on loading the internal port 46E8H.

Bit (6:5)

CRTC Address Counter Width.
Power-on-reset clears these bits to 0. These two bits determine the modulus of the CRT controller's address counter, allowing its count width to be limited to 64 Kbyte or 128 Kbyte locations (Byte, Word, Double word). These bits may be used in virtual VGA applications containing 512 Kbyte or 1024 Kbyte of video memory in which the CRT controller is limited to only 64 Kbyte or 128 Kbyte locations. Bit PR16(6) should be set to 1 to ensure that the VGA and EGA compatible operation of the address counter is limited to 64 Kbyte locations. The following table shows details:

PR16(6)	PR16(5)	COUNT WIDTH
0	0	256 Kbyte
0	1	128 Kbyte
1	X	64 Kbyte

Bit (4:3)

CRTC Address Counter Offset.
Bits 4 and 3 are summed with the CRT Controller's Address Counter bits CA(17) and CA(16), respectively. The 2-bit result defines the starting location of the displayed video buffer at one of the four 64 Kbyte boundaries.

Bit 2

Enable Page Bit for Odd/Even.
This bit affects addressing of memory by the system processor, if chain 2 (Odd/Even) has been selected by setting 3CF.06(1) to 1, setting 3C5.04(1) to 1, selecting extended memory, and setting 3C5.04(3) to 0 to deselect chain 4 addressing. It enables the "Page Bit for Odd/Even" [3C2(5)] to select between two pages of memory, by controlling video RAM address 0, regardless of the Memory Size bits PR1(7:6).

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Bit 1

VGA Memory Mapping.
Setting this bit to 1 selects 256 Kbyte IBM VGA Mapping, regardless of the Memory Size bits PR1(7:6).

Bit 0

Lock RAMDAC Write Strobe (3C6H - 3C9H).
Programming this bit to 1 causes output WPLTN to be forced to 1, disabling I/O writes to the video DAC registers. The DAC state register, located inside the WD90C20, is also protected from the modification but may still be read at the port 3C7h. For normal operation, program this bit to 0.

5.10.14 PR17 Miscellaneous Control 3 Read/Write Port = 3?5, Index = 30

This 2-bit register can be loaded only if PR10 (3?5.29) contains XXXXX101. It can be read only if PR10 contains 1XXX0XXX, and if both PR1B (7:5) is not 101 and PR30 (6:4) is not 011.

BIT	FUNCTION
(7:2)	Reserved
1	MDA Compatibility
0	Map Out 2 Kbyte From BIOS ROM

Bit (7:2)

Reserved.

Bit 1

MDA Compatibility Enable Bit.
Setting this bit to 1 enables MDA compatibility which will:

1. Disable I/O write to Hercules register 3BF.
2. Force Bit 7 of 3BA to 1.
3. Select underline decode of attribute XXXXX001 (if this bit is 0, underline decode is X000X001).

Reset sets this bit to 0.

Bit 0

Map Out 2 Kbyte of BIOS ROM.
Setting this bit to 1 disables access of the BIOS ROM in the system address range C6000H – C67FFH. Power-on-reset sets this bit to 1. Clearing this bit to 0 enables access to all 32 Kbyte addresses of the BIOS ROM from CC000H – C7FFFH.

5.10.15 PR18 Flat Panel Status Register Read Write Port = 3?5, Index = 31

Bit 7

DAC shut-off.
0 = the built-in DAC is enabled as normal.
1 = the built-in DAC is forced off.
(This bit is used for the WD90C20A only)

Bit 6

Reserved.

Bit 5

Reserved.

Bit 4 (WD90C20A)*

Enable Reverse Video in Flat Panel Mode.
This bit controls reverse video in text mode and normal video in graphics mode and is used to reverse the polarity of the video output data UD(3:0) and LD (3:0).

– For WD90C20A:
If PR18 (4) = 0, then only normal video displayed.
If PR18 (4) = 1 and PR39 (3) = 0, then reverse video is displayed in both text and graphics modes.
If PR18 (4) = 1 and PR39 (3) = 1, then reverse video is displayed only in text mode, while normal video is displayed in graphics mode.

PR39 (3)	PR18 (4)	TEXT	GRAPHICS
X	0	Normal	Normal
0	1	Reverse	Reverse
1	1	Reverse	Normal

x=don't care
* This feature is not available for WD90C20

Bit 3

Reserved.

Bit 2

TFT Color LCD Select.
This bit is not readable.
0 = Disable TFT type color LCD panel interface.
1 = Enable TFT type color LCD panel interface.

Bit(1:0)

Panel Select Bit 1 and Bit 0.
These two bits are used to select different sets of parameters which will be loaded into the CRT controller. The parameters should be locked after loading.

PSB (1)	PSB(0)	PANEL TYPE
0	0	Dual Panel LCD Display
1	0	EL Display
1	1	Single Panel LCD Display

5.10.16 PR19 Flat Panel Control Register, Read/Write Port = 3?5, Index 32

BIT	FUNCTION
7	Reserved
6	FP Timing Select
5	CRT Display Enable
4	Flat Panel Display Enable
3	Screen Auto-Centering/Vertical Expansion Select
2	Enable Auto Centering and Vertical Expansion
(1:0)	Adjustment of HSYNC Timing

Bit 7

Reserved.

Bit 6

FP Timing Select.
This bit is used to select two different frame pulse (FP) timings for different LCD panels.
0 = Select ON time during first horizontal line.
1 = Select ON time during second horizontal line.

Bit 5

CRT Display Enable.
This bit enables CRT to be the display device.
0 = Disable CRT display.
1 = Enable CRT display.
NOTE: Upon hardware reset, PR19 (5) =0

PR18(1)	PR18(0)	PR19(5)	PR19(4)	CRT CONTROLLER (TIMING)
0	0	0	1	Based on LCD
0	0	1	0	Based on CRT
0	1	1	0	Based on CRT
1	0	0	1	Based on EL
1	0	1	0	Based on CRT

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Bit 4
Flat Panel Display Enable.
This bit enables the flat panel as the display device.
0 = Disable Flat Panel display.
1 = Enable Flat Panel display.

The WD90C20A supports simultaneous display of both a CRT and single-panel color LCD with vertical expansion and autocentering. The following table shows the LCD/CRT polarity in various modes.

DISPLAY MODE	LBDIR
CRT only	H
Flat panel only	L
Simultaneous display	L

Notes:
1. Upon hardware reset, PR19 (4) = 1
2. When the flat panel display is not enabled, the outputs UD (3:0) and LD (3:0) are active and may be used as the pixel address to drive an external RAMDAC.
3. For simultaneous display of CRT and certain flat panel, set PR19 (5:4) = 11. In this case, the display is locked in 8-dot clock mode and the output -LCD/CRT = 0. The following flat panel may be displayed simultaneously with a CRT: plasma, TFT LCD, and color STN LCD.

Bit 3 (WD90C20A only)*
Screen Autocentering/Vertical Expansion Select.
0 = Autocentering (default).
1 = Reserved for Vertical Expansion (set to 0).
* This feature is not available for WD90C20.

Bit 2

Enable Autocentering and Vertical Expansion.
0 = Disable (default).
1 = Enable.

NOTE: This is used only for pulse wave modulation on the LCD panel.

Bit (1:0) (WD90C20A only)*

Adjustment of HSYNC timing.

PR19(7), PR19(1), and PR19(0) are used to select number of VCLK delays to adjust the HSYNC timing.
* This feature is not available for WD90C20.

PR19(7)	PR19(1)	PR19(0)	NUMBER OF VCLK DELAY
0	0	0	No Delay
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

5.10.17 PR1A Flat Panel Control II Register, Read/Write Port 3?5, Index = 33

BIT	FUNCTION
(7:6)	Select IOCHRDY Release Timing in CPU Memory Read Cycle
(5:4)	Select IOCHRDY Release Timing in CPU Memory Write Cycle
3	Enable CGA Color to Gray Scale Adjustment
2	Shading Method Select
1	Select Number of Memory Refresh Cycles
0	Select Memory Refresh Cycles Control

Bit(7:6)

Select IOCHRDY Release Timing in CPU Memory Read Cycle.

BIT 7	BIT 6	RELEASE TIMING
0	0	1 MCLK before CPU completes read cycle
0	1	2 MCLKs before CPU completes read cycle
1	0	3 MCLKs before CPU completes read cycle
1	1	4 MCLKs before CPU completes read cycle

Bit (5:4)

Select IOCHRDY Release Timing in CPU Memory Write Cycle

BIT 5	BIT 4	RELEASE TIMING
0	0	1 MCLK before CPU completes write cycle
0	1	2 MCLK delay after CPU wins arbitration
1	0	3 MCLK delay after CPU wins arbitration
1	1	4 MCLK delay after CPU wins arbitration

Bit 3

Enable CGA Color to Gray Scale Adjustment.
This bit is used to add adjustment of weighting equation in CGA mode to get 16 different gray scale codes.
0 = Disable.
1 = Enable.

NOTE: For VGA, bit should be set to 0.

Bit 2

Shading Method Select.
0 = Frame rate modulation (default).
1= Pulse width modulation.

Bit 1

Select Number of Memory Refresh Cycles.
0 = Select 1 refresh cycle/horizontal line.
1 = Select 2 refresh cycles/horizontal line.

Bit 0

Select Memory Refresh Cycles Control.
0 = Memory refresh cycles controlled by CRT controller.
1 = Memory refresh cycles controlled by PR1A(1).

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5.10.18 PR1B Flat Panel Unlock Register, Read/Write Port 3?5, Index = 34

This register is used to protect PR18, PR19, PR1A, PR 30, PR36 through PR41, and PR44 from being read from or written into. In order to unprotect (read or write) the above registers, PR1B must be first loaded with 101XXXXX. The above registers remain unprotected until another value is written into PR1B.

PR1B is also used to lock all Shadow registers. To unlock the Shadow registers, PR1B must be loaded first with XXXXX110; all Shadow registers remain unlocked until another value is written to the PR1B register.

In WD90C20A upon hardware reset, PR1B is initialized to 101XX110, and the Shadow registers PR18, PR19, PR1A, PR30, PR36 through PR41, and PR44 are unprotected.

5.10.19 PR30 Mapping RAM Unlock Register, Read/Write Port = 3?5, Index = 35

This register is used to protect mapping RAM registers (PR33 through PR35) from being accessed. In order to read or write to these registers, PR30 must be loaded first with X011XXXX; all mapping RAM registers remain unlocked until another value is written to the PR30 register.

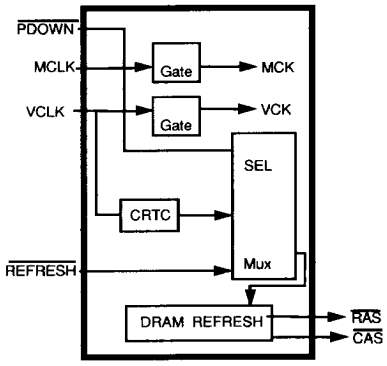
5.10.20 PR33 Mapping RAM Address Counter Register, Read/Write Port = 3?5, Index = 38

This register is used to select the RAM ADDRESS COUNTER register.

NOTE: Any I/O Read or Write to the I/O port 3?5.39H (Mapping RAM Data register) will increment the Mapping RAM Address Counter by one.

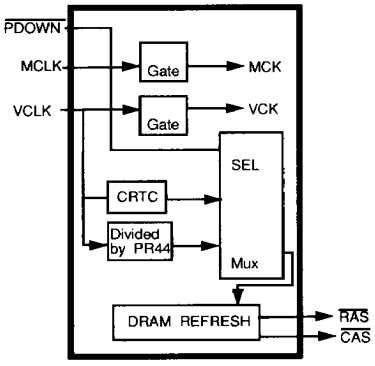
5.10.21 PR34 Mapping RAM Data Register, Read/Write Port = 3?5, Index = 39

This register is used to select the RAM data register for memory read or memory write.



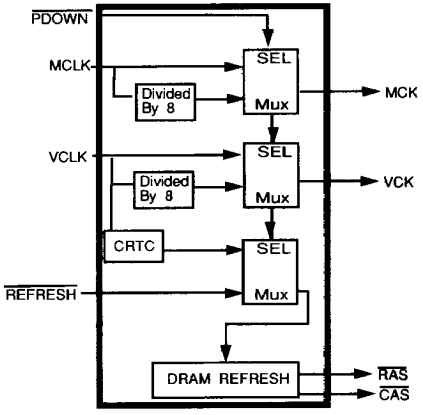
SYSTEM POWER DOWN MODE (SLEEP)

A. RAMDAC is off.
B. Clock inputs are turned off as they enter the chip.
C. CAS before RAS video memory refresh is generated from REFRESH input.
D. Neither video memory or I/O can be accessed in this mode.
E. RAMDAC and Mapping RAM contents are lost and must be reloaded to resume.



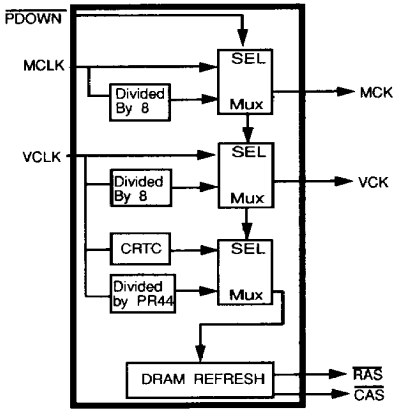
GENERAL POWER DOWN MODE (EXTERNAL CLOCK)

A. RAMDAC is off.
B. MCLK and VCLK are not modified; their speed is reduced by system resources.
C. Refresh cycles triggered by PR44 may be RAS only or CAS before RAS.
D. Video memory and I/O are accessable.



DISPLAY IDLE MODE (SUSPEND/RESUME)

A. RAMDAC is off.
B. MCLK and VCLK are divided by 8.
C. Refresh is CAS before RAS and generated by REFRESH input.
D. I/O is accessable and memory is not accessable.



GENERAL POWER DOWN MODE (INTERNAL CLOCK)

A. RAMDAC is off.
B. MCLK and VCLK are divided by 8.
C. Refresh cycles triggered by PR44 may be RAS only or CAS before RAS. PR44 can be RAS only.
D. Video memory and I/O are accessable.

FIGURE 5-1. SYSTEM POWER DOWN-MODE DISPLAY IDLE MODE

PR44(7)	PR35(7)	PR35(6)	MODE
0	1	X	System Power-Down Mode: MCLK and VCLK are turned off. Video memory refresh is generated from PDREF. Neither memory nor I/O can be accessed. RAMDAC and Mapping RAM must be reloaded.
0	0	X	Display Idle Mode: MCLK and VCLK are divided by 8 before being distributed across the chip. Video memory refresh is generated from PDREF. Only I/O can be accessed.
1	X	0	General Power-Down (External Clock Used): MCLK and VCLK inputs are used to drive the chip . The assumption is made that MCLK and VCLK have been reduced by some other part of the system. The video memory refresh period is readjusted for the slower clock by PR44(6:0). Both memory and I/O can be accessed.
1	X	1	General Power-Down (Internal Clock Used): MCLK and VCLK inputs are divided by 8 before being distributed across the chip. The video memory refresh period is readjusted for the slower clock by PR44(6:0). Both memory and I/O can be accessed.

5.10.22 PR35 Mapping RAM and Power-Down Control Register, Read/Write Port = 3?5, Index = 3A

BIT	FUNCTION
7[1]	Select System Power-Down Mode/Display Idle Mode
6[1]	Select Internal Divided By 8 Clock to Control General Power-Down Mode
5[1]	Host Release Control
4[1]	Reserved; set to 1.
3[1]	Reserved
2[1,2]	Enable $\overline{CAS}$ before $\overline{RAS}$ Memory Refresh Cycle
1	Enable Weighting Equation
0	Reserved; set to 1.

[1] Readable only in WD90C20A when PR30=X011XXXX.

[2] Used in WD90C20A only.

Bit 7

Select System Power-Down Mode/Display Idle Mode. Refer to Figure 5-1. This bit is not readable.

0 = Display idle mode (default).

1 = System power-down mode; MCLK and VCLK turned off.

Bit 6

Select Internal Divided by 8 Clock to Control General Power-Down Mode. This bit is active only when PR44(7) is set at 1. This bit is not readable.

0 = Disable internal clock.

1 = Enable internal clock; clock is divided by 8.

Bit 5

Host Release Control.

This bit is designed to allow another VGA controller in the I/O bus. When PR35(5) is set to 1 and PDOWN input is set to 0, the WD90C20 will not respond to any CPU memory or I/O accesses. All

output buffers of the system interface are turned off (tristate).

There are four power-down modes. The following conditions are true in each powerdown mode.
1. Video memory is maintained.
2. RAMDAC outputs are turned off.
3. Panel outputs are turned off.

Bit 4

Reserved. This bit is set at 1.

Bit 3

Reserved.

Bit 2 (WD90C20A)*

Enable CAS before RAS Memory Refresh Cycle.
0 = $\overline{RAS}$ only refresh cycle (default).
1 = $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
* This bit is used in WD90C20A only.

Bit 1

Enable Weighting Equation.

This bit is used to turn the IBM VGA weighting equation on and off in either color mode or monochrome mode.
0 = Disable weighting equation.
1 = Enable weighting equation.

Bit 0

Reserved. This bit is set at 1.

5.10.23 PR36 Panel Height Select Register, Read/Write Port = 3?5, Index = 3B

This register is loaded with the height, less 1, of a single panel. This information is used to calculate autocentering, vertical expansion, and related values. In a 640 by 480 dual panel display, this register should be loaded with "EF". (480/2)-1 = 239_{10} = EFH. In a 640 by 400 dual panel display, the equation is: (400/2)-1 = 199_{10} = C7H.

5.10.24 PR37 Flat Panel Blinking Control, Read/Write Port = 3?5, Index = 3C

This register is used to select cursor or character blinking rate on flat panels. In CRT mode, this register is ignored.

BIT	2	1	0	CURSOR BLINKING RATE SELECT
	0	0	0	No cursor blinking
	0	0	1	8 frames (8 on, 8 off)
	0	1	0	16 frames (16 on, 16 off)
	0	1	1	32 frames
	1	0	0	64 frames
	1	0	1	128 frames
BIT	**5**	**4**	**3**	**CHARACTER BLINKING RATE SELECT**
	0	0	0	No cursor blinking
	0	0	1	8 frames (8 on, 8 off)
	0	1	0	16 frames (16 on, 16 off)
	0	1	1	32 frames
	1	0	0	64 frames
	1	0	1	128 frames
BIT	**6**			**PLASMA SHIFT CLOCK SELECT**
	0			Select falling edge of the clock to latch data
	1			Select rising edge of the clock to latch data
BIT	**7**			**LCD LP SIGNAL SELECT**
	0			LP will be disabled during vertical blanking period
	1			LP will be generated continuously during vertical blanking period (SCLK will be turned off)

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5.10.25 PR39 Color LCD Control Register, Read/Write Port = 3?5, Index = 3E

This register is used to support color LCD panel.

BIT	FUNCTION
7	Enable Border LP Control
6	Color LCD Panel Border Select
5	Enable Color LCD Panel
4	Micro Channel Interface
3	Enable Reverse Video
2	Enable CRT VSYNC and HSYNC
1	FP Polarity Select
0	LP Polarity Select

Bit 7

Enable Border LP Control.
This bit is used to generate a special LP pulse to latch border information (black or white).
0 = Disable LP border control.
1 = Enable LP border control.

Bit 6

Color LCD Panel Border Select.
0 = Select black border.
1 = Select white border.

Bit 5

Enable Color LCD Panel.
This bit is used to select monochrome LCD or color LCD.
0 = Disable color LCD panel select.
1 = Enable color LCD panel select.

Bit 4

Enable Micro Channel Interface Enhancement.
This bit is used to select Micro Channel interface.
0 = Select default I/O cycle.
1 = Select synchronous-extended I/O cycle.

Bit 3

Enable Reverse Video.
See PR18 (4)

Bit 2 (WD90C20A)*

Enable CRT VSYNC and HYSNC
If PR39 (2) = 0, then LBDIR pin=LBDIR signal and HBDIR pin=HBDIR signal.
* This bit is used in WD90C20A only.

If PR39 (2) = 1, then LBDIR pin=CRT VSYNC signal and HBDIR pin=CRT HSYNC signal.

PR39 (2)	LBDIR	HBDIR
0	LBDIR	HBDIR
1	CRT VSYNC	CRT HSYNC

When the TFT panel is enabled, the polarities of CRT VSYNC and CRT HSYNC are now pulsed low, regardless of the values programmed in the Miscellaneous Output Register Bit 7 and Bit 6 in PR11(3).

Bit 1 (WD90C20A)*

FP Polarity Select.
If PR39 (1) = 0, then FP has normal polarity.
If PR39 (0) = 0, then FP has reverse polarity.
* This bit is used in WD90C20A only.

Bit 0 (WD90C20A)*

LP Polarity Select.
If PR39 (0) = 0, then LP has normal polarity.
If PR39 (0) = 1, then LP has reverse polarity.
* This bit is used in WD90C20A only.

PR39(1)	FP	PR39(0)	LP
0	Normal	0	Normal
1	Reverse	1	Reverse

5.10.26 PR41 Vertical Expansion Initial Value Register, Read/Write Port = 3?5, Index = 37

Reserved.

5.10.27 PR42 – PR43 Unlock Register, Write Only Port = 3C5, Index = 06

This register locks the PR VGA Status register. In order to read/write to the PR VGA status register (PR43), PR42 must be loaded first with X1X01XXX; PR43 will remain unlocked until another value is written to PR42.

5.10.28 PR43 PR VGA Status Register, Read/Write Port = 3C5, Index = 07

This register is used to indicate the current status of the PR VGA chip and to enhance programming compatibility.

BIT	FUNCTION
(7:4)	Read/Write Scratch Pad Bits
3	Color/Monochrome Emulation Status
2	Mode Type
1	EGA Compatibility Set
0	Display Type

Bit(7:4)

Read/Write Sctatch Pad Bits.
These four bits are available for temporary data storage.

Bit 3

Color/Monochrome Emulation Status.
Read only, Bit 0, of Miscellaneous Output register (3C2).
0 = Monochrome emulation is enabled.
1 = Color graphic emulation is enabled.

Bit 2

Mode Type.
Read only, Bit 6 of PR2.
0 = Either VGA or EGA mode is enabled.
1 = Non-VGA and non-EGA modes are enabled.

Bit 1

EGA Compatibility Set.
Read only of PR4, Bit 1.
0 = EGA compatibility is disabled.
1 = EGA compatibility and the ability to read PR0 – PR5 registers are enabled.

Bit 0

Display Type.
Read only of PR5, Bit 3.
0 = Analog (VGA-compatible) display is attached.
1 = TTL (EGA-compatible) display is attached.

5.10.29 PR44 Power-Down Memory Refresh Control Register, Read/Write Port = 3?5, Index = 3F

This register controls two power saving features when in the general power-down modes. Bit 7 is used with PR35(7:6) to determine which power-down mode is to be used. With some power-down modes, the clocks used to refresh memory are slowed or stopped. This is done because the power consumption of the CMOS chip is proportional to its clock frequency. PR44(6:0) are loaded with a value that modifies the video memory refresh period during power-down.

BIT	FUNCTION
7	General Power-Down Mode Enable
(6:0)	Memory Refresh Cycle Period

Bit 7

General Power-Down Mode Enable Bit.
This bit enables general power-down mode.
0 = Disables general power-down.
1 = Enables general power-down.

Bit(6:0)

Memory Refresh Cycle Period.
These bits are loaded with the value Z, which is used to determine the refresh period when general power-down mode is used. Refresh period = VCLK x 8 x (Z+5). For example, assume:

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1. Two memory refresh cycles are selected during horizontal blanking period in Flat Panel display mode.
2. Each horizontal line has 96 character clocks.
3. MCLK = 36 MHz, VCLK = 25 MHz.
4. PR44 = 8EH.

When in powerdown mode, POWRDN = 0, MCLK = VCLK = 5 MHz.

1. Z = 14.
2. Refresh Cycle = 200 ns x 8 x (14 + 5).
3. Maximum Refresh Period = 200 ns x 8 x (14 + 5 - 7) = 19.2 µs.
4. Refresh Active Time = MCLK x 9 x 2 (cycle) = 200 ns x 9 x 2 = 3.6µs.

5.11 INTERNAL I/O PORTS

5.11.1 AT Mode, Write Only Port 46E8H (Also at Port 56E8H, 66E8H, 76E8H)

BIT	FUNCTION
7 - 5	Unused
4	Setup
3	Enable I/O & Memory
2 - 0	External BIOS ROM Page Select

Bit(7:5)

Unused.

Bit 4

Setup.
Puts WD90C20 into setup mode where only I/O port 102H is accessible.

Bit 3

I/O and Memory Accesses.
0 = Disable I/O and memory accesses.
1 = Enable I/O and memory accesses.

Bit(2:0)

Unused Internally.
Used for BIOS ROM Page select. On I/O accesses to 46E8H, EBROMN becomes I/O write strobe for external implementation of BIOS ROM page mapping. Bits (2:0) are latched data bits to define 4 Kbyte pages on BIOS ROM. The external mapping logic affects the three most significant bits of address applied to the BIOS ROM. The ROM can, therefore, be thought of as consisting of eight, 4 Kbyte pages. External circuitry is required to implement the BIOS ROM page selection using bits D2:D0.

5.11.2 Setup Mode Video Enable, (AT and Micro Channel Modes) Read/Write Port = 102H (XXXX XXXX XXXX X010B)

BIT	FUNCTION
7 - 1	Unused
0	Wakeup VGA

Bit(7:1)

Unused.

Bit 0

Wakeup VGA for I/O and Memory Accesses. Only lower 3 address bits are decoded for this port and WD90C20 must be in SETUP mode. VGA Enable Sleep bit or Programmable Option Select (POS) register 102H bit 0 is used to awaken the WD90C20 after power on in MCA and AT mode. To enter the set up mode in AT bus applications, bit 4 of the partially decoded internal I/O port 46E8H is set to 1 before accessing the I/O port 102H. In MCA mode, when the $\overline{\text{CDSETUP}}$ (ALE) signal pin is active low, the WD90C20 is in setup mode and port 102H can be accessed.

5.12 VIDEO RAMDAC PORTS

The WD90C20 incorporates a complete Micro Channel-compatible RAMDAC, as well as the ability to support an optional external RAMDAC. Selection of the internal or external RAMDAC option is based on the state of the VREF pin when reset is de-asserted.

Data from the internal RAMDAC is always written to the data bus, even when the internal RAMDAC is configured for use with external RAMDAC. RPLT may be used as a gate to send data from an external RAMDAC to the data bus.

There are four operation modes for the built-in video RAMDAC:
- Palette Read Mode
- Palette Write Mode
- PEL Mask Mode
- Palette Status Mode

Which mode is activated depends on two conditions: 1) which I/O port is being addressed, and 2) whether a host write or a host read is being executed.

In other words, the registers, albeit at the same I/O port, may have different meanings, depending on the mode in which the color palette is being accessed. Specifically, the register at 03C7 may contain either PEL address or palette status, depending on whether the access is a read or write operation.

When in the Palette Read Mode, the PEL address is to be written into the 03C7 port. The data can then be read out through the SD bus by three successive read operations from the 03C9 port.

When in the Palette Write Mode, the PEL address is to be written into the 03C8 port. The data can then be written into the palette through the SD bus by three successive write operations into the 03C9 port.

During either Palette Read or Palette Write mode, the 03C7 port can be read to obtain the contents of the Palette Status Register. Please see below for more detail on the palette register.

5.12.1 PEL Mask Register, Read/Write Port = 03C6

The 8-bit PEL Mask Register, along with the eight bits of color information from the combination of the attribute controller and the color select register, are ANDed together and become the index into the color lookup table of the RAMDAC during display refresh. The contents of this register have no effect on host access to the lookup table. The host may access this register at any time without disturbing the contents of the lookup table. The contents of this register are undefined after reset.

5.12.2 Palette Status Register/ Palette-Read-MODE PEL Address Register Read/Write Port = 03C7

Palette Status Register (as a Read Port):
The Palette Status Register can be accessed by reading the 03C7 port (read only). Bits 0 and 1 of this register indicate whether the last active operation to the DAC was in Palette Read Mode or in Palette Write Mode. These bits are both 0 if a host write into the port 03C7 is more recent than a host write into the port 03C8. They are both 1 if a host write into the port 03C8 is more recent than a host write into the port 03C7.

Palette-Read-Mode PEL Address Register (as a Write Port):
The host reads data from the color palette RAM by first writing the index of the first location to be read into this PEL Address Register (write only). When this is done, the RAMDAC loads the RAM data specified by the index into an 18-bit holding

DAC ADDRESS	TYPE	REGISTER NAME
3C6H	Read/Write	PEL Mask
3C7H	Read/Write	When written: PEL Address (Read Mode); When read: Palette Status
3C8H	Read/Write	PEL Address (Write Mode)
3C9H	Read/Write	PEL Data Port

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register. The contents of this 18-bit register are read out via three reads from the PEL Data Port. The data read during these reads consists of six bits of color information packaged into the six least significant bits of the port. The two most significant bits of data during these reads are set to zero. The color information is delivered in the sequence: read, green, blue. After the three read cycles have completed, the contents of the PEL address register are automatically incremented by one. In this way, sequential locations can be read by sets of three reads from the PEL Data Port, 03C9.

5.12.3 Pallette-Write-Mode PEL Address Register Read/Write Port = 03C8

The host writes data from the color palette RAM by first writing the index of the first location to be written into this register. Completed PEL data to be written is then loaded into an 18-bit holding register via three writes to the PEL Data Port. This is accomplished by concatenating the six least significant bits of the data from the three writes. The color information is extracted in the sequence: red, green, blue. When this is done, the RAMDAC loads the contents of the holding register into the palette RAM location indexed by the contents of the PEL Address (write mode) register. After the data has been transferred to the RAM, the contents of the PEL address register are automatically incremented by one. In this way, sequential locations can be written by sets of three writes to the PEL Data Port.

5.12.4 PEL Data Read/Write Port = 03C9

This port is used to transfer 6-bit PEL data values to and from the palette RAM. The 18-bit palette locations are transferred in the order: red, green, blue.

5.13 WD90C20 CONFIGURATION BITS, CNF

The configuration register, CNF, is not a physical register, but a convenient way to reference the state of the video memory data lines which are latched at reset. These data lines–for the sake of convenience, collectively called the configuration register CNF– provide setup parameters to various areas on the chip.

When the WD90C20 is reset, it latches the state of the video memory data lines. This data provides setup parameters to various areas of the chip. In order to easily reference these individual bits, we collectively refer to them as the configuration register, (CNF). Only fifteen data lines are used in the WD90C20 and the data line MD10 is not used.

CNF (11)

Color/Mono LCD Panel Select.
This bit is latched internally at power-on-reset from corresponding memory data bus pin MD(15), provided with either pull-up or pull-down external resistors. This bit is read from PR11(7), I/O port 3?5.2A bit 7. This bit is affected by writing to 3?5.2A. Pulling up MD(15) causes CNF(11) to be latched high.
0 = Monochrome LCD panels.
1 = Color LCD panels.

CNF (10:9)

Panel Select Bits.
These bits are latched internally at power-on-reset from corresponding memory data bus pins MD(9:8), provided with either pull up or pull down external resistors. They are read only at I/O port 3?5.31 as bits 1:0 and are unaffected by writing to 3?5.31. Pulling up MD(9:8) data bus pin causes CNF (10:9) to be latched high.

CNF(10)	CNF(9)	DISPLAY TYPE
0	0	Dual Panel LCD Display
0	1	
1	0	EL Display
1	1	Single Panel LCD Display

CNF (8)

Analog/TTL Display Status Bit.
Bit CNF(8) is latched internally at power-on-reset from memory data bus pin MD(11), provided with either a pull-up or pull-down external resistor. Pulling up MD(11) causes CNF(8) to be latched low. This bit controls no internal functions and is read only as Bit 3 of PR5 (3CF.0F). CNF(8) is unaffected by writing to PR5 (3CF.0F).
0 = Analog (VGA - compatible) display is attached.
1 = TTL (EGA-compatible) display is attached.

CNF (7:4)

General Purpose Status Bits.
Bits CNF (7:4) are latched internally at power-on-reset from corresponding memory data bus pins MD (7:4), provided with either pull-up or pull-down external resistors. These are read only bits at PR5 (3CF.0F) positions (7:4). They are unaffected by writing to PR5(3CF.0F). Pulling up MD (7:4) causes CNF (7:4) to be latched low.

CNF (3)

Video Clock Source Control.

This bit cannot be written to or read as I/O port. Pulling up MD (3) causes CNF(3) to be latched high. It configures WD90C20 pins VCLK1 and VCLK2 as inputs or outputs.
0= For inputs.
1= For outputs.

When used as inputs, these pins supply alternate video dot clocks. Selection of the dot clock is by an internal multiplexor. When used as outputs, VCLK1 supplies an active low load pulse for an external clock chip during I/O writes to port 3C2H. This load pulse may be inhibited by setting PR11(2)=1. VCLK2 becomes a third clock select input to the external clock chip, which supplies multiple dot clock frequencies to the VCLK0 input. VCLK1 and VCLK2 outputs are equal to Bits 2 and 3 of the Miscellaneous output register at 3C2H, respectively, when PR15 Bit 5 is set to 1.

CNF (2)

Bus Architecture Select.
This bit cannot be written to or read as I/O. Pulling up MD(2) causes CNF(2) to be latched high.
0 = Micro Channel architecture.
1 = AT BUS architecture.

Selecting CNF(2) will change the pinout definition between AT bus and Micro Channel bus. Refer to the pinout description.

PC AT BUS	I/O	MC	I/O
$\overline{\text{MEMCS16}}$	OUT	$\overline{\text{CDDS16}}$	OUT
IOCHRDY	OUT	CDCHRDY	OUT
$\overline{\text{EBROM}}$	OUT	$\overline{\text{CDSFDBK}}$	OUT
$\overline{\text{EIO}}$	IN	3C3D0	IN
$\overline{\text{MEMR}}$	IN	M/IO	IN
$\overline{\text{MEMW}}$	IN	$\overline{\text{S0}}$	IN
$\overline{\text{IOR}}$	IN	$\overline{\text{S1}}$	IN
$\overline{\text{IOW}}$	IN	$\overline{\text{CMD}}$	IN
IRQ	OUT	$\overline{\text{IRQ}}$	OUT
ALE	IN	$\overline{\text{CDSETUP}}$	IN

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5.14 MAPPING RAM – 32 by 5 STATIC RAM

The 32 by 5 SRAM is designed for dithering pattern selecting. This memory is used to adjust the color-to-gray scale mapping from the weighting equation. This mapping RAM can be read or written to by the CPU. During normal operation, the outputs from the weighting equation (5 bits) will be connected to the inputs of the mapping RAM (address input). The outputs of the mapping RAM (5 bits) are connected to the dithering logic.

To Write:

OUT 3?4, 35H	Program the index register.
OUT 3?5, 33H	Unlock the mapping RAM registers.
OUT 3?4, 3AH	Program the index register.
OUT 3?5, 01H	Select mapping RAM.
OUT 3?4, 38H	Program the index register.
OUT 3?5, 00H	Load WRITE starting address register with 00.
OUT 3?4, 39H	Program the index register.
OUT 3?5, 0AH	Write 0A directly to the mapping RAM at location 00.
OUT 3?5, 0BH	Write 0B directly to the mapping RAM at location 01.

To Read:

OUT 3?4, 35H	Program the index register.
OUT 3?5, 33H	Unlock mapping RAM registers.
OUT 3?4, 3AH	Program the index register.
OUT 3?5, 01H	Select mapping RAM.
OUT 3?4, 38H	Program the index register.
OUT 3?5, 00H	Load READ starting address register with 00.
OUT 3?4, 39H	Program the index register.
IN 3?5	Read directly from the mapping RAM at 00.
IN 3?5	Read directly from the mapping RAM at 01.

NOTE: There is a minimum timing requirement between two consecutive RAM reads or writes (4 x VCLK period). If the system is running faster than 16 MHz, a "NOP" instruction should be inserted between consecutive reads and/or writes.

5.15 SHADOW TIMING REGISTERS

The shadow timing registers control the timing in the CRTC. When the regular timing registers are written to, the shadow timing registers, if unlocked (in CRT mode, they are unlocked), receive the same data. Locking the shadow timing registers is controlled by PR1B.

Timing data is always read from the regular timing registers. The WD90C20 never reads from the shadow timing registers.

In Flat Panel mode, the shadow timing registers are loaded once and then locked by PR1B. Once they are locked, data written to the timing registers is not passed through to the shadow timing registers and the flat panel timing is not affected.

There are eleven shadow timing registers. All are indexed in port 03?5.

NAME	INDEX	SAMPLE VALUE*
Horizontal Total	00H	5FH
Start Horizontal Blanking	02H	50H
End Horizontal Blanking	03H	82H
Start Horizontal Retrace	04H	54H
End Horizontal Retrace	05H	80H
Vertical Total	06H	F2H
Overflow **	07H	00H
Vertical Retrace Start	10H	F0H
Vertical Retrace End	11H	02H
Start Vertical Blank	15H	F0H
End Vertical Blank	16H	F2H

* The sample values are for a monochrome dual panel LCD with 640 by 480 pixels.

** Only bits 7, 5, 3, 2 and 0 are locked by PR1B.

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6.0 RAMDAC

6.1 GENERAL DESCRIPTION

The on-board RAMDAC was designed specifically for Personal System/2 compatible color graphics in a laptop computer environment. It integrates the functions of a color lookup table, digital-to-analog converters, power saving features and PS/2 compatible monitor detection logic.

The 256 by 18 color lookup table has triple 6 bit video D/A converters. A pixel mask register and composite blank generation on the three channels are provided. The RAMDAC also supports the use of an external voltage reference.

Without external buffering, the RAMDAC will generate RS-343A compatible video signals into a doubly-terminated 75 ohm load, and RS-170 compatible video signals into a singly-terminated 75 ohm load. Integral and differential linearity errors are a maximum of +/- 1/2 LSB.

The WD90C20A's improved RAMDAC was redesigned to do the following:

- reduce power dissipation
- reduce overshoot and undershoot noise
- reduce ampflier gain error
- improve linearity
- increase yield

6.2 FUNCTIONAL DESCRIPTION

The RAMDAC architecture consists of five major modules:

- Address Register
- Pixel Mask Register
- Color Palette RAM
- Power-Down Control
- Digital-to-Analog Converter (with automatic power-on reset)

Color Palette RAM: There are three 256 by 6 color palette RAMs for the red, green and blue polygun. They provide color information to the triple 6-bit D/A converters. The RAMDAC's color palette RAM memory cell is a custom, power saving cell.

Power-Down Control: The RAMDAC supports an intelligent power-down control sequence. When $\overline{\text{PWRDN}}$ input is low, the entire RAMDAC will enter the "IDLE" state; both the DAC and the color palette RAM will be turned off regardless of the CRT/-LCD signal. When $\overline{\text{PWRDN}}$ input is high in CRT mode, the RAMDAC will operate with the DAC and the color palette RAM always enabled. In LCD mode, when $\overline{\text{PWRDN}}$ input is high, the DAC is turned off. The color palette RAM will be enabled only when the MPU is accessing the RAMDAC because of the intelligent "MPU operation auto-detecting" circuit implemented.

Automatic Power-on Reset: The RAMDAC supports an "automatic poweron-reset" circuit that enables its DAC portion to initialize very quickly after power-on. And, since the DAC is totally turned off in LCD mode, a triggered signal will also initialize the "reset operation" of the DAC during the mode change from LCD mode to CRT mode.

See Section 5.12 and Appendix F for descriptions of RAMDAC registers.

6.3 FEATURES

- Personal System/2 compatible
- Bt471/478 and Bt476 compatible
- Power management features
- On-chip monitor detection logic
- Video signal output into 37.5 or 50 ohms
- 256 by 18 color palette RAM
- Triple 6-bit D/A converters
- Pixel mask register
- Up to 8 bits input per pixel
- RS-343/RS-170 compatible outputs
- 1.25 micron CMOS (WD90C20)
- 0.9 micron CMOS (WD90C20A)

6.4 TEST MODE

The WD90C20A has a new test mode which directly tests the built-in DAC. This allows the DAC to be tested more completely than in the WD90C20 and at the same time more efficiently.

7.0 POWER-DOWN MODES

7.1 SYSTEM POWER-DOWN MODE

7.1.1 Description of System Power-Down Mode (Sleep Mode)

System Power-Down mode is used when the entire system goes to sleep and provides the most power savings. Current requirements for this mode are approximately 4mA. This mode also requires the most system overhead and therefore in addition to being the most miserly in terms of power consumption, it is also the slowest. When the VGA subsystem has been placed in System Power-Down mode, the only activity required of the VGA subsystem is saving the contents of the video display buffer which is accomplished by maintaining refresh of the DRAM. In this mode the system CPU has no access to the display memory nor any access to the I/O of the WD90C20 VGA controller.

Power savings is achieved by:

1. Turning off the display.
2. Turning off the DACs (if in CRT mode).
3. Turning off the internal MCLK and VCLK signals.
4. Executing CAS before RAS refresh (PDREF) instead of RAS only refresh.
5. Denying the CPU access to WD90C20 I/O registers.
6. Denying the CPU access to video memory.

In System Power-Down mode only the content of the video display buffer is saved which implies that the rest of the dynamic data contained in the VGA subsystem is corrupted. This includes the color content of the RAMDAC palette and the content of the mapping RAM is lost when in this mode.

7.1.2 Entering System Power-Down Mode

To select System Power-Down mode, load bit PR35(7) with "1" (default value is "0"). The WD90C20 will enter a System Power-Down mode cycle when the motherboard power manager drives the "PDOWN" input of the WD90C20 low. After "PDOWN" is driven low, the CPU can not access the WD90C20.

The WD90C20's internal memory and video clocks will automatically be turned off (to save power) after the following time interval: 4 horizontal scan lines PLUS 3 "REFRESH" cycles.

The WD90C20 uses the "REFRESH" input to generate "CAS before RAS" memory refresh cycles which refresh display memory. The internal RAMDAC is also turned off, and display memory refresh is the only WD90C20 activity during this power-down mode. The VCC pins of the WD90C20 must remain powered.

Primary input MCLK may be clocked at the same frequency as VCLK, or may be left at a static "1" or "0". Primary input VCLK must NOT be turned off but may be reduced to as low as 8 KHz. When the VCLK and MCLK frequencies are reduced, they should not be reduced until the following time interval has passed: the time to display 4 horizontal lines PLUS 3 "REFRESH" cycles.

There are several ways to slow down the clocks of the WD90C61. The most effective way is to use the "FCLKIN" input frequency. This is done by driving the "FCLKSEL" input low. "FCLKIN" could be connected to a slow frequency clock which is available on the motherboard.

During the System Power-Down Mode, the "OE10", "OE32", "WE0", "WE1", "WE2", "WE3" and MA(8:0) outputs are all driven high. The memory data bus, MD(15:0), will be in an unknown state. Note that all primary inputs must be driven to either VCC or VSS, as required by the system design. No inputs may be left floating.

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7.1.3 Exiting System Power-Down Mode

Before returning to normal display mode, the power manager must first return the WD90C20 clock inputs back to their original frequencies (if they were slowed down during the power-down mode). Care must be taken to ensure that the clock inputs to the WD90C20 are stable BEFORE driving the "PDOWN" input high.

To return to normal mode, the power manager drives "PDOWN" high; the WD90C20 returns to normal operation mode after the following time interval; the time to display 4 horizontal lines PLUS 3 "REFRESH" cycles. The screen automatically displays the information in video memory.

The power-up service routine must reload the RAMDAC RAM data and the 32 by 5 dithering mapping RAM data after the system returns to normal operation mode.

7.2 DISPLAY IDLE MODE

7.2.1 Description Of Display Idle Mode

The Display Idle Mode is used when the user can allow the display to be turned off, for example, when a keyboard key has not been pressed for five minutes. The DAC and LCD panel interfaces are turned off in this mode. Internal clocks are divided by eight from the primary inputs, thus internal logic runs eight times slower. The CPU can access I/O registers of the WD90C20, but it can not access display memory.

Power saving is achieved by:

1. Turning off the display.
2. Turning off the DACs (if in CRT mode).
3. Dividing internal WD90C20 clocks by eight.
4. Executing CAS before RAS refresh (PDREF) instead of RAS only refresh.
5. Denying the CPU access to video memory.

7.2.2 Entering Display Idle Mode

Register bits PR35(7) and PR44(7) must be set to "0" (default values) to use this mode. The WD90C20 will enter a Display Idle Mode cycle when the motherboard power manager drives the "PDOWN" input of the WD90C20 low.

The WD90C20 will then divide the internal VCLK and MCLK signals by eight. For example, if the input VCLK is 32 MHz and the input MCLK is 44.9 MHz, the internal VCLK will be 4 MHz and the internal MCLK will be 5.61 MHz. Power consumption in this mode is approximately 1/10 of normal consumption. The internal RAMDAC turns off and screen refresh cycles are stopped. The WD90C20 uses the "REFRESH" input to generate "CAS before RAS" cycles to refresh display memory. The CPU will be the only user to access the display memory. There is no arbitration between CPU cycles and CRT cycles, or between CPU cycles and refresh cycles.

While in the Display Idle Mode, the video system continues to run, allowing the user to read/write WD90C20 I/O registers, however, the CPU CAN NOT read/write display memory.

7.2.3 Exiting Display Idle Mode

To return to normal operation mode, the power manager simply drives "PDOWN" high. The screen automatically displays the original picture. External clocks must maintain original frequencies for the Display Idle Mode.

7.3 GENERAL POWER-DOWN MODES

7.3.1 Description of General Power-Down Modes

There are two General Power-Down modes. These modes are used when: 1)the user doesn't need to view the display, 2)he needs to keep the system running, but 3)he can afford to reduce the frequencies of both MCLK and VCLK. Video system performance is reduced in exchange for significant power savings. Another advantage is that activating the WD90C20 PDOWN input is the only software interaction required.

One of the General Power-Down modes is designed to interface with an intelligent clock generator like the WD90C61, which slows down the clocks to the WD90C20 to a selectable frequency during the power-down interval. This is called the General Power-Down mode with External Clock Control.

The other is designed to be independent of the external clock control; the external clock maintains the same frequency during power-down, however internal clock circuitry in the WD90C20 divides the input clock by eight. This is called General Power-Down mode with Internal Clock Control.

Both General Power-Down modes allows the CPU to access BOTH I/O registers and display memory.

Power savings is achieved by:

1. Turning off the display.
2. Turning off the DACs (if in CRT mode).
3. Dividing the MCLK and VCLK inputs by a system chosen factor (external) or by eight (internal).

7.3.2 Entering General Powerdown Mode with External Clock Control

To select General Power-Down mode with External Clock Control, load bit PR44(7) with "1" and bit PR35(6) with "0". PR44(6:0) should be preloaded with its correct value, based on the power-down clock frequency.

The WD90C20 will enter a General Power-Down mode with External Clock Control cycle when the motherboard power manager drives the "$\overline{\text{PDOWN}}$" input of the WD90C20 low. At this time the PR44 register will replace the CRTC registers to control memory refresh timing.

7.3.3 Exiting General Power-Down Mode With External Clock Control

Before returning to normal display mode, the power manager must first return the WD90C20 clock inputs back to their original frequencies. Care must be taken to ensure that the clock inputs to the WD90C20 are stable BEFORE driving the "$\overline{\text{PDOWN}}$" input high.

To return to normal mode, the power manager drives "$\overline{\text{PDOWN}}$" high; the WD90C20 then returns to normal operation mode and displays the screen that is stored in video memory.

7.3.4 Entering General Power-Down Mode with Internal Clock Control

To enter the General Power-Down mode with the internal clock control, PR44(7) must be set to a "1" and PR35(6) must be set to a "1". PR44(6:0) should be pre-loaded with its correct value based on the VCLK frequency and the PR1A(1:0) value. The PR1A(1:0) is used to select different memory refresh cycles per each horizontal line.

After the input "$\overline{\text{PDOWN}}$" is driven low by the system, the WD90C20 will enter General Power-Down mode automatically. Register PR44 will replace the CRTC registers to control memory refresh timing.

7.3.5 Exiting General Power-Down Mode with Internal Clock Control

To return to normal mode, the power manager drives "PDOWN" high; the WD90C20 then returns to normal operation mode and returns the internal MCLK and VCLK signals to their normal frequencies. The information stored in video memory is displayed on the screen.

7.3.6 Example Calculations of PR44(6:0) Values

Described below are examples of how to calculate correct values of PR44(6:0) for both General Power-Down modes. Calculation of PR44(6:0) value is based upon the following equation:

7.3.7 Disabling the WD90C20 to Accommodate an Alternate VGA Controller

PR35 Bit 5 allows the WD90C20 to accommodate an alternate VGA controller. When the WD90C20 detects that "PDOWN" is low and PR35(5) is high, the WD90C20 isolates itself from the system I/O bus regardless of the programmed power-down mode. In this case, the CPU CAN NOT access the WD90C20. All outputs and I/Os of the host interface are tristated. This feature allows another VGA or graphic controller on the system I/O bus in case the system designer wished to switch display environments.

To return to normal operation mode, the CPU must drive "PDOWN" high.

PR44(6:0) = ((Refresh Rate*PR1A(1:0))/((1/(CLK/8))*Character)) - 5

Where: Refresh Rate = Period defined for Refresh of the DRAMs

CLK = External Clock input for General Power-Down mode with External Clock
VCLK input for General Power-Down mode with Internal Clock.

Example for General Power-Down mode with External Clock Control:

Example A == > How to calculate the value of PR44(6:0)
PR44(7) = 1, PR35(6) = 0
PR1A(1:0) = 11 (2 memory refresh cycles/horizontal line)
Normal Operation: VCLK = 32 MHz, MCLK = 44.9 MHz
Power-Down Mode: VCLK = 5 MHz, MCLK = 8 MHz (external control)

CALCULATE ==>
15 us x 2 = 30 us (2 refreshes/line)
1/5 MHz x 8 = 200 ns x 8 = 1.6 us (1 character clock in power-down mode)
(30 us / 1.6 us) - 5 = 14 (PR44(6:0) = OE hex)

Example B ==> How to calculate the value of PR44(6:0)
PR44(7) = 1, PR35(6) = 1 (internal divided by 8 control)
PR1A(1:0) = 01 (1 memory refresh cycle/horizontal line)
Normal Operation: VCLK = 28 MHz, MCLK = 42 MHz
Power-Down Mode: VCLK = 3.5 MHz, MCLK = 5.25 MHz (internal control)

CALCULATE ==>
15 us x 1 = 15 us (1 refresh/line)
285.7 ns x 8 = 2.286 us (1 character clock in power-down mode)
(15 us/ 2.286 us) - 5 = 2 (PR44(6:0) = 02 hex)

The following are descriptions of the output states of all output pins during the four power-down modes. These states are given for both "AT" and "Micro Channel" modes of operation. This information is provided for reference to the system designer.

PC-AT MODE					
OUTPUT STATE					
Pin No.	**Pin**	**System Powerdown Mode**	**Display Idle Mode**	**General Mode w/Ext. Clock**	**General Mode w/Int. Clock**
	SD[15:0]	Z	N	N	N
15	IOCHRDY	Z	N	N	N
12	IRQ	Z	N	N	N
14	MEMCS16	Z	N	N	N
13	EBROM	H	N	N	N
16	HBDIR	H	N	N	N
17	LBDIR	H	N	N	N
57	RAS32	N	N	N	N
56	RAS10	N	N	N	N
59	CAS32	N	N	N	N
58	CASA10	N	N	N	N
65	OE32	H	N	N	N
64	OE10	H	N	N	N
	WE[3:0]	H	N	N	N
	MA[8:0]	H	N	N	N
	MD[15:0]	Z	N	N	N
110	LCD/CRT	N	N	N	N
	UD[3:0]	L	L	L	L
	LD[3:0]	L	L	L	L
91	FR	L	L	L	L
90	FP	L	L	L	L
89	LP	L	L	L	L
87	XSCLK	L	L	L	L
88	WGTCLK	L	L	L	L
92	RPLT	H	N	N	N
93	WPLT	H	N	N	N
86	PCLK	L	N	N	N
116	RED	L	L	L	L
115	GREEN	L	L	L	L
114	BLUE	L	L	L	L

LEGEND: Z = High impedance, tri-state.
H = Logic High, "1" state.
L = Logic Low, "0" state.
N = Normal state, could be "1", "0", or tri-state.

NOTES: For on-chip pullups and pulldowns, see Section 4.0 "Signal Description."

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MICRO CHANNEL MODE					
OUTPUT STATE					
Pin No.	Pin	System Powerdown Mode	Display Idle Mode	General Mode w/Ext. Clock	General Mode w/Int. Clock
	SD[15:0]	Z	N	N	N
15	IOCHRDY	H	N	N	N
12	IRQ	H	N	N	N
14	$\overline{\text{MEMCS16}}$	H	N	N	N
13	$\overline{\text{EBROM}}$	H	N	N	N
16	HBDIR	H	N	N	N
17	LBDIR	H	N	N	N
57	$\overline{\text{RAS32}}$	N	N	N	N
56	$\overline{\text{RAS10}}$	N	N	N	N
59	$\overline{\text{CAS32}}$	N	N	N	N
58	$\overline{\text{CASA10}}$	N	N	N	N
65	$\overline{\text{OE32}}$	H	N	N	N
64	$\overline{\text{OE10}}$	H	N	N	N
	$\overline{\text{WE}}$[3:0]	H	N	N	N
	MA[8:0]	H	N	N	N
	MD[15:0]	Z	N	N	N
110	$\overline{\text{LCD}}$/CRT	N	N	N	N
	UD[3:0]	L	L	L	L
	LD[3:0]	L	L	L	L
91	FR	L	L	L	L
90	FP	L	L	L	L
89	LP	L	L	L	L
87	XSCLK	L	L	L	L
88	WGTCLK	L	L	L	L
92	$\overline{\text{RPLT}}$	H	N	N	N
93	$\overline{\text{WPLT}}$	H	N	N	N
86	PCLK	L	N	N	N
116	RED	L	L	L	L
115	GREEN	L	L	L	L
114	BLUE	L	L	L	L

LEGEND: Z = High impedance, tri-state.
H = Logic High, "1" state.
L = Logic Low, "0" state.
N = Normal state, could be "1", "0", or tri-state.

8.0 LCD PANEL CONTROL

This section describes external power on/off control logic for an LCD panel interface.

8.1 DESCRIPTION OF SIGNALS FOR FIGURE 8-1

Described below are the signals related to the poweron/off control logic in Figure 8-1.

POWER-ON
(General motherboard signal, input to control logic)

Active high signal: indicates that the LCD +5 volt power supply (+VDD_LCD) and the backlight power supply (+VBL) are stable.

$\overline{\text{PDOWN}}$, +PDOWN
(General motherboard signal, input to control logic)

Active low and active high signals, respectively; indicate that the system has entered the POWER-DOWN mode.

RSET
(General motherboard signal, input to control logic)

Active high signal; is generated during power-on or system reset.

$\overline{\text{LCD}}$
(WD90C20 output)

WD90C20 active low output; indicates that the LCD panel is selected as main display.

$\overline{\text{LCDEN}}$
(Output of control logic)

Active low signal which is connected to the LCD panel to enable the LCD drivers and DC power.

$\overline{\text{CFLEN}}$
(Output of control logic)

Active low signal which is connected to the LCD panel to enable backlight power.

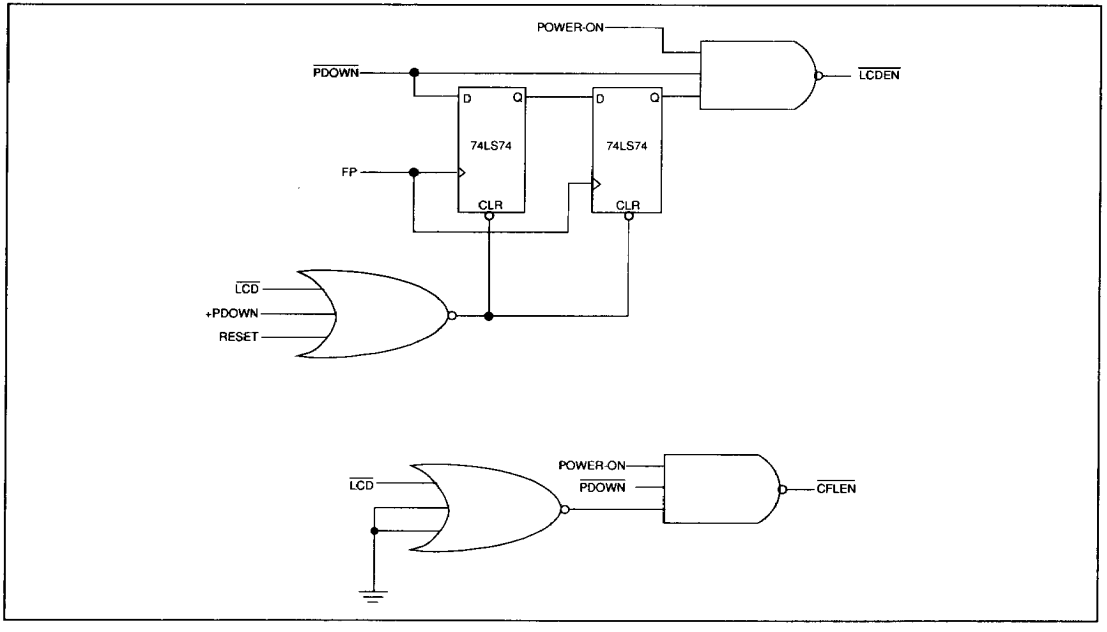

FIGURE 8-1. LCD PANEL CONTROL

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9.0 LCD POWER-ON/OFF OPERATIONS DESCRIPTION

9.1 SYSTEM POWER-ON

When main power is turned on, RESET guarantees the "LCDEN" remains "HIGH" during the power-on interval. This protects the LCD panel from damage. After RESET goes inactive and if a CRT monitor is connected, the "LCD" output from the WD90C20 will be a "1" which forces "LCDEN" high, keeping the LCD panel disabled.

After RESET goes inactive and if an LCD panel is connected, the "LCD" output from the WD90C20 will be a "0." Two "FP" strobes (one to two vertical frames) after "LCD" goes low, "LCDEN" is driven low, enabling LCD power. "CFLEN" (backlight power) is driven low immediately after "LCD" goes low.

9.2 SYSTEM POWER-OFF

When main power is turned off "POWERON" goes low, forcing both "-LCDEN" and "CFLEN" high, which immediately disables both LCD panel power and backlight power.

9.3 SWITCHING FROM CRT MODE TO LCD MODE

The system must:

1. Reset the CRT mode bit PR19(5) to "0."
2. Read and save the CRTC registers.
3. Load the shadow registers with default values from the table.
4. Lock the shadow registers.
5. Write back the CRTC registers.
6. Enable the LCD mode by setting PR19(4)=1 (which sets "LCD"=0).

Two "FP" strobes (one to two vertical frames) from "LCD" going low, "LCDEN" is driven low, enabling LCD power. "CFLEN" is driven low immediately after "LCD" goes low.

9.4 SWITCHING FROM LCD MODE TO CRT MODE

The system must:

1. Reset the LCD mode bit PR19(4) to "0", thus setting the WD90C20 output "LCD" to a "1" (since "LP" and "FP" are still toggling).
2. Read and save the CRTC registers.
3. Unlock the shadow registers.
4. Write back the CRTC registers.
5. Set the CRT mode bit PR19(5) to a "1".

9.5 ENTERING POWER-DOWN MODE

The system drives "PDOWN" low and "+PDOWN"high to enter a power-down mode. Both "LCDEN" and "CFLEN" are driven high immediately (before "LP" and "FP" stop toggling).

9.6 LEAVING POWER-DOWN MODE

When in LCD Mode: The system drives "PDOWN" high and "+PDOWN" low to leave a power-down mode (to return to normal operation mode). "LCDEN" remains high for two "FP" strobes (one to two vertical frame periods). This guarantees the "LP" and "FP" will be toggling before LCD panel power is turned on.

When in CRT Mode: Because "LCD" is always a "1" when entering and leaving a power-down mode, "LCDEN" and "CFLEN" will also remain high for the entire period, thus leaving the LCD panel power off.

A.0 APPLICATIONS APPENDIX

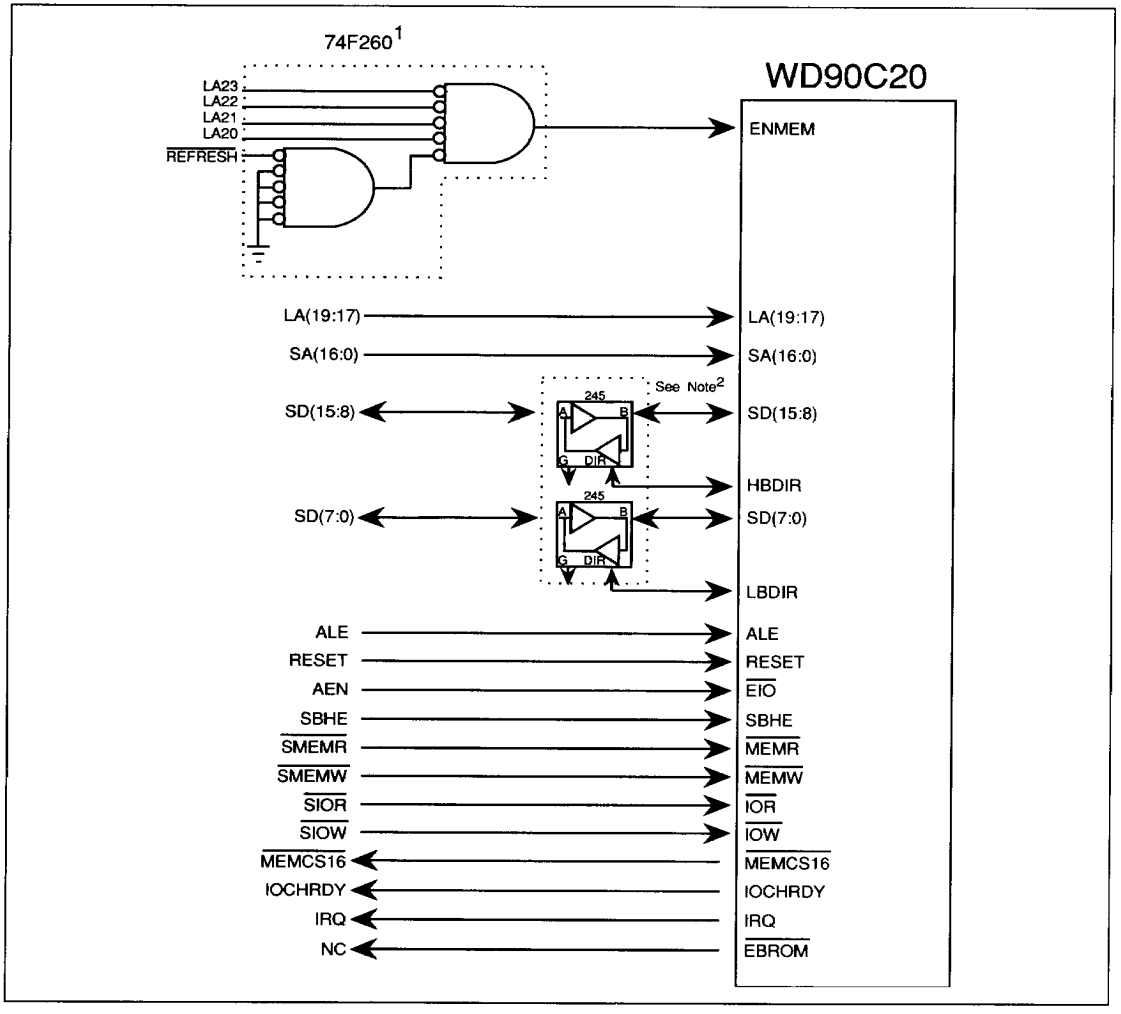

FIGURE A-1. PC/AT INTERFACE

NOTES:

[1] The 74F260 is used to determine if the current address is in the first megabyte. This function is already provided by most core logic chip sets.

[2] The 74245 buffers are only needed if system drive requirements exceed chip capabilities.

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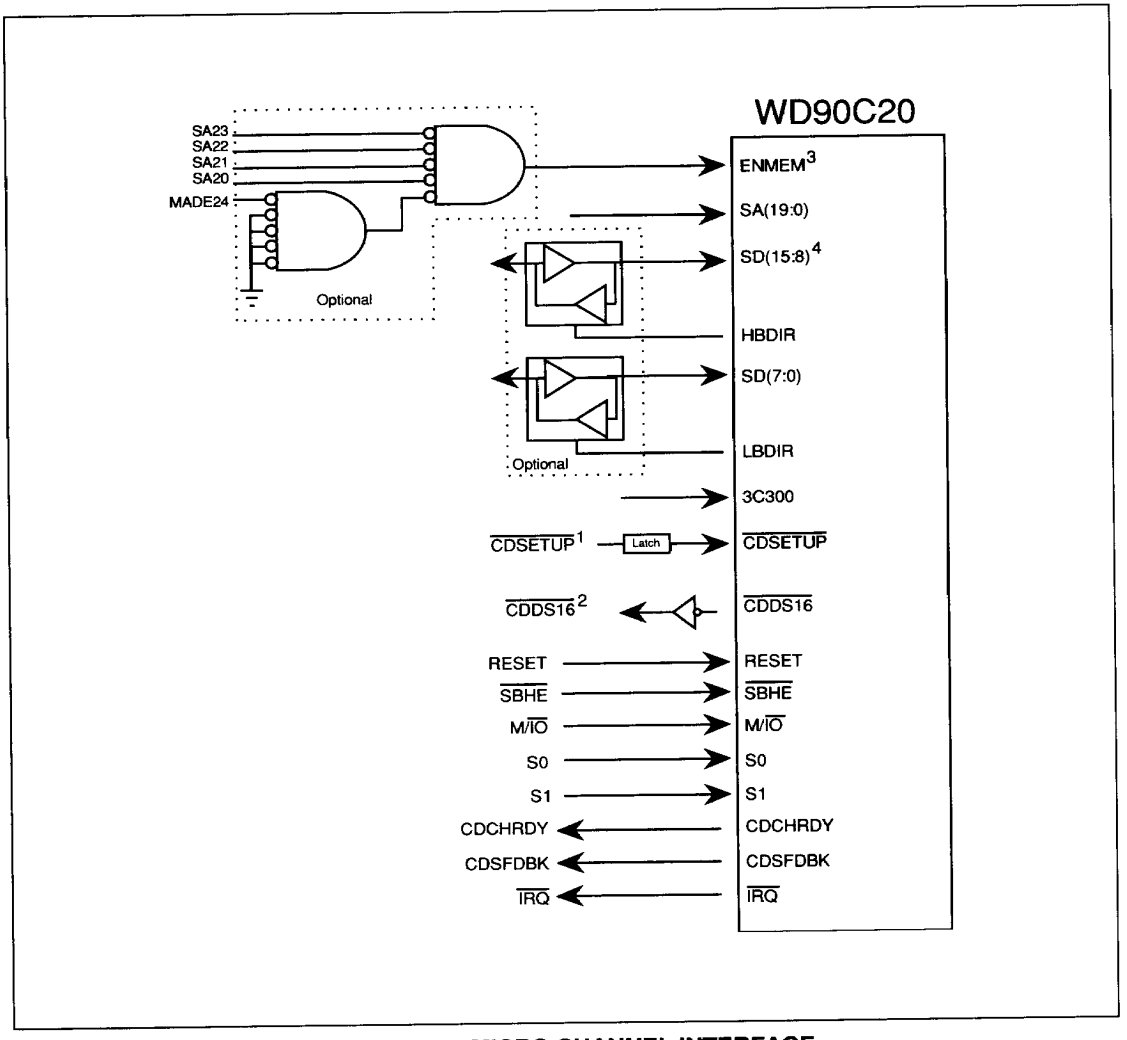

FIGURE A-2. MICRO CHANNEL INTERFACE

NOTES:

1 $\overline{\text{CDSETUP}}$ must be latched if core logic does not already latch it.
2 CDDS16 requires an inverter (changed in future revisions).
3 ENMEN must be qualified for the first megabyte of memory space. This is provided in many core logic designs; the two And Gates are not required.
4 The bidirectional buffers are only needed if the system design requires more current than the WD90C20 can deliver.

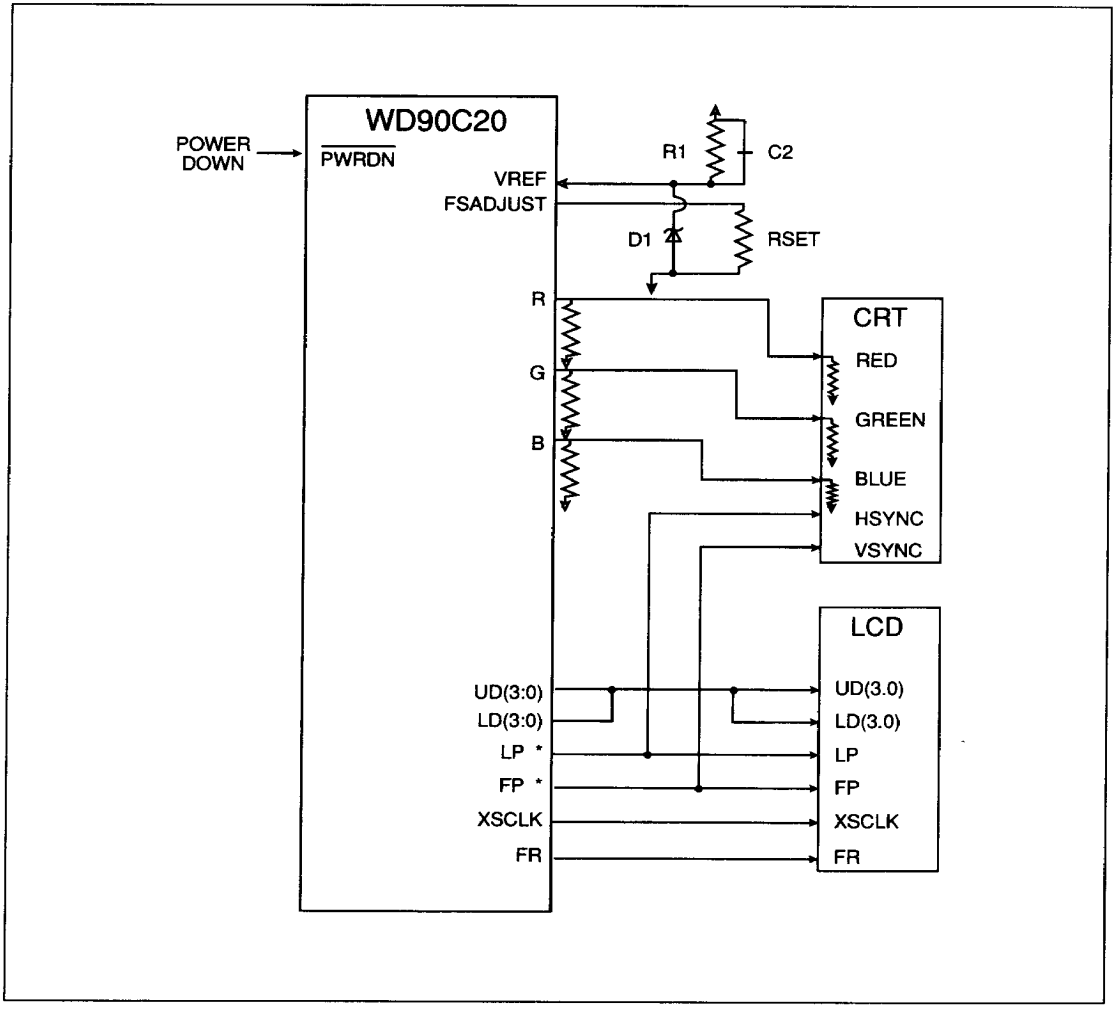

FIGURE A-3. WD90C20 DISPLAY INTERFACE

FULL-SCALE-VOLTAGE CALCULATION EXAMPLE:

$$V_{FULL\ SCALE} = [\ I_{FULL\ SCALE}] \quad [\ RLD\ ]$$

$$= \left[\frac{\text{code} \times 0.04 \times \text{VREF}}{\text{RSET}}\right] [\ RLD\ ]$$

$$= \left[\frac{63 \times 0.04 \times 1.235}{221}\right] [\ 50\ ] = 0.704 \text{ volts}$$

* These signals may require buffering if monitor sinks more than the 6mA drive of the WD90C20.

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B.0 EGA MODE APPENDIX

This appendix provides a general description of EGA mode. Details of the actual software implementation are not covered.

For those registers that are the same in both VGA and EGA mode, refer to the VGA description. Only the differences are described in this section. Bits not used should be set to 0 unless otherwise noted.

1. Load Configuration register bit 8. Logic 0 for VGA compatible PS/2 display or Logic 1 for EGA compatible TTL monitor by appropriate pullup or pulldown resistor on MD(11). (Pull-up resistor on MD11 causes CNF(8) to be latched with logic 0, for Analog PS/2 compatible display). This is status for the BIOS or application to signify monitor type attached.

2. Unlock all the PR registers.

3. Program PR2(6) to 0 for EGA mode.

4. Set PR4 Bit 1 to logic 1 for EGA compatibility.

5. Load PR11(7:4) with EGA Configuration switches by using pullup or pulldown resistors on pins MD(15:12). (Pullup resistor causes logic 1 to be latched after power-on-reset.)

6. The EGA switch setting may then be read from PR11(7:4) at I/O port 3C2 Bit 4.

7. If EGA is to be emulated on the IBM PS/2 type analog display, follow the steps listed below:

   - Initialize all the registers
   - Lock CRT controller registers
   - Force Clock Control rate of the CRT controller

8. Set EGA emulation mode by programming:

   - PR11(3)=1; Set EGA emulation on PS/2 type display
   - PR14(6)=1; Vertical double scan
   - PR11(2)=1; Lock clock select
   - PR11(0)=1; Lock 8/9 dot timing
   - PR14(7)=1; Enable IRQ (optional)

9. Lock the PR registers PRO-PR5 and PR10-PR17.

10. Read protect PR registers.

11. When EGA is required on a TTL monitor, the suggested steps are:

   - Initialize all the registers
   - Set EGA TTL mode by programming:
     PR11(3)=0;EGA TTL
     PR14(7)=1;Enable IRQ
     PR15(6)=1;Set Low Clock
     PR14(7)=1;Enable IRQ
   - Lock PR registers PRO-PR5 and PR10-PR17
   - Read protect PR registers

For more details on the PR registers, refer to the PR registers section. The EGA register summary shown on the next page highlight all the EGA mode registers.

REGISTERS	EGA	I/O PORT
General Registers:		
Miscellaneous Output Reg	WO	3C2
Input Status Reg 0	RO	3C2
Input Status Reg 1	RO	3?A
Feature Control Reg	WO	3?A
Sequencer Registers:		
Sequencer Index Reg	WO	3C4
Sequencer Data Reg	WO	3C5
CRT Controller Registers:		
Index Reg	WO	3C4
CRT Controller Data Reg Except the Following:	WO	3?5
Start Address High (Index=0C)	RW	3?5
Start Address Low (Index=0D)	RW	3?5
Cursor Location High (Index=0E)	RW	3?5
Cursor Location Low (Index=0F)	RW	3?5
High Pen High (Index=10)	R	3?5
Light Pen Low (Index=11)	R	3?5
Graphics Controller Registers:		
Index Reg	WO	3CE
Other Graphics Reg	WO	3CF
Attribute Controller Registers:		
Index Reg	WO	3C0*
Attribute Controller Data Reg	WO	3C0*

TABLE B-1. EGA REGISTERS SUMMARY

NOTES:
1. RO = Read Only, WO = Write Only, and RW = Read/Write.
2. All register addresses are in hex.
3. ? = B in monochrome modes or D in color modes.
4. * = Identical responses from I/O ports 3C0 and 3C1.

B.1 GENERAL REGISTERS

The General Registers and the bit definitions that differ from VGA mode are covered below.

B.1.1 Miscellaneous Output Register (Write Port 3C2)

Bits (7:5)

EGA: Same as Miscellaneous Output Register Bits (7:5) definition in the VGA section.

Bit 4

Disables internal video drivers.
0 = Activate video drivers.
1 = Disable video drivers.

Bits (3:2)

EGA:

BIT 3	BIT 2	DESCRIPTION
0	0	14.318 MHz clock (VCLK0) is selected.
0	1	16.257 MHz clock (VCLK1) is selected if Configuration Register Bit 3 is 0.
1	0	External User Defined Clock (VCLK2) from the feature connector is selected if Configuration Register Bit 3 is 0.
1	1	Not Used. VCLK2 selected if Configuration Register Bit 3 is 0

Bit (0)

EGA: Identical to Miscellaneous Output Register Bit 0 definition in the VGA section.

B.1.2 Input Status Register 0 (Read Port 3C2)

Bit 7

EGA: Same as input Status Register 0, Bit 7 definition in the VGA section.

Bits (6:5)

EGA: Not Used.

Bit 4

EGA: Information on the four configuration switches stored in PR11 can be read at this bit if PR4(1) has been set to 1.

Bits (3:0)

EGA: Not Used = 1

B.1.3 Input Status Register 1 (READ PORT 3?A)

Bit (7)

EGA: Not Used.

Bit 6

EGA: Not Used = 1.

Bits (5:3)

EGA: Identical to Input Status Register 1 Bits (5:3) definition in the VGA section.

Bit 2

EGA: The following Light Pen Switch definition is applicable:
0 = Light Pen Switch is Closed.
1 = Light Pen Switch is Open.

Bit 1

EGA: The following Light Pen Trigger definition is applicable:
0 = Light Pen Trigger is Reset.
1 = Light Pen Trigger is Set.

Bit (0)

EGA:
Same as Input Status Register 1 Bit 0 definition in the VGA Section.

B.1.4 Feature Control Register (Write Port 3?A)

Bits (7:0)

EGA: Not Used.

B.2 SEQUENCER REGISTERS (PORT 3C5)

B.2.1 Clocking Mode Register , (Index = 01)

Bits (7:4)

EGA: Not Used.

Bits (3,2)

EGA: Same as Clocking Mode Register Bits (3,2) definition in the VGA section.

Bit 1

EGA: Set to Zero.

Bit (0)

EGA: Identical to Clocking Mode Register Bit 0 definition in the VGA section.

B.2.2 Character Map Select Register, (Index 03)

Bits (7:4)

EGA: Not Used.

Bits (3:2)

EGA: Character Map Select A:

BIT 3	BIT 2	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8 Kbyte
0	1	1	Second 8 Kbyte
1	0	2	Third 8 Kbyte
1	1	3	Fourth 8 Kbyte

Bits (1:0)

EGA: Character Map Select B:

BIT 1	BIT 0	MAP SELECTED	FONT TABLE/PLANE 2 LOCATION
0	0	0	First 8 Kbyte
0	1	1	Second 8 Kbyte
1	0	2	Third 8 Kbyte
1	1	3	Fourth 8 Kbyte

NOTE: 1. Character Map selection from Plane 2 is determined by Bit 3 of the attribute code.

B.2.3 Memory Mode Register, (Index = 04)

Bits (7:3)

EGA: Not Used.

Bits (2:1)

EGA: Identical to Memory Mode Register Bits (2,1) definition in the VGA section.

Bit 0

EGA: Alpha Mode Bit.
A logic 1 shows that Alpha mode is active and character map selection is enabled. A logic 0 disables Alpha mode and enables non-Alpha mode.

B.3 CRT CONTROLLER REGISTERS (PORT 3?5)

The EGA registers that are different are listed. For similar registers and identical bits within registers refer to the VGA section. A "?" implies that a register is mapped into either 3B5 or 3D5 for Monochrome or Color display modes, respectively.

B.3.1 Index Register (Port = 3?4)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Five bits point to the CRT Register Address index where the data is to be written.

B.3.2 Horizontal Total Register, (Index = 00)

Bits (7:0)

EGA:
Eight bits of value for the "Total Character Count Less 2" are loaded into this register. They define number of characters to be displayed per horizontal line.

B.3.3 End Horizontal Blanking Register, (Index = 03)

Bits (7)

EGA: Not Used.

Bits (6:5)

EGA: These bits define display enable skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0)

EGA: Five bits of character count are loaded to determine when the horizontal blanking signal becomes inactive.

B.3.4 End Horizontal Retrace Register, (Index = 05)

Bit 7

EGA: It defines the start of the odd or even CRT counter memory address following the horizontal retrace time. Logic "1" = Odd Address and logic "0" = Even Address.

Bits (6:0)

EGA: Same as End Horizontal Retrace Registers Bits (6:0) definition in VGA section.

B.3.5 Vertical Total Register, (Index = 06)

Bits (7:0)

EGA: Lower eight bits of the CRT vertical frame time in scan lines including the vertical retrace.

B.3.6 CRT Controller Overflow Register, (Index = 07)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Same as Preset Row Scan Register Bit (4:0) definitions in the VGA section.

B.3.7 Preset Row Scan Register, (Index = 08)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Same as Preset Row Scan Register (4:0) definition in the VGA section.

B.3.8 Maximum Scan Line Register, (Index = 09)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Same as maximum Scan Line Register Bits (4:0) definition in the VGA section.

B.3.9 Cursor Start Register (Index = 0A)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Same as Cursor Start Register Bits (4:0) definition in the VGA section.

B.3.10 Cursor End Register (Index = 0B)

Bit(7)

EGA: Not Used.

Bits (6:5)

EGA: They define cursor signal skew in character clocks.

BIT 6	BIT 5	SKEW
0	0	0
0	1	0
1	0	1
1	1	2

Bits (4:0)

EGA: These bits define Cursor End value of row scan address counter. The programmed value is equal to "N+1" where "N" is the last row of the Cursor to be displayed.

B.3.11 Vertical Retrace Start Register, (Index = 10) - Write

(Light Pen High register, Index = 10 - Read)

Bits (7:0)

EGA: Lower eight bits of the vertical retrace start position programmed in horizontal scan lines.

B.3.12 Vertical Retrace End Register, (Index = 11) - Write

(Light Pen Low register, Index = 11 - Read)

Bits (7:6)

EGA: Not Used.

Bit 5

EGA: It enables the IRQ output buffer control if Logic 0 is programmed. The IRQ latch within the CRT controller determines the logic state of the IRQ output signal. If programmed as logic 1, the IRQ buffer is switched to a high impedance state.

Bit 4

EGA: When programmed to logic 0, the IRQ latch is reset and cleared to 0 if Bit 5 = 0. If it is logic 1, the IRQ latch gets set at the end of the vertical display.

Bits (3:0)

EGA: Identical to Vertical Retrace End Register Bits (3:0) definition in the VGA section.

B.3.13 Underline Location Register, (Index = 14)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Horizontal scan row where the underline will be displayed. Value programmed is one less than the scan line desired.

B.3.14 End Vertical Blanking Register, (Index = 16)

Bits (7:5)

EGA: Not Used.

Bits (4:0)

EGA: Identical to End Vertical Blanking Register Bits (4:0) definition in the VGA section.

B.3.15 Mode Control Register, (Index = 17)

Bits (7:5)

EGA: Same as Mode Control Register Bits (7:5) definition in the VGA section.

Bit 4

EGA: Not Used.

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

B.4 GRAPHICS CONTROLLER REGISTERS (PORT 3CF)

B.4.1 Read Map Select Register, (Index = 04)

Bits (7:3)

EGA: Not Used.

Bits (2:0)

EGA: Map selected bits (2:0) which represent encoded value of the memory plane in binary as shown below:

D2	D1	D0	MAP SELECTED
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3

B.4.2 Mode Register, (Index = 05)

Bit (7:6)

EGA: Not Used.

Bits (5:2)

EGA: Identical to Mode Register Bits (5:2) definition in the VGA section.

Bits (1:0)

EGA: Binary coded write bits define the write modes per table below:

BIT 1	BIT 0	FUNCTION
0	0	Write mode 0 - Refer to earlier section
0	1	Write mode 1 - Refer to earlier section
1	0	Write mode 2 - Refer to earlier section
1	1	Write mode 3 - Not Legal. Selects write mode 1.

B.5 ATTRIBUTE CONTROLLER REGISTERS (PORTS = 3C0/3C1)

Palette Registers (Index = 00 through 0F)

Bits (7:6)

EGA: Not Used.

Bits (5:0)

EGA: Dynamic color selection. Logic 0 = Color deselection, and Logic 1 = color selection per the table below:

BITS	COLOR	PIXEL
5	Sec. Red	VID 5
4	Sec Green/Inten	VID 4
3	Sec Blue/Mono	VID 3
2	Red	VID 2
1	Green	VID 1
0	Blue	VID 0

B.5.1 Mode Control Register, (Index = 10)

Bits (7:4)

EGA: Not Used.

Bits (3:0)

EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

B.5.2 Overscan Color Register, (Index = 11)

Bits (7:6)

EGA: Not Used.

Bits (5:0)

EGA: Overscan color for the border. For a monochrome display, set all the 6 bits to logic 0. The border color is defined by the color table for the Palette registers shown above.

B.5.3 Color Plane Enable Register, (Index = 12)

Bits (7:6)

EGA: Same as Color Plane Enable Register Bits (7,6) in the VGA section.

Bits (5:4)

EGA:
Determines two of six colors for the Video Status Multiplexer according to the following table.

BIT 5	BIT 4	INPUT STATUS REGISTER 1 (PORT 3?A)	
		BIT 5	BIT 4
0	0	VID 2 (Red)	VID 0 (Blue)
0	1	VID 5 (SRed)	VID 4 (SGreen)
1	0	VID 3 (SBlue)	VID 1 (Green)
1	1	VID 5 (SRed)	VID 4 (SGreen)

Bits (3:0)

EGA: Same as Color Plane Enable Register Bits (3:0) definition in the VGA section.

B.5.4 Horizontal PEL Panning Register, (Index = 13)

Bits (7:4)

EGA: Not Used.

Bits (3:0)

EGA: These 4 bits determine the horizontal left shift of the video data in number of pixels. In monochrome alpha numeric modes, a 9-dots/character image can be shifted by 9 pixels. For all other graphics or alpha numeric modes, a maximum left shift of 8 pixels is permitted. Refer to the left shift pixel table of the Horizontal PEL Panning Register Bits (3:0) described in the VGA section.

B.6 MONITOR DETECTION

The DAC output currents I_{RED}, I_{GREEN}, and I_{BLUE}, develop a voltage across the load resistances R_{LD}. These voltages are sent to comparators against a voltage derived from the external voltage reference V_{REF}. For the WD90C20, the output current is determined by the formula:

$$I = \frac{code \times 0.04 \times V_{REF}}{R_{SET}}$$

where the codes range from 0 to 63 (0H to 3FH) for a 6-bit DAC.

For the WD90C20A, the output current is determined by the formula:

$$I = \frac{code \times V_{REF} \times 1.036}{R_{SET}}$$

The output signal MDETECT is readable at port 3C2H bit 4. It is important to read during active video ouput, not during retrace or any other blanking period.

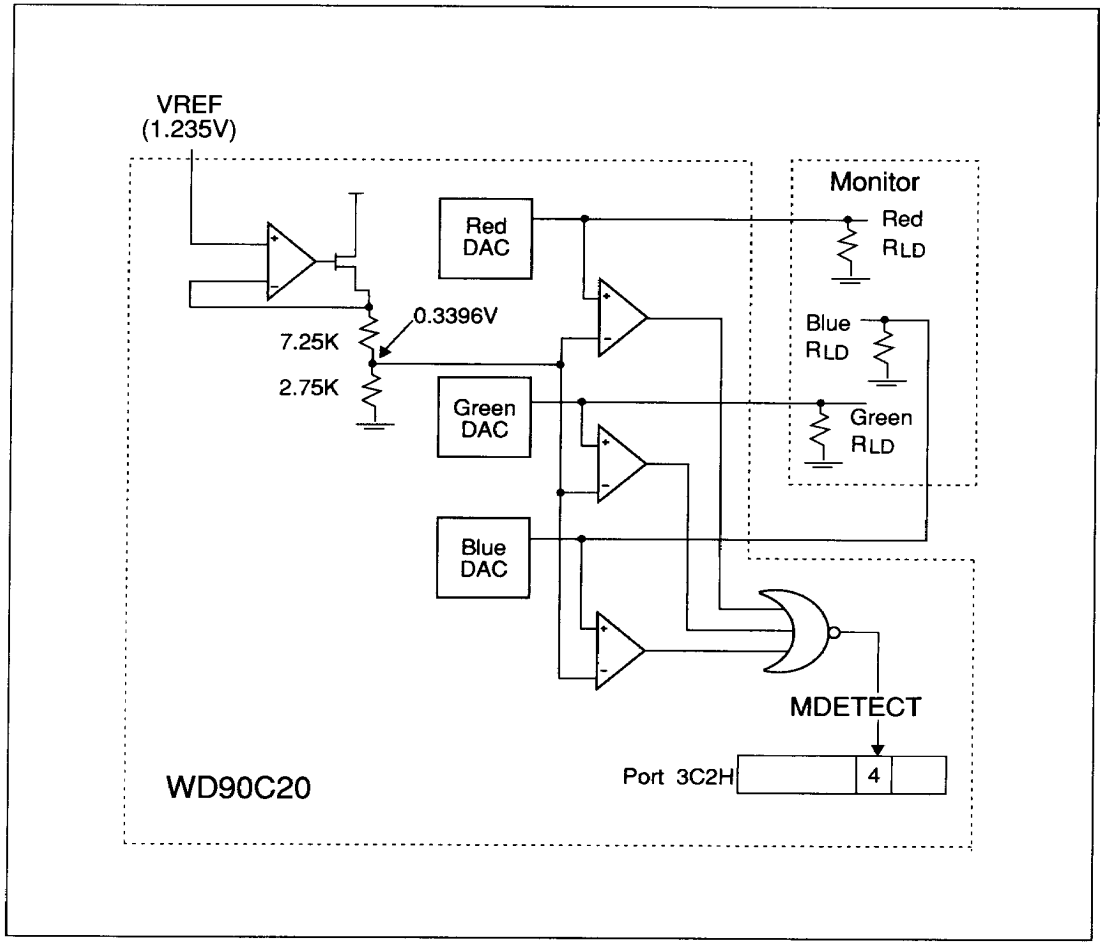

FIGURE B-1. MONITOR DETECTION FOR INTERNAL RAMDAC

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C.0 AC OPERATING CHARACTERISTICS AND TIMING DIAGRAMS

FIGURE NUMBER	TITLE
C-1	I/O Write – AT Mode
C-2	I/O Read – AT Mode
C-3	Memory Write – AT Mode
C-4	Memory Read – AT Mode
C-5	I/O Write – Micro Channel Mode
C-6	I/O Read – Micro Channel Mode
C-7	Memory Write – Micro Channel Mode
C-8	Memory Read – Micro Channel Mode
C-9	CPU Write with Non-Page Mode
C-10	CPU Read Non-Page Mode, CRT Read
C-11	DRAM Page Mode Read Timing
C-12	WD90C20 LCD Timing (t = VCLK)
C-13	RAMDAC Timing
C-14	CRT Clock Timing
C-15	Reset Timing
C-16	RAS OnlyDRAM Refresh Timing
C-17	CAS Before RAS DRAM Refresh Timing
C-18	CAS Before RAS Refresh (Power-Down Mode)
C-19	STN Color LCD Interface Timing
C-20	IOCHRDY Release Timing in Memory Read Cycle
C-21	IOCHRDY Release Timing in Memory Write Cycle

TABLE C-1. TIMING DIAGRAMS

NOTE:

The following timing values are the same for the WD90C20 and WD90C20A, except as noted.

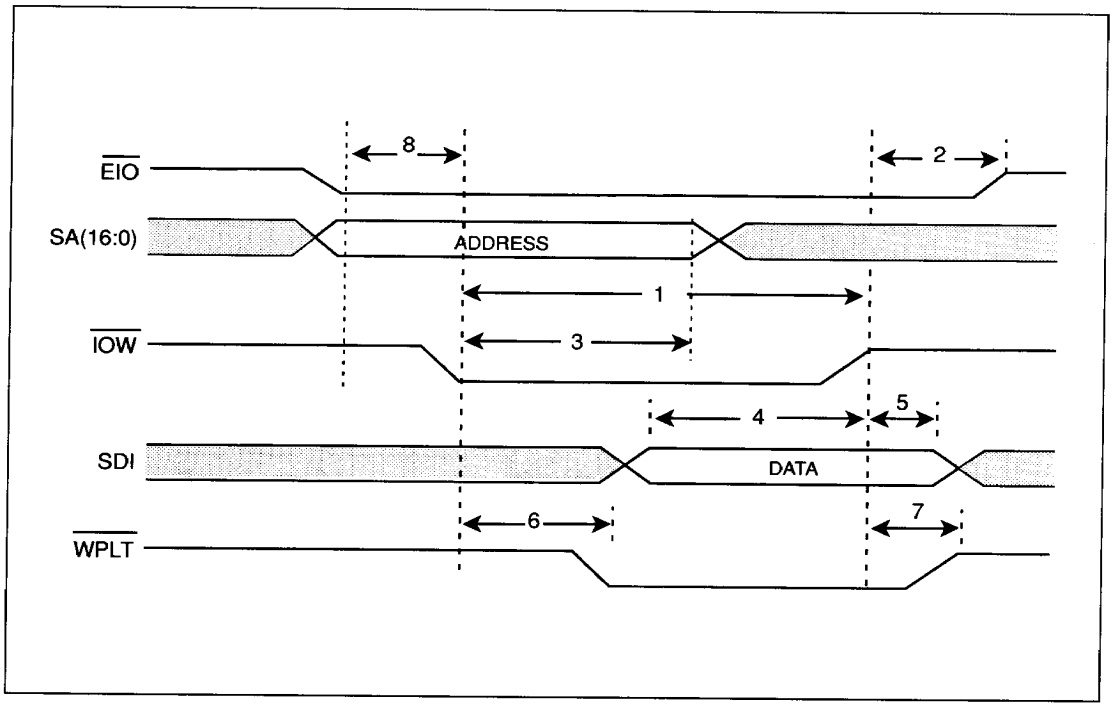

FIGURE C-1. I/O WRITE-AT MODE

NO.	I/O WRITE AT MODE			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1	$\overline{IOW}$	active pulse width		2.5t			
2	$\overline{EIO}$	hold from	$\overline{IOW}$ inactive (high)	10			
3	SA(16:0),	hold from	$\overline{IOW}$ active	30		25	
4	Write Data SDI	setup to	$\overline{IOW}$ inactive	30			
5	Write Data SDI	hold from	$\overline{IOW}$ inactive	10			
6	$\overline{WPLT}$	active from	$\overline{IOW}$ active (C_L = 15pF)		50		45
7	$\overline{WPLT}$	inactive from	$\overline{IOW}$ inactive (C_L = 15pF)		50		45
8	$\overline{EIO}$, SA(16:0)	setup to	$\overline{IOW}$ active	15			

t = 1/MCLK

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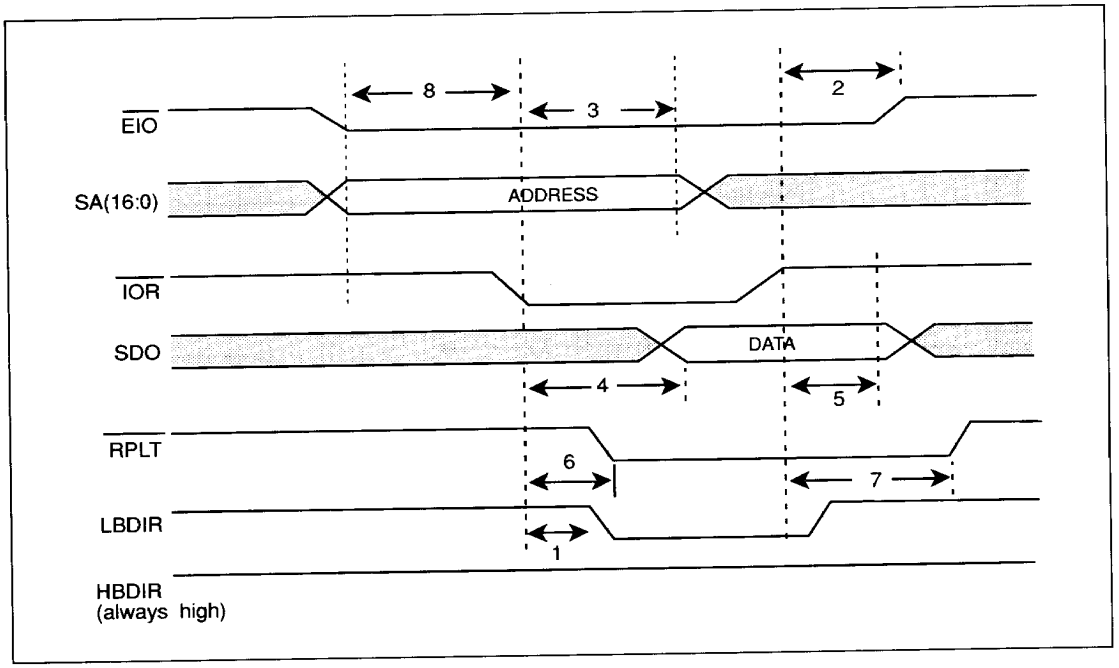

FIGURE C-2. I/O READ-AT MODE

NO.	I/O READ AT MODE			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1	LBDIR	delay from	$\overline{IOR}$		48		43
2	$\overline{EIO}$	hold from	$\overline{IOR}$ inactive (high)	10			
3	SA(16:0),	hold from	$\overline{IOR}$ active	25			
4a	Read Data SDO	valid from	$\overline{IOR}$ active	.5T	1.5T+65		1.5t+60
4b	Read Data SDO	valid from for mapping RAM only	$\overline{IOR}$ active		4t+65		1.5t+60
5	Read Data SDO	hold from	$\overline{IOR}$ inactive	10	40		
6	$\overline{RPLT}$	active from	$\overline{IOR}$ active (C_L = 15pF)		50		45
7	$\overline{RPLT}$	inactive from	$\overline{IOR}$ inactive (C_L = 15pF)		50		45
8	$\overline{EIO}$, SA(16:0)	setup to	$\overline{IOR}$ active	15			

T = 1/MCLK

Note: For mapping RAM access, a minimum inactive time of 3 VCLK cycles are required between consecutive I/O transfers.

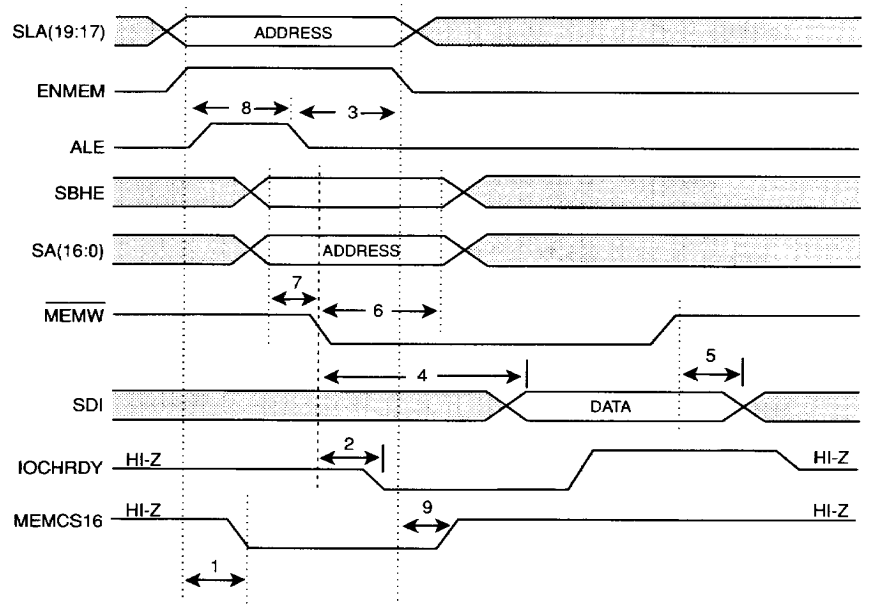

FIGURE C-3. MEMORY WRITE - AT MODE

NO.	MEMORY WRITE AT MODE			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1	MEMCS16	valid from	SLA (19:17) ENMEM valid		21		
2	IOCHRDY	inactive from	MEMW active	10			
3	SLA(19:17), ENMEM	hold from	ALE inactive	5			
4	Data SDI	valid from	MEMW active	30		25	
5	Data SDI	hold from	MEMW inactive	5			
6	SA(16:0), SBHE	hold from	MEMW active	20			
7	SA(16:0), SBHE	setup to	MEMW active	25			
8	SLA(19:17), ENMEM	setup to	ALE inactive	25			
9	MEMCS16	invalid from	SLA (19:17) ENMEM invalid		35		30

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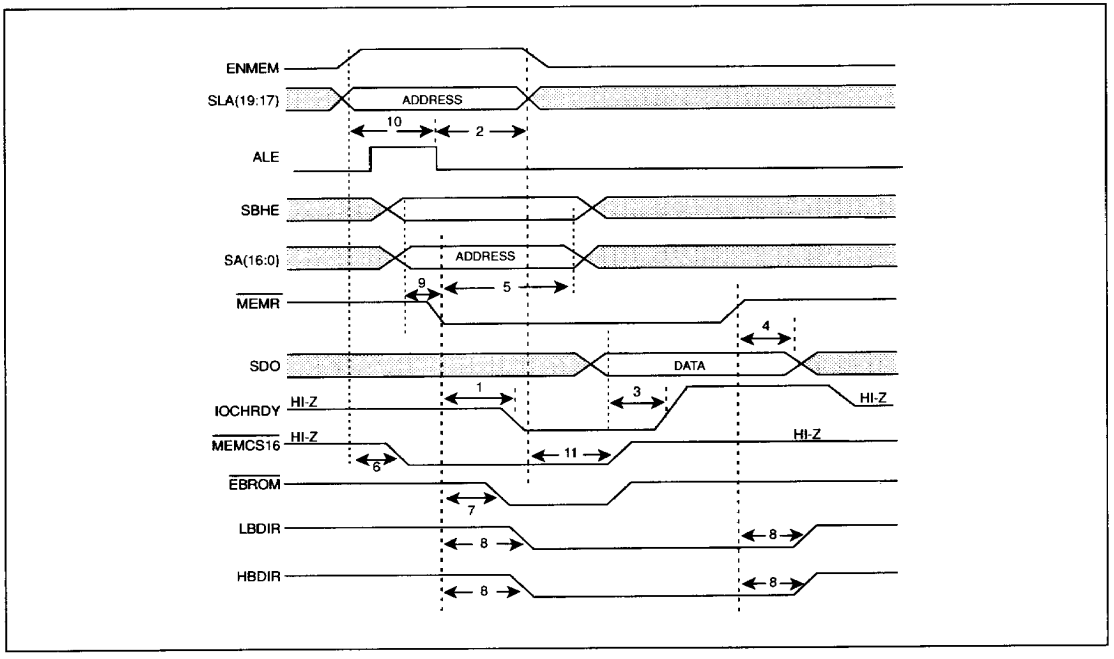

FIGURE C-4. MEMORY READ - AT MODE

NO.	MEMORY READ – AT MODE			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1	IOCHRDY	inactive from	MEMR active		26		
2	SLA(19:17), ENMEM	hold from	ALE inactive	30		25	
3	Data SDO	valid setup to	IOCHRDY active	1.5t-25			
4	Data SDO	hold from	MEMR	10	50		
5	SA(16:0), SBHE	hold from	MEMR active	20			
6	MEMCS16	valid from	SLA(19:17) ENMEM valid		24		
7	MEMR	active to	EBROM active		50		45
8	LBDIR HBDIR	delay from	MEMR		60		45
9	SA(16:0), SBHE	setup to	MEMR active	25			
10	SLA(19:17), ENMEM	setup to	ALE inactive	25			
11	MEMCS16	invalid from	SLA(19:17) ENMEM invalid		35		30

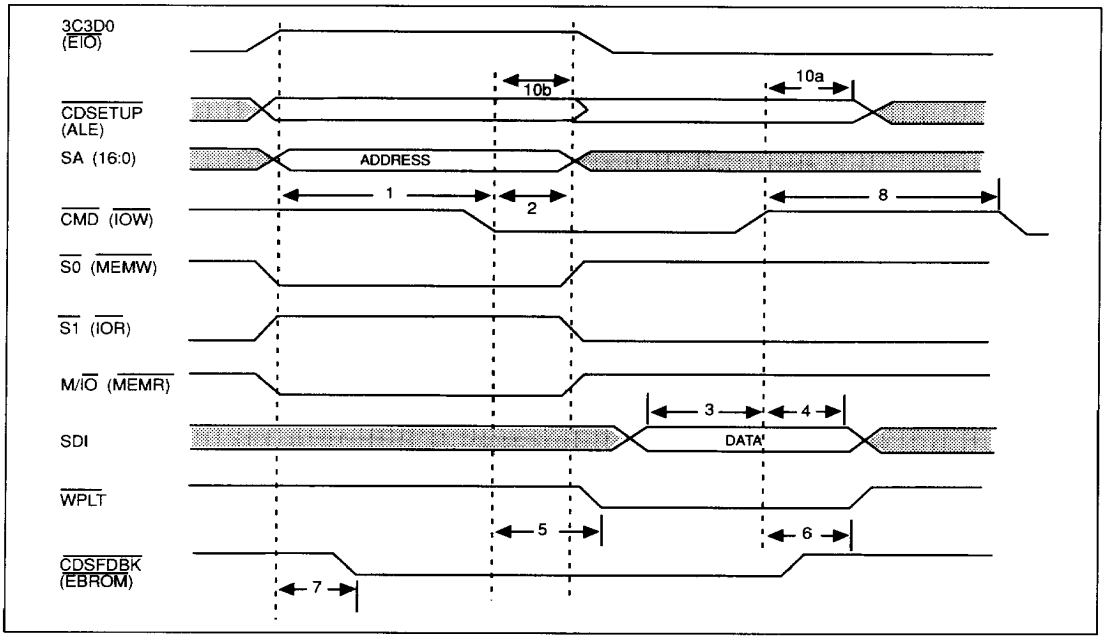

FIGURE C-5. I/O WRITE-MICRO CHANNEL MODE

NO.	I/O WRITE – MC MODE			WD90C20		WD90C20A	
				MIN.	MAX	MIN.	MAX
1	SA(16:0), S0, S1 3C3D0, CDSETUP, M/IO	setup to	CMD active (low)	15			
2	SA(16:0), S0, S1 3C3D0, M/IO	hold from	CMD active	30		25	
3	Write data SDI	setup to	CMD inactive	30			
4	Write data SDI	hold from	CMD inactive	10			
5*	WPLT	active from	CMD active		50		45
6*	WPLT	inactive from	CMD inactive		50		45
7	CDSFDBK	active from	Address Valid		58		53
8	CMD	inactive pulse width		2t			
9	CMD	active pulse width		2.5t			
10a	CDSETUP (WD90C20)	hold from	CMD inactive (high)	2t+30		2t+25	
10b	CDSETUP (WD90C20A)	hold from	CMD active (low)	30		25	

* C_L = 15pF
t = 1/MCLK

Note: For mapping RAM access, a minimum inactive time of 3 VCLK cycles are required between consecutive I/O transfers.

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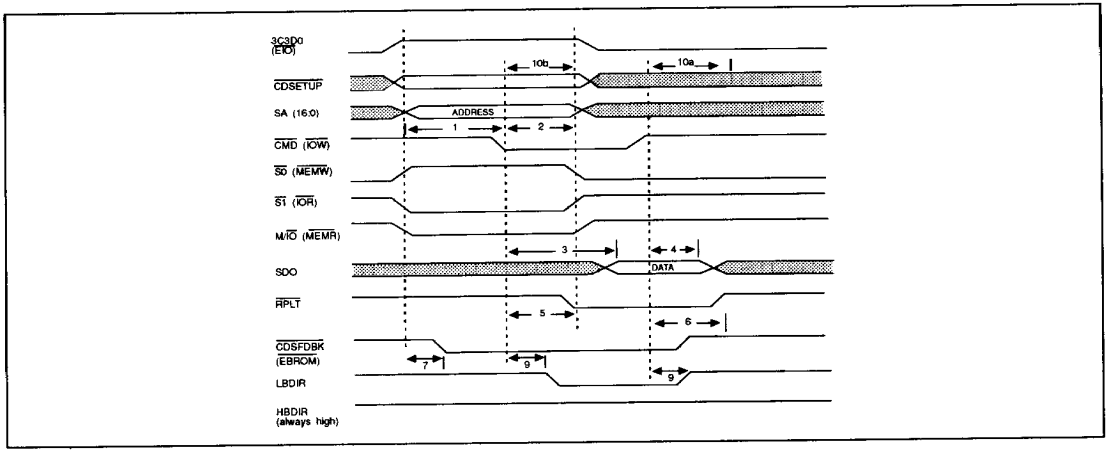

FIGURE C-6. I/O READ - MICRO CHANNEL MODE

NO.	I/O READ MC MODE			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1	SA(16:0), $\overline{S0}$, $\overline{S1}$, 3C3D0, $\overline{CDSETUP}$, M/$\overline{IO}$	setup to	$\overline{CMD}$ active (low)	15			
2	SA(16:0), $\overline{S0}$, $\overline{S1}$, 3C3D0, M/$\overline{IO}$	hold from	$\overline{CMD}$ active	30		25	
3a	Read data SDO	valid from	$\overline{CMD}$ active	.5T	1.5T+65		1.5t+60
3b	Read data SDO	valid from mapping RAM only	$\overline{CMD}$ active		4t+65		4t+60
4	Read data SDO	hold from	$\overline{CMD}$ inactive	10	40		
5	$\overline{RPLT}$	active from	$\overline{CMD}$ active (C_L = 15pF)		50		45
6	$\overline{RPLT}$	inactive from	$\overline{CMD}$ inactive (C_L = 15pF)		50		45
7	$\overline{CDSFDBK}$	active from	Address Valid		58		53
8a 8b	$\overline{CMD}$ $\overline{CMD}$	active pulse width active pulse width mapping RAM only		130 4t+30		4t+25	
9	LBDIR	delay from	$\overline{CMD}$		48		43
10a 10b	$\overline{CDSETUP}$ (WD90C20) $\overline{CDSETUP}$ (WD90C20A)	hold from $\overline{CMD}$ inactive (high) hold from CMD active (low)		2t+30 30		2t+25 25	

T = 1/MCLK

Note: For mapping RAM access, a minimum inactive time of 3 VCLK cycles are required between consecutive I/O transfers.

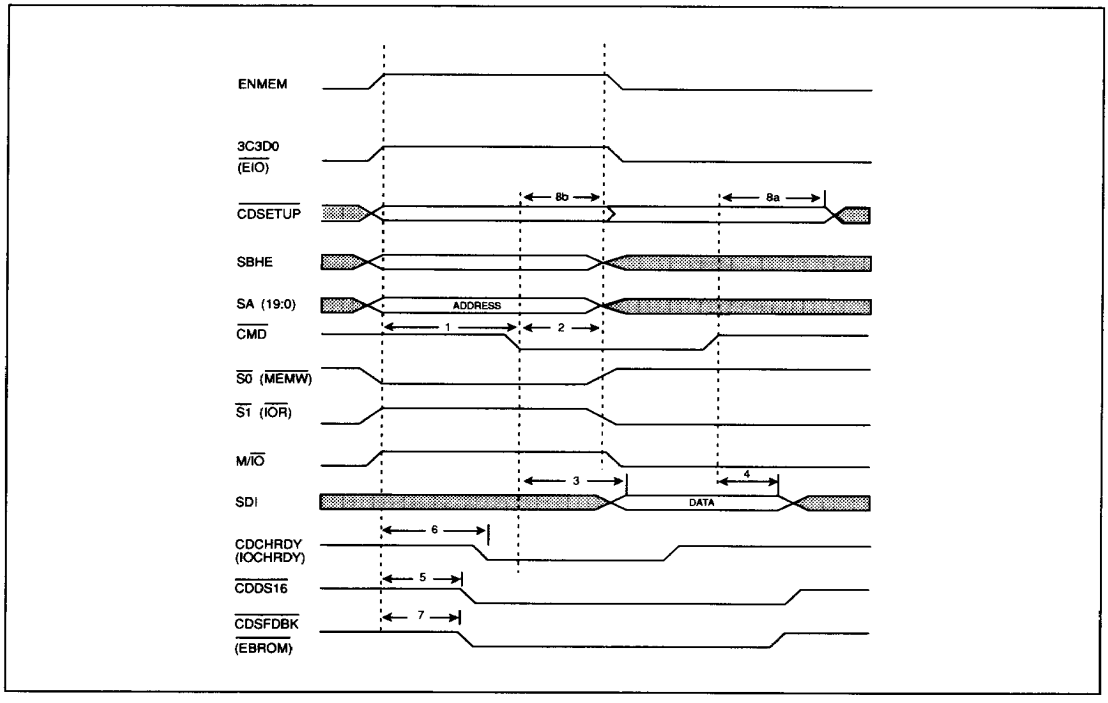

FIGURE C-7. MEMORY WRITE-MICRO CHANNEL MODE

NO.	MEMORY WRITE MC MODE			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1	SA(19:0), S0, S1, ENMEM, SBHE, 3C3D0, CDSETUP, M/IO	setup to	CMD active (low)	25			
2	SA(19:0), S0, S1, ENMEM, SBHE, 3C3D0, M/IO	hold from	CMD active	30		25	
3	Data SDI	valid from	CMD active		25		
4	Data SDI	hold from	CMD inactive	0			
5	CDDS16	valid from	SA(19:0) ENMEM valid		45		
6	SA(19:10) S0, S1	valid to	CDCHRDY inactive (low)		40		
7	CDSFDBK	active from	Address Valid		58		53
8a	CDSETUP (WD90C20)	hold from	CMD inactive (high)	2t+30		2t+25	
8b	CDSETUP(WD90C20A)	hold from	CMD active (low)	30		25	

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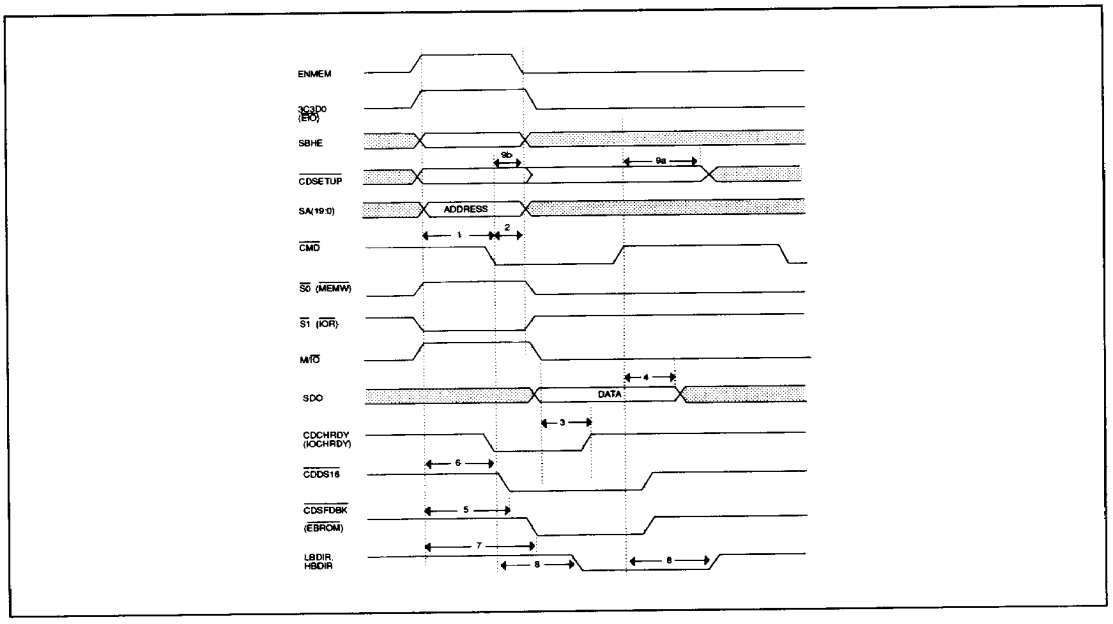

FIGURE C-8. MEMORY READ-MICRO CHANNEL MODE

NO.	MEMORY READ MC MODE		WD90C20		WD90C20A	
			MIN.	MAX.	MIN.	MAX.
1	SA(19:0), $\overline{S0}$, $\overline{S1}$, ENMEM, SBHE, 3C3D0, $\overline{CDSETUP}$, M/$\overline{IO}$	setup to $\overline{CMD}$ active (low)	25			
2	SA(19:0), $\overline{S0}$, $\overline{S1}$ ENMEM, SBHE, 3C3D0, M/$\overline{IO}$	hold from $\overline{CMD}$ active	30		25	
3*	Read data SDO valid	setup to CDCHRDY active (high)	1.5t-25			
4	Read data SDO	hold from $\overline{CMD}$ inactive	10	50		45
5	$\overline{CDDS16}$	valid from SA(19:0) $\overline{ENMEM}$ valid		45		40
6	SA(19:0) $\overline{S0}$, $\overline{S1}$	valid to CDCHRDY inactive (low)		40		
7	$\overline{CDSFBK}$	active from Address Valid		58		53
8	HBDIR, LBDIR	delay from $\overline{CMD}$		60		55
9a 9b	$\overline{CDSETUP}$ (WD90C20) $\overline{CDSETUP}$ (WD90C20A)	hold from $\overline{CMD}$ inactive (high) hold from $\overline{CMD}$ active (low)	2t+30 30			2t+25 25

NOTES: * PR1A (7:6) = 00

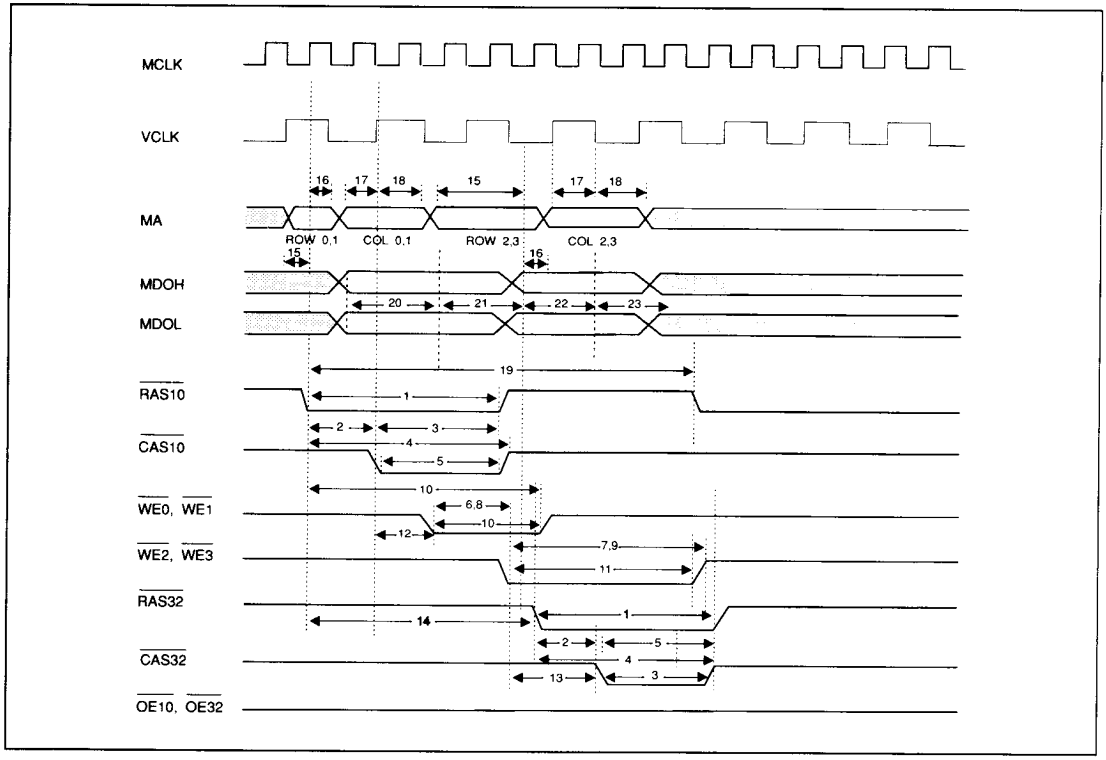

FIGURE C-9. CPU WRITE WITH NON-PAGE MODE

NO.	CPU WRITE MCLK = 45.046 MHz		WD90C20		WD90C20A	
			MIN.	MAX.	MIN.	MAX.
1	$\overline{RAS10}$ ($\overline{RAS32}$)	pulse width low	5t-25	5t	5t-20	
2	$\overline{RAS10}$ ($\overline{RAS32}$)	low to $\overline{CAS10}$ ($\overline{CAS32}$)(low)	2t-11	2t+2	2t-6	
3	$\overline{CAS10}$ ($\overline{CAS32}$)	low to $\overline{RAS10}$ ($\overline{RAS32}$)(high)	3t-20	3t+10	3t-5	
4	$\overline{RAS10}$ ($\overline{RAS32}$)	low to $\overline{CAS10}$ ($\overline{CAS32}$)(high)	5t-25	5t	5t-20	
5	$\overline{CAS10}$ ($\overline{CAS32}$)	pulse width low	3t-25	3t	3t-20	
6	$\overline{WE0}$, $\overline{WE1}$	low to $\overline{CAS10}$ (high)	2.5t-20	2.5t	2.5t-15	
7	$\overline{WE2}$, $\overline{WE3}$	low to $\overline{CAS32}$ (high)	5t-20	5t	5t-15	
8	$\overline{WE0}$, $\overline{WE1}$	low to $\overline{RAS10}$ (high)	2.5t-20	2.5t+2	2.5t-15	
9	$\overline{WE2}$, $\overline{WE3}$	low to $\overline{RAS32}$ (high)	5t-20	5t+2	5t-15	
10	$\overline{WE0}$, $\overline{WE1}$	pulse duration	3t-20	3t	3t-15	
11	$\overline{WE3}$, $\overline{WE2}$	pulse duration	5t-20	5t	5t-15	
12	$\overline{WE0}$, $\overline{WE1}$	low from $\overline{CAS10}$ (low)	0.5t-5	0.5t+6		

t = 1/MCLK

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NO.	CPU WRITE MCLK = 45.046 MHz (CONTINUED)		WD90C20		WD90C20A	
			MIN.	MAX.	MIN.	MAX.
13	$\overline{WE2}$, $\overline{WE3}$	low to $\overline{CAS32}$ (low)	2t-10	2t		
14	$\overline{RAS10}$	low to $\overline{RAS32}$ (low)	4.5t-7	4.5t+7		
15	Row address	setup to $\overline{RAS10}$, $\overline{RAS32}$ (low)	t-15	t+15		
16	Row address	hold from $\overline{RAS10}$, $\overline{RAS32}$ (low)	t-5	t+15		
17	Column address	setup to $\overline{CAS10}$, $\overline{RAS32}$ (low)	t-25	t+10	t-20	
18	Column address	hold from $\overline{CAS10}$, $\overline{CAS32}$ (low)	1.5t-5	1.5t+20		1.5t+15
19	Random Write Cycle		9t			
20	Write Data	setup to $\overline{WE0}$, $\overline{WE1}$ (low)	t-10			
21	Write Data	hold from $\overline{WE0}$, $\overline{WE1}$ (low)	2t-5			
22	Write Data	setup to $\overline{CAS32}$ (low)	2t-5			
23	Write Data	hold from $\overline{CAS32}$ (low)	t-5			

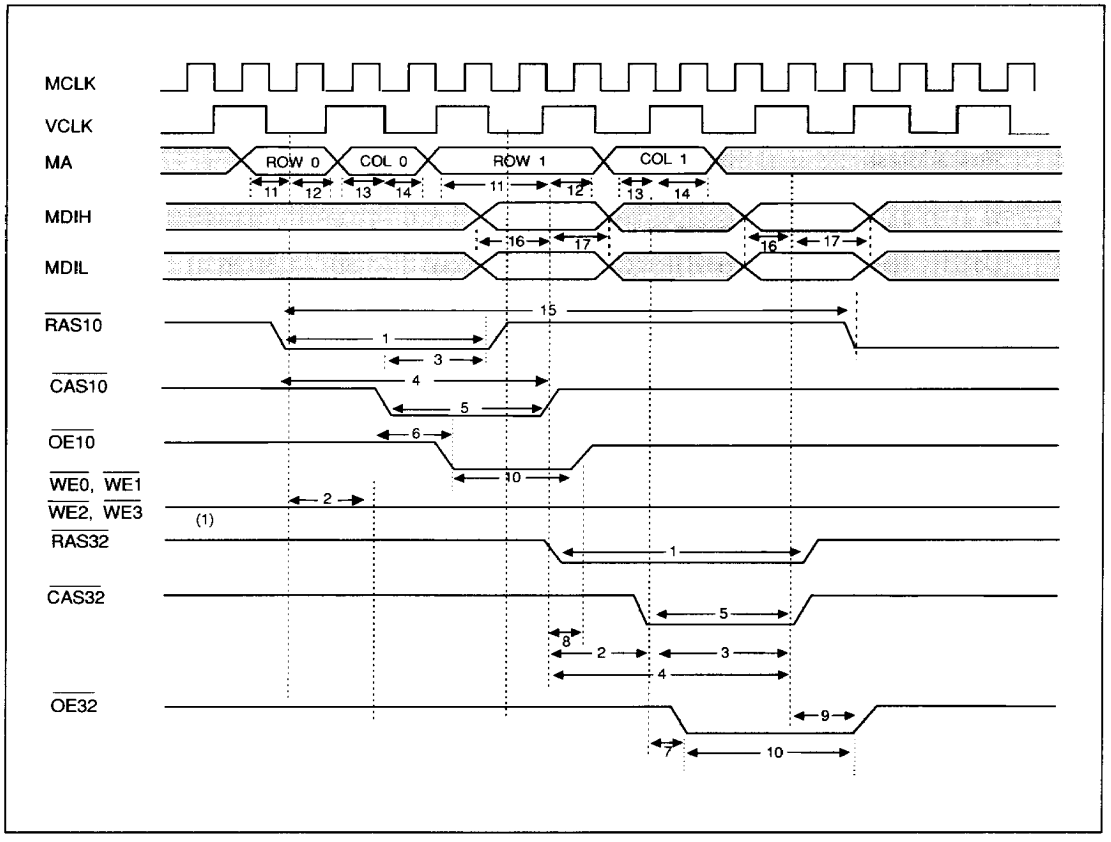

FIGURE C-10. CPU READ NON-PAGE MODE, CRT READ

NO.	CPU READ AND CRT READ, NON-PAGE MODE MCLK = 45.046 MHz			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1	RAS10 (RAS32)	pulse width low		5t-25	5t	5t-20	
2	RAS10 (RAS32)	low to	CAS10 (CAS32)(low)	2t-11	2t+2		
3	CAS10 (CAS32)	low to	RAS10 (RAS32)(high)	3t-15	3t+10	3t-12	
4	RAS10 (RAS32)	low to	CAS10 (CAS32)(high)	5t-20	5t	5t-15	
5	CAS10 (CAS32)	pulse width low		3t-20	3t	3t-15	
6	CAS10	low to	OE10 (low)	t-6	t+5		
7	CAS32	low to	OE32 (low)	t-6	t+5		
8	CAS10	high to	OE10 (high)	t-6	t+5		

t = 1/MCLK

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NO.	CPU READ AND CRT READ, NON-PAGE MODE MCLK = 45.046 MHz (CONTINUED)		WD90C20		WD90C20A	
			MIN.	MAX.	MIN.	MAX.
9	$\overline{CAS32}$ high	to $\overline{OE32}$ (high)	t-6	t+5		
10	$\overline{OE10}$, $\overline{OE32}$	pulse width low	3t-20	3t	3t-15	
11	Row address	setup to $\overline{RAS10}$, $\overline{RAS32}$ (low)	t-12	t+10		
12	Row Address	hold from $\overline{RAS10}$, $\overline{RAS32}$ (low)	t-5	t+15		t+12
13	Column Address	setup to $\overline{CAS10}$, $\overline{CAS32}$ (low)	t-12	t+10		
14	Column Address	hold from $\overline{CAS10}$,$\overline{CAS32}$ (low)	1.5t	1.5t+25		1.5t+20
15	Random Read Cycle		9t-2			
16	Read Data	setup to $\overline{CAS10}$, $\overline{CAS32}$ (high)	10			
17	Read Data	hold from $\overline{CAS10}$, $\overline{CAS32}$ (high)	15			

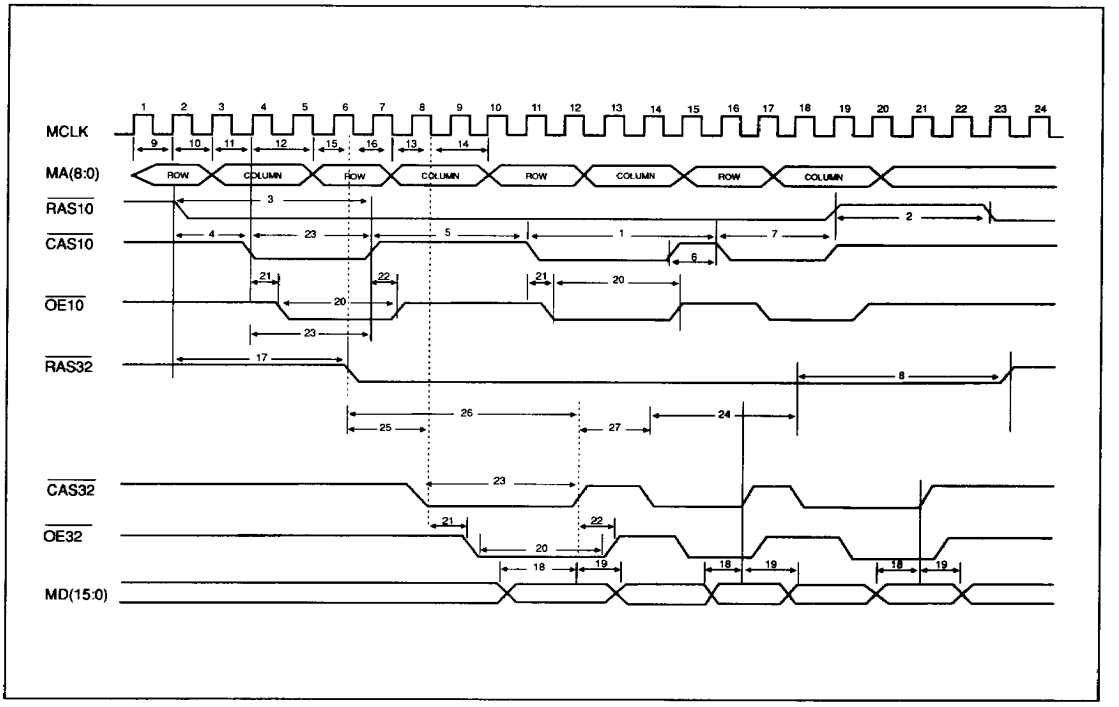

FIGURE C-11. DRAM PAGE MODE-READ TIMING

NO.	PAGE MODE READ ACCESSES MCLK = 45.046 MHz			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1*	Page mode	cycle time	$\overline{CAS10}$ low to CAS low	5t-2			
2	$\overline{RAS10}$	Precharge		4t-6	4t+14		4t+10
3	$\overline{RAS10}$	low to	$\overline{CAS10}$ high (first)	5t-20	5t-2	5t-15	
4	$\overline{RAS10}$	low to	$\overline{CAS10}$ low	2t-11	2t+2		
5	First $\overline{CAS10}$	pulse width high		4t-10	4t+10		
6	$\overline{CAS10}$	pulse width high		2t-10	2t+10		
7	$\overline{CAS10}$	low to	$\overline{RAS10}$ high	3t-15	3t+4	3t-12	
8	$\overline{CAS32}$	low to	$\overline{RAS32}$ high	5t-15	5t+4	5t-12	
9	Row address	setup to	$\overline{RAS10}$ low	t-5	t+16		t+12
10	Row address	hold from	$\overline{RAS10}$ low	t-5	t+5		
11	Column address	setup to	$\overline{CAS10}$ low	t-15	t+1		
12	Column address	hold from	$\overline{CAS10}$	1.5t	1.5t+18		
13	Column address	setup to	$\overline{CAS32}$	t-15	t+8		

* First cycle is +2t longer than this spec
t = 1/MCLK

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NO.	PAGE MODE READ ACCESSES MCLK = 45.046 MHz (CONTINUED)			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
14	Column address	hold from	$\overline{CAS32}$ low	1.5t-15	1.5t+2	1.5t-12	
15	Row address	setup to	$\overline{RAS32}$ low	t-15	t+5	t-12	
16	Row address	hold from	$\overline{RAS32}$ low	t-8	t+5		
17	$\overline{RAS32}$	low from	$\overline{RAS10}$ low	4.5t-7	4.5t+7		
18	Read data	setup to	CAS high	15			
19	Read data	hold from	CAS high	15			
20	$\overline{OE10}$ ($\overline{OE32}$)	pulse width low		3t-20	3t	3t-15	
21	$\overline{OE10}$ ($\overline{OE32}$)	low after	$\overline{CAS10}$ low ($\overline{CAS32}$)	t-6	t+6		
22	$\overline{OE10}$ ($\overline{OE32}$)	high after	$\overline{CAS10}$ high ($\overline{CAS32}$)	t-6	t+6		
23	$\overline{CAS10}$ ($\overline{CAS32}$)	pulse width low		3t-20	3t	3t-15	
24	Page mode	cycle time	$\overline{CAS32}$ low to $\overline{CAS32}$ low	5t-2			
25	$\overline{RAS32}$	low to	$\overline{CAS32}$ high (first)	5t-22	5t	5t-15	
26	$\overline{RAS32}$	low to	$\overline{CAS32}$ low	2t-11	2t+2		
27	First $\overline{CAS32}$	pulse width high		2t-11	2t+11		

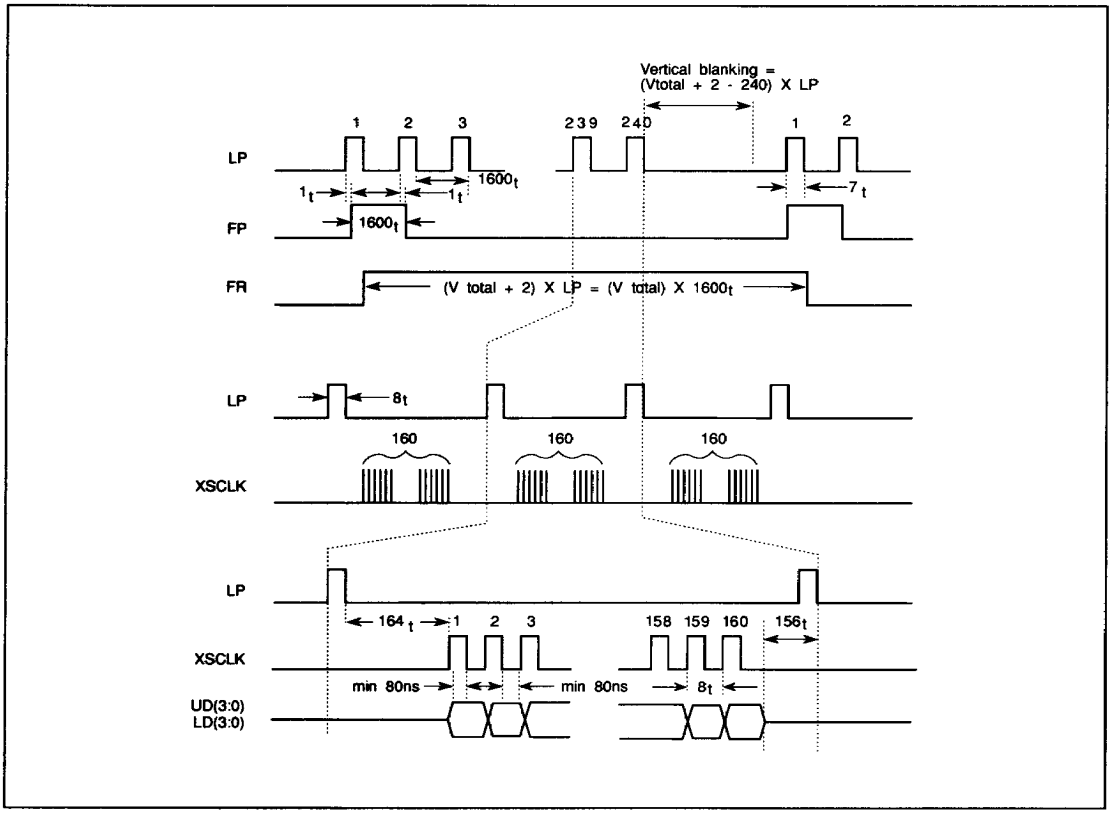

FIGURE C-12. WD90C20 LCD TIMING DIAGRAM (t=VCLK)

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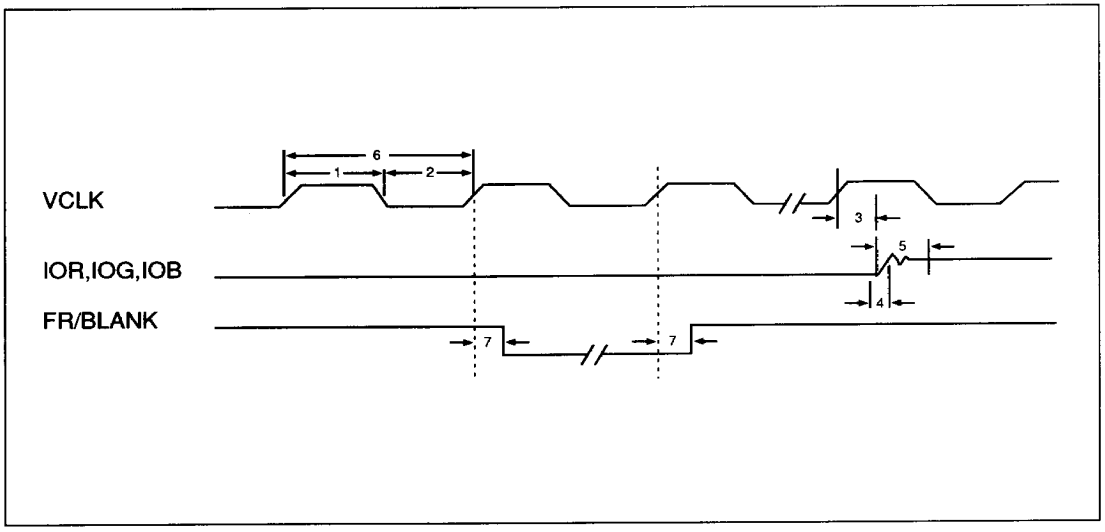

FIGURE C-13. RAMDAC TIMING

NO.	PARAMETER	WD90C20			WD90C20A			UNITS
		MIN.	TYP	MAX	MIN.	TYP	MAX	
1	VCLK Pulse Width High Time	9						ns
2	VCLK Pulse Width Low Time	9						ns
3	Analog Output Delay			30			25	ns
4	Analog Output Rise/Fall Time		3					ns
5	Analog Output Settling Time		20					ns
6	Clock Frequency			45			50	MHz
7	Blanking Delay Time			45				ns

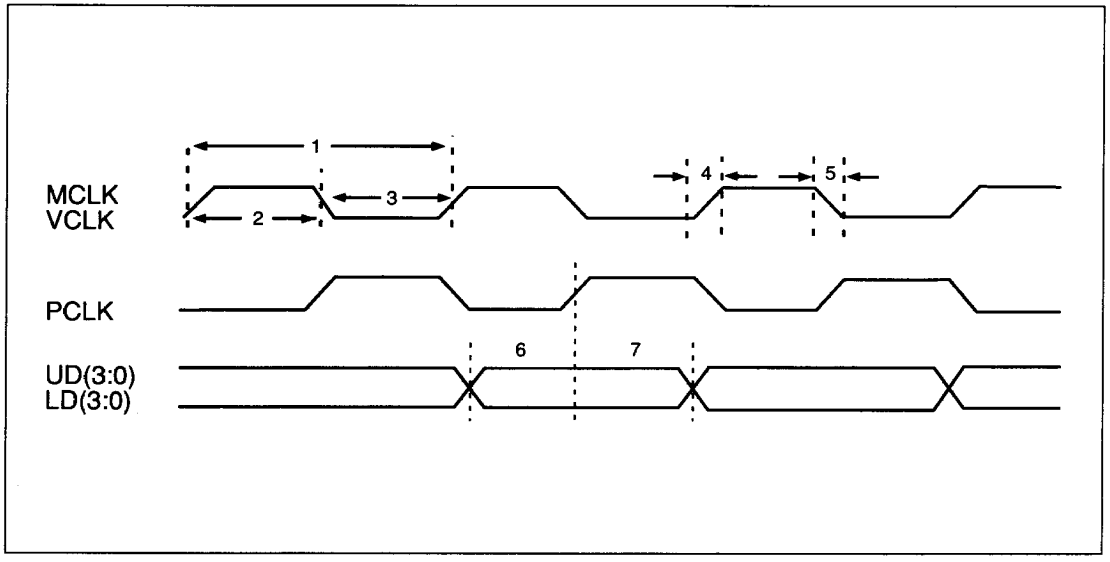

FIGURE C-14. CRT CLOCK TIMING

NO.	PARAMETER	WD90C20		WD90C20A	
		MIN.	MAX	MIN.	MAX
1	Input Clock (VCLK, MCLK)	t	t		
2	Input Clock High Time	40%	60%		
3	Input Clock Low Time	40%	60%		
4	Input Clock Rise Time		3		
5	Input Clock Fall Time		3		
6*	UD(3:0), LD(3:0) setup time to PCLK (high)				
	Mode 0	20			
	Mode 3	10			
	Mode 4	20			
	Mode 12	10			
	Mode 13	15		20	
7*	UD(3:0), LD(3:0) hold time from PCLK (high)				
	Mode 0	10			
	Mode 3	10			
	Mode 4	10			
	Mode 12	10			
	Mode 13	-25		20	

* For external RAMDAC

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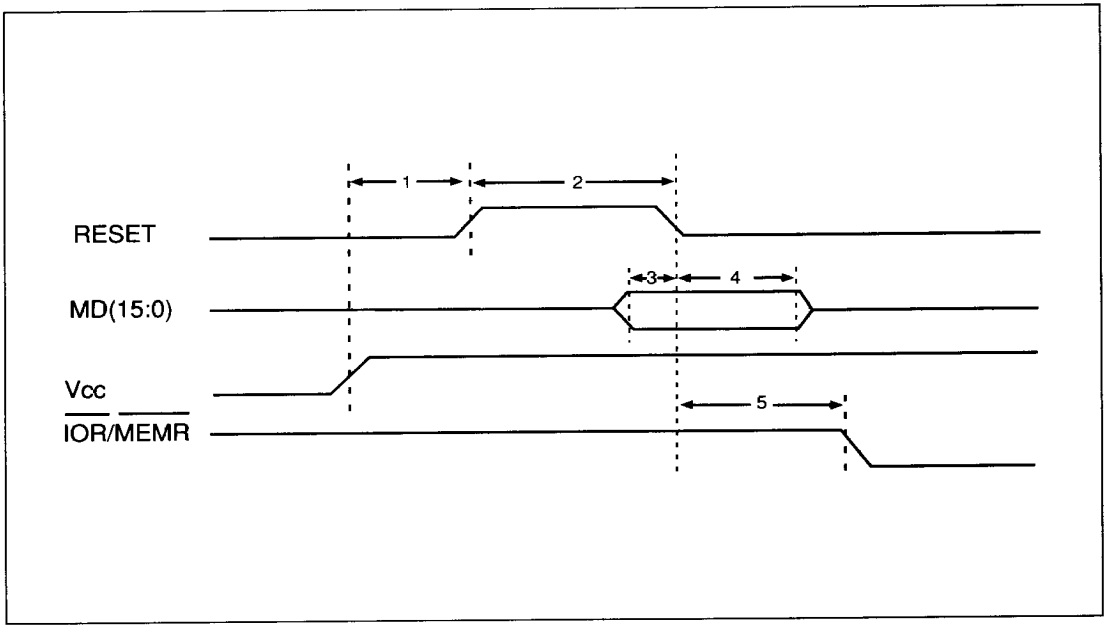

FIGURE C-15. RESET TIMING

NO.	PARAMETER			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1	Vcc	high to	RESET (high)	100ns			
2	RESET	pulse width		100t			
3	MD(15:0)	setup to	RESET (low)	2t			
4	MD(15:0)	hold from	RESET (low)	2t			
5	RESET	to first	$\overline{IOR}/\overline{MEMR}$	10t			

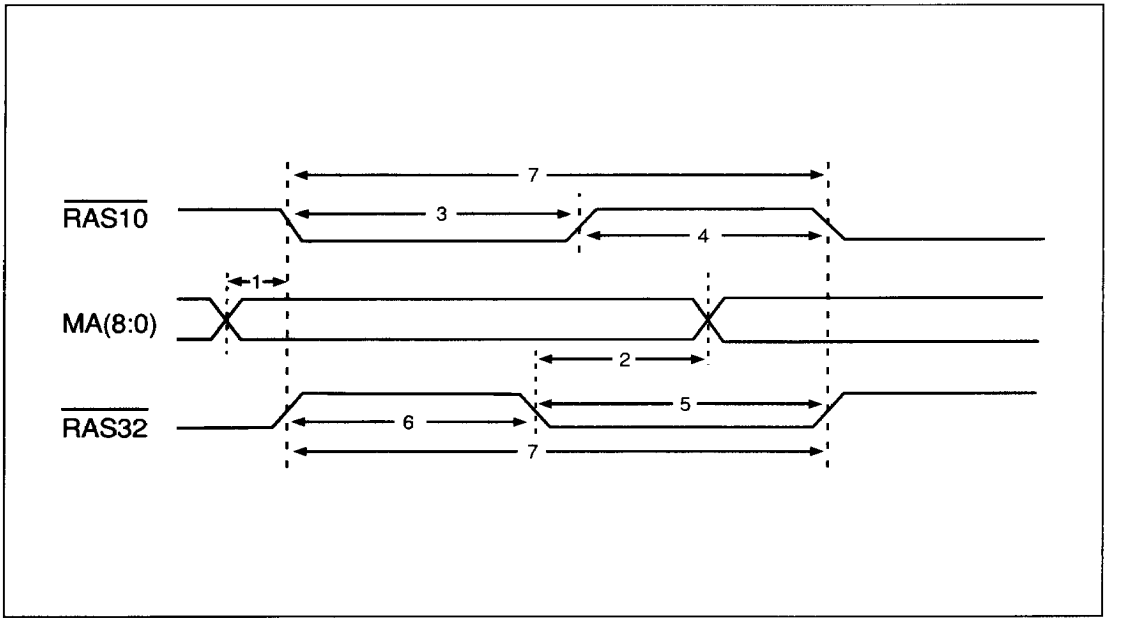

FIGURE C-16. RAS ONLY DRAM REFRESH TIMING

NO.	PARAMETER			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1	MA(8:0)	setup to	$\overline{RAS10}$ active	t			
2	MA(8:0)	hold to	$\overline{RAS32}$ active	t			
3	$\overline{RAS10}$	low time		5t-20	5t+10	5t-15	
4	$\overline{RAS10}$	high time		4t-10	4t+10		
5	$\overline{RAS32}$	low time		5t-20	5t+10	5t-15	
6	$\overline{RAS32}$	high time		4t-10	4t+10		
7	$\overline{RAS}$	cycle time		9t-10	9t+10		

t = 1/MCLK

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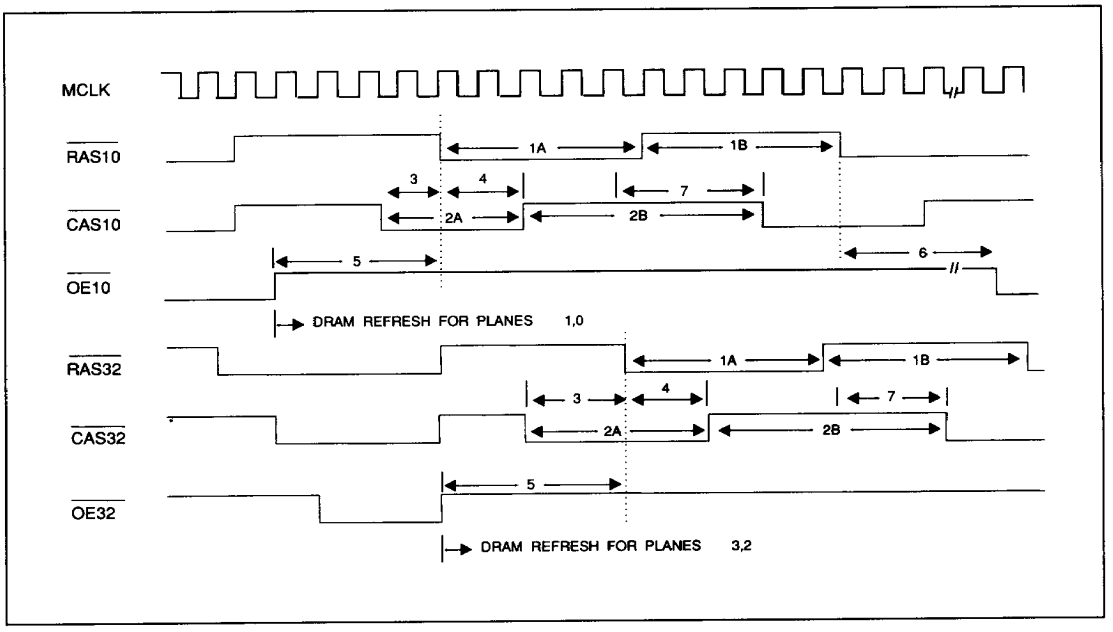

FIGURE C-17. CAS BEFORE RAS DRAM REFRESH TIMING

* (VALID ONLY FOR WD90C20A)

NO.	CAS BEFORE RAS DRAM REFRESH TIMING		WD90C20		WD90C20A	
			MIN.	MAX.	MIN.	MAX.
1A	$\overline{RAS10}$ ($\overline{RAS32}$) pulse width low		5t-10	5t+10		
1B	$\overline{RAS10}$ ($\overline{RAS32}$) pulse width high		5t-10	5t+10		
2A	$\overline{CAS10}$ ($\overline{CAS32}$) pulse width low		4t-5	4t+5		
2B	$\overline{CAS10}$ ($\overline{CAS32}$) pulse width high		6t-5	6t+5		
3	$\overline{CAS10}$ ($\overline{CAS32}$) low to	$\overline{RAS10}$ ($\overline{RAS32}$) (low)	2t-10	2t+10		
4	$\overline{RAS10}$ (RAS32) low to	$\overline{CAS10}$ ($\overline{CAS32}$) (high)	2t-10	2t+10		
5	$\overline{OE10}$ ($\overline{OE32}$) high to	$\overline{RAS10}$ ($\overline{RAS32}$) (low)	4t-8	5t+8		
6	$\overline{RAS10}$ (RAS32) low to	$\overline{OE10}$ ($\overline{OE32}$) (low)	30t			
7	$\overline{RAS10}$ (RAS32) high to (Precharge)	$\overline{CAS10}$ ($\overline{CAS32}$) (low)	3t-5	3t+20		3t+15

t = 1/MCLK

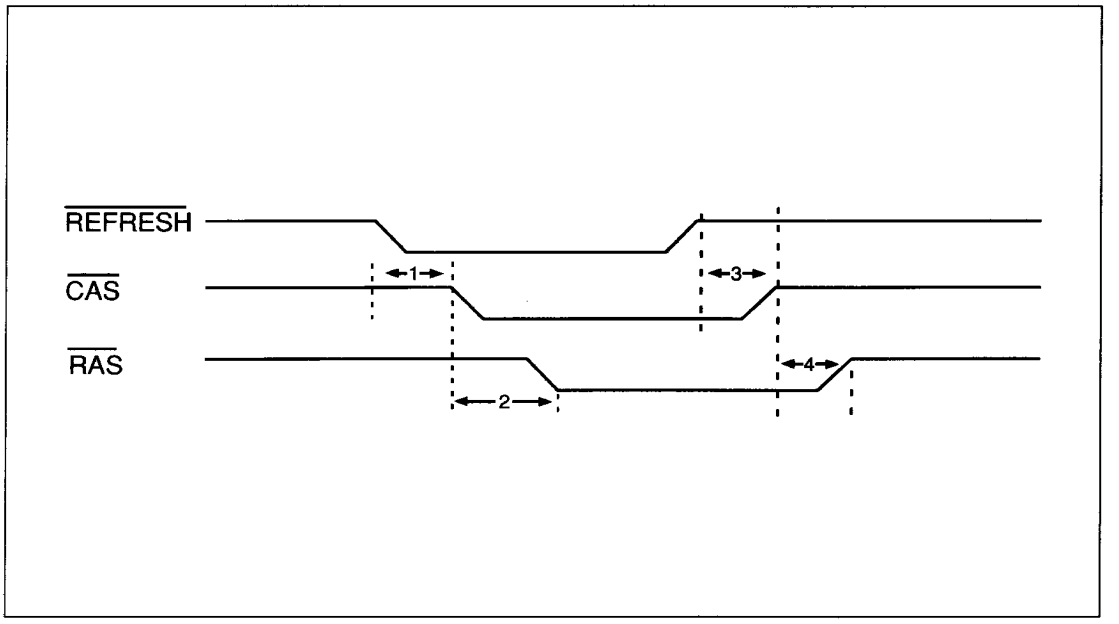

FIGURE C-18. CAS BEFORE RAS REFRESH (Power-Down Mode)

NO.	PARAMETER			WD90C20		WD90C20A	
				MIN.	MAX.	MIN.	MAX.
1	$\overline{CAS}$ low	from	$\overline{REFRESH}$ (low)	20			
2	$\overline{RAS}$ low	from	$\overline{CAS}$ (low)	20			
3	$\overline{CAS}$ high	from	$\overline{REFRESH}$ (high)	15			
4	$\overline{RAS}$ high	from	$\overline{CAS}$ (high)	20			

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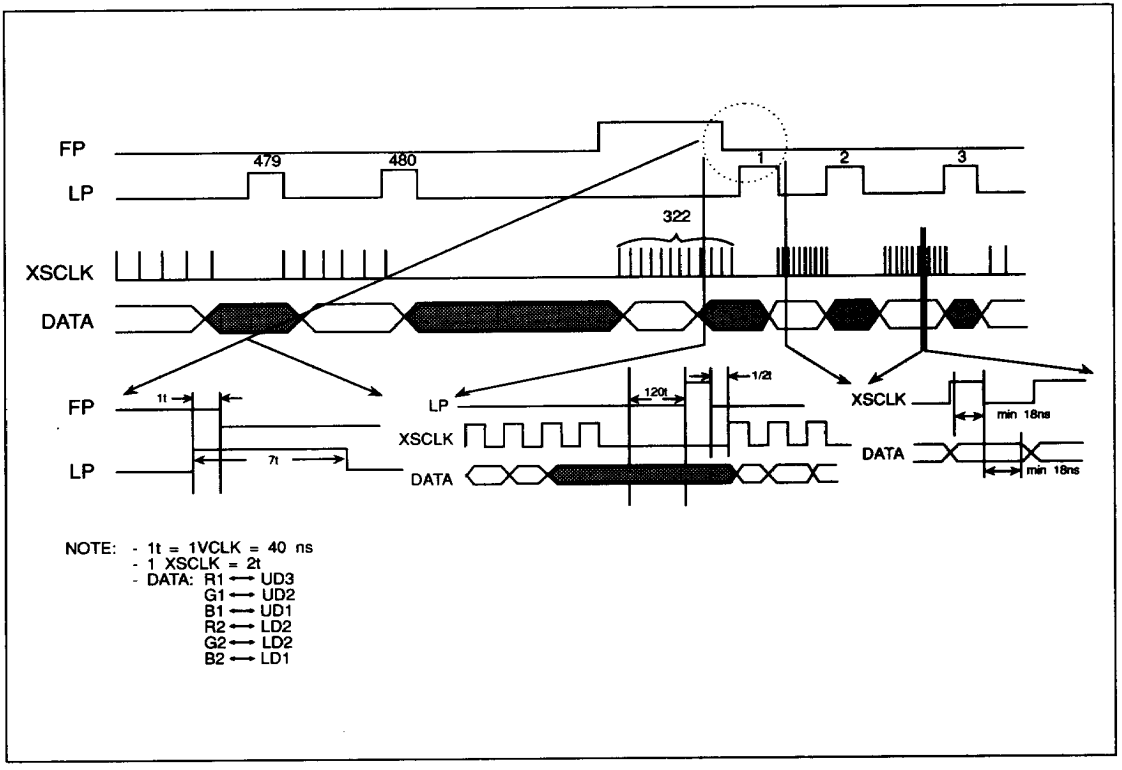

FIGURE C-19. STN COLOR LCD INTERFACE TIMING

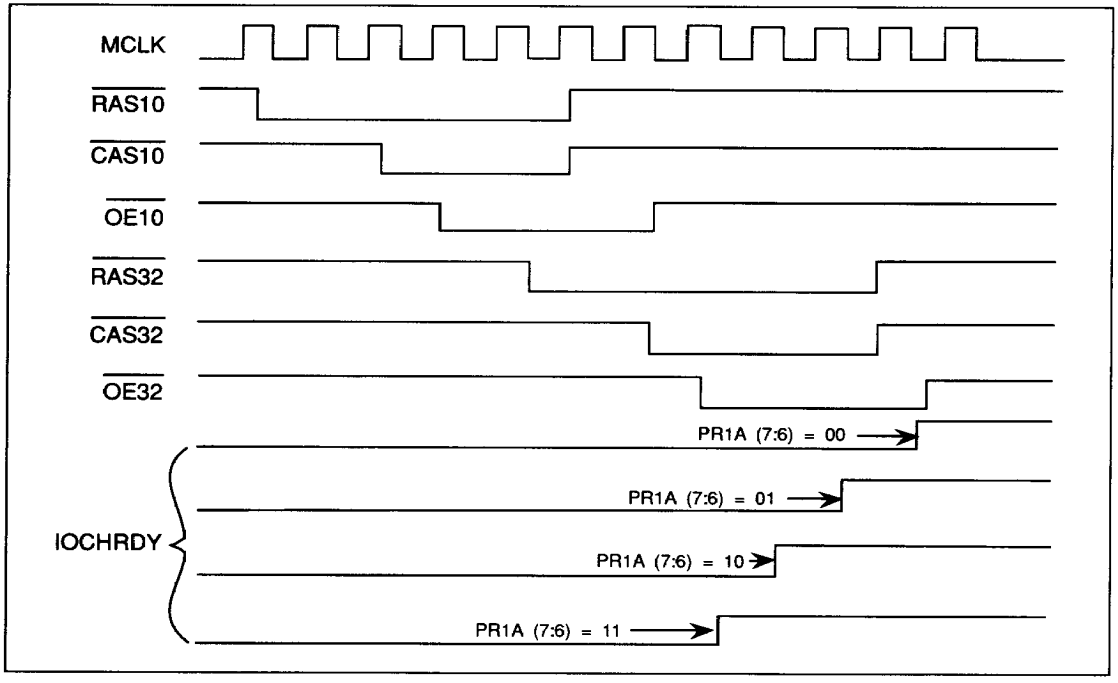

FIGURE C-20. IOCHRDY RELEASE TIMING IN MEMORY READ CYCLE

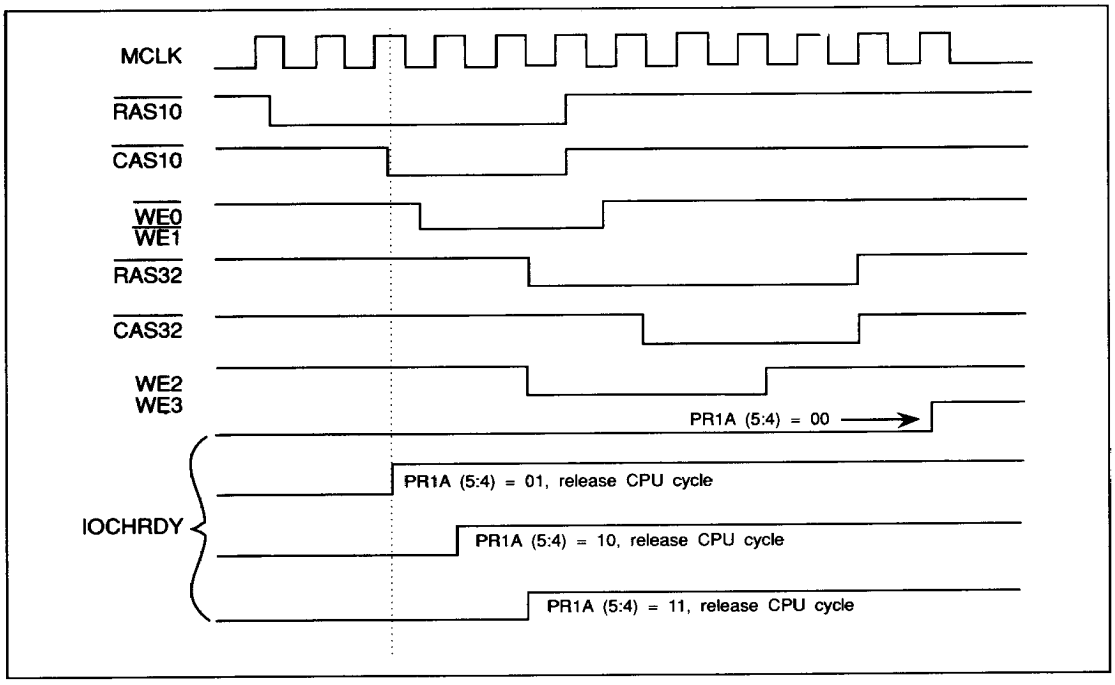

FIGURE C-21. IOCHRDY RELEASE TIMING IN MEMORY WRITE CYCLE

C.1 DC AND RAMDAC SPECIFICATIONS

SUPPLY PINS			
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VCC	4.1V	4.7V	Pins 9, 28, 53, 67, 94
RVCC	4.75V	5.25V	Pin 108
AVCC	4.75V	5.25V	Pin 123

WD90C20 TYPICAL AND MAXIMUM CURRENT/POWER CONSUMPTION						
MODE	**FREQUENCY (MHz)**					
	25 MHz		**28 MHz**		**32 MHz**	
	TYPICAL	**MAX.**	**TYPICAL**	**MAX.**	**TYPICAL**	**MAX.**
DISPLAY ACTIVE	149.4 mA 671.5 mW	179.3 mA 805.8 mW	166.8 mA 750.0 mW	200.2 mA 900.0 mW	182.8 mA 822.2 mW	219.4 mA 986.6 mW
SYSTEM POWERDOWN *	- -	- -	- -	- -	- -	- -
DISPLAY IDLE	22.0 mA 98.3 mW	27.5 mA 122.9 mW	24.3 mA 108.5 mW	30.4 135.6 mW	27.2 mA 121.5 mW	34.0 mA 151.9 mW
GENERAL POWERDOWN W/EXT. CLK CONTROL **	11.0 mA 49.7 mW	14.3 mA 64.6 mW	11.0 mA 49.7 mW	14.3 mA 64.6 mW	11.0 mA 49.7 mW	14.3 mA 64.6 mW
GENERAL POWERDOWN W/INT. CLK CONTROL	22.0 mA 98.4 mW	27.5 mA 123.0 mW	24.8 mA 110.6 mW	31.0 mA 138.3 mW	26.9 mA 120.0 mW	33.6 mA 150.0 mW

Conditions: AVCC (pin 123) = 5.0 volts, MCLK=44.9 MHz
RVCC (pin 108) = 5.0 volts,
DIGITAL VCCs (pins 9, 28, 53, 67, 94) = 4.4 volts
Display type active when measurements taken: LCD.

* - Not available for WD90C20
** - VCLK = 2.0 MHz, MCLK = 6.9 MHz

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WD90C20A TYPICAL AND MAXIMUM CURRENT/POWER CONSUMPTION						
MODE	FREQUENCY (MHz)					
	25 MHz		28 MHz		32 MHz	
	TYPICAL	MAX.	TYPICAL	MAX.	TYPICAL	MAX.
DISPLAY ACTIVE	74.0 mA 346.0 mW	88.8 mA 415 mW	83 mA 388.0 mW	99.6 mA 465 mW	91.0mA 425.0 mW	109.2 mA 510 mW
SYSTEM POWERDOWN *	4.5 mA 21.0 mW	10.0 mA 46.6 mW	4.5 mA 21.0 mW	10.0 mA 46.6 mW	4.5 mA 21.0 mW	10.0 mA 46.6 mW
DISPLAY IDLE	11.9 mA 56.6 mW	15.5 mA 73.6 mW	13.1 mA 62.5 mW	17.0 mA 81.3 mW	14.7 mA 70 mW	19.1 mA 91.0 mW
GENERAL POWERDOWN W/EXT. CLK CONTROL **	17.5 mA 82.6 mW	21.9 mA 103.3 mW	17.5 mA 82.6 mW	21.9 mA 103.3 mW	17.5 mA 82.6mW	21.9 mA 103.3 mW
GENERAL POWERDOWN W/INT. CLK CONTROL	11.9 mA 56.6 mW	15.5 mA 73.6 mW	13.1 mA 62.5 mW	17.0 mA 81.3 mW	14.7 mA 70 mW	19.1 mA 91.0 mW

Conditions: AVCC (pin 123) = 5.0 volts, MCLK=44.9 MHz
RVCC (pin 108) = 5.0 volts,
DIGITAL VCCs (pins 9, 28, 53, 67, 94) = 4.4 volts
Display type active when measurements taken: LCD.

* - VCLK = MCLK = 0 Hz
** - VCLK = MCLK = 6.9 MHz

INPUT PINS			
PINS	LA17-19, SBHE, MEMEN, EIO/3C3D0, ALE, MEMR/M/IO, PWRDN, MEMW/S0, IOR/S1, IOW/CMD, RESET, REFRESH, MCLK, VCLK0, SA0-16 (PINS 3-8, 11, 38-44, 98, 99, 117-122, 124-132, 1, 2)		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VIL	-0.5V	0.8V	
VIH	2.0V	VCC+0.6	
IIL	-10 uA	10 uA	VIN = 0V TO VCC
PIN	**VREF (PIN 111)**		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VIN ANALOG	-0.5V	2.0V	See RAMDAC specifications
IIL	-10 uA	10 uA	VIN = 0V TO VCC
	-100 uA	100 uA	VIN = 0V TO VCC+0.6V

PIN	**MDETECT/FSADJUST (PIN 112)**		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VIL	-0.5V	0.8V	
VIH	2.0V	VCC+0.6	
IIL	-10 uA	10 uA	VIN = 0V TO VCC

PIN	**ALL INPUTS**		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
CIN		6 PF	

PINS	**IRQ/IRQ, MA0-8, RAS10, RAS32, CAS10, CAS32, WE0, WE1, WE2, WE3, OE10, OE32 (PINS 12, 45-52, 55-65)**		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VOL		0.4V	IOL = 3.0mA
VOH	2.4V		IOH = -4.8mA (WD90C20 only) IOH = -6.0mA (WD90C20A only)

PINS	**EBROM/CDSFDBK, HBDIR, LBDIR, LP/HSYNC, FP/VSYNC, FR/BLANK, RPLT, WPLT/VD9, LD0-3, UD0-3, (PINS 13, 16, 17, 89-93, 100-107)**		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VOL		0.4V	IOL = 1.5mA
VOH	2.4V		IOH = -3.6mA

PINS	**MEMCS16\CDS16, IOCHRDY (PINS 14, 15)**		
PARAMETER	**MIN**	**MAX**	**CONDITIONS**
VOL		0.4V	IOL = 16.0mA
VOH	2.4V		IOH = -8.0mA

TABLE C-2. D.C. TEST SPECIFICATIONS

PINS	RED, GREEN, BLUE (PINS 114-116)		
PARAMETER	MIN	MAX	CONDITIONS
VOUT	-0.5	1.5	See RAMDAC Specification

PIN	LCD/CRT (PIN 110)		
PARAMETER	MIN	MAX	CONDITIONS
VOL		0.4V	IOL = 6.0 mA
VOH	2.4V		IOH = -6.0mA

PINS	PCLK, XSCLK, WGTCLK (PINS 86-88)		
PARAMETER	MIN	MAX	CONDITIONS
VOL		0.4V	IOL = 6.0 mA
VOH	2.4V		IOH = -6.0mA

I/O PINS			
PINS	VCLK2, VCLK1 (PINS 96, 97)		
PARAMETER	MIN	MAX	CONDITIONS
VIL	-0.5V	0.8V	
VIH	2.0V	VCC+0.6	
VOL		0.4V	IOL = 1.5 mA
VOH	2.4V		IOH = -3.6mA
IOZ	-50 uA	50uA	VOUT = 0V TO VCC

PINS	SD0-15, MD0-15 (PINS 36-29, 26-19, 84-77, 75-68)		
PARAMETER	MIN	MAX	CONDITIONS
VIL	-0.5V	0.8V	
VIH	2.0V	VCC+0.6	
VOL		0.4V	IOL = 3.0 mA
VOH	2.4V		IOH = -4.8mA (WD90C20 only)
IOZ	-50 uA	50uA	IOH = -6.0mA (WD90C20A only)
			VOUT = 0V TO VCC

PINS	ALL OUTPUTS AND I/O'S		
PARAMETER	MIN	MAX	CONDITIONS
COUT		30 PF	

TABLE C-2. TEST SPECIFICATIONS (CONTINUED)

PINS	BLUE, GREEN, RED PINS (114-116)			
PARAMETER	**MIN**	**TYP**	**MAX**	**CONDITIONS**
DAC RESOLUTION		6 BITS		
INTEGRAL LINEARITY ERROR			1/2 LSB	Least Squares Fit
DIFFERENTIAL LINEARITY ERROR			1/2 LSB	Least Squares Fit
WHITE LEVEL RELATIVE TO BLACK	13.38mA	14.08mA	14.79mA	VREF = 1.235, RSET = 221 Ohms
BLACK LEVEL	-20uA		20uA	
GRAY SCALE CURRENT RANGE			20mA	
LSB SIZE		223.5 uA		VREF = 1.235, RSET = 221 Ohms
GRAY SCALE ERROR			5.0%	
GLITCH ENERGY			50 pJOULES	
SETTLING TIME			20 NS	R <= 150 Ohms, 100 PF
CLOCK FEED THROUGH			20 pCOULOMB	
DAC TO DAC MATCHING			5%	
OUTPUT COMPLIANCE CURRENT TOLERANCE	-5%		+5%	
OUTPUT COMPLIANCE VOLTAGE RANGE	-0.5V		+1.5V	
VOLTAGE REFERENCE	1.14	1.235	1.26	
VOLTAGE REFERENCE INPUT CURRENT			10 uA	

TABLE C-3. RAMDAC SPECIFICATIONS (WD90C20 ONLY)

D.0 PACKAGE DIMENSIONS AND SPECIFICATIONS

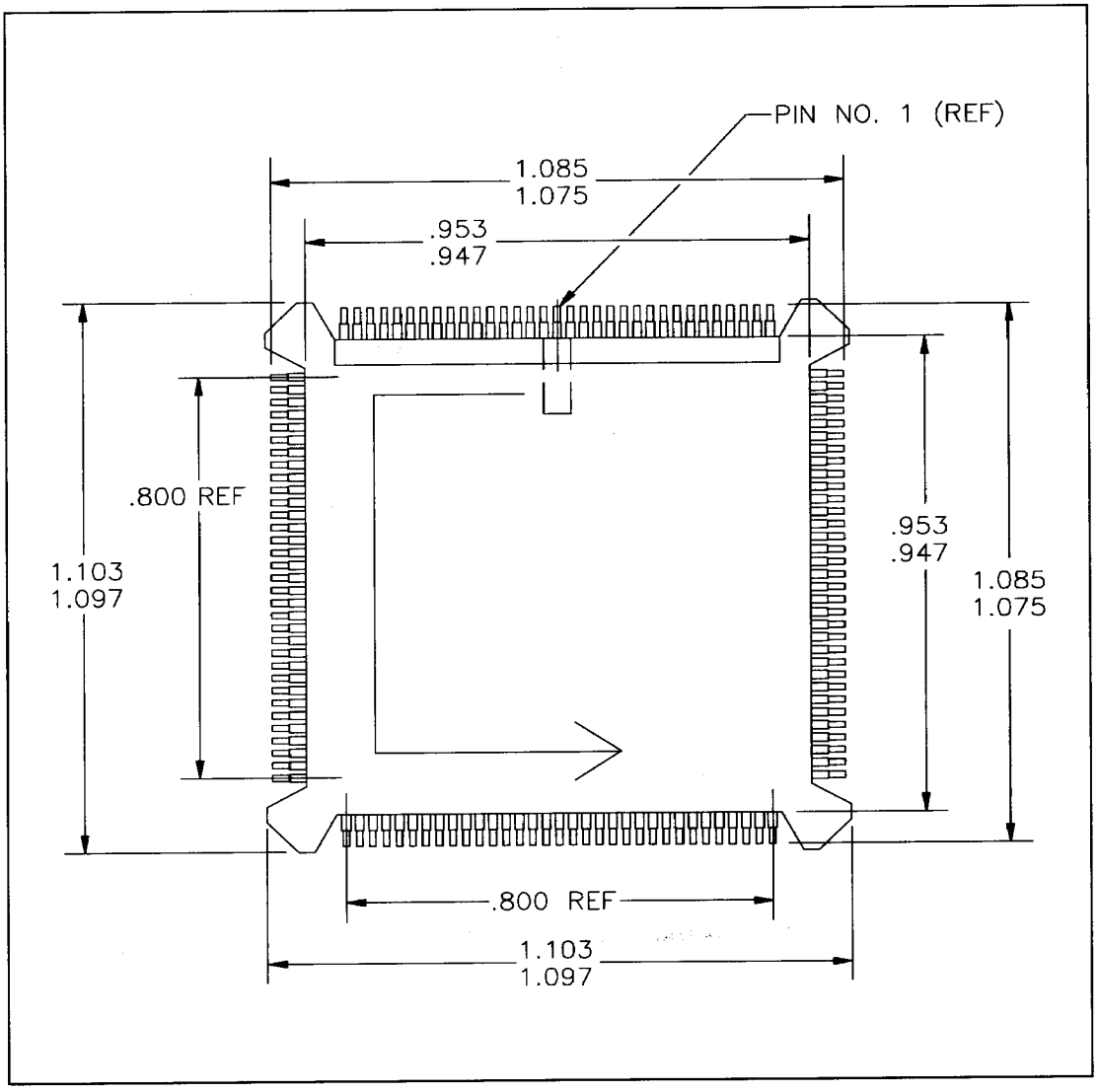

FIGURE D-1. 132-PIN PQFP PLASTIC FLAT PACKAGE

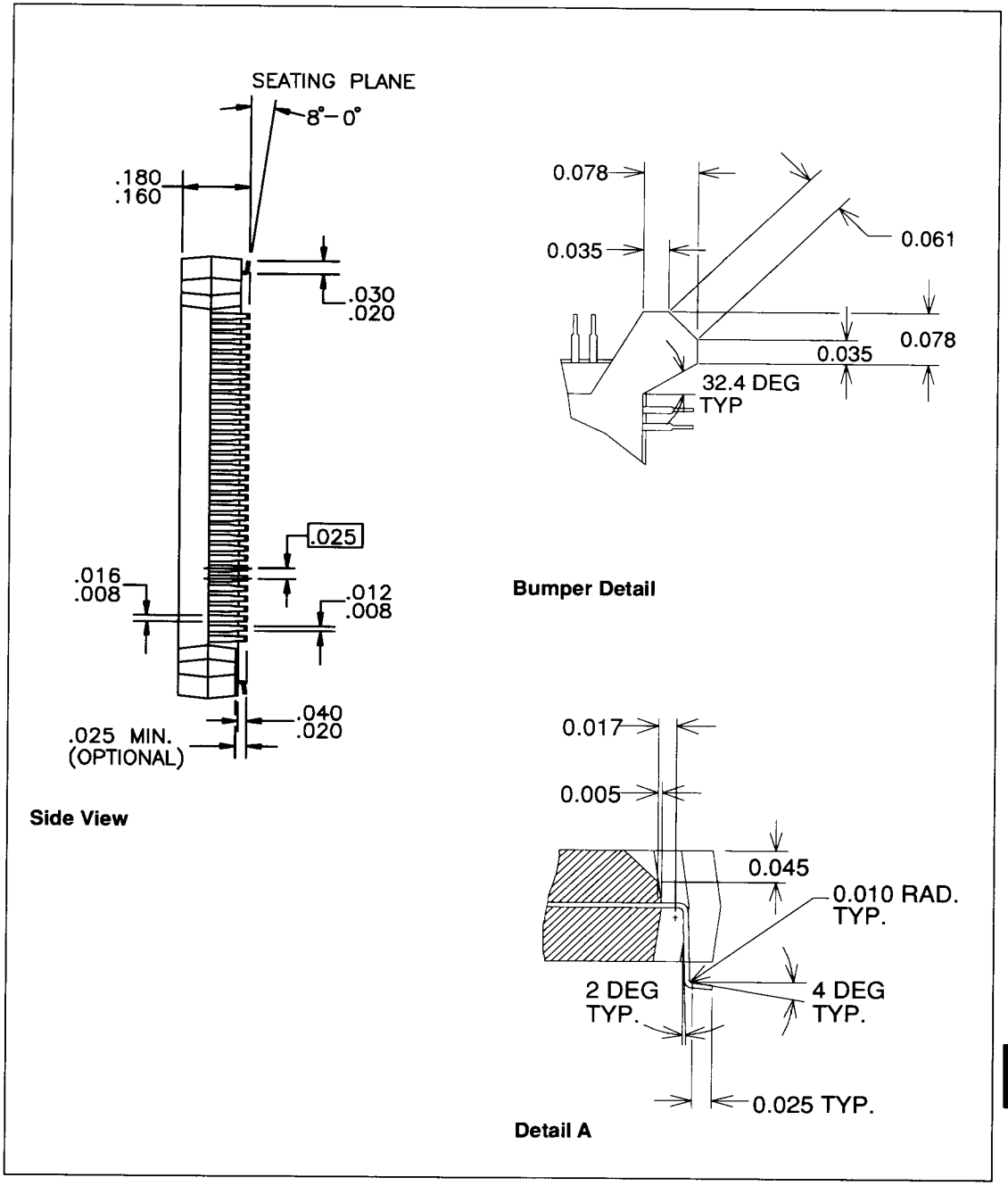

FIGURE D-1. 132-PIN PQFP PLASTIC FLAT PACKAGE (CONTINUED)

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E.0 MAXIMUM RATINGS

Ambient temperature under bias	$0^{o}C$ to 70^{o} C
Storage temperature	$-40^{o}C$ to $125^{o}C$
Voltage on all inputs and outputs with respect to Vss	-0.3 to 6.5 Volts
Power dissipation	1.2 Watts
Power Supply Voltage	4.1 to 4.7 Volts

NOTE: Stresses above those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to maximum rating conditions for extended periods may affect product reliability.

F.0 DIFFERENCES BETWEEN WD90C20 AND WD90C20A

The WD90C20A is a 0.9 micron version of the WD90C20 VGA controller chip. The submicron process design delivers reduced power consumption, true hardware vertical expansion, and an enhanced color palette for Super Twisted Nematic (STN) color LCDs.

Since the WD90C20A uses the smaller 0.9 micron geometry, smaller capacitances are required; therefore, a system designed with the WD90C20A uses less power than a comparable system using a 1.25 micron geometry VGA chip. Because the WD90C20A is pin-to-pin compatible with the WD90C20, you can keep your current designs and upgrade them for lower overall power consumption.

F.1 FUNCTIONAL CHANGES

- DC specifications for some of the output buffers have changed. See sections C.1 and F.4 for the WD90C20A DC specifications.
- Internal pullups on the SD bus are eliminated for the WD90C20A.
- The primary output $\overline{\text{MEMCS16}}$ is tristated when PWRDNN=0 and PR35(5)=1 for the WD90C20A.
- The continuous LP pulses during vertical blanking are now selectable on the WD90C20A for color LCDs (in addition to mono LCDs).

F.2 FEATURE ENHANCEMENTS FOR WD90C20A

F.2.1 DAC Enhancement

The WD90C20A DAC shuts off through software. Setting PR18(7)=0 enables the DAC to operate as normal; setting PR18(7)=1 forces the WD90C20A DAC to be shut off.

F.2.2 Micro Channel Interface Enhancement

The WD90C20A has additional support for the Micro Channel interface.If PR39(4)=0, then the default I/O cycle is selected.

If PR39(4)=1, then the synchronous-extended I/O cycle is selected.

F.2.3 Monochrome LCD Contrast Enhancement

Reverse video in text mode only and normal video in graphics mode.

If PR18 (4) = 0, then only normal video displayed.

If PR18 (4) = 1 and PR39 (3) = 0, then reverse video is displayed in both text and graphics modes. The WD90C22 also has this feature.

If PR18 (4) = 1 and PR39 (3) = 1, then reverse video is displayed only in text mode, while normal video is displayed in graphics mode.

PR39 (3)	PR18 (4)	TEXT	GRAPHICS
X	0	Normal	Normal
0	1	Reverse	Reverse
1	1	Reverse	Normal

X= don't care

F.2.4 Plasma Panel Support

Plasma panel support is not available for the WD90C20A.

F.2.5 Color LCD Display Enhancement

The WD90C20A increases the number of display colors from 512 to 4K for STN color LCDs.

The WD90C20A has simultaneous display of both the CRT and single panel color LCDs with vertical expansion and autocentering.

The LCD/CRT polarity is shown as follows:

In the WD90C20

DISPLAY MODE	$\overline{\text{LCD/CRT}}$
CRT only	H
Flat panel only	L

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In the WD90C20A

DISPLAY MODE	$\overline{\text{LCD}}$/CRT
CRT only	H
Flat panel only	L
Simultaneous display	L

The WD90C20A has multiplexed outputs for CRT VSYNC and CRT HSYNC.

For bit 2: Enable CRT VSYNC and CRT HYSNC
If PR39 (2) = 0, then LBDIR pin=LBDIR signal and HBDIR pin=HBDIR signal.

If PR39 (2) = 1, then LBDIR pin=CRT VSYNC signal and HBDIR pin=CRT HSYNC signal.
See the following table.

PR39 (2)	LBDIR	HBDIR
0	LBDIR	HBDIR
1	CRT VSYNC	CRT HSYNC

When the TFT panel is enabled, the polarities of CRT VSYNC and CRT HSYNC are now pulsed low, regardless of the values programmed in the Miscellaneous Output Register Bit 7 and Bit 6 in PR11(3).

The WD90C20A has programmable polarities of FP and LP.

For bit 1: FP Polarity Select.
If PR39 (1) = 0, then FP has normal polarity.
If PR39 (1) = 1 then FP has reverse polarity.

For bit 0: LP Polarity Select.
If PR39 (0) = 0, then LP has normal polarity.
If PR39 (0) = 1, then LP has reverse polarity.

PR39(1)	FP	PR39(0)	LP
0	Normal	0	Normal
1	Reverse	1	Reverse

The WD90C20A has software adjustment of HSYNC timings through PR19(7, 1,0). The WD90C20A and WD90C22 have the same timings for these signals.

PR19(7)	PR19(1)	PR19(0)	NUMBER OF VCLK DELAY
0	0	0	No Delay
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

F.2.6 Power Management Enhancement

The WD90C20A dot clock dithering logic is stopped whenever the on-chip hardware dithering in not required. This can reduce the power dissipation by as much as 100mW.

The panel display data, VUD[3:0] and VLD[3:0], are set to logic low during reset or any of the powerdown modes to avoid potential current drain.

F.3 PERFORMANCE ENHANCEMENTS FOR WD90C20A

F.3.1 DAC Improvements

The WD90C20A's improved RAMDAC was redesigned to do the following:

- reduce power dissipation
- reduce overshoot and undershoot noise
- reduce ampflier gain error
- improve linearity
- increase yield

R_{SET} requires a new value resistor, which reduces both power dissipation and ampflier gain.

The new WD90C20A DAC specifications are in the table on the next page.

AC CHARACTERISTICS				
Parameter	**Min**	**Typ**	**Max**	**Units**
Analog output capacitance		80		pF
DAC switching speed			50	MHz
Output setting time (to ±1/4 LSB)		20		ns
Rise/fall time		3		ns
DC CHARACTERISTICS				
Resolution	6	6	6	bits
Accuracy (each DAC) Integral non-linearity (INL) Differential non-linearity (DNL) Gray scale error Monotonicity		 guaranteed	 ±1/2 ±1/2 ±5	 LSB LSB % full scale
LSB current 37.5 ohm load 50 ohm load		 296 222		 µA µA
Full scale current (each DAC) 37.5 ohm load 50 ohm load		 18.67 14		 mA mA
R_{SET} 37.5 ohm load 50 ohm load		 4320±1% 5760±1%		 ohm ohm
DAC to DAC matching			5	%
P_{TOTAL} (all three DACs) 37.5 ohm load		 230		mW
RECOMMENDED OPERATING CONDITIONS				
Power Supply AV_{DD}	4.5	5.0	5.5	volts
Pixel clock frequency f			50	MHz
Ambient temperature T_A	0		70	degrees C

TABLE F-1. WD90C20A RAMDAC SPECIFICATIONS

$$I_{FULL\ SCALE} = \frac{63 \times 1.036 \times V_{REF}}{R_{SET}}$$

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F.4 WD90C20A DC SPECIFICATIONS

Below are the updated WD90C20A DC specifications.

OUTPUT CAPACITANCE LOADING			
SIGNAL	**TRISTATE (Y/N)**	**MIN**	**MAX**
$\overline{\text{MEMCS16}}$	Yes		70 pF
OICHRDY	Yes		100 pF
$\overline{\text{EBROM}}$	No		40 pF
IRQ	Yes		70 pF
HBDIR	No		40 pF
LBDIR	No		40 pF
MA(7:0)	Yes	40 pF	70 pF
$\overline{\text{RAS10}}$	Yes	40 pF	70 pF
$\overline{\text{RAS32}}$	Yes	40 pF	70 pF
$\overline{\text{WE0}}$	Yes	40 pF	70 pF
$\overline{\text{WE1}}$	Yes	40 pF	70 pF
$\overline{\text{WE2}}$	Yes	40 pF	70 pF
$\overline{\text{WE3}}$	Yes	40 pF	70 pF
$\overline{\text{OE10}}$	Yes	40 pF	70 pF
$\overline{\text{OE32}}$	Yes	40 pF	70 pF
$\overline{\text{WPLT}}$	No		30 pF
$\overline{\text{RPLT}}$	No		30 pF
VUD(0:3)	Yes	20 pF	40 pF
VLD(0:3)	Yes	20 pF	40 pF
FR	Yes		40 pF
FP	Yes		40 pF
LP	Yes		40 pF
XSCLK	No		40 pF
PCLK	No		70 pF
WGTCLK	No		40 pF
$\overline{\text{LCD}}$	No		30 pF
SD(15:0)	Yes		70 pF
MD(15:0)	Yes		70 pF
$\overline{\text{CAS10}}$	Yes	40 pF	70 pF
$\overline{\text{CAS32}}$	Yes	40 pF	70 pF
VCLK1	---		30 pF
VCLK2	---		30 pF

TABLE F-2. WD90C20A DC SPECIFICATIONS