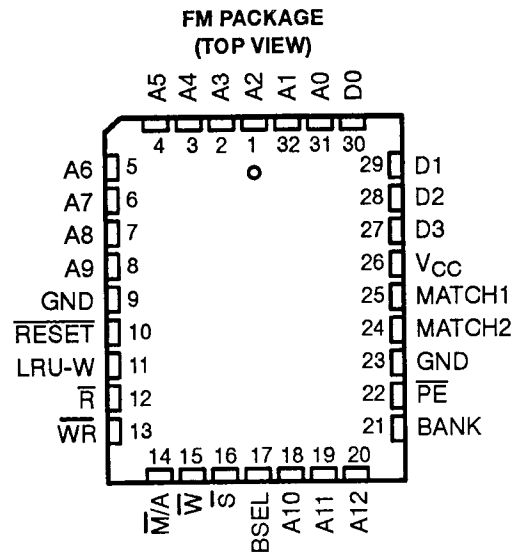# SN74BCT2160
8K × 4 2-WAY CACHE ADDRESS COMPARATOR/TAG RAM

SCHS011 – D3512, JUNE 1990 – REVISED MARCH 1992

- **Fast Address to Match Time . . . 12 ns Max**

- **Upgrade of the SN74ACT2160**

- **2-Way Architecture Significantly Improves Hit Rate**

- **Implements LRU Replacement Algorithm**

- **Useful for Bus Watching**

- **On-Chip Parity Generator and Checker**

- **Easily Expandable in Depth and Width**

- **Open-Drain Look-Ahead Circuitry on Match Outputs**

- **Self-Timed Write Circuitry**

- **Fully TTL Compatible**

FM PACKAGE
(TOP VIEW)

Top pins (left to right): A5, A4, A3, A2, A1, A0, D0

Pin			Pin
A6	5	29	D1
A7	6	28	D2
A8	7	27	D3
A9	8	26	V$_{CC}$
GND	9	25	MATCH1
RESET	10	24	MATCH2
LRU-W	11	23	GND
R̄	12	22	P̄E
W̄R̄	13	21	BANK

Pins 14–20: M/A, W/S, BSEL, A10, A11, A12

description

The SN74BCT2160 is a valuable building block for implementing fast two-way set associative caches. This device consists of two separate 8Kx5 RAMs for tag and parity storage, an 8K x 1 LRU RAM, two high-speed comparators, and the control circuitry necessary to give the designer the freedom to determine how this device will be used. The SN74BCT2160 also includes single-entry invalidation circuitry and parity generation and checking for ease of design and high system reliability.

The SN74BCT2160 is fabricated using advanced BiCMOS technology for high speed and simple interface with bipolar TTL circuits. By combining the SN74BCT2160 with programmable logic, a cache can be constructed that specifically addresses the individual system requirements. Significant reductions in cache memory component count, board area, and power dissipation can be achieved by using this device.

direct-mapped versus two-way set associative caches

A cache memory is a small high-speed memory that is used to store a portion of the data found in the larger main memory to achieve optimum processor performance and to reduce main memory bus traffic. Since the cache memory is smaller than the main memory, only part of the address, the least significant bits referred to as the index, is used to address the cache memory. The most significant address bits, called the tag, are stored along with the cache data and are used to identify what data is stored in an indexed location. When the processor requests data, the index portion of the processor address points to a word of data in the cache-data RAM and to a tag in the cache tag RAM. If the upper portion of the processor address is equal to the stored tag, a cache hit is said to occur and the cached data can be immediately sent to the processor.

In a direct-mapped or one-way set associative cache, only one data word and tag exist in cache for each index. This means that when the processor requests data, only one cache memory location can contain the requested data. Also, if the requested data is not in the cache and the cache is updated, the data in the indexed cache memory location will be written over regardless of how recently it has been used.

In a two-way set associative cache, two data words and tags exist for each index. This means that the requested data can reside in one of two cache locations. When a miss occurs and the cache is updated, the least recently used data can be written over. As would be expected, studies have shown that the hit rate improves significantly when using a two-way cache design over a one-way or direct-mapped cache design. Through use of the 'BCT2160, the logic complexity and parts count usually associated with a two-way cache are greatly reduced.

This device is covered by U.S. Patents 4,831,625; 4,837,743; 4,858,182; 4,860,262; 4,884,270; and additional patents pending.

TEXAS INSTRUMENTS

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address comparison

The 'BCT2160 compares the contents of the memory location addressed by A0–A12 with the address bits (or tag) applied at D0–D3. An equality is indicated by a high level on the MATCH1 or MATCH2 outputs. MATCH1 is high when the applied tag is equal to the stored tag in bank 1. MATCH2 is high when the applied tag is equal to the stored tag in bank 2.

writing to the 'BCT2160

The 'BCT2160 has been designed with self-timed write circuitry. A high-to-low transition at the $\overline{W}$ input initiates an internally generated write pulse. After a high-to-low transistion at $\overline{W}$, $\overline{W}$ may be held low without initiating additional write pulses. The manual/auto ($\overline{M}$/A) input on the 'BCT2160 provides two methods of selecting which tag bank will be written to when the write input ($\overline{W}$) is taken low. When $\overline{M}$/A is low, the bank select input (BSEL) selects the bank to be written to. BSEL low selects bank 1 and BSEL high selects bank 2. When $\overline{M}$/A is high, the least recently used (LRU) circuitry automatically selects the bank written to when $\overline{W}$ is taken low. The BANK output is latched when $\overline{W}$ goes low. This latch will return transparent when $\overline{W}$ returns high. When $\overline{W}$ is low, the D0–D3 outputs are disabled. A high-to-low transition at the $\overline{S}$ input when $\overline{W}$ is low will not initiate a write (self-timed) pulse.

writing to the cache data RAMs

When a read or a write miss occurs and the cache is updated, the BANK output indicates to which bank the data should be written (BANK is the output of the internal 8K x 1 LRU RAM). If BANK is low, bank 1 should be written, if BANK is high, bank 2 should be written. When writing a tag with $\overline{M}$/A low, the BANK output does not indicate which bank is being selected by the BSEL input. When a write hit occurs, the match outputs indicate to which bank the data should be written.

LRU replacement circuitry

A concept commonly referred to in cache design is the property of locality. An aspect of the property of locality says that the information currently in use is likely to be used again soon. Based on this property, it is desirable to replace the information that has not been used recently when writing to cache. With a set size of two, this is easily done using one bit to indicate which of the two addressed locations is oldest or least recently used. The 'BCT2160 contains an 8K×1 RAM and the necessary circuitry to implement the LRU replacement algorithm.

The $\overline{M}$/A input allows the user to choose between automatic LRU and manual replacement. When $\overline{M}$/A is high, the LRU RAM output selects which bank to write to. When the LRU bit for a given address is low, a write pulse will write D0–D3 to bank 1. When the LRU bit for a given address is high, a write pulse will write D0–D3 to bank 2. The LRU RAM is updated every time a write, a match (with LRU-W signal), or a word reset occurs.

When a write occurs with $\overline{M}$/A high, the addressed LRU bit is inverted and written back in so that the next write with $\overline{M}$/A high to that address will be to the other bank. When a write occurs with $\overline{M}$/A low, the bank is selected by the BSEL input and the addressed LRU bit is adjusted so that the next write to the same address with $\overline{M}$/A high will be to the other bank.

With a match output high indicating a match, the LRU RAM will also be updated when the LRU-W input is taken low. The logic level at each match output is fed back internally to the LRU circuitry. If MATCH1 or MATCH2 are high, the LRU-W input provides an LRU write timing signal that causes an internal LRU write pulse to be generated. With MATCH1 high, the LRU bit is set high so the next write to the same address with $\overline{M}$/A high will be to bank 2. With MATCH2 high, the LRU bit is set low so the next write to the same address with $\overline{M}$/A high will be to bank 1. When cascading these devices for wider address coverage, the MATCH1 outputs must be wire-ANDed together so an LRU write will not occur unless all MATCH1 outputs are high. In the same manner, the MATCH2 outputs (in width) must be tied together. When MATCH1 and MATCH2 are forced high during deselect, write, read, word reset, or reset, and LRU-W is taken low, a false LRU write will not occur. When a word reset occurs, the addressed LRU bit is updated so that the next write to that address will be to the reset (invalidated) location.

TEXAS INSTRUMENTS

parity generation and checking

The 'BCT2160 contains parity generation and checking circuitry. When the $\overline{PE}$ output goes low, a parity error exists in one of the two tag RAMs.

During a write cycle, address bits or data on D0–D3 plus generated odd parity are written into the 5-bit memory location in either bank 1 or bank 2 that is addressed by A0–A12. The bank written to is selected automatically or manually via the BSEL input depending on the state of the $\overline{M}$/A input. Also during write, a parity error may be forced for diagnostic purposes by holding the $\overline{R}$ input low. The addressed parity bits are included in the comparator circuitry of the 'BCT2160 so if a parity error occurs, the corresponding match output will be forced low. The LRU bit is not parity protected. The BANK outputs of the 'BCT2160s that are cascaded in width could be externally exclusive ORed to provide protection for the LRU bits.

operation as a data RAM

The 'BCT2160 can be used as a two-way 8K×4 data RAM with parity generation and checking. By tying the manual/auto ($\overline{M}$/A) pin low, the BSEL input can be used to select which bank is being written to or read from. Through the use of the select pin, the 'BCT2160 can be cascaded for a deeper data RAM. Inputs $\overline{WR}$ and LRU-W should be tied high when using the 'BCT2160 as a data RAM.

initialization

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all three 8K RAM locations are cleared to zero (with valid parity) and the MATCH1 and MATCH2 outputs are forced high. If a D0–D3 input of zero is compared to any memory location that has not been written into since reset, MATCH1 and/or MATCH2 will be high indicating that D0–D3 plus generated parity is equal to the reset memory location. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction, only one bit needs to be tied high regardless of the address width. After reset, $\overline{PE}$ will be high for every addressed memory location indicating no parity error in the RAM data. After power-up, the 'BCT2160 must be initialized by resetting the device to ensure that all memory locations are at a known state. The 'BCT2160 could also be initialized by writing to every memory location (both banks).

single-entry invalidation

In cache tag systems, it is often necessary to invalidate a tag memory location when data in the cache becomes inconsistent with the data in main memory or in additional caches. The word-reset function on the 'BCT2160 allows any addressed memory location to be cleared to zero with valid parity by taking the word reset pin ($\overline{WR}$) low. By tying one of the D0–D3 input pins high, that particular bit can be used as a valid bit. Whenever D0–D3 is compared to a memory location cleared by $\overline{WR}$ (or by the master $\overline{RESET}$), a miss will occur. If a D0–D3 input pin is not tied high, a false match will occur whenever a D0–D3 of zero is compared to a reset location. Word reset is independent of the input at the D0–D3 pins. The $\overline{M}$/A input must be low for a word reset to occur when $\overline{WR}$ is taken low. Word reset can also be accomplished by holding $\overline{WR}$ low and taking $\overline{M}$/A low to reset the addressed location. At the same time that an addressed location is reset, the addressed LRU bit is updated so that the next write to the same address with $\overline{M}$/A high will be to the reset location. Input BSEL determines which bank $\overline{WR}$ affects. When cascading in width, all devices must receive the word-reset pulse for proper LRU RAM update.

Since the LRU bit is updated during a word reset operation, attention must be given when designing cache systems as to when the operation occurs. For instance, if a word reset is allowed at the same time as a cache line fill and it is followed by a tag write, the tag could actually be written to the wrong bank. This would result in the tag residing in one bank with its corresponding data residing in the other bank (a fatal error).

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SN74BCT2160
8K × 4 2-WAY CACHE ADDRESS COMPARATOR/TAG RAM

cascading the 'BCT2160

The 'BCT2160 is easily cascaded in width and depth. Wider addresses can be compared by driving the A0–A12 inputs of each device with the same index and applying the additional address bits to the D0–D3 inputs. The select ($\overline{S}$) input allows this device to be easily cascaded in depth. When a device is deselected, the MATCH1 and MATCH2 outputs are driven high. This allows the match outputs to be wire tied or gated together when cascading in depth. A decoder can be used to drive the select inputs since the propagation delay from select to match is much faster than from address to match. MATCH1 and MATCH2 are open-drain outputs for easy wire-ANDing and must be wired-ANDed in the width direction to ensure proper LRU update. Figure 16 shows the 'BCT2160 cascaded.

cache coherency through bus watching

When implementing cache designs, cache coherency is usually a concern. A solution to this problem is to implement bus watching using the 'BCT2160. By storing the same tags in the bus watcher RAM as are stored in the cache tag RAM, the bus watcher will indicate a hit every time a cached address passes down the main address bus. If data is being modified in main memory, the index can be passed to the cache tag RAM for invalidation. Figure 17 shows a possible bus-watching application.

## 'BCT2160/'ACT2160 comparison

When designing a system that will use the 'BCT2160 and the slower 'ACT2160 interchangeably, the following difference should be noted. The 'ACT2160 uses conventional write circuitry where data is written into the device as long as the write enable ($\overline{W}$) is low. Address and data setup and hold times are with respect to the rising edge of $\overline{W}$. The 'BCT2160 uses self-timed write circuitry where an internal write pulse is generated when the write enable ($\overline{W}$) is taken low. Address and data setup and hold times are with respect to the falling edge of $\overline{W}$.
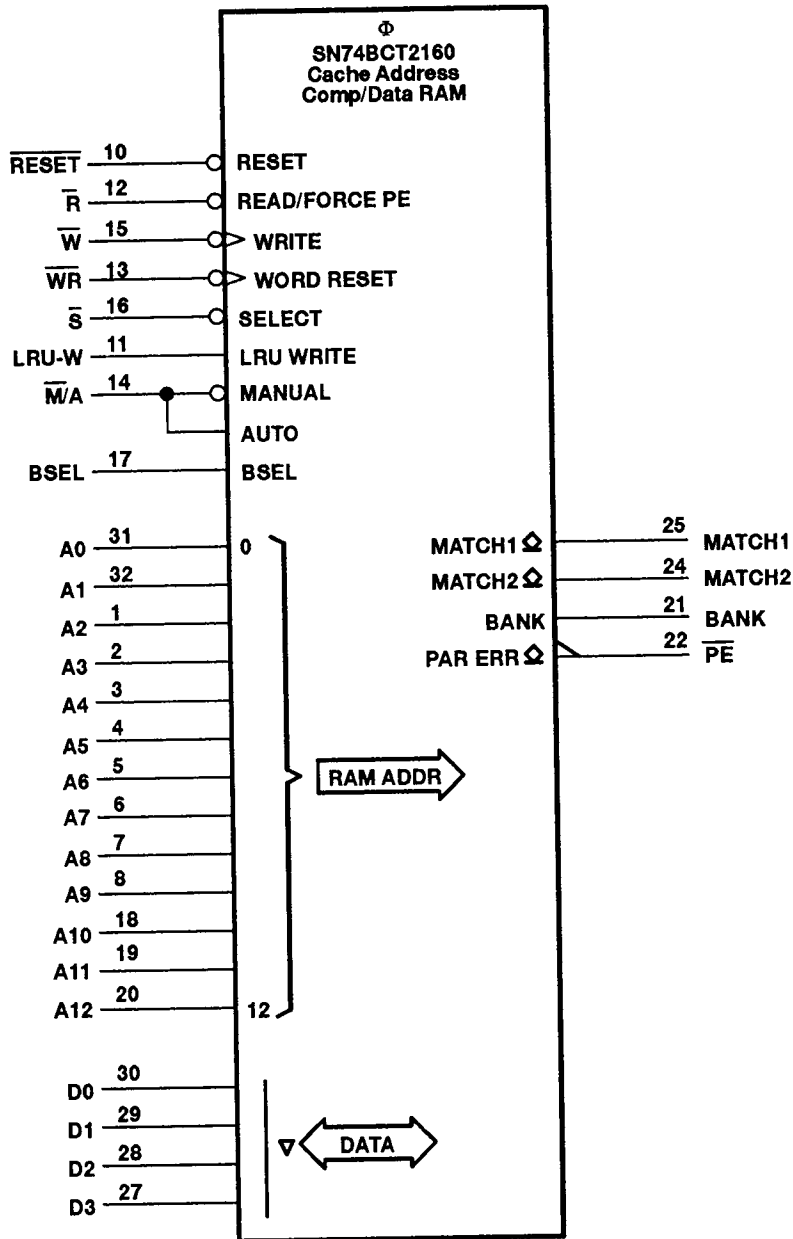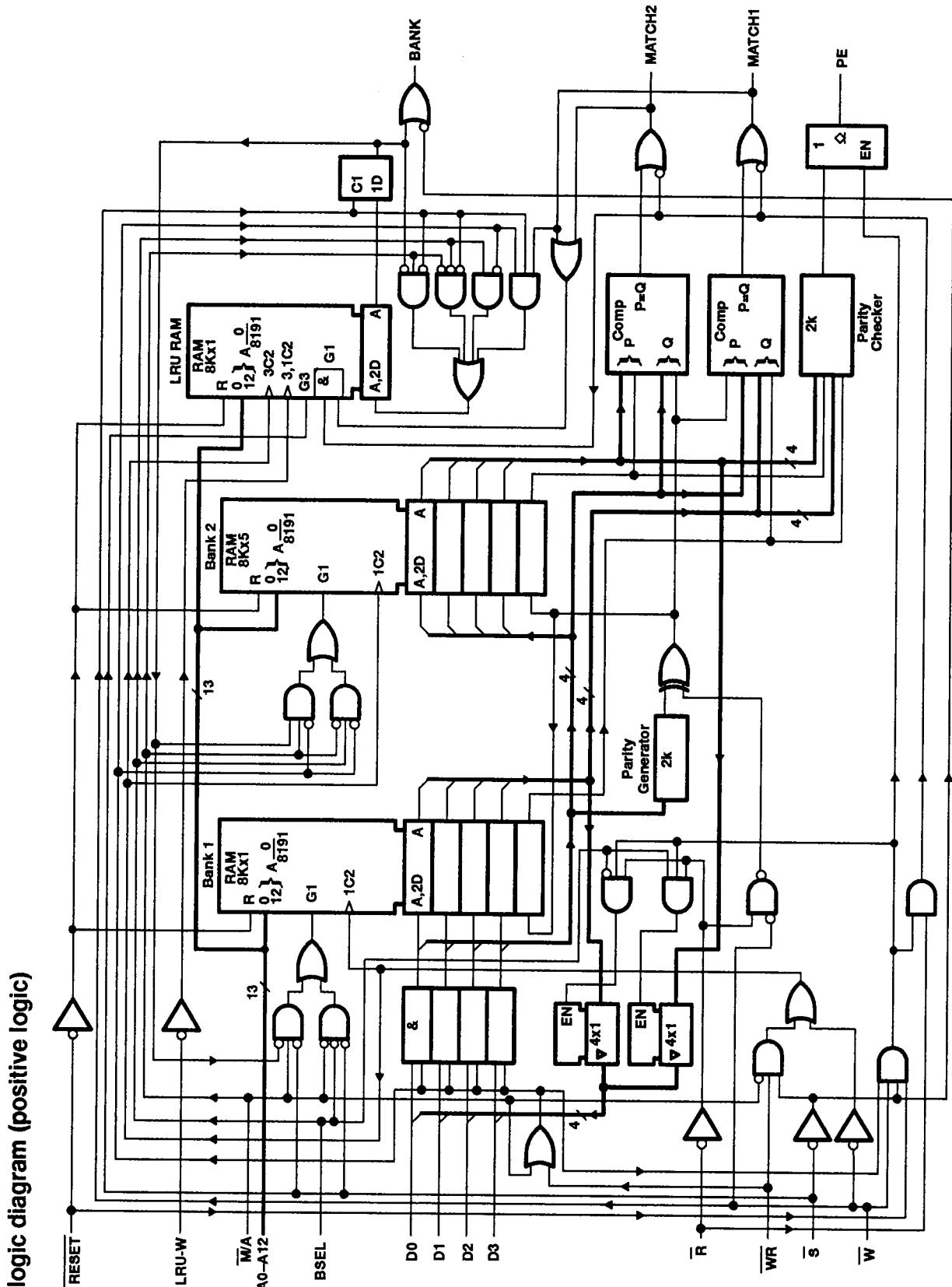
logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984.

SN74BCT2160
8K × 4 2-WAY CACHE ADDRESS COMPARATOR/TAG RAM

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logic diagram (positive logic)

Terminal Functions

PIN NAME	DESCRIPTION
A0–A12	Address inputs. Addresses a memory location in each of the three 8K RAM arrays. Address must be stable for the duration of the write cycle.
BSEL	Bank select input. This input is used in conjunction with the manual/auto, read and word reset functions. When BSEL is low, bank 1 is selected. When BSEL is high, bank 2 is selected. When M̄/A is high, the BSEL input does not affect writing.
BANK	Bank output. The BANK output is used during a write to indicate which bank D0–D3 is being written into when M̄/A is high. BANK is low for bank 1 and high for bank 2. BANK is forced high during reset and deselect. BANK is used to indicate which cache SRAM bank the system data should be written into. When W̄ is taken low, the output of the LRU RAM is latched causing BANK to remain stable. When W̄ returns high, the latch returns transparent and the BANK output will switch if the LRU bit was changed. BANK is a totem-pole output.
D0-D3	Data (tag) inputs and outputs. Provides input to RAM bank 1 or bank 2 depending on the state of the S̄, W̄, BSEL, M̄/A, and W̄R̄ pins. When in the compare mode, D0-D3 plus generated parity are compared to the addressed 5-bit memory location in bank 1 and bank 2. D0–D3 also function as outputs (see the R̄ pin description).
LRU-W	Least recently used write timing signal. In the compare mode, a falling edge on LRU-W will initiate an LRU write pulse if MATCH1 and/or MATCH2 are high. If a falling edge at LRU-W occurs before MATCH1 or MATCH2 are valid, the LRU write may not occur or a false LRU write could occur – this is critical when cascading. LRU-W will only initiate a LRU write pulse on a falling edge. LRU-W has no effect during any other mode of operation.
M̄/A	Manual/auto input. The M̄/A input determines the bank select mode for writing data. When M̄/A is low, the bank to be written into is selected manually via the BSEL input. When the M̄/A input is high, the bank selection is done automatically. An internal 8K x 1 RAM is used to keep track of the bank to be written into using the least recently used (LRU) replacement algorithm. After the device is reset, the first write is into bank 1. The next time data is written to the same address, it will be stored in bank 2. Successive writes to the same address automatically alternate between bank 1 and bank 2. M̄/A can also be used to perform the word reset function. With W̄R̄ low, the addressed location in the selected bank will be reset when M̄/A is taken low.
MATCH1 MATCH2	Match outputs. When MATCH1 or MATCH2 are high during a compare cycle, D0–D3 plus generated parity equal the contents of one of two memory locations addressed by A0–A12. MATCH1 is high when D0–D3 matches D0–D3 stored in bank 1. MATCH2 is high when D0–D3 matches D0–D3 stored in bank 2. The match outputs are high during deselect, write, read, word reset, and reset. The logic level at the match outputs is fed back to the internal LRU circuitry. If a match output is high indicating a match when LRU-W is taken low, the LRU bit is adjusted so that the next write into that address will be into the other bank (LRU concept). If a match occurs with both banks (MATCH1 and MATCH2 high) and LRU-W is taken low, bank 2 will be written into next, if M̄/A was low; bank 1 will be written into next, if M̄/A was high. Since this device features open-drain match outputs, an external pullup resistor of 180 Ω minimum is required. If a parity error is present in bank 1 or bank 2 during compare, the corresponding match output will be forced low.
P̄Ē	Parity error output. During compare cycles, a low level at P̄Ē indicates a parity error in one of the 8K x 5 RAMs. A parity error will force the corresponding match output low. P̄Ē will also indicate an error during read cycles. P̄Ē is an open-drain output and an external pullup resistor is required. P̄Ē is disabled during write, reset, word reset, and deselect.
R̄	Read input. When R̄ is low and the device is selected, D0–D3 are enabled as outputs. The output data (tag) is determined by A0–A12 and the BSEL input. Outputs D0–D3 are disabled during write, word reset, reset, deselect, and when R̄ is high. During write cycles, a parity error can be forced into the memory location addressed by A0–A12 of the selected bank when R̄ is taken low.
R̄Ē̄S̄Ē̄T̄	Reset input. Asynchronously clears all three RAM arrays to zero with valid parity independent of the select pin when R̄Ē̄S̄Ē̄T̄ is low. By tying a single data input high, a false match will not occur when a tag of zero is applied after initialization.
S̄	Chip select input. Enables device when S̄ is low. When S̄ is high, MATCH1 and MATCH2 are forced high. P̄Ē and D0–D3 are disabled when S̄ is high and BANK is forced high.
W̄R̄	Word Reset input. The W̄R̄ input allows any addressed memory location to be cleared to zero with valid parity. This is achieved by taking W̄R̄ low while in the manual mode (M̄/A low). The desired bank is selected using the BSEL input. When W̄R̄ is asserted, the addressed LRU bit is adjusted so that the next write to that address (with M̄/A high) is into the reset memory location. By tying a single D0–D3 input high, this bit will act as a valid bit assuring that a false match will not occur with a reset memory location.
W̄	Write control input. When the device is selected and W̄ is taken low, D0–D3 and generated parity are written into the addressed memory location in either bank 1 or bank 2. The RAM bank to be written into can be selected automatically or manually depending on the M̄/A input.

FUNCTION TABLES

WRITE MODE

INPUTS							OUTPUTS				I/O	FUNCTION
$\overline{W}$	$\overline{R}$	$\overline{S}$	$\overline{M}$/A	BSEL	$\overline{RESET}$	$\overline{WR}$	MATCH1	MATCH2	$\overline{PE}$	BANK†	D0–D3	
↓	H	L	L	L	H	H	H	H	H	H	Input	Write into bank 1
↓	H	L	L	H	H	H	H	H	H	H	Input	Write into bank 2
↓	H	L	H	X	H	X	H	H	H	L	Input	LRU write into bank 1
↓	H	L	H	X	H	X	H	H	H	H	Input	LRU write into bank 2
↓	L	L	L	L	H	H	H	H	H	H	Input	Write parity error into bank 1
↓	L	L	L	H	H	H	H	H	H	H	Input	Write parity error into bank 2
↓	L	L	H	X	H	H	H	H	H	L	Input	LRU write parity error into bank 1
↓	L	L	H	X	H	H	H	H	H	H	Input	LRU write parity error into bank 2
↓‡	H	L	L	X	H	L‡	H	H	H	H‡	Hi-Z	Write zero into selected bank‡
L	X	↓	X	X	H	H	H	H	H	H or L	Hi-Z	No write occurs
L	X	↓	H	X	H	X	H	H	H	H or L	Hi-Z	No write occurs

READ MODE

INPUTS							OUTPUTS				I/O	FUNCTION
$\overline{W}$	$\overline{R}$	$\overline{S}$	$\overline{M}$/A	BSEL	$\overline{RESET}$	$\overline{WR}$	MATCH1	MATCH2	$\overline{PE}$	BANK	D0–D3	
H	L	L	X	L	H	H	H	H	H	H or L	Output	Read bank 1
H	L	L	X	H	H	H	H	H	H	H or L	Output	Read bank 2
H	L	L	H	L	H	X	H	H	H	H or L	Output	Read bank 1
H	L	L	H	H	H	X	H	H	H	H or L	Output	Read bank 2
H	L	L	X	X	H	H	H	H	L	H or L	Output	Parity error in bank 1 or 2
H	H	L	X	X	H	H	H or L	H or L	EN	H or L	Hi-Z	Disable/compare

COMPARE MODE

INPUTS							OUTPUTS				I/O	FUNCTION
$\overline{W}$	$\overline{R}$	$\overline{S}$	$\overline{M}$/A	BSEL	$\overline{RESET}$	$\overline{WR}$	MATCH1	MATCH2	$\overline{PE}$	BANK	D0–D3	
							H	L	H	H or L		Match bank 1, miss bank 2
							L	H	H	H or L		Match bank 2, miss bank 1
H	H	L	X	X	H	H	H	H	H	H or L		Match bank 1 and 2
			or				L	L	H	H or L	Input	Miss bank 1 and 2
H	H	L	H	X	H	X	L	L	L	H or L		Parity error bank unknown
							L	H	L	H or L		Parity error bank 1, match bank 2
							H	L	L	H or L		Parity error bank 2, match bank 1

EN denotes enabled, H denotes a high level, L denotes a low level, X denotes a don't care level, ↓ denotes the falling edge of the signal.

† The BANK output is transparent when $\overline{W}$ is high and latched when $\overline{W}$ is low, if $\overline{M}$/A is high. When writing with $\overline{M}$/A high, the BANK output indicates which bank D0–D3 is being written into. When writing with $\overline{M}$/A low, the BANK output will not indicate which bank is being written into. After $\overline{W}$ returns high with $\overline{M}$/A low, the BANK output will indicate the correct LRU bit state.

‡ The state of BANK after $\overline{W}$ and $\overline{M}$/A or $\overline{W}$ and $\overline{WR}$ return high is indeterminate. This operation is not recommended.

FUNCTION TABLES (Continued)

RESET, WORD RESET, AND DESELECT MODE

INPUTS							OUTPUTS				I/O D0–D3	FUNCTION
$\overline{W}$	$\overline{R}$	$\overline{S}$	$\overline{M}$/A	BSEL	$\overline{RESET}$	$\overline{WR}$	MATCH1	MATCH2	$\overline{PE}$	BANK		
H	X	L	X	X	L	H	H	H	H	L	Hi-Z	Memory reset-selected
H	X	L	H	X	L	X	H	H	H	L	Hi-Z	Memory reset-selected
X	X	H	X	X	L	X	H	H	H	H	Hi-Z	Memory reset-deselect
H	X	L	L or ↓	L	H	↓	H	H	H	L†	Hi-Z	Word reset in bank 1
H	X	L	↓	L	H	L or ↓	H	H	H	L†	Hi-Z	Word reset in bank 1
H	X	L	L or ↓	H	H	↓	H	H	H	L†	Hi-Z	Word reset in bank 2
H	X	L	↓	H	H	L or ↓	H	H	H	L†	Hi-Z	Word reset in bank 2
H	X	↓	L	X	H	L	H	H	H	H	Hi-Z	No word reset
H	X	L	H	X	H	X	H or L	H or L	EN	H or L	Hi-Z	Word reset disabled
H	X	L	X	X	H	H	H or L	H or L	EN	H or L	Hi-Z	Word reset disabled
X	X	H	X	X	H	X	H	H	H	H	Hi-Z	Device disabled

LRU WRITE

$\overline{S}$	$\overline{WR}$	$\overline{W}$	$\overline{M}$/A	BSEL	LRU-W‡	MATCH1	MATCH2	QI§	LRU WRITE	QN¶	FUNCTION
L	X	↓	H	X	X	H	H	L	YES	H	Write to bank 1, selected by LRU circuitry
L	X	↓	H	X	X	H	H	H	YES	L	Write to bank 2, selected by LRU circuitry
L	H	↓	L	L	X	H	H	X	YES	H	Write to bank 1, selected by BSEL input
L	H	↓	L	H	X	H	H	X	YES	L	Write to bank 2, selected by BSEL input
↓	H	L	X	X	X	H	H	X	NO	QI	No write occurs
↓	X	L	H	X	X	H	H	X	NO	QI	No write occurs
L	H	H	X	X	↓	L	L	X	NO	QI	Miss, no LRU update
L	H	H	X	X	↓	H	L	X	YES	H	Match bank 1, LRU update
L	X	H	H	X	↓	H	L	X	YES	H	Match bank 1, LRU update
L	H	H	X	X	↓	L	H	X	YES	L	Match bank 2, LRU update
L	X	H	H	X	↓	L	H	X	YES	L	Match bank 2, LRU update
L	H	H	L	X	↓	H	H	X	YES	H	Match bank 1 and 2, LRU update
L	X	H	H	X	↓	H	H	X	YES	L	Match bank 1 and 2, LRU update
L	↓	H	L	L	X	H	H	X	YES	L	Word reset in bank 1
L	L	H	↓	L	X	H	H	X	YES	L	Word reset in bank 1
L	↓	H	L	H	X	H	H	X	YES	H	Word reset in bank 2
L	L	H	↓	H	X	H	H	X	YES	H	Word reset in bank 2
L	↓	H	H	X	X	H	H	X	NO	QI	Word reset disabled
L	H	H	↓	X	X	H	H	X	NO	QI	Word reset disabled
↓	L	H	L	X	X	H	H	X	NO	QI	No word reset occurs
H	X	X	X	X	X	H	H	X	NO	QI	Device disabled

H denotes a high level, L denotes a low level, X denotes a don't care level, ↓ denotes the falling edge of the signal.

† The BANK output is forced low during word reset. After a word reset in bank 2, the BANK output will be high.

‡ LRU-W is falling-edge-triggered and has effect only during the compare mode. A falling edge at LRU-W must not be allowed immediately after $\overline{W}$ or $\overline{WR}$ high, since the match outputs may be switching.

§ QI is the state of the LRU RAM output before a LRU write occurs.

¶ QN is the state of the LRU RAM output after a LRU write occurs. This level will be seen at the BANK output, when the write ($\overline{W}$) and word reset ($\overline{WR}$ or $\overline{M}$/A) signals are high.

SN74BCT2160
8K × 4 2-WAY CACHE ADDRESS COMPARATOR/TAG RAM

SCHS011 – D3512, JUNE 1990 – REVISED MARCH 1992

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) .... −1.5 V to 7 V
Input voltage range, any input .... −1.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) .... ± 25 mA
Output clamp current, I_{OK} ($V_I < 0$ or $V_I > V_{CC}$) .... ± 25 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) :   D0–D3, BANK .... ± 25 mA
                                                  MATCH1, MATCH2, $\overline{PE}$ .... ± 50 mA
Continuous current through V_{CC} or GND .... ± 200 mA
Operating free-air temperature range .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .... 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: All voltage values are with respect to GND.

recommended operating conditions (see important notice)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2.2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
V_{OH}	High-level output voltage, MATCH1, MATCH2, and $\overline{PE}$				5.25	V
I_{OH}	High-level output current, D0–D3 and BANK				−8	mA
I_{OL}	Low-level output current	D0–D3, BANK			8	mA
		MATCH1, MATCH2, $\overline{PE}$			27	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

important notice

Negative undershoot at the address or data inputs could cause this device to reset if the V_{IH} level at $\overline{RESET}$ is at its minimum high level (2.2 V). In systems with − 1.5 V or more of undershoot at the address and data inputs, it is recommended that the minimum V_{IH} level at $\overline{RESET}$ be 4 V. As with all designs, proper termination and capacitive bypass techniques should be employed. Unused inputs should be tied to either V_{CC} or GND.

Due to the high-performance characteristics of this device and to ensure the integrity of stored data (or tag), the address inputs must not be allowed to float through the input threshold region (1.2 V – 1.8 V). Rise and fall times at the threshold region of the address inputs must not exceed 20 ns/V. Slow rise and fall times through the threshold region may be eliminated by not using pullup resistors on the address lines and minimizing the high-impedance time when switching between bus drivers. An alternate approach is to use latches or registers in front of the cache tag address inputs to eliminate floating-address conditions. Ground bounce, due to simultaneous switching, into the threshold region of the address inputs should be avoided in order to ensure that a slow rise/fall condition does not occur.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN74BCT2160-12 MIN	TYP[†]	MAX	UNIT
V_{OH} High-level output voltage	D0–D3, BANK	V_{CC} = 4.75 V, I_{OH} = –8 mA	2.4			V
V_{OL} Low-level output voltage	D0–D3, BANK	V_{CC} = 4.75 V, I_{OL} = 8 mA			0.4	V
	MATCH1, MATCH2, $\overline{PE}$	V_{CC} = 4.75 V, I_{OL} = 27 mA			0.4	
I_{OH} High-level output current	MATCH1, MATCH2, $\overline{PE}$	V_{CC} = 4.75 V, V_{OH} = 5.25 V			10	µA
I_I Input current		V_{CC} = 5.25 V, V_I = 0 to V_{CC}			±5	µA
I_{OZ} Off-state output current		V_{CC} = 5.25 V, V_O = 0 to V_{CC}, $\overline{S}$ at V_{IH}			±10	µA
I_{CC1} Supply current (operating)		V_{CC} = 5.25 V, $\overline{RESET}$ at V_{CC}, $\overline{S}$ at 0 V		110	180	mA
I_{CC2} Supply current (reset)		V_{CC} = 5.25 V, $\overline{RESET}$ at 0 V, $\overline{S}$ at 0 V		38	75	mA
I_{CC3} Supply current (deselected)		V_{CC} = 5.25 V, $\overline{RESET}$ at V_{CC}, $\overline{S}$ at V_{CC}		80	150	mA
C_i Input capacitance[‡]		f = 1 MHz			5	pF
C_o Output capacitance[‡]		f = 1 MHz			5	pF

‡ This is the capacitance at an input, output, or I/O pin.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

pulse durations

PARAMETER		SN74BCT2160-12 MIN	TYP[†]	MAX	UNIT
t_{w1} Pulse duration, LRU-W	High	7			ns
	Low	7			
t_{w2} Pulse duration, $\overline{W}$ low		10.5			ns
t_{w3} Pulse duration, $\overline{RESET}$ low		35			ns
t_{w4} Pulse duration, word reset	$\overline{WR}$ low with $\overline{M/A}$ low	10			ns
	$\overline{M/A}$ low with $\overline{WR}$ low	10			

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

setup and hold times

PARAMETER			SN74BCT2160-12 MIN	SN74BCT2160-12 MAX	UNIT
t_{su1}	Setup time, MATCH1 and MATCH2 valid before LRU-W↓		3		ns
t_{su2}	Setup time, $\overline{S}$ low before $\overline{W}$↓	$\overline{M}/A = L$	0		ns
		$\overline{M}/A = H$	8		
t_{su3}	Setup time, address before $\overline{W}$↓	$\overline{M}/A$ high	8		ns
		$\overline{M}/A$ low	0		
t_{su4}	Setup time, BSEL before $\overline{W}$↓ with $\overline{M}/A$ low		0		ns
t_{su5}	Setup time, $\overline{M}/A$ before $\overline{W}$↓		0		ns
t_{su6}	Setup time, D0–D3 before $\overline{W}$↓		0		ns
t_{su7}	Setup time, $\overline{R}$ low before $\overline{W}$↓ (see Note 3)		−1	4	ns
t_{su8}	Setup time, $\overline{RESET}$ inactive before $\overline{W}$↓		12		ns
t_{su9}	Setup time, address before word reset↓	$\overline{WR}$ and $\overline{M}/A$ low	0		ns
t_{su10}	Setup time, BSEL before word reset↓	$\overline{WR}$ and $\overline{M}/A$ low	0		ns
t_{su11}	Setup time, $\overline{S}$ low before word reset↓	$\overline{WR}$ and $\overline{M}/A$ low	0		ns
t_{su12}	Setup time, word reset	$\overline{M}/A$ low before $\overline{WR}$ low	0		ns
		$\overline{WR}$ low before $\overline{M}/A$ low	0		
t_{h1}	Hold time, address after LRU-W↓ (see Note 4)		8		ns
t_{h2}	Hold time, $\overline{S}$ low after LRU-W↓		7		ns
t_{h3}	Hold time, address after $\overline{W}$↓		12		ns
t_{h4}	Hold time, $\overline{S}$ low after $\overline{W}$↓		10		ns
t_{h5}	Hold time, BSEL after $\overline{W}$↓		14		ns
t_{h6}	Hold time, $\overline{M}/A$ after $\overline{W}$↓		14		ns
t_{h7}	Hold time, D0–D3 after $\overline{W}$↓		12		ns
t_{h8}	Hold time, $\overline{R}$ low after $\overline{W}$↓ (see Note 3)		12		ns
t_{h9}	Hold time, address after word reset↓	$\overline{WR}$ and $\overline{M}/A$ low	10		ns
t_{h10}	Hold time, BSEL after word reset↓	$\overline{WR}$ and $\overline{M}/A$ low	12		ns
t_{h11}	Hold time, $\overline{S}$ low after word reset↓	$\overline{WR}$ and $\overline{M}/A$ low	10		ns
t_{h12}	Hold time, word reset↓	$\overline{M}/A$ low after $\overline{WR}$↓	10		ns
		$\overline{WR}$ low after $\overline{M}/A$↓	10		

NOTES: 3. Parameters t_{su7} and t_{h8} apply only during the write cycle timing when writing a parity error. It should be noted that if $\overline{R}$ is low when $\overline{W}$ is high, D0–D3 are enabled as outputs. The maximum specification for t_{su7} avoids possible bus contention on D0–D3.

4. Minimum t_{h1} is the time interval after LRU-W goes low during which the address must remain valid to ensure that an internal LRU write occurs.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

propagation delay times

	PARAMETER	SN74BCT2160-12 MIN	SN74BCT2160-12 TYP†	SN74BCT2160-12 MAX	UNIT
t_{pd1}	Propagation delay time, address to MATCH1 and MATCH2		8	12	ns
t_{pd2}	Propagation delay time, D0–D3 to MATCH1 and MATCH2		8	12	ns
t_{pd3}	Propagation delay time, $\overline{S}$ low to MATCH1 and MATCH2		6	10	ns
t_{pd4}	Propagation delay time, $\overline{S}$ high to MATCH1 and MATCH2 high		4	8	ns
t_{pd5}	Propagation delay time, address to $\overline{PE}$		10	15	ns
t_{pd6}	Propagation delay time, $\overline{S}$ to $\overline{PE}$		8	14	ns
t_{pd7}	Propagation delay time, $\overline{S}$ to BANK		5	10	ns
t_{pd8}	Propagation delay time, address to BANK		8	13	ns
t_{pd9}	Propagation delay time, LRU-W↓ to BANK		8.5	12	ns
t_{pd10}	Propagation delay time, address to D0–D3		9	14.5	ns
t_{pd11}	Propagation delay time, BSEL to D0–D3		4	9	ns
t_{pd12}	Propagation delay time, $\overline{W}$ high to BANK		4	11.5	ns
t_{pd13}	Propagation delay time, $\overline{W}$ low to MATCH1 and MATCH2 high		4	8.5	ns
t_{pd14}	Propagation delay time, $\overline{W}$ low to $\overline{PE}$ high		4	9	ns
t_{pd15}	Propagation delay time, RESET low to MATCH1 and MATCH2 high		4	9.5	ns
t_{pd16}	Propagation delay time, word reset to MATCH1 and MATCH2		5.5	10	ns
t_{pd17}	Propagation delay time, $\overline{W}$ high to MATCH1 and MATCH2			10	ns
t_{pd18}	Propagation delay time, $\overline{W}$ high to $\overline{PE}$			13	ns
t_{pd19}	Propagation delay time, $\overline{RESET}$ high to MATCH1 and MATCH2			25	ns
t_{pd20}	Propagation delay time, $\overline{RESET}$ high to $\overline{PE}$			25	ns
t_{pd21}	Propagation delay time, Word reset to $\overline{PE}$ high		5	9	ns

enable and disable times

	PARAMETER	SN74BCT2160-12 MIN	SN74BCT2160-12 TYP†	SN74BCT2160-12 MAX	UNIT
t_{en1}	Enable time, $\overline{S}$ low to D0–D3		8.5	14	ns
t_{en2}	Enable time, $\overline{R}$ low to D0–D3		5	9	ns
t_{en3}	Enable time, $\overline{RESET}$ high to D0–D3		16	22	ns
t_{dis1}	Disable time, $\overline{R}$ high to D0–D3		4.5	8	ns
t_{dis2}	Disable time, $\overline{S}$ high to D0–D3		5	9	ns
t_{dis3}	Disable time, $\overline{RESET}$ low to D0–D3		5.5	10	ns
t_{dis4}	Disable time, $\overline{W}$ low to D0–D3		5	11	ns

valid times

	PARAMETER	SN74BCT2160-12 MIN	SN74BCT2160-12 MAX	UNIT
t_{v1}	Valid time, MATCH1 and MATCH2 after change of data	1		ns
t_{v2}	Valid time, MATCH1 and MATCH2 after change of address	1		ns
t_{v3}	Valid time, MATCH1 and MATCH2 low after $\overline{S}$ high	0		ns
t_{v4}	Valid time, $\overline{PE}$ after change of address	1		ns
t_{v5}	Valid time, $\overline{PE}$ low after $\overline{S}$ high	0		ns
t_{v6}	Valid time, D0–D3 after change of address	1		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

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INSTRUMENTS

TYPICAL CHARACTERISTICS

LOW-TO-HIGH TRANSITION
OF $\overline{PE}$ OUTPUT
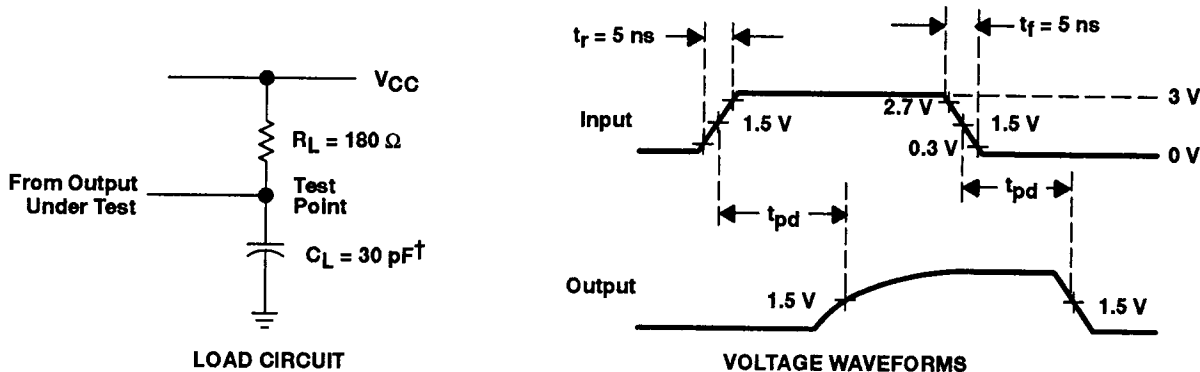### FOR VARIOUS LOADS
OUTPUT VOLTAGE vs TIME
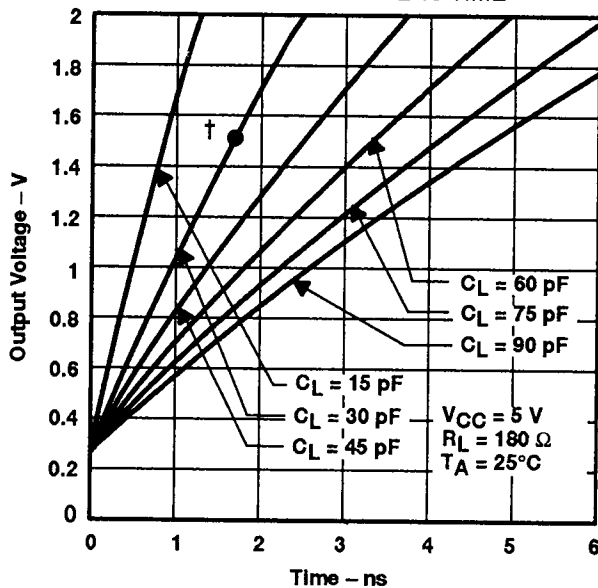
$\dagger$ Specified switching characteristics for open-drain outputs are specified at V_O = 1.5 V with C_L = 30 pF.

Figure 1

Figure 1 is provided as a tool to determine how propagation delay specifications for a 27-mA open-drain output will change with different load capacitance. For example from Figure 1, it can be seen that a 15-pF load will cause about a 1-ns decrease in specified propagation delay while a 60-pF load will cause a 1.7-ns increase in a specified propagation delay. Outputs MATCH1 and MATCH2 have similar characteristics, however, the address to match specification t_{pd1} will not increase until capacitive loading exceeds 75 pF. For an explanation of the match output look-ahead circuit see the *Advantages of Cache Tag RAMs Using Look-Ahead Open-Drain Ouptuts* application report.

PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

$\dagger$ C_L includes probe and test fixture capacitance.

VOLTAGE WAVEFORMS

Figure 2. Open-Drain Outputs

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PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

PROPAGATION-TIME VOLTAGE WAVEFORMS
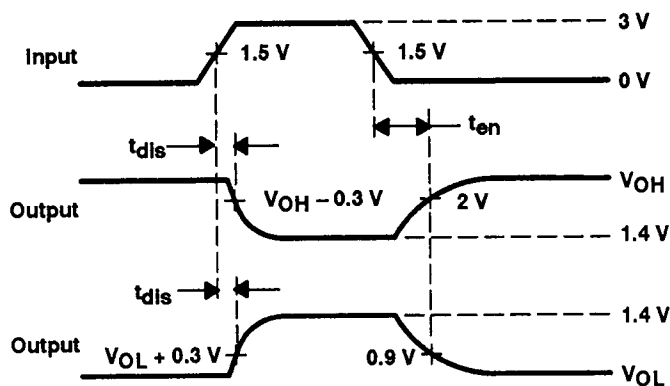
ENABLE/DISABLE VOLTAGE WAVEFORMS

† C_L includes probe and test fixture capacitance.

Figure 3. All Other Outputs

PARAMETER MEASUREMENT INFORMATION

Figure 4. Compare Cycle Timing

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PARAMETER MEASUREMENT INFORMATION
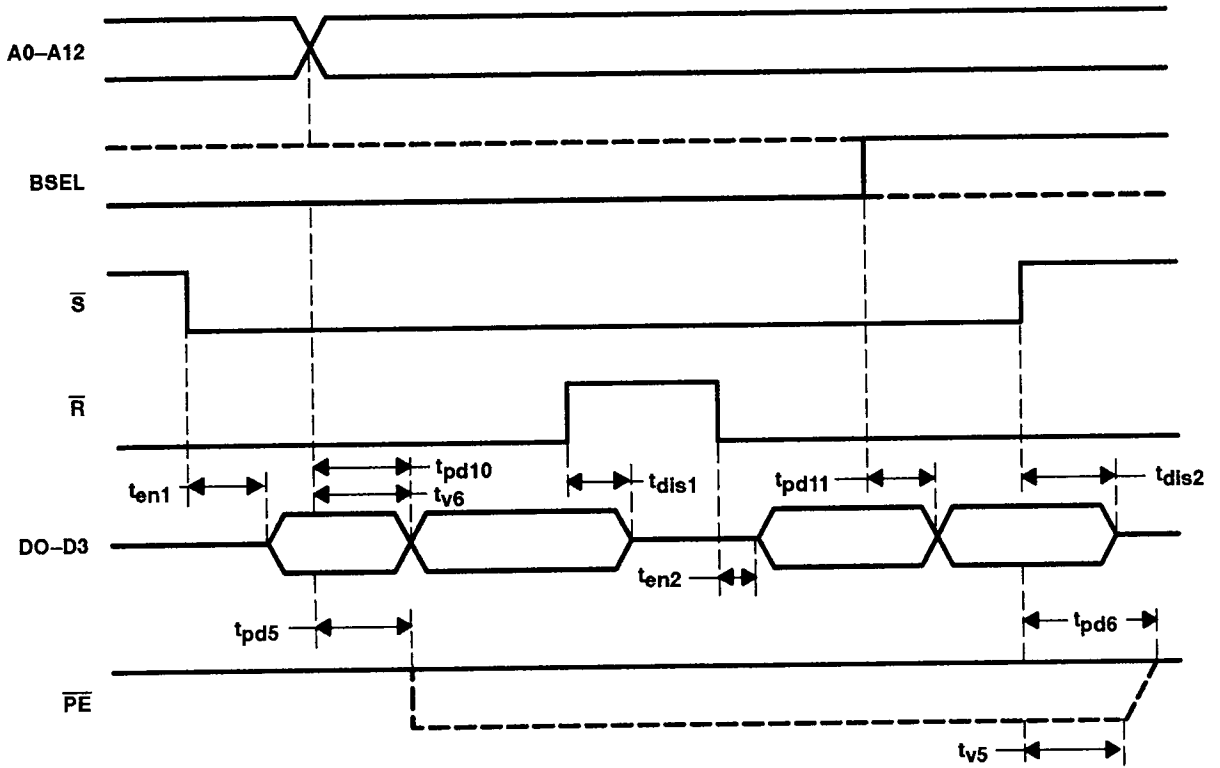
Figure 5. Read Cycle Timing

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PARAMETER MEASUREMENT INFORMATION
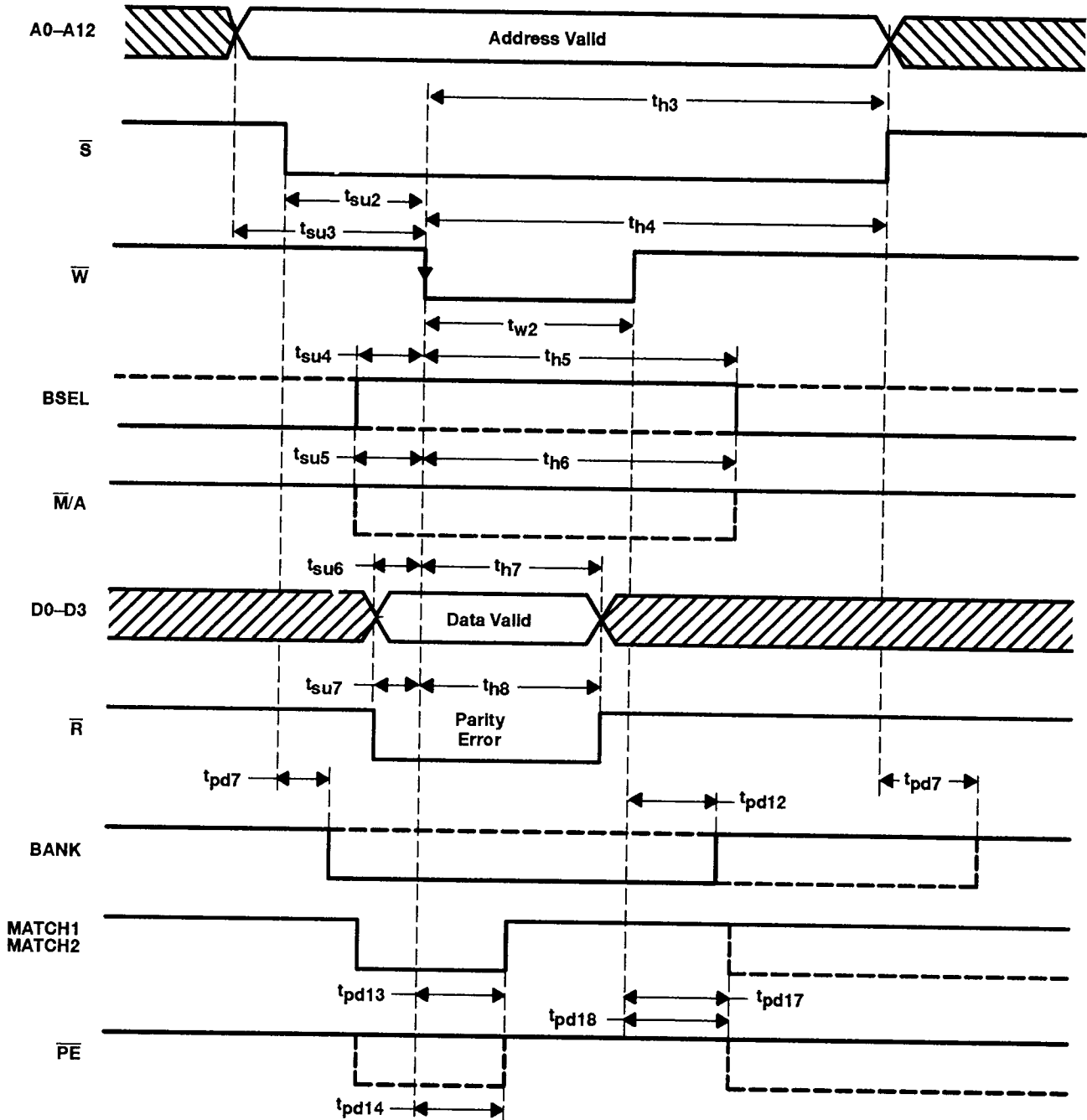
Figure 6. Write Cycle Timing

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PARAMETER MEASUREMENT INFORMATION
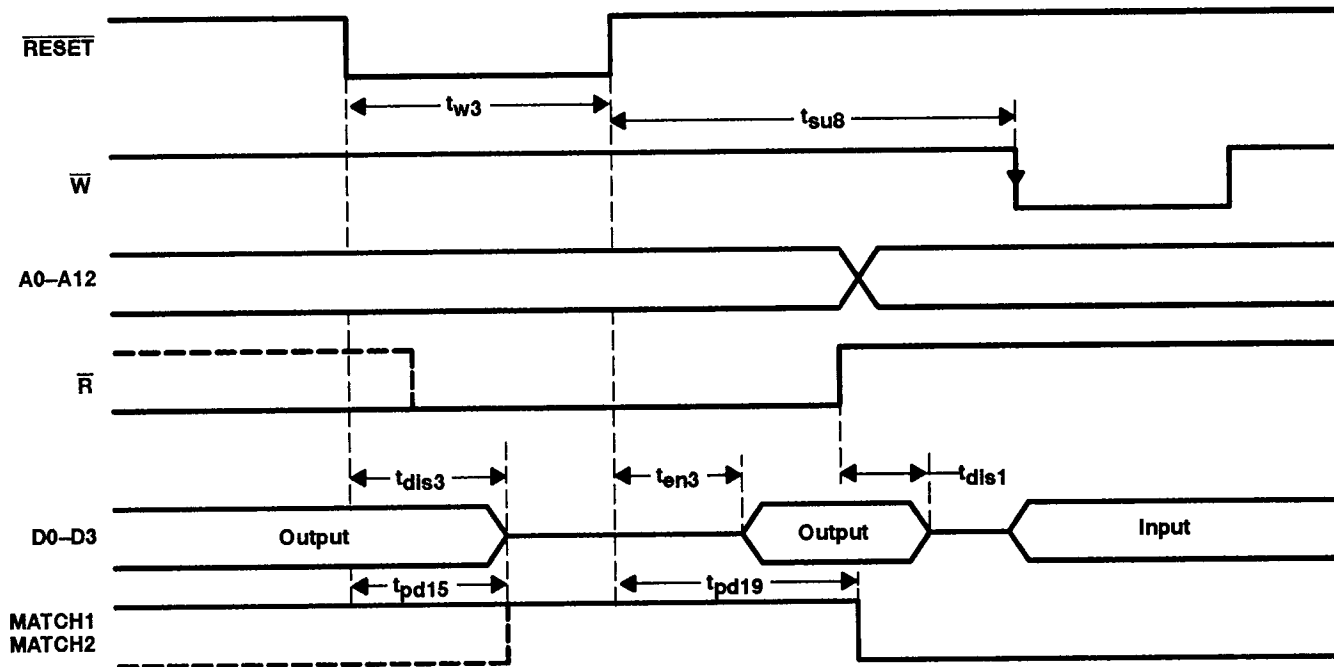
Figure 7. Reset Cycle Timing
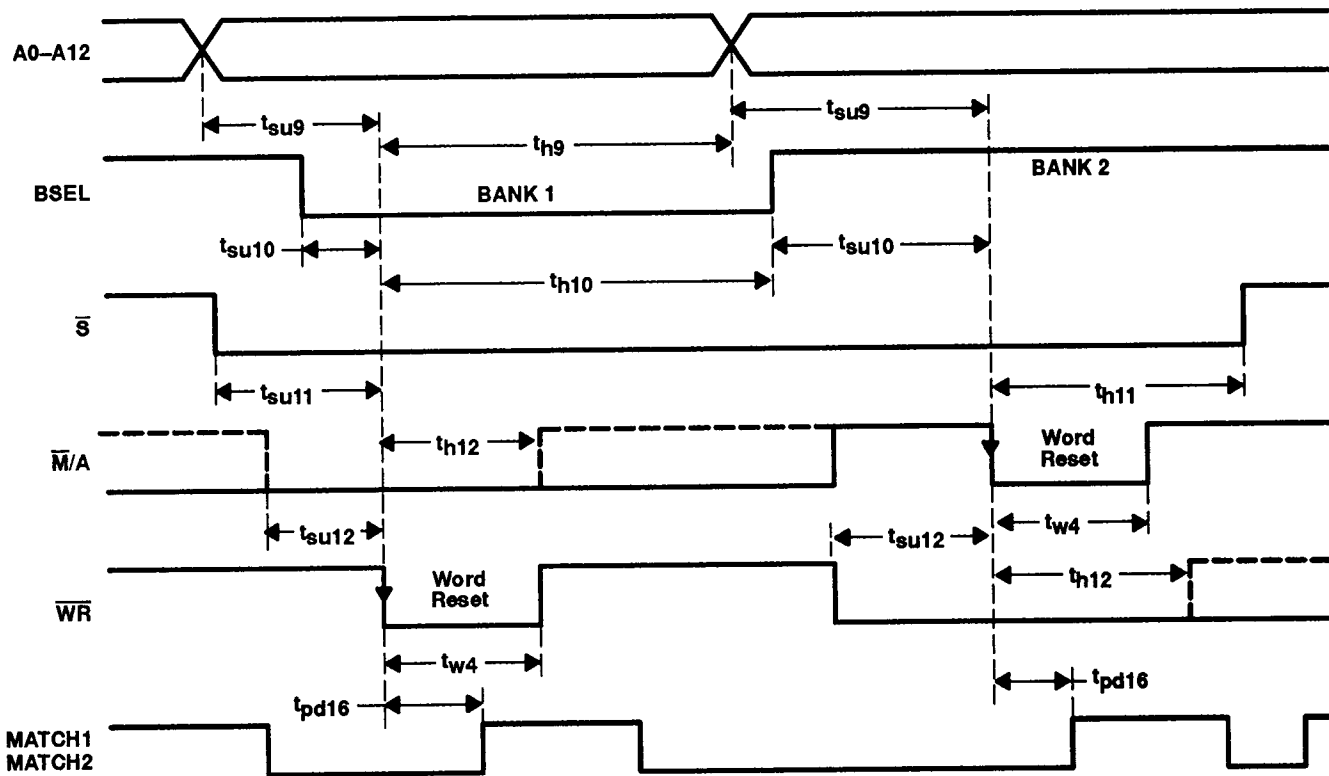
Figure 8. Word Reset Timing

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APPLICATION INFORMATION

Figure 9. Cache Cycles

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APPLICATION INFORMATION

Read Miss	Read or Write Hit	Read or Write Hit	Word Reset
Tag (and data) is written in cache as data comes from main memory to the processor. A LRU write occurs so that the next write (with M̄/A high) to the same indexed location will occur in the other bank.	Read or write hit in Bank 1. LRU write occurs so that the next write (with M̄/A high) to the same index will occur in Bank 2.	Read or write hit in Bank 2. LRU write occurs so that the next write (with M̄/A high) to the same index will occur in Bank 1.	Word reset at Bank 2. LRU write occurs so that the next write (with M̄/A high) to the same index will occur in Bank 2.

Figure 10. LRU Write Timing Diagram

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APPLICATION INFORMATION

DEPTH CASCADING
NUMBER OF DEVICES
CACHE SIZE
vs
LINE SIZE†

† Direct-mapped caches

Figure 11

WIDTH CASCADING
NUMBER OF DEVICES
MAIN MEMORY COVERAGE
vs
LINE SIZE‡
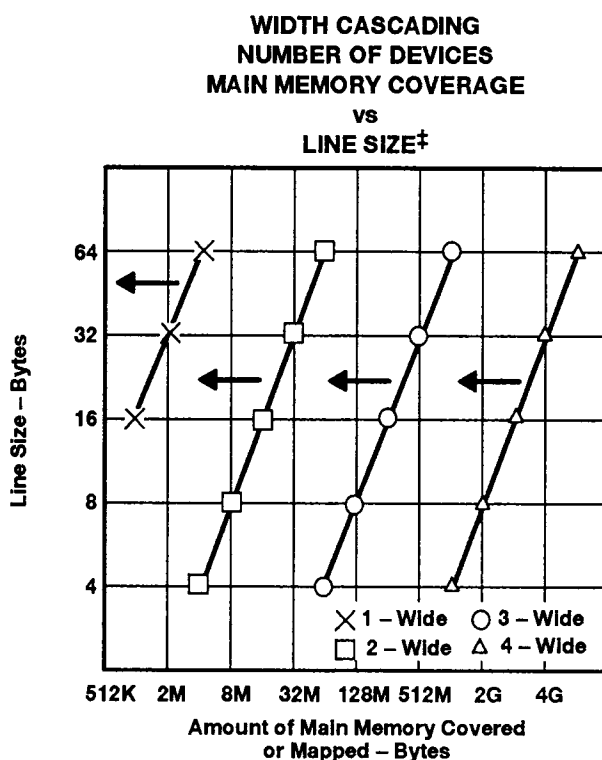
‡ One tag/line

Figure 12

depth cascading

For four-way caches, each solution shown in Figure 11 is moved to the right one increment doubling the cache size and the number of devices used.

width cascading

Memory coverage assumes one bit used as a valid bit (see Figure 12). Each solution for a given line size can be moved to the left covering smaller amounts of memory. Each increment moved represents an unused tag bit. When cascading in depth memory coverage increases, i.e., two deep — twice as much memory.

usage explanation and example

Figures 11 and 12 provide a quick means for determining if the 'BCT2160 will provide a good solution and the number of devices needed for implementation. For example, a design requires 256K bytes of two-way cache, memory coverage of 64M bytes, and a line size of 16 bytes. From Figure 11, it is determined that one 'BCT2160 deep will provide a 256K byte cache with a 16-byte line size. From Figure 12, it is determined that three 'BCT2160s cascaded in width will map 64M bytes of memory (or as much as 256M bytes). Therefore, one deep by three wide (three 'BCT2160s) are needed to meet the design's requirements.

APPLICATION INFORMATION
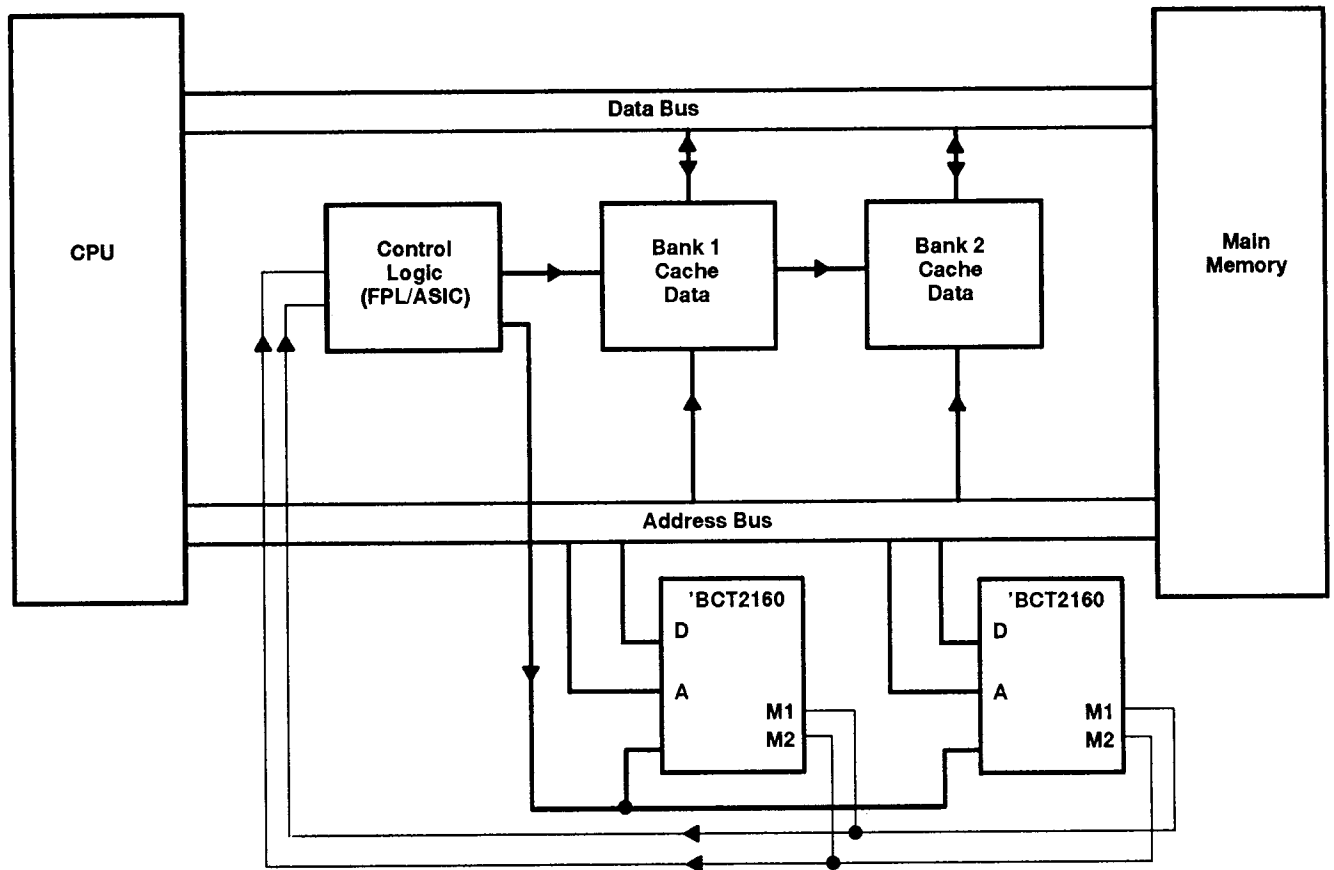
CACHE SIZE[†]	LINE SIZE[†]
(BYTES)	(BYTES)
64K	4
128K	8
256K	16
512K	32
1M	64

† Assumes 1 tag per line and 8K of tag depth. The cache size line size relationship shown can be changed by cascading the 'BCT2160 in depth.

Figure 13. 2-Way Cache Using the 'BCT2160

APPLICATION INFORMATION
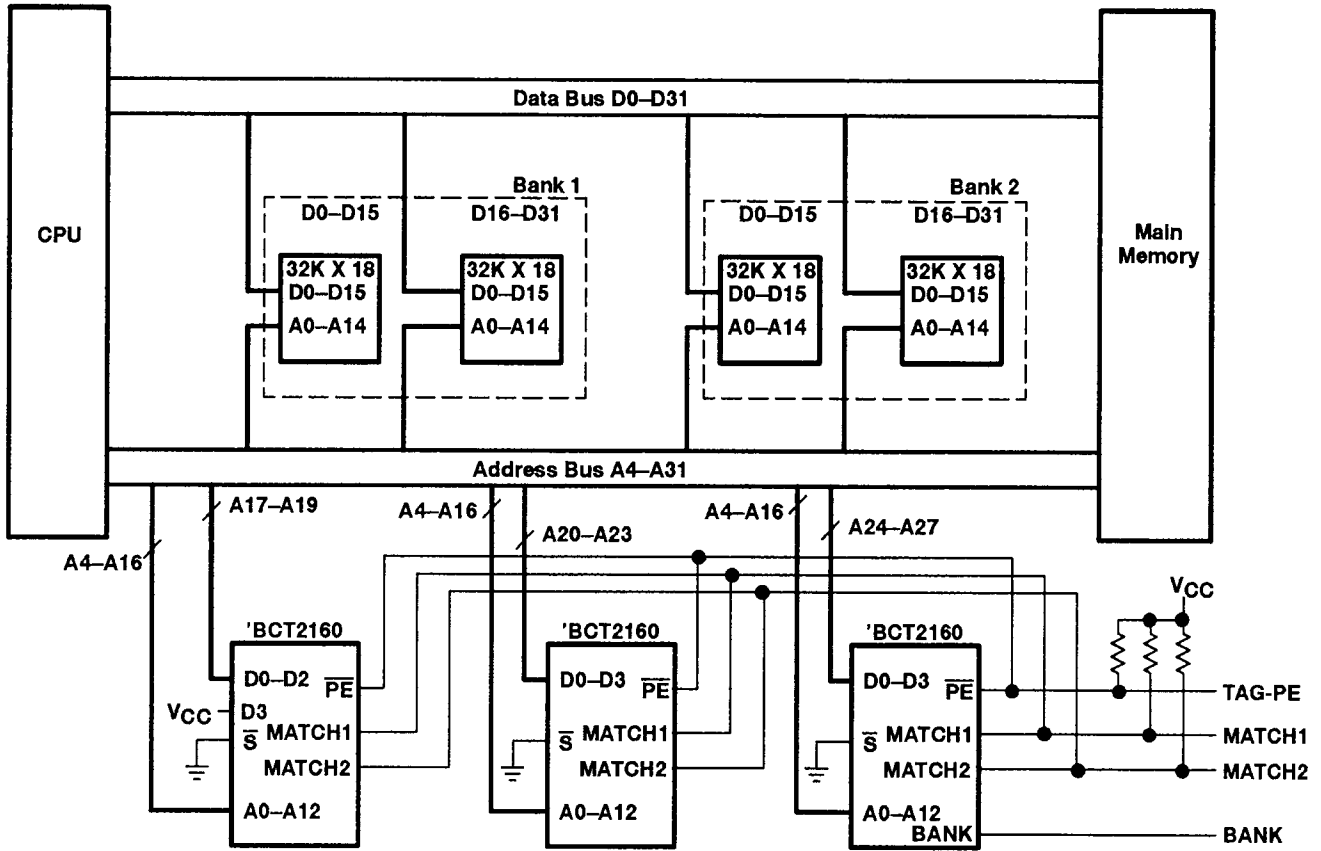
Figure 14. 256K Byte 2-Way Set Associative Cache, Line Size = 16 Bytes
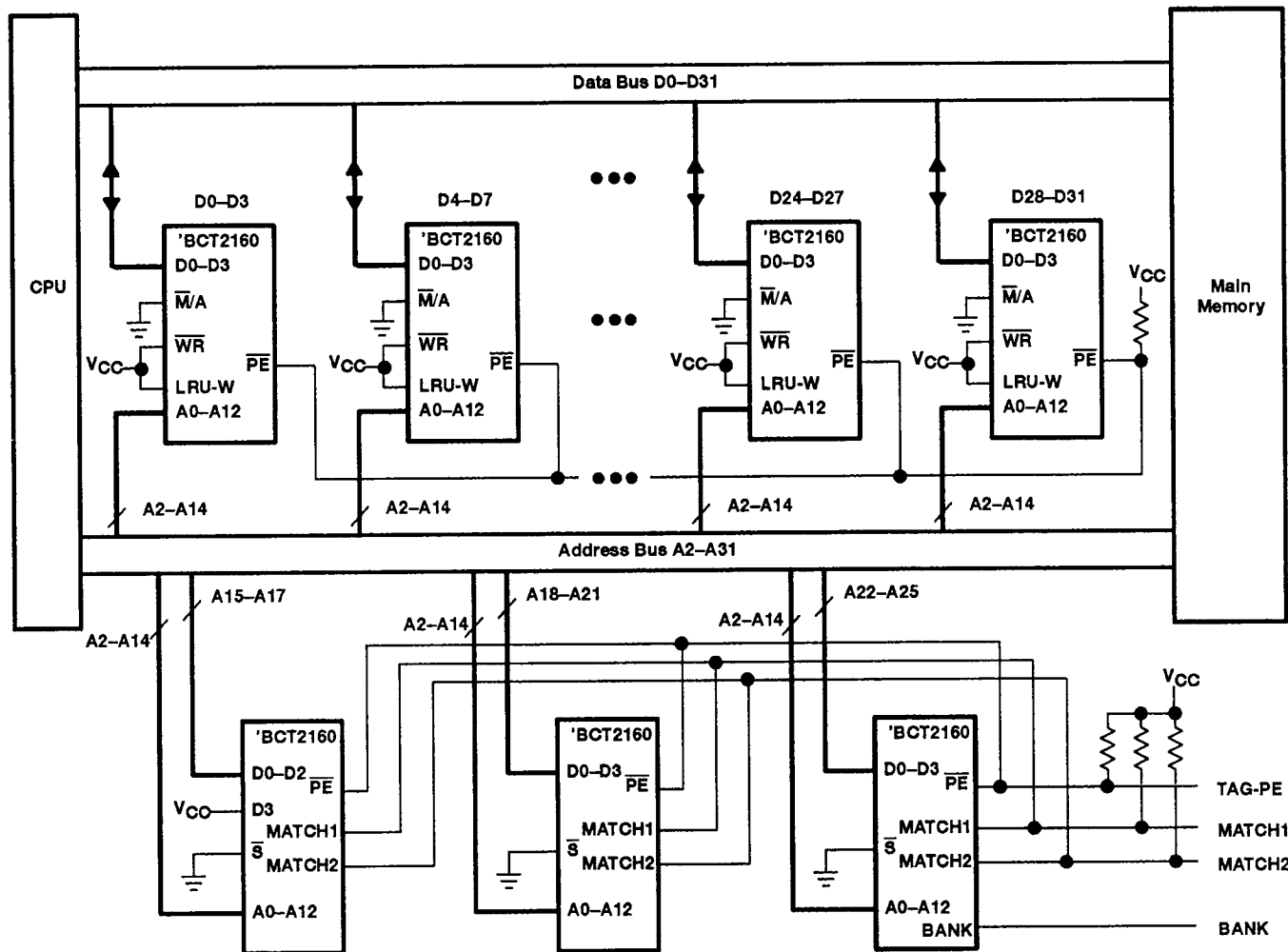
APPLICATION INFORMATION

Figure 15. 64K Byte 2-Way Associative Cache, Line Size = 4 Bytes

APPLICATION INFORMATION

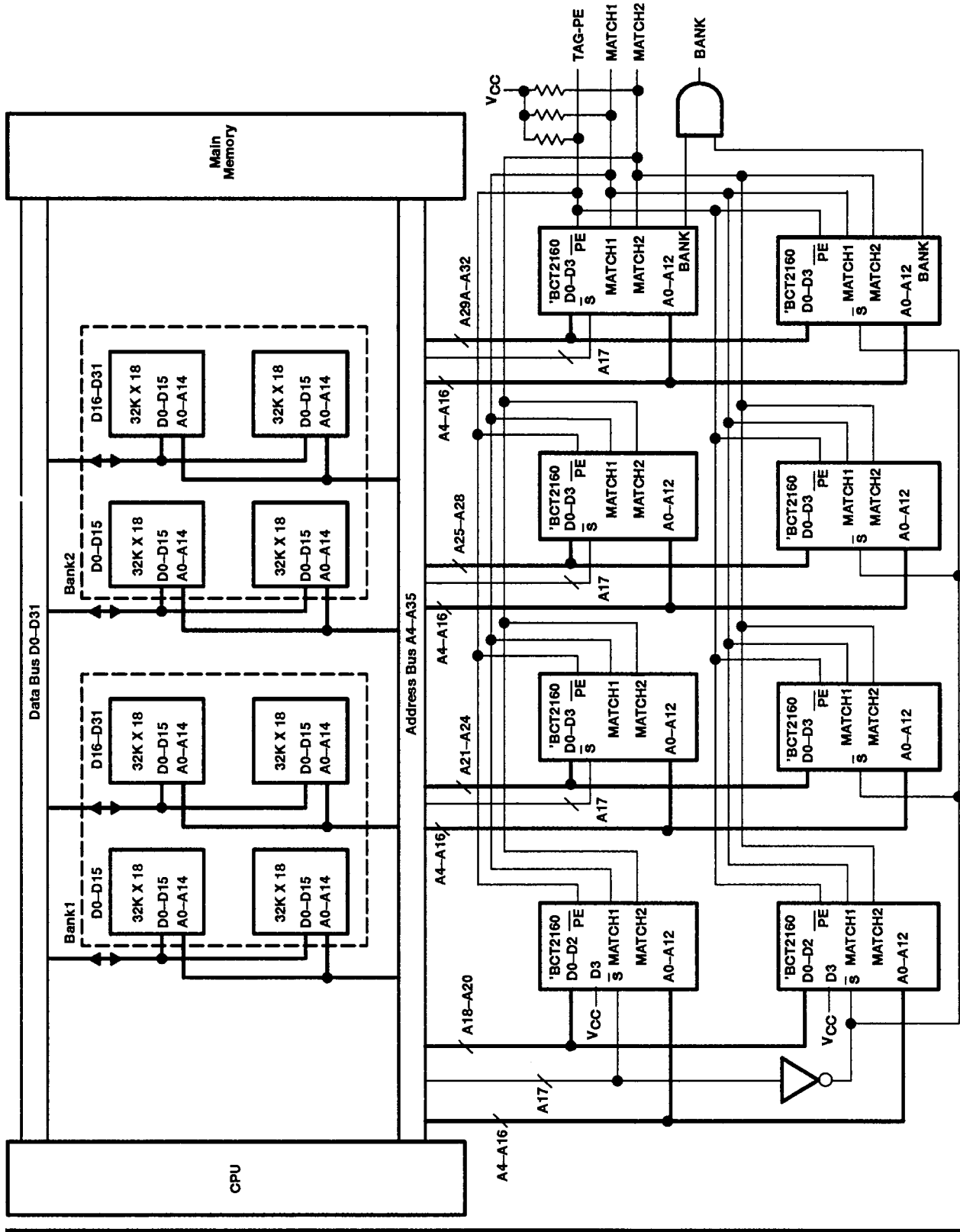Figure 16. 512K Byte Cache, Line Size = 16 Bytes

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APPLICATION INFORMATION
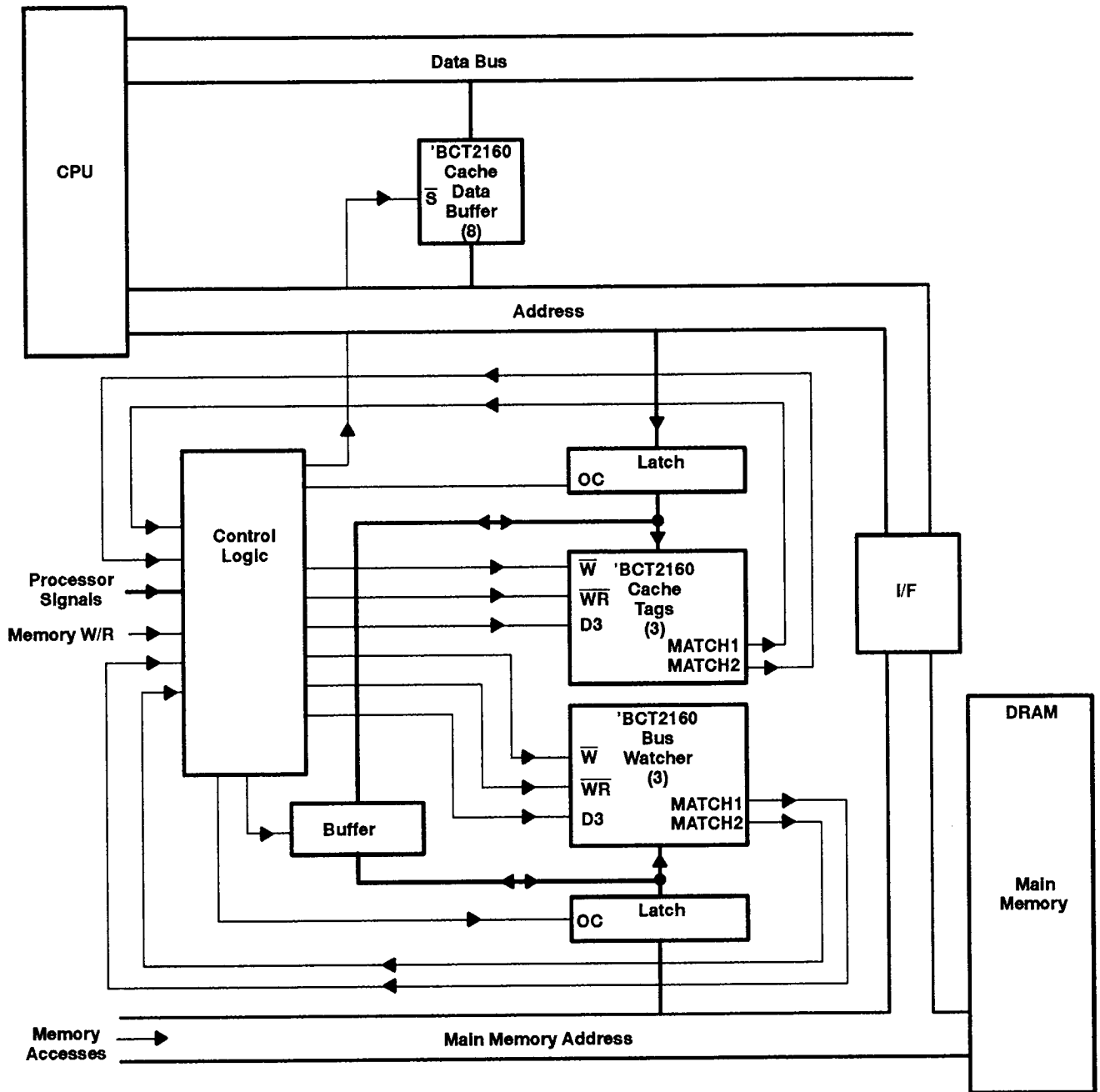
Figure 17. Bus Watching With the 'BCT2160

APPLICATION INFORMATION
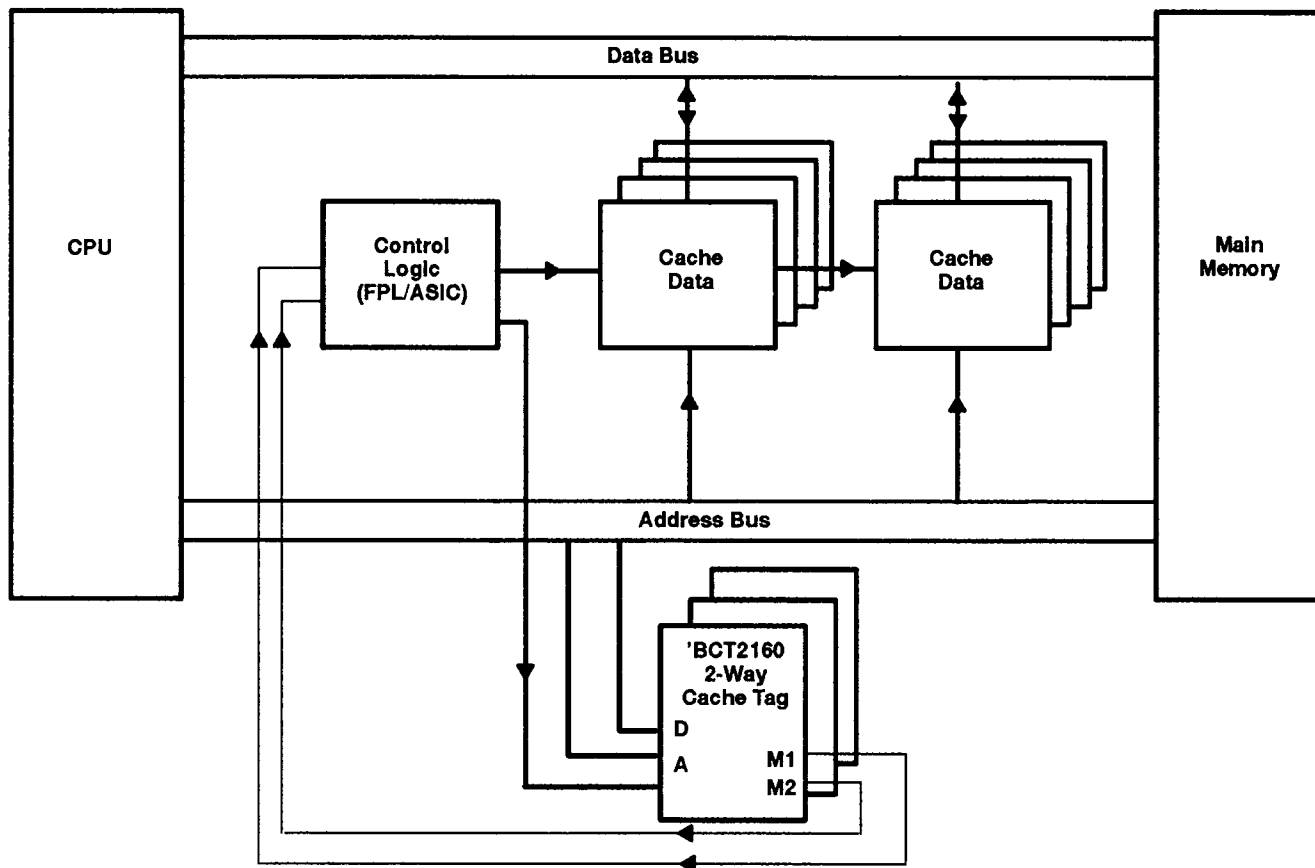
Figure 18. 256K Byte 2-Way Set Associative Cache, Line Size = 16 Bytes

MECHANICAL DATA

FM032
plastic chip carrier

This chip carrier package consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The package is intended for surface mounting on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FM032

Designation per JEDEC Std 30:
R-PLCC-J32

12,57 (0.495) / 12,32 (0.485)

11,51 (0.453) / 11,35 (0.447)

14,05 (0.553) / 13,89 (0.547)

15,11 (0.595) / 14,86 (0.585)

Index Corner

Index Dot

10,80 (0.425) / 10,54 (0.415)

13,34 (0.525) / 13,08 (0.515)

1,27 (0.050) NOM

Seating Plane

3,56 (0.140) / 3,35 (0.132)

1,24 (0.049) / 1,09 (0.043)

0,20 (0.008) NOM

0,76 (0.030) NOM

0,51 (0.020) / 0,38 (0.015)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHICALLY IN INCHES

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