DRAM

MT4C16257

FEATURES

- Industry-standard x16 pinouts, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- All inputs, outputs and clocks are TTL-compatible
- 512-cycle refresh in 8ms (9 rows, 9 column addresses)
- Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR), optional Extended and HIDDEN
- FAST PAGE MODE access cycle
- BYTE WRITE access cycle
- BYTE READ access cycle

OPTIONS MARKING

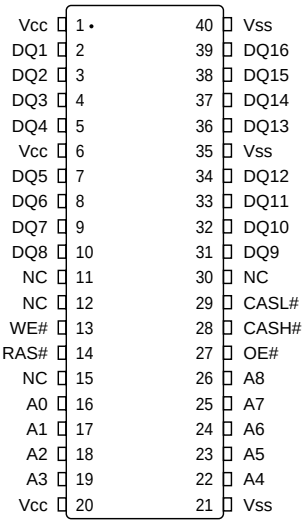
- Timing
  60ns access -6
- Package
  Plastic SOJ (400 mil) DJ
- Part Number Example: MT4C16257DJ-6

KEY TIMING PARAMETERS

SPEED	^tRC	^tRAC	^tPC	^tAA	^tCAC	^tRP
-6	110ns	60ns	35ns	30ns	15ns	40ns

PIN ASSIGNMENT (Top View)

40-Pin SOJ
(DA-6)



Note: The # symbol indicates signal is active LOW.

GENERAL DESCRIPTION

The MT4C16257 is a randomly accessed, solid-state memory containing 4,194,304 bits organized in a x16 configuration. The MT4C16257 has both BYTE WRITE and WORD WRITE access cycles via two CAS# pins.

The MT4C16257 CAS# function and timing are determined by the first CAS# (CASL# or CASH#) to transition LOW and by the last to transition back HIGH. Use of only one of the two results in a BYTE WRITE cycle. CASL# transitioning LOW selects a WRITE cycle for the lower byte (DQ1-DQ8) and CASH# transitioning LOW selects a WRITE cycle for the upper byte (DQ9-DQ16). BYTE READ cycles are achieved through CASL# or CASH# in the same manner during READ cycles for the MT4C16257.

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 18 address bits during READ or WRITE cycles. These are entered 9 bits (A0-A8) at a time. RAS# is used to latch the first 9 bits and CAS# the latter 9 bits.

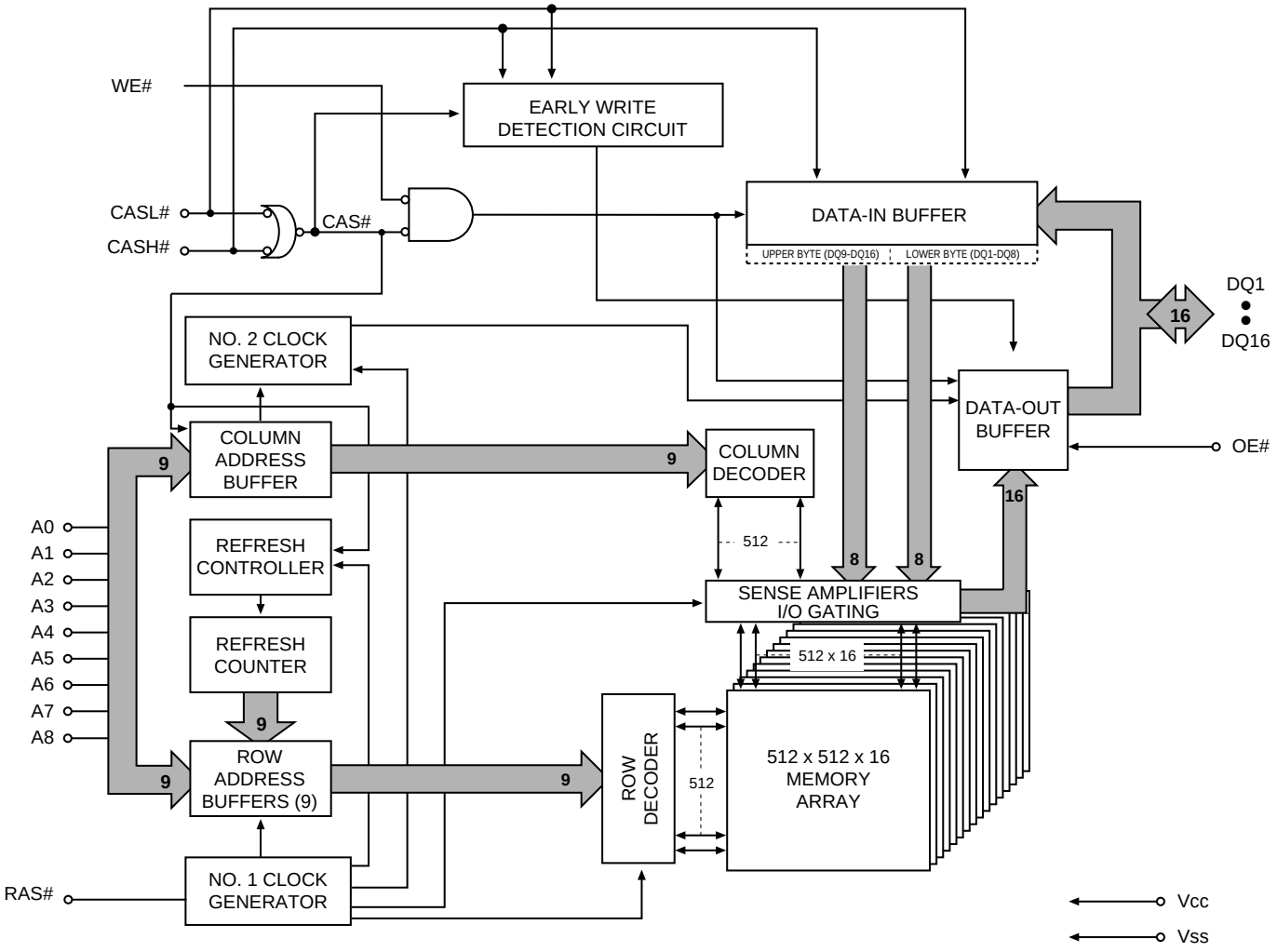
The CAS# control also determines whether the cycle will be a refresh cycle (RAS#-ONLY) or an active cycle (READ, WRITE or READ WRITE) once RAS# goes LOW.

The CASL# and CASH# inputs internally generate a CAS# signal functioning in an identical manner to the single CAS# input on the other 256K x 16 DRAMs. The key difference is each CAS# controls its corresponding DQ tristate logic (in conjunction with OE# and WE#). CASL# controls DQ1 through DQ8 and CASH# controls DQ9 through DQ16.

The MT4C16257 CAS# function is determined by the first CAS# (CASL# or CASH#) to transition LOW and the last one to transition back HIGH. The two CAS# controls give the MT4C16257 both BYTE READ and BYTE WRITE cycle capabilities.

A logic HIGH on WE# dictates READ mode while a logic LOW on WE# dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. Taking WE# LOW will ini-

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION (continued)

tiate a WRITE cycle, selecting DQ1 through DQ16. If WE# goes LOW prior to CAS# going LOW, the output pin(s) remain open (High-Z) until the next CAS# cycle. If WE# goes LOW after CAS# goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as CAS# and OE# remain LOW (regardless of WE# or RAS#). This late WE# pulse results in a READ WRITE cycle.

The 16 data inputs and 16 data outputs are routed through 16 pins using common I/O, and pin direction is controlled by OE#.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A8) page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS# followed by a column address strobed-in by CAS#. CAS# may be toggled by holding RAS# LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST PAGE MODE operation.

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the RAS# high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# refresh cycle (RAS#-ONLY, CBR, or HIDDEN) so that all 512 combinations of RAS# addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

Extended refresh is a CBR REFRESH performed at the extended refresh rate with CMOS input levels. This mode provides a lower-current data-retention cycle.

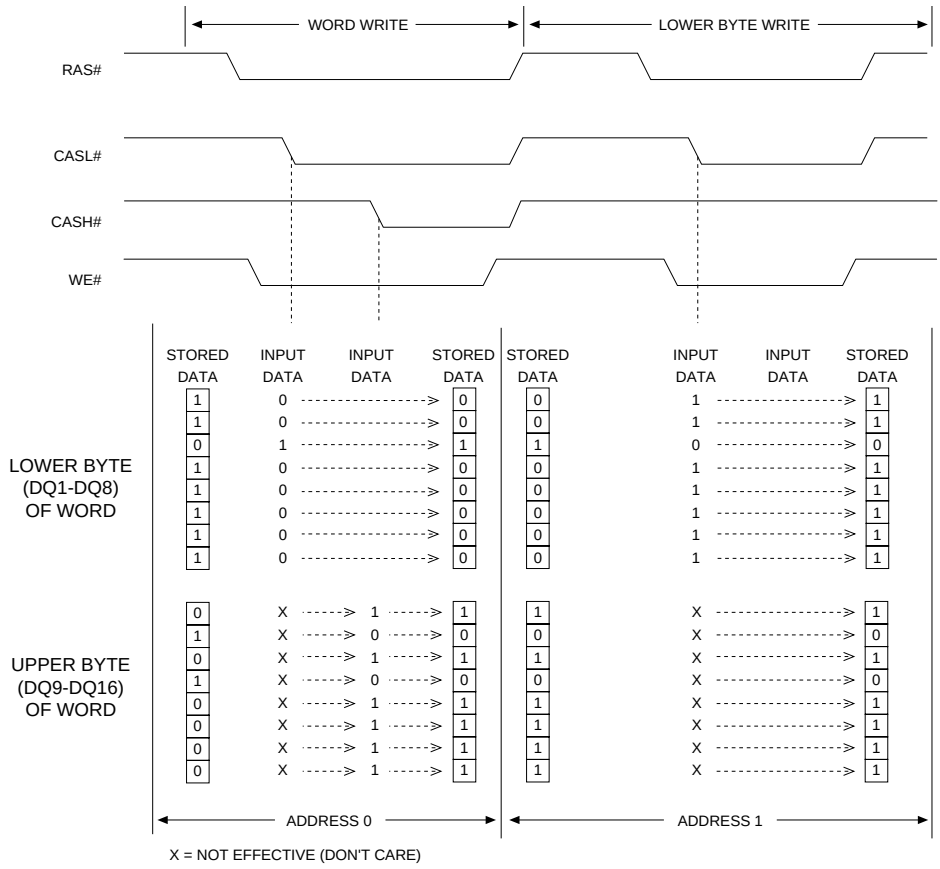


Figure 1
WORD AND BYTE WRITE EXAMPLE

BYTE ACCESS CYCLE

The BYTE WRITE mode is determined by the use of CASL# and CASH#. Enabling CASL# will select a lower BYTE WRITE cycle (DQ1-DQ8) while enabling CASH# will select an upper BYTE WRITE cycle (DQ9-DQ16). Enabling both CASL# and CASH# selects a WORD WRITE cycle.

The MT4C16257 can be viewed as two 256K x 8 DRAMS which have common input controls, with the exception of the CAS# inputs. Figure 1 illustrates the MT4C16257 BYTE WRITE and WORD WRITE cycles.

The MT4C16257 also has BYTE READ and WORD READ cycles. Figure 2 illustrates the MT4C16257 BYTE READ and WORD READ cycles.

Additionally, both bytes must always be of the same mode of operation if both bytes are active. A CAS# precharge must be satisfied prior to changing modes of operation between the upper and lower bytes. For example, an EARLY WRITE on one byte and a LATE WRITE on the other byte is not allowed during the same cycle. However, an EARLY WRITE on one byte and, after a CAS# precharge has been satisfied, a LATE WRITE on the other byte is permissible.

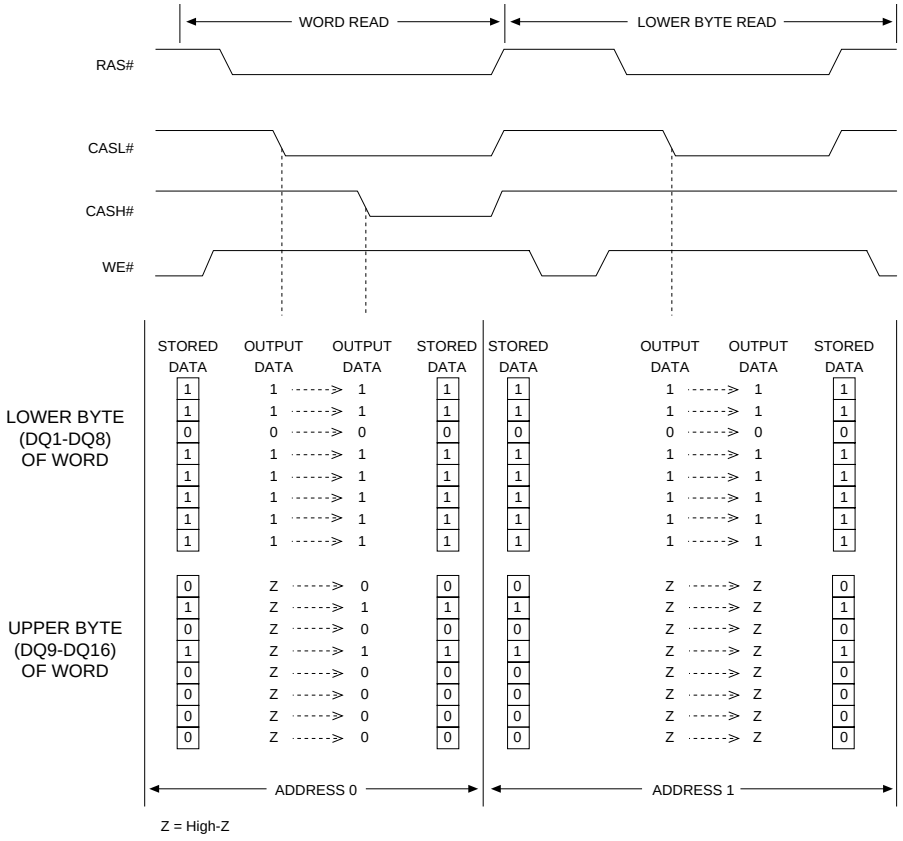


Figure 2
WORD AND BYTE READ EXAMPLE

TRUTH TABLE

FUNCTION		RAS#	CASL#	CASH#	WE#	OE#	ADDRESSES ^tR	ADDRESSES ^tC	DQs	NOTES
Standby		H	H→X	H→X	X	X	X	X	High-Z	
READ: WORD		L	L	L	H	L	ROW	COL	Data-Out	
READ: LOWER BYTE		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out Upper Byte, High-Z	
READ: UPPER BYTE		L	H	L	H	L	ROW	COL	Lower Byte, High-Z Upper Byte, Data-Out	
WRITE: WORD (EARLY WRITE)		L	L	L	L	X	ROW	COL	Data-In	
WRITE: LOWER BYTE (EARLY)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In Upper Byte, High-Z	
WRITE: UPPER BYTE (EARLY)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z Upper Byte, Data-In	
READ WRITE		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
PAGE-MODE	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
READ	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-Out	2
PAGE-MODE	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
WRITE	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-In	1
PAGE-MODE	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
READ-WRITE	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1, 2
HIDDEN	READ	L→H→L	L	L	H	L	ROW	COL	Data-Out	2
REFRESH	WRITE	L→H→L	L	L	L	X	ROW	COL	Data-In	1, 3
RAS#-ONLY REFRESH		L	H	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	L	X	X	X	X	High-Z	4

NOTE: 1. These WRITE cycles may also be BYTE WRITE cycles (either CASL# or CASH# active).
2. These READ cycles may also be BYTE READ cycles (either CASL# or CASH# active).
3. EARLY WRITE only.
4. At least one of the two CAS# signals must be active (CASL# or CASH#).

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1.2W
Short Circuit Output Current 50mA
No-connect pins not to exceed ..... V_{CC}

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 5, 6) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC} +1	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{CC} +1.0V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (DQ is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

		MAX		
PARAMETER/CONDITION	SYMBOL	-6	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS# = CAS# = V_{IH})	I_{CC1}	2	mA	
STANDBY CURRENT: (CMOS) (RAS# = CAS# = V_{CC} -0.2V)	I_{CC2}	1	mA	22
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: ^tRC = ^tRC [MIN])	I_{CC3}	195	mA	3, 34
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	120	mA	3, 34
REFRESH CURRENT: RAS# ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	195	mA	3, 34
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^tRC = ^tRC [MIN])	I_{CC6}	180	mA	3, 4

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C_{I1}	5	pF	2
Input Capacitance: RAS#, CASL#, CASH#, WE#, OE#	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6			
PARAMETER	SYM	MIN	MAX	UNITS	NOTES
Access time from column address	^tAA		30	ns	
Column-address hold time (referenced to RAS#)	^tAR	50		ns	
Column-address setup time	^tASC	0		ns	26
Row-address setup time	^tASR	0		ns	
Column-address to WE# delay time	^tAWD	55		ns	18
Access time from CAS#	^tCAC		15	ns	28
Column-address hold time	^tCAH	10		ns	26
CAS# pulse width	^tCAS	15	10,000	ns	31
CAS# hold time (CBR REFRESH)	^tCHR	10		ns	4, 27
Last CAS# going LOW to first CAS# returning HIGH	^tCLCH	10		ns	29
CAS# to output in Low-Z	^tCLZ	3		ns	28
CAS# precharge time	^tCP	10		ns	13
Access time from CAS# precharge	^tCPA		35	ns	28
CAS# to RAS# precharge time	^tCRP	10		ns	27
CAS# hold time	^tCSH	60		ns	27
CAS# setup time (CBR REFRESH)	^tCSR	10		ns	4, 26
CAS# to WE# delay time	^tCWD	40		ns	18, 26
Write command to CAS# lead time	^tCWL	15		ns	23, 27
Data-in hold time	^tDH	10		ns	19, 28
Data-in setup time	^tDS	0		ns	19, 28
Output disable time	^tOD	3	15	ns	25, 33
Output enable time	^tOE		15	ns	28
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^tOEH	15		ns	26
Output buffer turn-off delay	^tOFF	3	15	ns	17, 25, 28
OE# setup prior to RAS# during HIDDEN REFRESH cycle	^tORD	0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	^tPC	35		ns	30
FAST-PAGE-MODE READ-WRITE cycle time	^tPRWC	85		ns	30
Access time from RAS#	^tRAC		60	ns	
RAS# to column-address delay time	^tRAD	15		ns	15
Row-address hold time	^tRAH	10		ns	
RAS# pulse width	^tRAS	60	10,000	ns	
RAS# pulse width (PAGE MODE)	^tRASP	60	100,000	ns	
Random READ or WRITE cycle time	^tRC	110		ns	
RAS# to CAS# delay time	^tRCD	20		ns	14, 26
Read command hold time (referenced to CAS#)	^tRCH	0		ns	16, 23, 27

AC ELECTRICAL CHARACTERISTICS

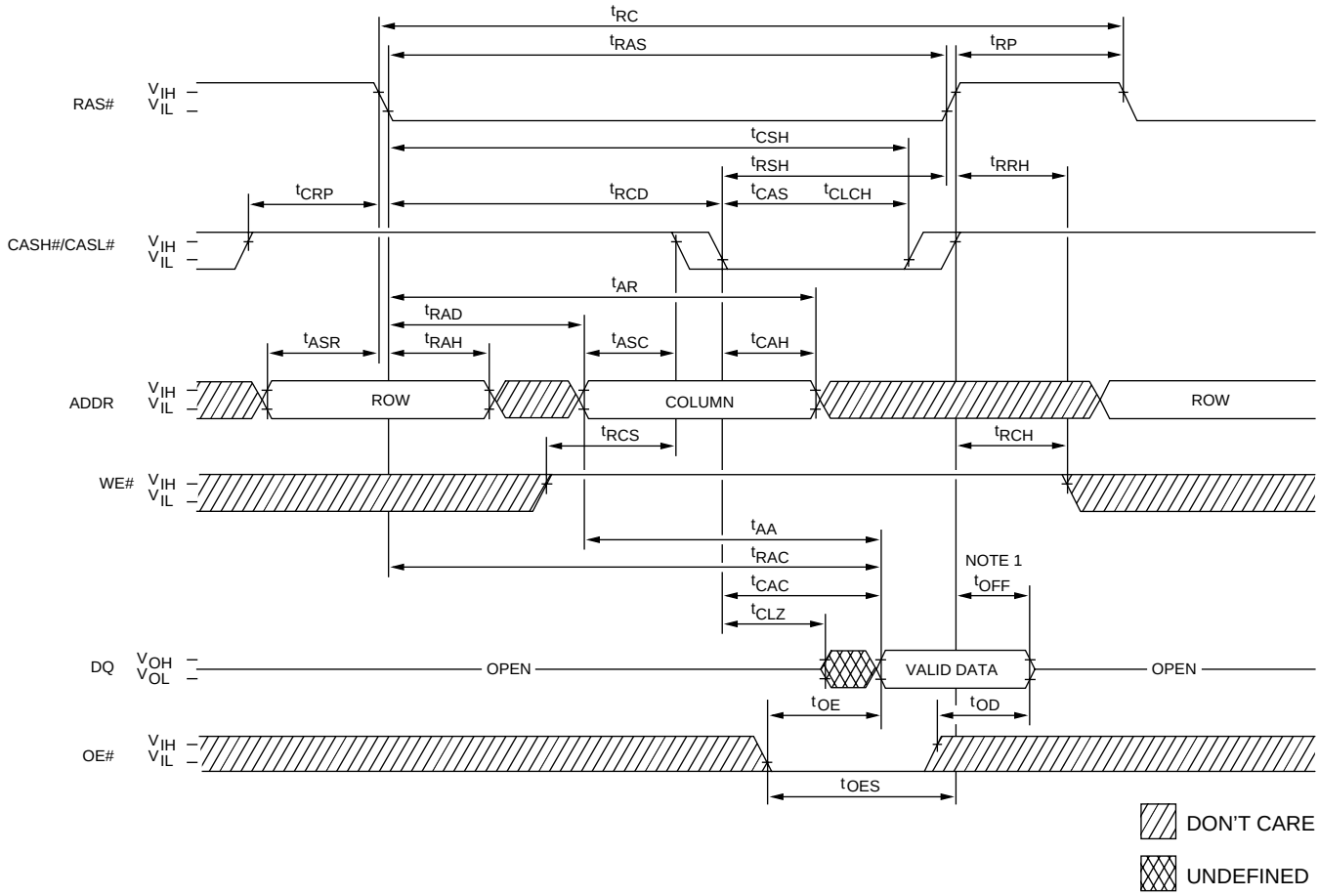
(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (Vcc = +5V ±10%)

AC CHARACTERISTICS		-6			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read command setup time	^{t}RCS	0		ns	23, 26
Refresh period (512 cycles)	^{t}REF		8	ms	
RAS# precharge time	^{t}RP	40		ns	
RAS# to CAS# precharge time	^{t}RPC	10		ns	
Read command hold time (referenced to RAS#)	^{t}RRH	0		ns	16
RAS# hold time	^{t}RSH	15		ns	32
READ WRITE cycle time	^{t}RWC	150		ns	
RAS# to WE# delay time	^{t}RWD	85		ns	18
Write command to RAS# lead time	^{t}RWL	15		ns	23
Transition time (rise or fall)	^{t}T	2	50	ns	
Write command hold time	^{t}WCH	10		ns	23, 32
Write command hold time (referenced to RAS#)	^{t}WCR	45		ns	23
Write command setup time	^{t}WCS	0		ns	18, 23, 26
Write command pulse width	^{t}WP	10		ns	23
WE# hold time (CBR REFRESH)	^{t}WRH	10		ns	
WE# setup time (CBR REFRESH)	^{t}WRP	10		ns	

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 4.5V; f = 1 MHz.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is ensured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# refresh cycles (RAS#-ONLY or CBR), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
7. AC characteristics assume ^tT = 5ns.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH}, data output is High-Z.
11. If CAS# = V_{IL}, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF, V_{OL} = 0.80 and V_{OH} = 2V.
13. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, CAS# must be pulsed HIGH for ^tCP.
14. The ^tRCD (MAX) limit is no longer specified. ^tRCD (MAX) was specified as a reference point only. If ^tRCD was greater than the specified ^tRCD (MAX) limit, then access time was controlled exclusively by ^tCAC (^tRAC [MIN] no longer applied). With or without the ^tRCD limit, ^tAA and ^tCAC must always be met.
15. The ^tRAD (MAX) limit is no longer specified. ^tRAD (MAX) was specified as a reference point only. If ^tRAD was greater than the specified ^tRAD (MAX) limit, then access time was controlled exclusively by ^tAA (^tRAC and ^tCAC no longer applied). With or without the ^tRAD (MAX) limit, ^tAA, ^tRAC and ^tCAC must always be met.
16. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
17. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The 3ns minimum is a parameter guaranteed by design.
18. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge ^tWCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge ^tRWD$ (MIN), $^tAWD \ge ^tAWD$ (MIN) and $^tCWD \ge ^tCWD$ (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of Q (at access time and until CAS# or OE# goes back to V_{IH}) is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW result in a LATE WRITE (OE#-controlled) cycle.
19. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
20. During a READ cycle, if OE# is LOW then taken HIGH before CAS# goes HIGH, Q goes open. If OE# is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
21. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
22. All other inputs at V_{CC} -0.2V.
23. Write command is defined as WE# going LOW.
24. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if CAS# remains LOW and OE# is taken back LOW after ^tOEH is met. If CAS# goes HIGH prior to OE# going back LOW, the DQs will remain open.
25. The DQs open during READ cycles once ^tOD or ^tOFF occur. If CAS# goes HIGH before OE#, the DQs will open regardless of the state of the OE#. If CAS# stays LOW while OE# is brought HIGH, the DQs will open. If OE# is brought back LOW (CAS# still LOW), the DQs will provide the previously read data.
26. The first CASx# edge to transition LOW.
27. The last CASx# edge to transition HIGH.
28. Output parameter (DQx) is referenced to corresponding CAS# input, DQ1-DQ8 by CASL# and DQ9-DQ16 by CASH#.
29. Last falling CASx# edge to first rising CASx# edge.
30. Last rising CASx# edge to next cycle's last rising CASx# edge.
31. Each CASx# must meet minimum pulse width.
32. Last CASx# to go LOW.
33. All DQs controlled, regardless CASL# and CASH#.
34. Column address changed once each cycle.

READ CYCLE

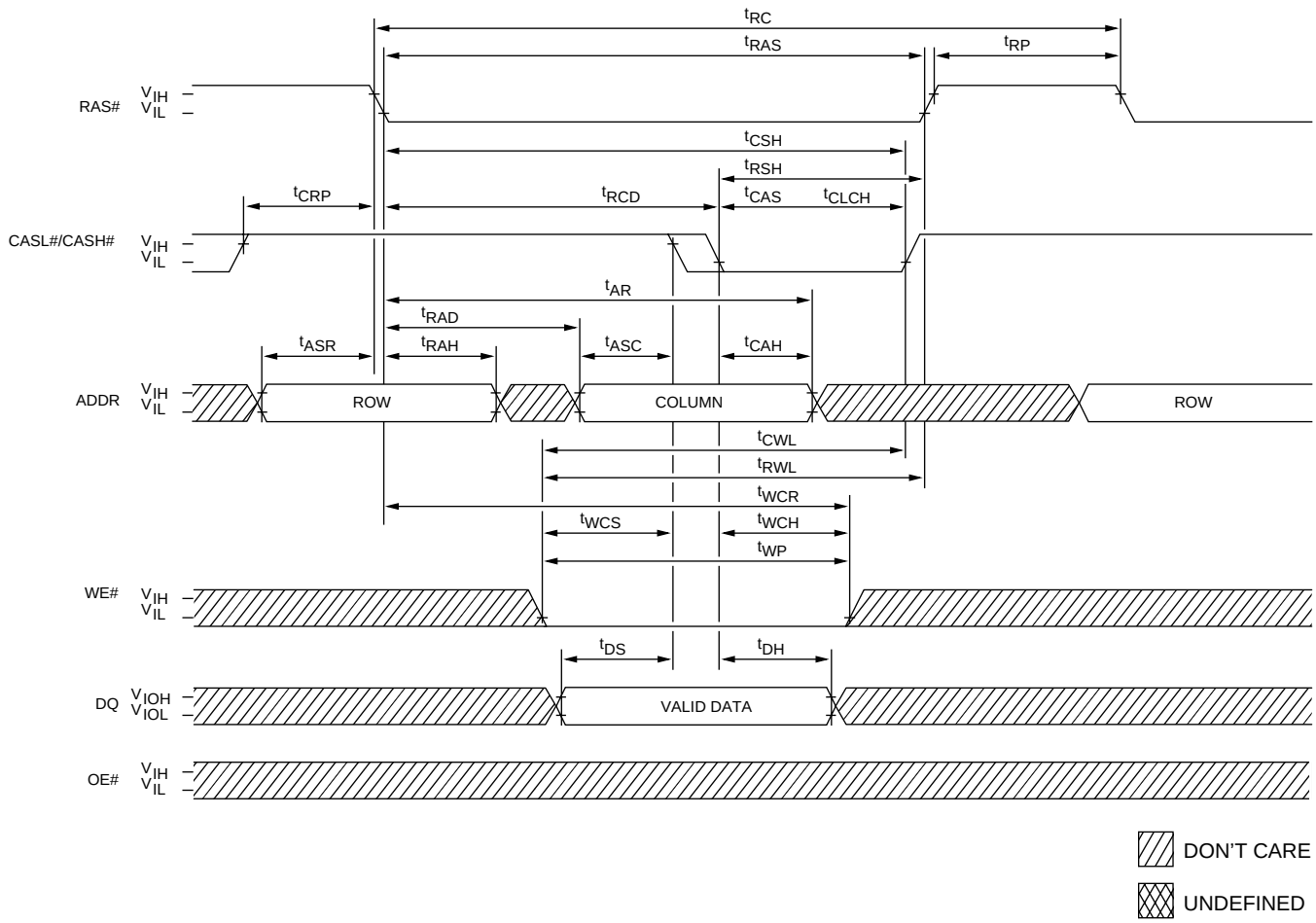


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	50		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLCH	10		ns
tCLZ	3		ns
tCRP	10		ns
tCSH	60		ns
tOD	3	15	ns
tOE		15	ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOFF	3	15	ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRAS	60	10,000	ns
tRC	110		ns
tRCD	20		ns
tRCH	0		ns
tRCS	0		ns
tRP	40		ns
tRRH	0		ns
tRSH	15		ns

EARLY WRITE CYCLE



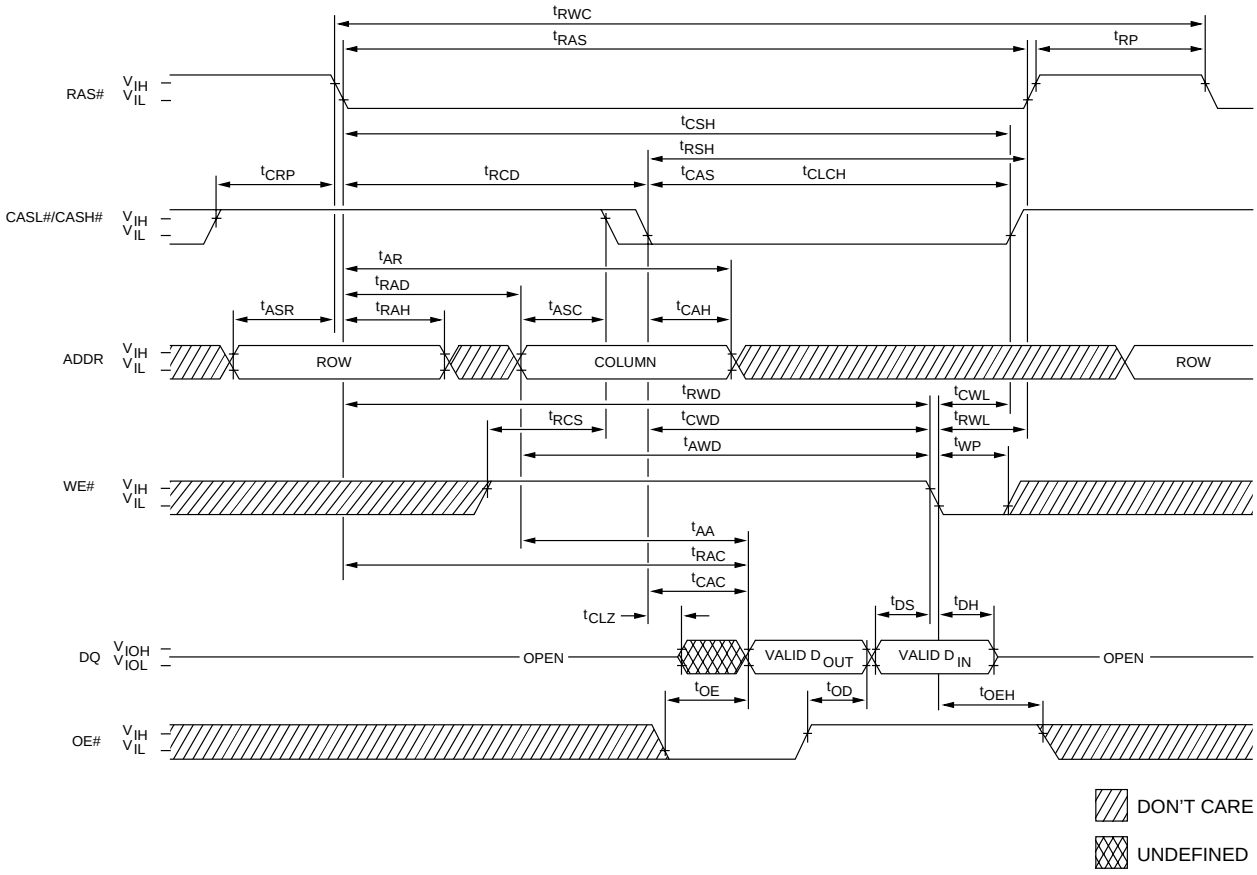
TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAR	50		ns
tASC	0		ns
tASR	0		ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLCH	10		ns
tCRP	10		ns
tCSH	60		ns
tCWL	15		ns
tDH	10		ns
tDS	0		ns
tRAD	15		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tRAH	10		ns
tRAS	60	10,000	ns
tRC	110		ns
tRCD	20		ns
tRP	40		ns
tRSH	15		ns
tRWL	15		ns
tWCH	10		ns
tWCR	45		ns
tWCS	0		ns
tWP	10		ns

READ WRITE CYCLE

(LATE WRITE and READ-MODIFY-WRITE cycles)

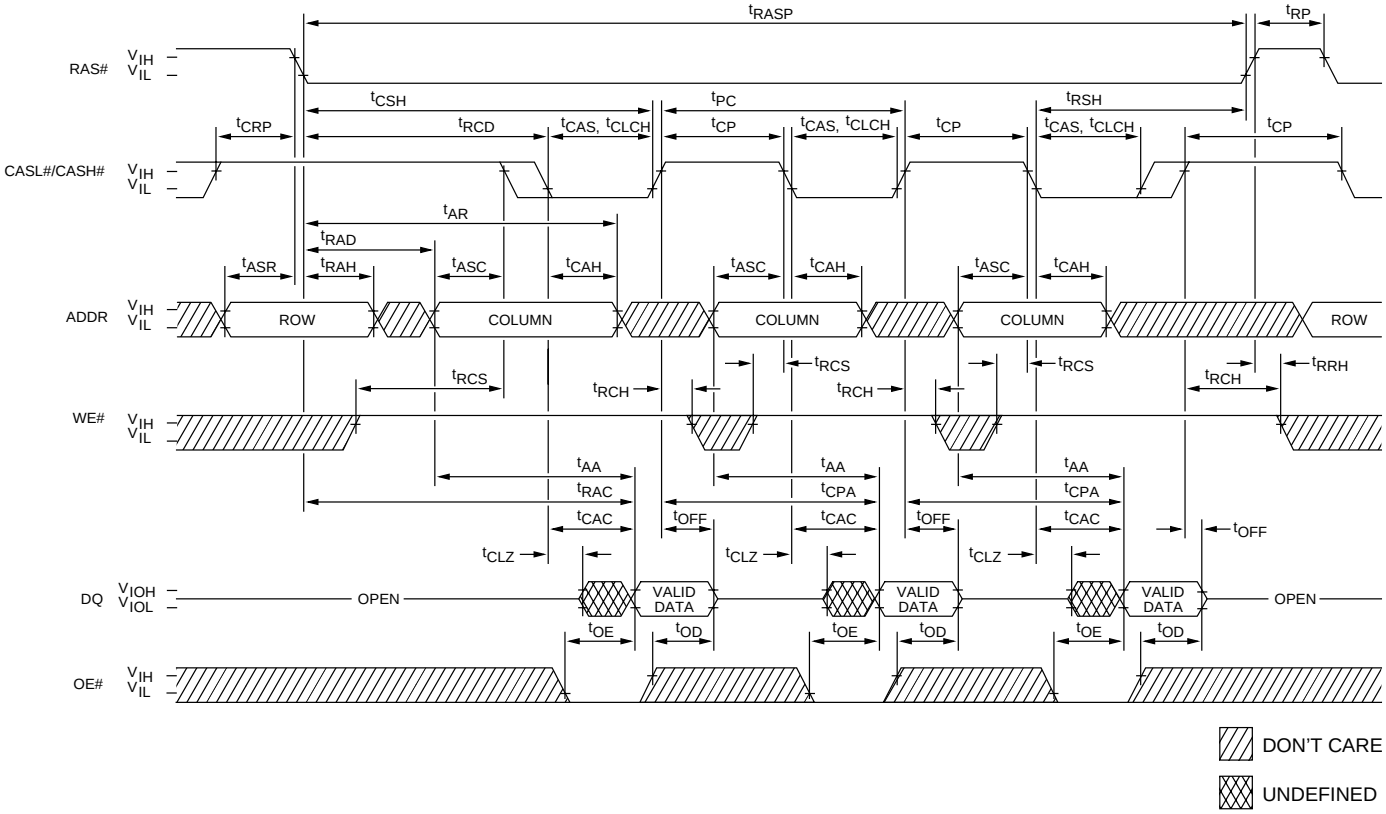


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	50		ns
tASC	0		ns
tASR	0		ns
tAWD	55		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLCH	10		ns
tCLZ	3		ns
tCRP	10		ns
tCSH	60		ns
tCWD	40		ns
tCWL	15		ns
tDH	10		ns
tDS	0		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOD	3	15	ns
tOE		15	ns
tOEH	15		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRAS	60	10,000	ns
tRCD	20		ns
tRCS	0		ns
tRP	40		ns
tRSH	15		ns
tRWC	150		ns
tRWD	85		ns
tRWL	15		ns
tWP	10		ns

FAST-PAGE-MODE READ CYCLE

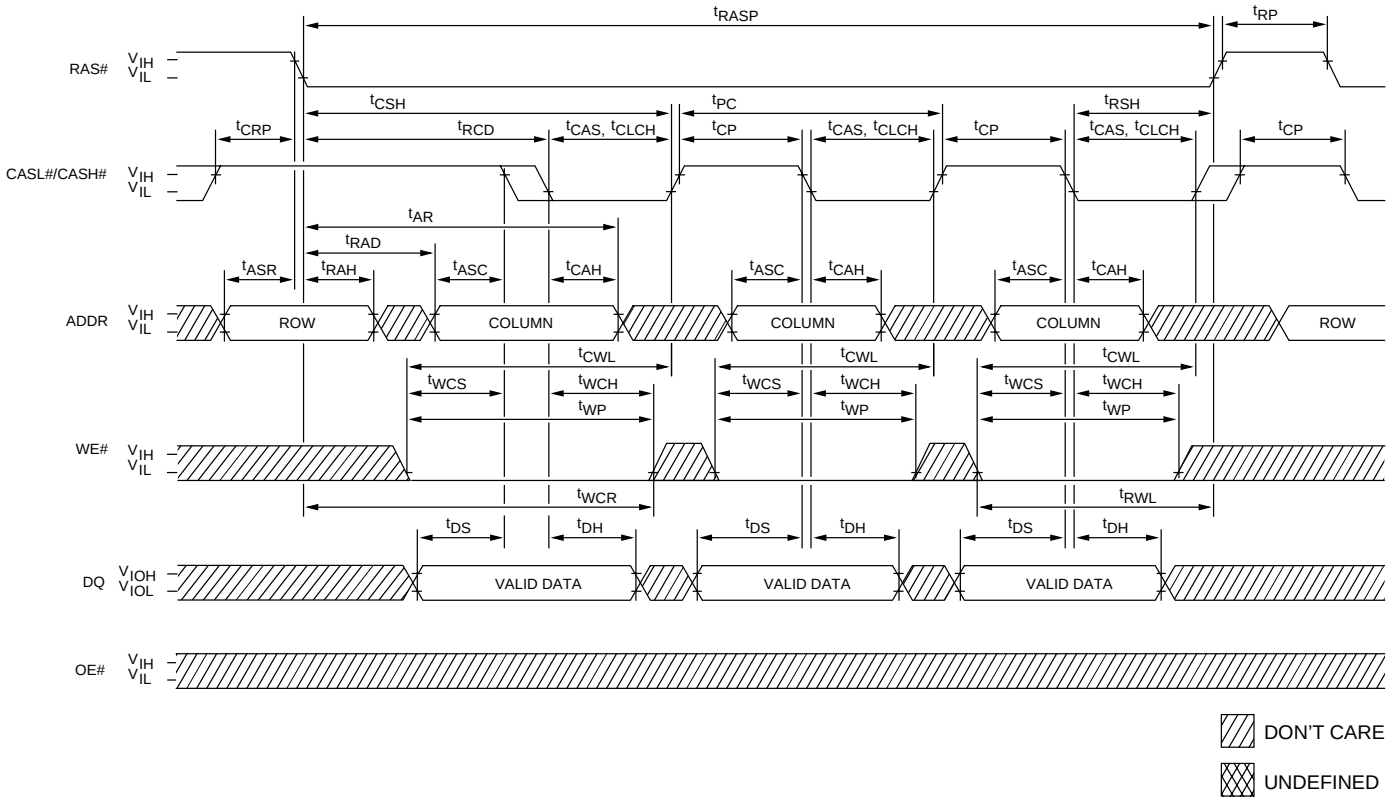


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	50		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLCH	10		ns
tCLZ	3		ns
tCP	10		ns
tCPA		35	ns
tCRP	10		ns
tCSH	60		ns
tOD	3	15	ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOE		15	ns
tOFF	3	15	ns
tPC	35		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	100,000	ns
tRCD	20		ns
tRCH	0		ns
tRCS	0		ns
tRP	40		ns
tRRH	0		ns
tRSH	15		ns

FAST-PAGE-MODE EARLY-WRITE CYCLE

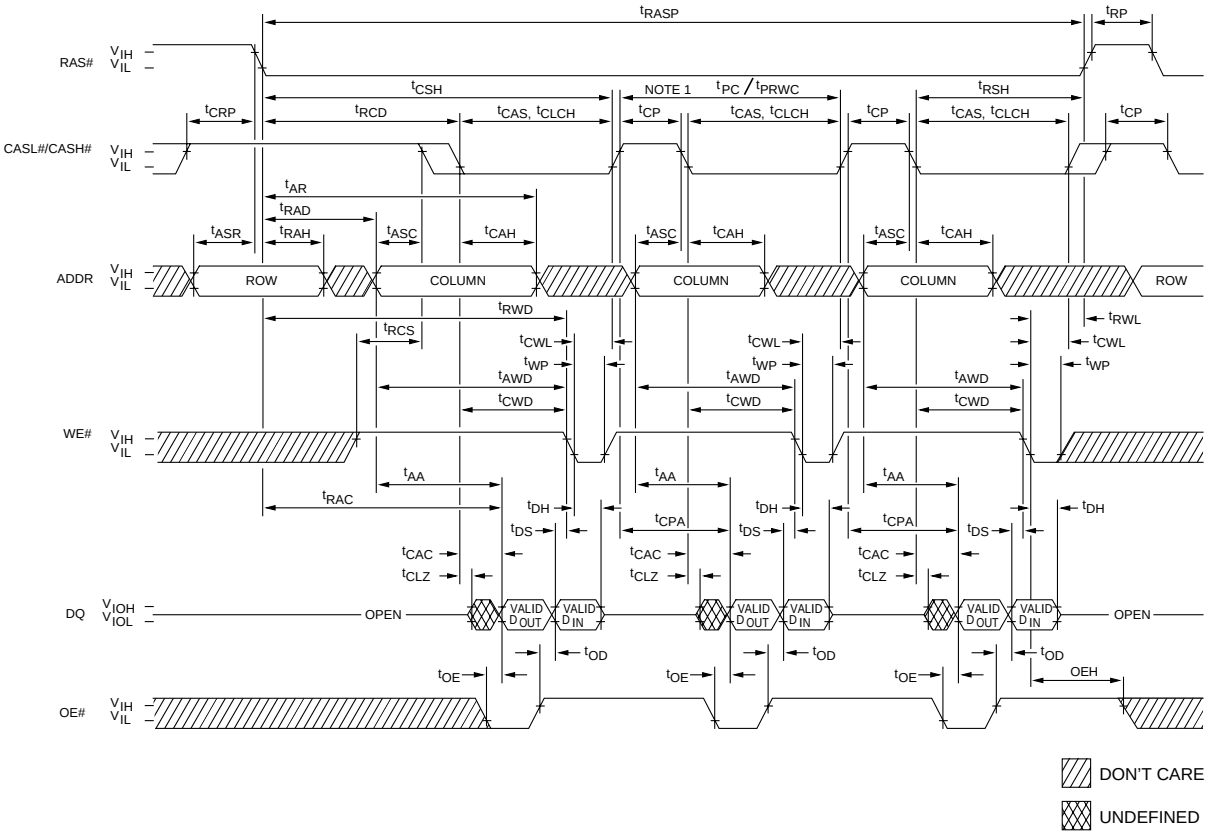


TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAR	50		ns
tASC	0		ns
tASR	0		ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLCH	10		ns
tCP	10		ns
tCRP	10		ns
tCSH	60		ns
tCWL	15		ns
tDH	10		ns
tDS	0		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tPC	35		ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	100,000	ns
tRCD	20		ns
tRP	40		ns
tRSH	15		ns
tRWL	15		ns
tWCH	10		ns
tWCR	45		ns
tWCS	0		ns
tWP	10		ns

FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



TIMING PARAMETERS

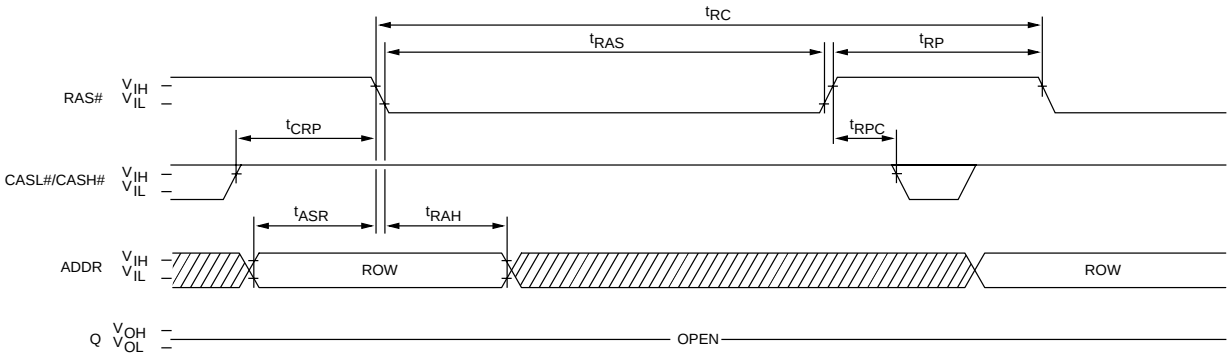
SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	50		ns
tASC	0		ns
tASR	0		ns
tAWD	55		ns
tCAC		15	ns
tCAH	10		ns
tCAS	15	10,000	ns
tCLCH	10		ns
tCLZ	3		ns
tCP	10		ns
tCPA		35	ns
tCRP	10		ns
tCSH	60		ns
tCWD	40		ns
tCWL	15		ns
tDH	10		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tDS	0		ns
tOD	3	15	ns
tOE		15	ns
tOEH	15		ns
tPC	35		ns
tPRWC	85		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRASP	60	100,000	ns
tRCD	20		ns
tRCS	0		ns
tRP	40		ns
tRSH	15		ns
tRWD	85		ns
tRWL	15		ns
tWP	10		ns

NOTE: tPC is for LATE WRITE only.

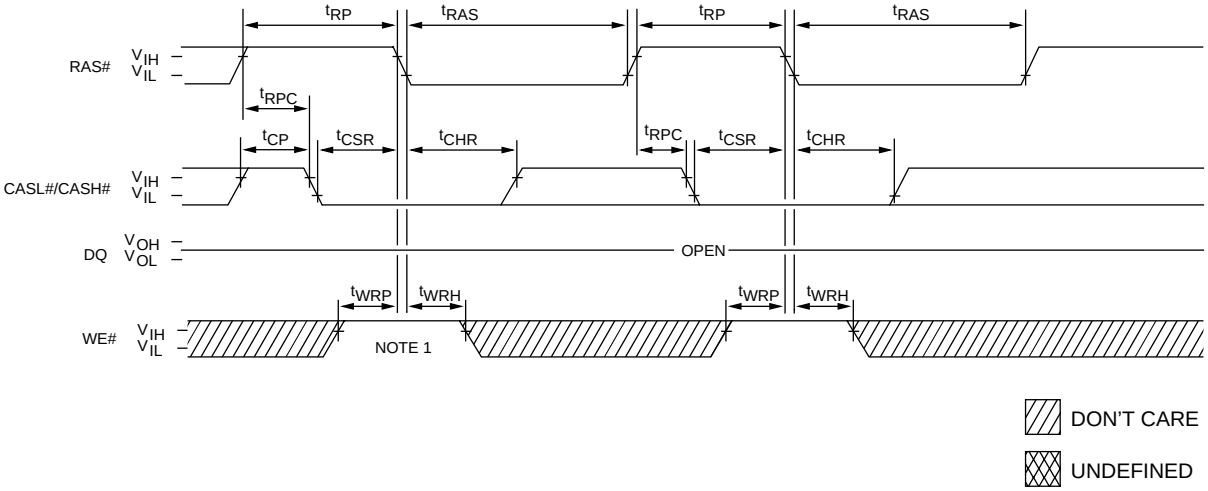
RAS#-ONLY REFRESH CYCLE

(Addresses; OE#, WE# = DON'T CARE)



CBR REFRESH CYCLE

(Addresses and OE# = DON'T CARE)



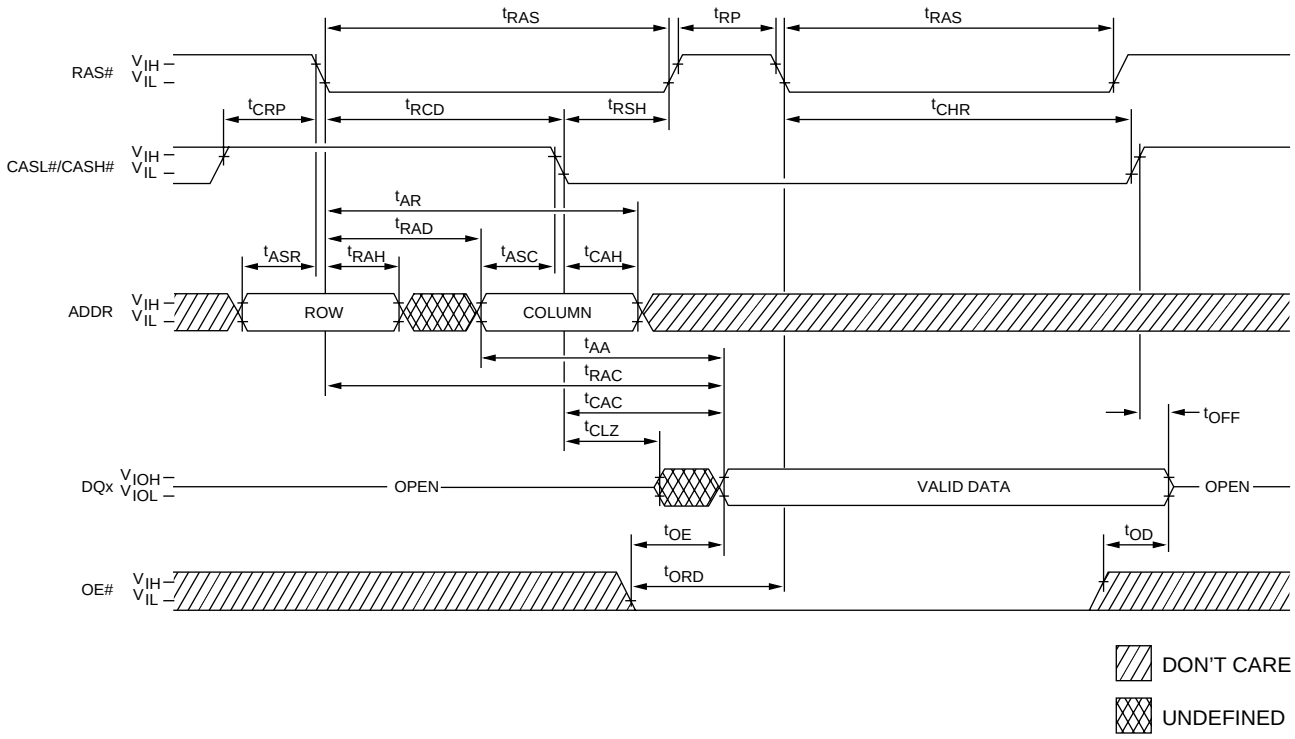
TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tASR	0		ns
tCHR	10		ns
tCP	10		ns
tCRP	10		ns
tCSR	10		ns
tRAH	10		ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tRAS	60	10,000	ns
tRC	110		ns
tRP	40		ns
tRPC	10		ns
tWRH	10		ns
tWRP	10		ns

NOTE: 1. tWRP and tWRH are for system design reference only. The WE# signal is actually a "don't care" at RAS# time during a CBR REFRESH. However, WE# should be held HIGH at RAS# time during a CBR REFRESH to ensure compatibility with other DRAMs which require WE# HIGH at RAS# time during a CBR REFRESH.

HIDDEN REFRESH CYCLE [21]
(WE# = HIGH; OE# = LOW)



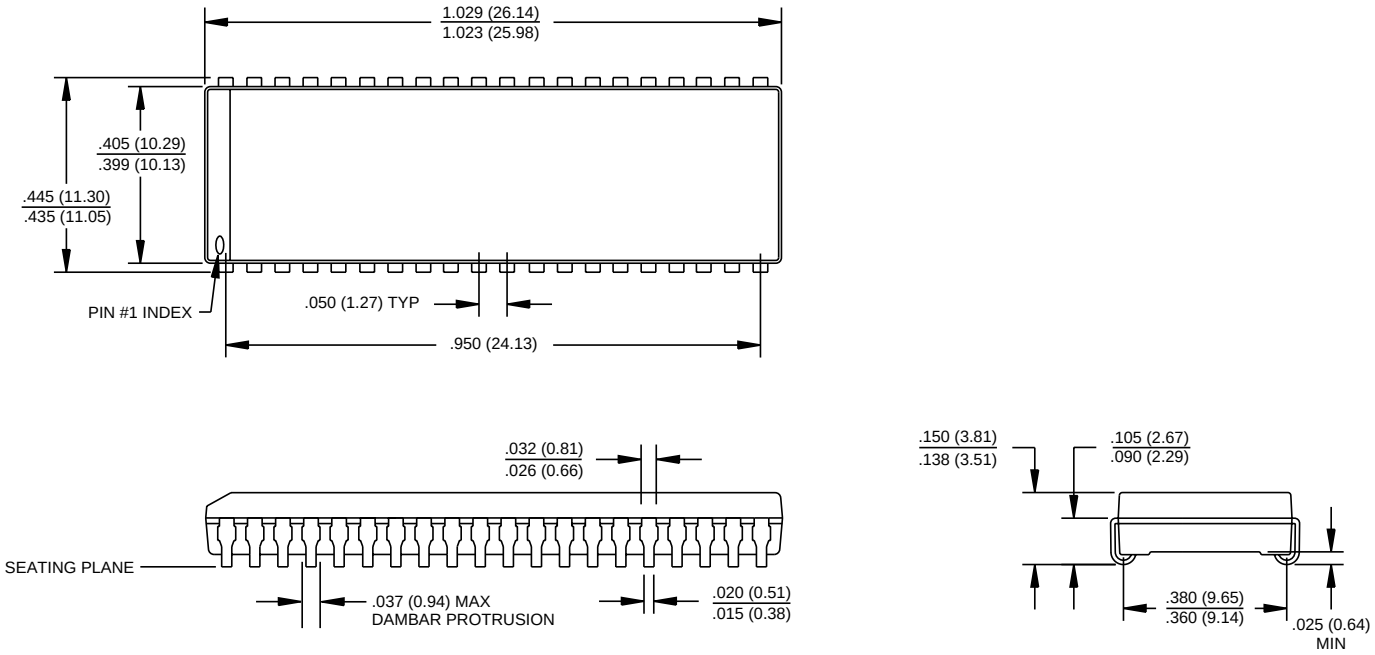
TIMING PARAMETERS

SYMBOL	-6 MIN	-6 MAX	UNITS
tAA		30	ns
tAR	50		ns
tASC	0		ns
tASR	0		ns
tCAC		15	ns
tCAH	10		ns
tCHR	10		ns
tCLZ	3		ns
tCRP	10		ns
tOD	3	15	ns

SYMBOL	-6 MIN	-6 MAX	UNITS
tOE		15	ns
tOFF	3	15	ns
tORD	0		ns
tRAC		60	ns
tRAD	15		ns
tRAH	10		ns
tRAS	60	10,000	ns
tRCD	20		ns
tRP	40		ns
tRSH	15		ns

40-PIN PLASTIC SOJ (400 mil)

DA-6



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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