4K x 4 CMOS Cache-Tag Static RAM — L7C180/181

FEATURES

- 4K x 4 CMOS Static RAM with 4-bit Tag Comparison Logic
- High Speed Address-to-MATCH — 10 ns maximum
- Totem Pole (L7C180) or Open Drain (L7C181) MATCH Output
- High Speed Flash Clear
- Auto-Powerdown™ Design
- Low Power Operation
  Active: 225 mW typical at 25 ns
  Standby: 100 µW typical
- Data Retention at 2 V for Battery Backup Operation
- Plug Compatible with IDT 6178, SSL4180, SSL4181, MK41H80, MCM4180
- Package Styles Available:
  22-pin Plastic DIP
  22-pin Sidebraze Hermetic DIP
  22-pin CerDIP
  24-pin SOJ

DESCRIPTION

The **L7C180** and **L7C181** are high performance, low power CMOS static RAMs optimized for use as the address tag comparator in high speed cache memory systems. The storage circuitry is organized as 4096 words by 4-bits per word and includes a 4-bit data comparator with MATCH output. The 4-bit data is input/output on shared I/O pins and comparison performed between 4-bit incoming data and accessed memory locations. Wide tag addresses are easily accommodated by paralleling devices and ANDing or Wire-ORing the MATCH outputs when working with L7C180's or L7C181's respectively. For either device, a low on the MATCH output indicates a data mismatch.

Also provided is a high speed $\overline{\text{CLEAR}}$ control which clears all memory locations to zero when activated. This allows all address tag bits to be cleared when powering on or flushing the cache.

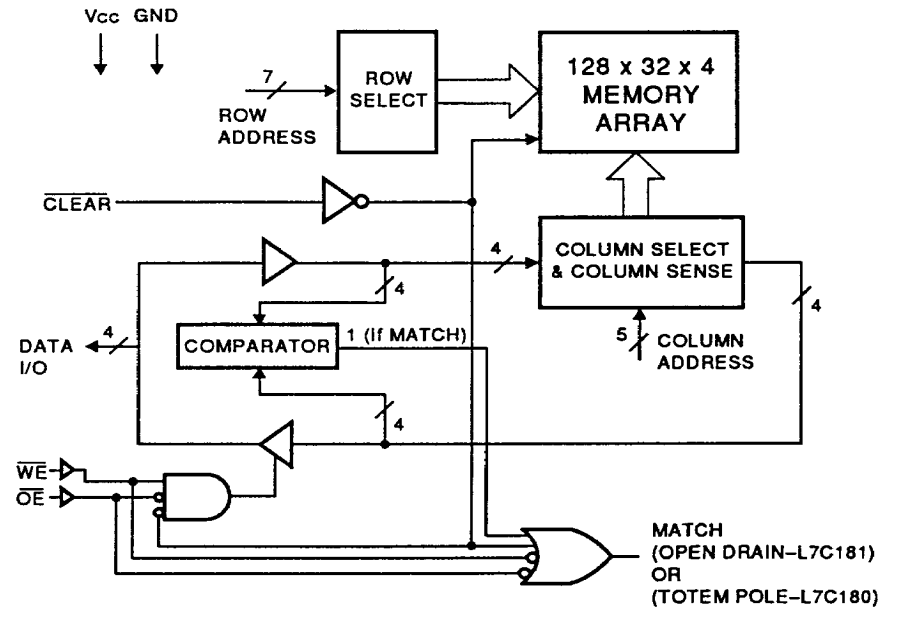
These devices are available in five speed grades with maximum address-to-MATCH times of 10 ns to 25 ns. Operation is from a single +5 V power supply with power consumption only 255 mW (typical) at 25 ns. Dissipation drops to 75 mW (typical) when the memory powers down.

Two power saving standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically whenever the inputs are stable for longer than the minimum access time. For minimal power consumption, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C180 and L7C181 consume only 15 µW (typical) at 3 V allowing effective battery backup operation.

The L7C180 and L7C181 provide fully asynchronous (unclocked) operation with matching access and cycle times. Memory locations are specified on address pins A0 through A11 with functions defined in the Truth Table on the next page. Data In has the same polarity as Data Out.

Latchup and static discharge protection are provided on-chip. The L7C180 and L7C181 can withstand an injection current of up to 200 mA an any pin without damage.

L7C180/181 Block Diagram



Truth Table

$\overline{WE}$	$\overline{OE}$	$\overline{CLR}$	MATCH	I/O	FUNCTION
X	X	L	H	High Z	Clear all bits to low
H	H	H	L	DIN	No MATCH
H	H	H	H	DIN	MATCH
H	L	H	H	DOUT	Memory Read
L	X	H	H	DIN	Memory Write

X = Don't Care; L = VIL; H = VIH

Maximum Ratings

Above which useful life may be impaired (Notes 1, 2)

Storage temperature ..... −65°C to +150°C
Operating ambient temperature ..... −55°C to +125°C
VCC supply voltage with respect to ground ..... −0.5 V to +7.0 V
Input signal with respect to ground ... −3.0 V to +7.0 V
Signal applied to high impedance output ..... −3.0 V to +7.0 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ VCC ≤ 5.5 V
Active Operation, Military	−55°C to +125°C	4.5 V ≤ VCC ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ VCC ≤ 5.5 V
Data Retention, Military	−55°C to +125°C	2.0 V ≤ VCC ≤ 5.5 V

Electrical Characteristics *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VOH	Output High Voltage	IOH = −4.0 mA, VCC = 4.5 V (all except MATCH pin)	2.4			V
	(Note 11)	IOH = −12.0 mA, VCC = 4.5 V (MATCH pin–L7C180)	2.4			V
VOL	Output Low Voltage	IOL = 8.0 mA (all except MATCH pin)			0.4	V
	(Note 11)	IOL = 10.0 mA (all except MATCH pin)			0.5	V
		IOL = 24.0 mA (MATCH pin)			0.4	V
		IOL = 30.0 mA (MATCH pin)			0.5	V
VIH	Input High Voltage		2.0		VCC + 0.3	V
VIL	Input Low Voltage	(Note 3)	−3.0		0.8	V
IIX	Input Current	GND ≤ VIN ≤ VCC	−10		+10	µA
IOZ	Output Leakage Current	GND ≤ VOUT ≤ VCC, $\overline{OE}$ = VCC (except MATCH pin)	−10		+10	µA
IOS	Output Short Current	VOUT = GND, VCC = Max (Note 4)			−350	mA
ICC2	VCC Current, TTL Inactive	(Notes 5, 7)		15	30	mA
ICC3	VCC Current, CMOS Standby	(Note 8)		20	100	µA
ICC4	VCC Current, Data Retention	VCC = 3.0 V (Note 9)		5	50	µA
CIN	Input Capacitance	Ambient Temp = 25°C, VCC = 5.0 V			5	pF
COUT	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7	pF

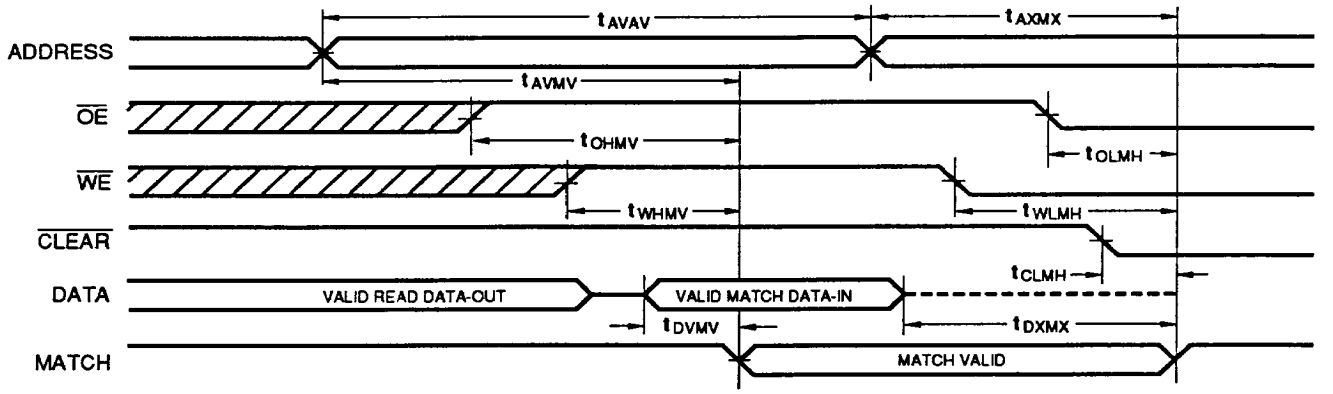
Symbol	Parameter	Test Condition	L7C180/181- 25	20	15	12	10		Unit
ICC1	VCC Current, Active	(Notes 5, 6)	60	75	100	120	130		mA

SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

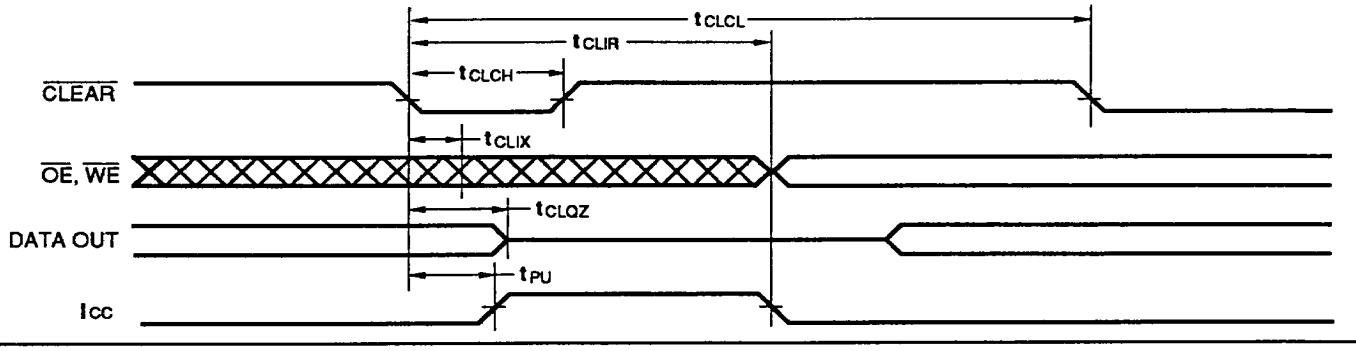
MATCH AND CLEAR CYCLE TIMING (Notes 11, 12, 20, 21, 22)

Symbol	Parameter	L7C180/181- 25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	Min	Max
tAVAV	MATCH Cycle Time	25		20		15		12		10			
tAVMV	Address Valid to MATCH Valid		22		20		15		12		10		
tAXMX	Address Change to MATCH Change	3		3		3		3		3			
tOHMV	Output Enable High to MATCH Valid		15		15		13		10		8		
tOLMH	Output Enable Low to MATCH High	3		3		3		3		3			
tWHMV	Write Enable High to MATCH Valid		15		15		13		10		8		
tWLMH	Write Enable Low to MATCH High	3		3		3		3		3			
tCLMH	$\overline{\text{CLEAR}}$ Low to MATCH High	0	20	0	15	0	12	0	10	0	8		
tDVMV	Data Valid to MATCH Valid		15		15		13		10		8		
tDXMX	Data Change to MATCH Change	0		0		0		0		0			
tCLCL	$\overline{\text{CLEAR}}$ Cycle Time (23)	55		45		35		30		25			
tCLCH	$\overline{\text{CLEAR}}$ Pulse Width (23)	15		15		12		12		10			
tCLIX	$\overline{\text{CLEAR}}$ Low to Inputs Don't Care (23)	0		0		0		0		0			
tCLQZ	$\overline{\text{CLEAR}}$ Low to Output High Z (18, 19)		15		15		10		10		8		
tCLIR	$\overline{\text{CLEAR}}$ Low to Inputs Recognized (23)		55		45		35		30		25		

MATCH TIMING (Note 17)



CLEAR TIMING (Note 23)

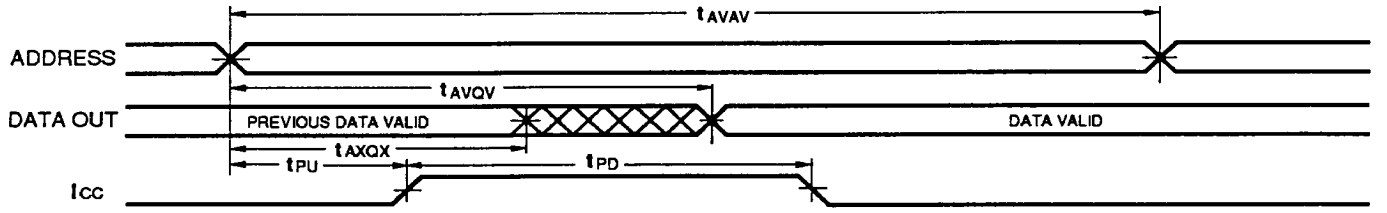


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

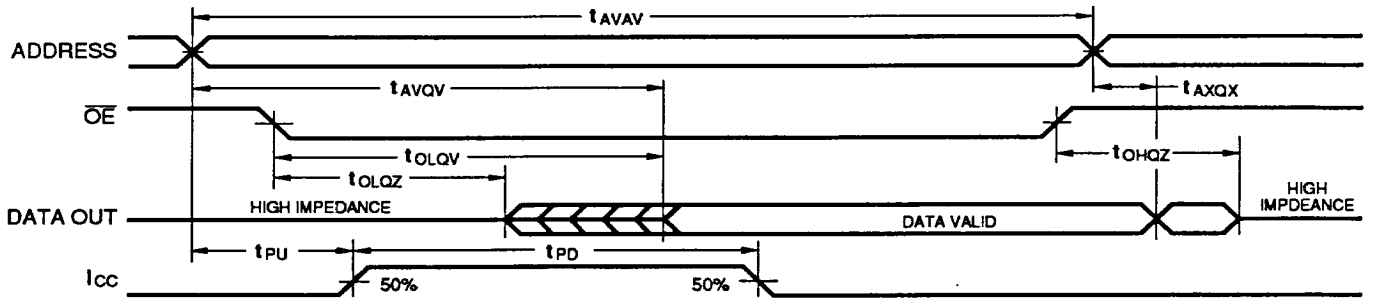
READ CYCLE *(Notes 11, 12, 20, 21, 22)*

Symbol	Parameter	L7C180/181- 25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	Min	Max
t_{AVAV}	Read Cycle Time	25		20		15		12		10			
t_{AVQV}	Address Valid to Output Valid (13, 14)		25		20		15		12		10		
t_{AXQX}	Address Change to Output Change	3		3		3		3		3			
t_{OLQV}	Output Enable Low to Output Valid		12		10		8		6		4		
t_{OLQZ}	Output Enable Low to Output Low Z (18, 19)	0		0		0		0		0			
t_{OHQZ}	Output Enable High to Output High Z (18, 19)		10		8		8		5		4		
t_{PU}	Input Change to Power Up (10, 17)	0		0		0		0		0			
t_{PD}	Power Up to Power Down (10, 17)		25		20		20		20		18		
t_{CHVL}	Control Input High to Data Retention (10)	0		0		0		0		0			

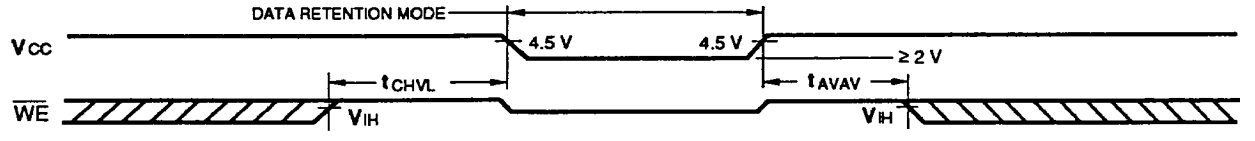
READ CYCLE — ADDRESS CONTROLLED *(Notes 13, 14)*



READ CYCLE — OE CONTROLLED *(Notes 13, 15)*



DATA RETENTION

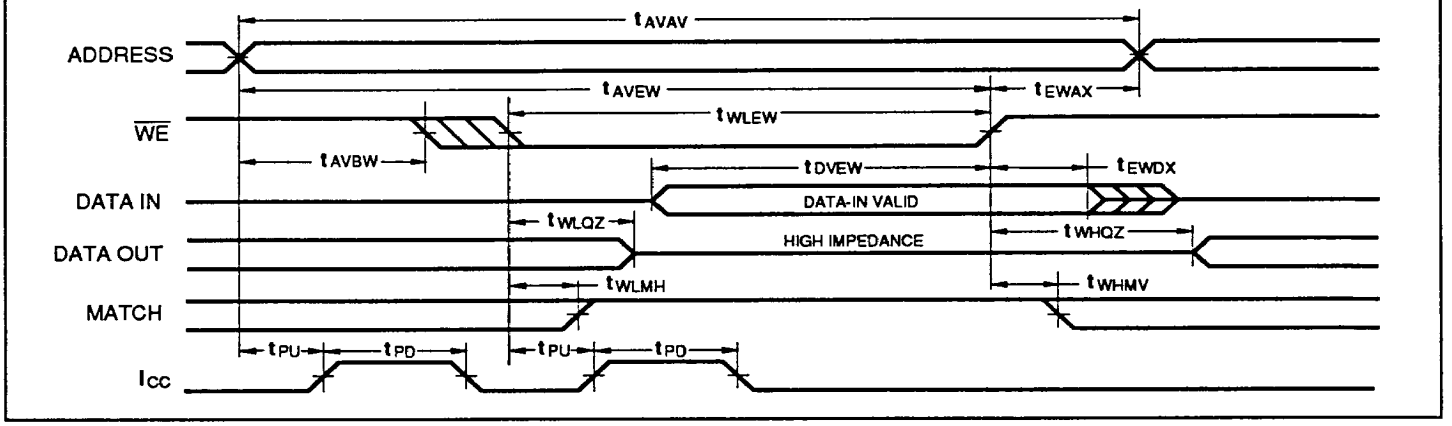


SWITCHING CHARACTERISTICS *Over Operating Range (ns)*

WRITE CYCLE (Notes 11, 12, 20, 21, 22)

Symbol	Parameter	L7C180/181- 25 Min	25 Max	20 Min	20 Max	15 Min	15 Max	12 Min	12 Max	10 Min	10 Max	Min	Max
tAVAV	Write Cycle Time	20		20		15		12		10			
tAVBW	Address Valid to Beginning of Write Cycle	0		0		0		0		0			
tAVEW	Address Valid to End of Write Cycle	15		15		12		10		8			
tEWAX	End of Write Cycle to Address Change	0		0		0		0		0			
tWLEW	Write Enable Low to End of Write Cycle	15		15		12		10		8			
tDVEW	Data Valid to End of Write Cycle	10		10		7		6		5			
tEWDX	End of Write Cycle to Data Change	0		0		0		0		0			
tWHQZ	Write Enable High to Output Low Z (18, 19)	0		0		0		0		0			
tWLQZ	Write Enable Low to Output High Z (18, 19)		7		7		5		4		4		

WRITE CYCLE — $\overline{WE}$ CONTROLLED (Notes 16, 17)



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Duration of the output short circuit should not exceed 30 seconds.

5. 'Typical' supply current values are not shown but may be approximated. At a VCC of +5.0 V, an ambient temperature of +25°C and with nominal manufacturing parameters, the operating supply currents will be approximately 3/4 or less of the maximum values shown.

6. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously enabled for reading, i.e., $\overline{OE} \le$ VIL, $\overline{WE}$ & $\overline{CLEAR} \ge$ VIH. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs ≥ VIH. The device is continuously disabled, i.e., $\overline{WE}$, $\overline{OE}$, & $\overline{CLEAR} \ge$ VIH.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{WE}$, $\overline{OE}$, and $\overline{CLEAR}$ = VCC. Input levels are within 0.2 V of VCC or GND.

9. Data retention operation requires that VCC never drop below 2.0 V. $\overline{WE}$, $\overline{OE}$, and $\overline{CLEAR}$ must be ≥ VCC – 0.2 V. For all other inputs VIN ≥ VCC – 0.2 or VIN ≤ 0.2 V is required to ensure full powerdown.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified IOL and IOH plus 30 pF (Figs. 1a, 1c, and 1d), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{WE}$ high and $\overline{OE}$ low).

15. All address lines are valid t_{AVQV} to t_{OLQV} prior to the $\overline{OE}$ transition to low.

16. The internal write cycle of the memory is defined by $\overline{WE}$ low. The address and data setup and hold times should be referenced to $\overline{WE}$ falling and rising edges.

17. Powerup from ICC2 to ICC1 occurs as a result of any of the following conditions:

a. Falling edge of $\overline{WE}$.
b. Transition on any address line.
c. Transition on any data line ($\overline{WE}$ active).
d. Falling edge of $\overline{CLEAR}$.

The device automatically powers down from ICC1 to ICC2 after t_{PD} has elapsed from any of the power up triggers. The exception is $\overline{CLEAR}$ where the device remains powered up for the duration of the Clear cycle. This means that power dissipation is dependent on only cycle rate, and not on Write Enable pulse width.

18. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

19. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This para-meter is sampled and not 100% tested.

20. All address timings are referenced from the last valid address line to the first transitioning address line.

21. $\overline{WE}$ must be high during address transitions.

22. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the VCC and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between VCC and ground. To avoid signal reflections, proper terminations must be used.

23. The Clear cycle is edge-triggered on the falling edge of $\overline{CLEAR}$. While the internal Clear cycle is in progress, all inputs, including multiple $\overline{CLEAR}$ pulses, are ignored. Inputs are recognized after t_{CLR} has elapsed from the falling edge of $\overline{CLEAR}$. For proper operation, Vcc must be within its specified normal operating voltage prior to assertion of $\overline{CLEAR}$.

FIGURE 1a.

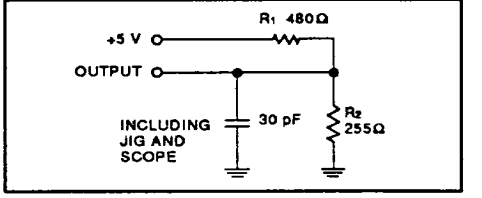


FIGURE 1b.

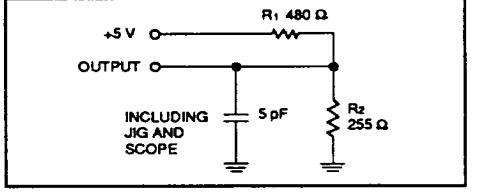


FIGURE 1c. MATCH OUTPUT TOTEM POLE

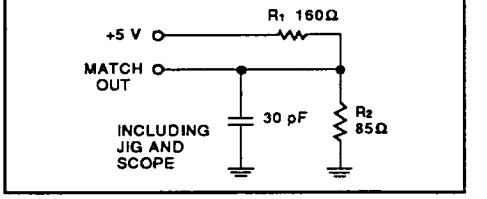


FIGURE 1d. MATCH OUTPUT OPEN DRAIN

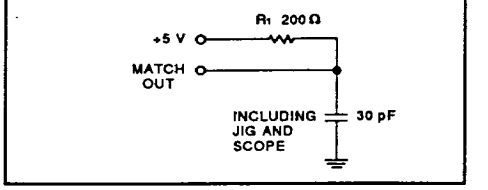
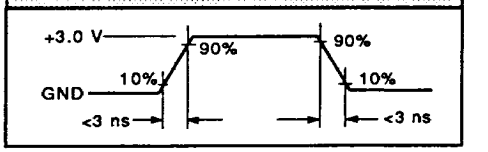
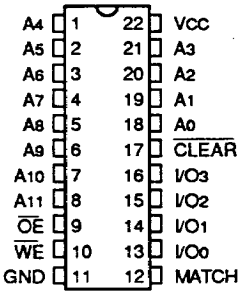


FIGURE 2.

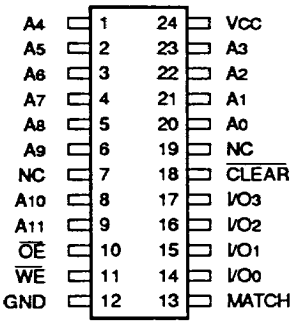


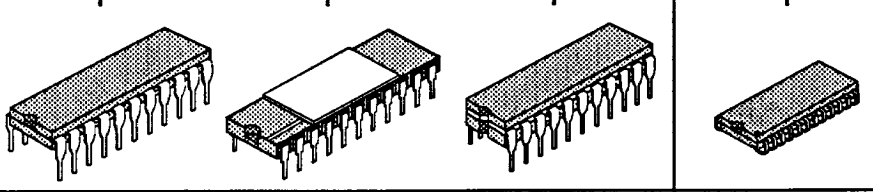
ORDERING INFORMATION

22-pin
(0.3" wide)



24-pin





Speed	Plastic DIP (P8)	Sidebraze Hermetic DIP (D8)	CerDIP (C3)	Plastic SOJ (.300"— W2)		
	0°C to +70°C — Commercial Screening					
25 ns 20 ns 15 ns 12 ns 10 ns 8 ns	L7C180PC or L7C181PC — 25, 20, 15, 12, 10	L7C180DC or L7C181DC — 25, 20, 15, 12, 10	L7C180CC or L7C181CC — 25, 20, 15, 12, 10	L7C180WC or L7C181WC — 25, 20, 15, 12, 10		
	–55°C to +125°C — Commercial Screening					
25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C180DM or L7C181DM — 25, 20, 15, 12	L7C180CM or L7C181CM — 25, 20, 15, 12			
	–55°C to +125°C — Extended Screening					
25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C180DME or L7C181DME — 25, 20, 15, 12	L7C180CME or L7C180CME — 25, 20, 15, 12			
	–55°C to +125°C — MIL-STD-883 Compliant					
25 ns 20 ns 15 ns 12 ns 10 ns 8 ns		L7C180DMB or L7C181DMB — 25, 20, 15, 12	L7C180CMB or L7C181CMB — 25, 20, 15, 12			