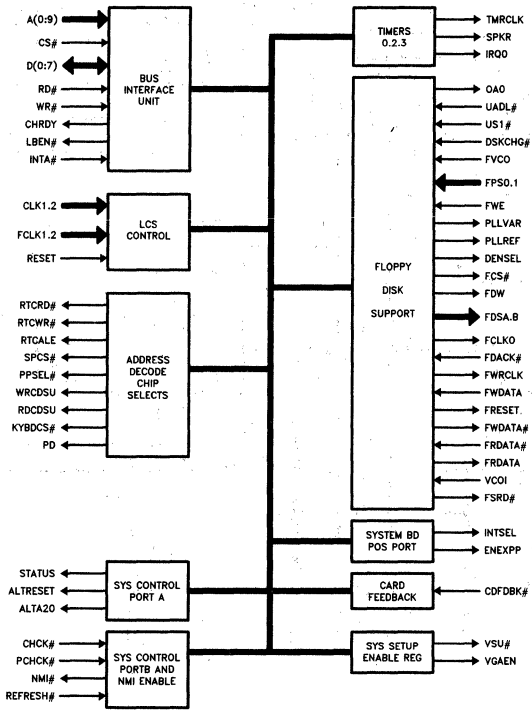
82306
LOCAL CHANNEL SUPPORT CHIP

- **Supports I/O Peripherals on the Local Channel**
- **Supports VGA Controller on the VGA Graphics Channel**
- **Floppy Disk Sub-System Support**
  - **— 8272A Interface for IBM Micro Channel Compatible 3½" Drives (Dual Speed Drives −250/500 Kbps)**
  - **— 82072 Interface for IBM Micro Channel Compatible 3½" Drives (250/500 Kbps) and AT Compatible 5¼" Drive (250/300/500 Kbps)**
- **Integrated Programmable Timer/ Counters (0, 2, 3)**
- **Integrates System Registers and Ports**
- **Low Power CHMOS Technology**
- **100-Pin Plastic Quad Flat Pack Packaging**
  (See Packaging Guide Order # 231369)

The 82306 Local Channel Support chip is the register level implementation of the equivalent VLSI device in the IBM Micro Channel systems. It provides FDC interface to support IBM compatible 3½" disk drives when used with 8272A FDA and 3½" & 5¼" (AT Compatible) disk drives when used with the 82072 FDC.

The 82306 also has integrated I/O ports and registers for miscellaneous system board functions, Integrated Address decoder for generaing chip selects for the I/O devices on the Local Channel and 8254 like programmable timers (0, 2, 3) to support speaker tone generation, watch-dog timer and periodic interrupts.



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Order Number: 290183-001

FLOPPY DISK CONTROLLER INTERFACE

The Floppy Disk Controller (FDC) function of the 82306 Local Channel Support chip has two FDC interfaces: 8272A FDC interface as used in IBM Micro Channel systems Model 50/60 and 80, and 82072 FDC interface for value-added performance and compatibility.

The 82306 Local Channel Support chip integrates glue logic required to support the 8272A and the 82072 Floppy Disk Controllers. The FDC interface includes the pre-compensation logic, digital portion of the read data separator logic, and status registers (03F1H, 03F2H, 03F7 ports). The integrated prescaler supports 250 Kbits/sec and 500 Kbits/sec as required in the IBM Micro Channel compatible system. With the 82072 FDC, however, an additional 300 Kbits/sec data stream is supported for interfacing to a standard AT 5¼" drive.

The Floppy Disk subsystem support includes generation of the chip select for the FDC when ports 03F4H or 03F5H are referenced. The Floppy status register (Read only) is implemented externally on the motherboard. To read this register, the 82306 generates the decoded read signal for address 03F0H.

The clock for 8272A is generated by the 82306 Local Channel Support chip, from an external 16 MHz frequency source. The 82072 utilizes its own fixed clock source of 24 MHz.

LOCAL CHANNEL ADDRESS DECODER

The 82306 Local Channel Support provides the Address decoding for the following devices and addresses.

- 8742 Keyboard Interface Chip
- Serial Port
- Parallel Port
- Ports 096H and 097H
- Real-Time Clock (Read, Write and Address Latch Enable)

SYSTEM TIMERS 0, 2, 3

The timers used for periodic interrupt (timer 0), tone generation for audio (timer 2) and watch-dog function (timer 3) are integrated on the 82306 Local Channel Support chip. Timer 0 and 2 are identical in their functionality as the timers in IBM PC/AT, XT and PC systems. The watch-dog timer 3 provides error detection capability and via BIOS, the watch-dog function can be enabled and disabled.

These timers can be programmed via ports 40, 42, 43, 44 and 47.

INTEGRATED SYSTEM REGISTER AND PORTS

The 82306 Local Channel Support chip has the following registers and ports integrated on the chip:

- System Control Port A & B (092H and 061H)
- Card Selected Feedback Register (091H)
- System Board POS Port (102H)
- Port 070H (Write Only)
- System Board Set Up (094H)

The POS register space as defined in the Micro Channel architecture is 100H to 107H. The 82306 integrates 102H on chip and generates PD signal during set-up mode for external implementation of POS ports 100, 101 and 103–107H. POS port 102H is programmed during set-up to enable serial, parallel port and the Floppy Disk Controller.

VGA ENABLE PORT 3C3H

When bit 0 of port 3C3H is programmed as 1, the VGA sub-system is enabled. The chip enable VGAEN is deactivated when a zero is written to the bit. On power up or reset, the VGA sub-system is enabled.

I/O DEVICE MAP

The following table lists the ports and registers integrated on the 82306 Local Channel Support chip.

I/O Register Address	Function
03F1H	Floppy Status Register B
03F2H	Floppy Digital Output Register
03F7H	Digital Input/Config. Register
061H	System Control Port B
092H	System Control Port A
091H	Card Selected Feedback Register
102H	System Board POS Port
070H	NMI Enable (Write Only)
094H	System Board Set-Up
3C3H	VGA Enable Port
40H, 42H, 43H, 44H, 47H	System Timer Ports

For programming and register level details, please refer to IBM technical reference manual.

82306 Local Channel Support Chip Pin Definitions

Signal Name	Pin Number	I/O	Description
A<0:9>	98–89	I	Address inputs.
D<0:7>	86–79	B	Bi-directional data bus.
CS#	78	I	Device chip select.
RD#, WR#	70, 69	I	I/O read and write command inputs.
REFRESH#	67	I	Refresh request generated by the DMA Controller.
RESET	5	I	System power-up reset.
CHRDY	6	O	Channel Ready signal. Driven low (not ready) by the Local Channel Support to extend accesses to its internal ports and to other local I/O bus devices that require a longer cycle time.
CDFDBK#	7	I	Latched card feedback signal.
TMRCLK	9	I	1.193 MHz clock input generated by the Address Bus Controller. It drives the clock inputs of system timers 0 and 2.
SPKR	10	O	Output of system timer 2 gated by bit 1 of Port 61H. It drives the Micro Channel audio sum node.
CLK1, CLK2	72, 3	I	Clock inputs.
FCLK1, FCLK2	71, 4	I	16 MHz (tied high for 82072 interface), clock inputs for 8272A interface.
VSU#	23	O	VGA Setup. It puts the VGA into set-up mode when low.
VGAEN	8	O	VGA chip enable. (Active High) A low level disables the VGA subsystem.
ENEXPP	22	O	Parallel port "extended mode" enable. When high, the parallel port can function bi-directionally. When low, the port is in "compatible mode" i.e., write only.
SPCS#	31	O	Serial port chip select. Can be mapped to COMM1 or COMM2.
INTSEL	32	O	Selects either IRQ3# (COMM2) or IRQ4# (COMM1) to serve as the interrupt request for the serial port.
STATUS	33	O	Floppy Disk Active Status
RTCWR# RTCRD# RTCALE	34 36 35	O	Write, Read and Address latch enable signal to the real time clock chip.
FSRD#	37	O	Read command for the Read-only floppy status port 3F0H.
WRCDSU	40	O	Write CD Setup Register. Active high write command generated on writes to port 96H (adapter enable setup register).
RDCDSU#	49	O	Read CD setup register. Active low signal reads port 96H.
LBEN#	42	O	Local Bus Engage. It is "OR"ed with the LBEN# output of the DMA/CACP to become one of the qualifiers that enable the data buffer between Micro Channel Bus and motherboard I/O bus. The LCS enable this buffer for accesses to the local I/O bus.
KYBDCS#	43	O	8742 keyboard controller chip select.
ALTRESET	44	O	Processor reset under software control. Except for a shorter reset pulse width, it is identical in function to the reset generated under software control by the 8742. (Optimized for switching between Real-mode and Protected-mode tasks.)

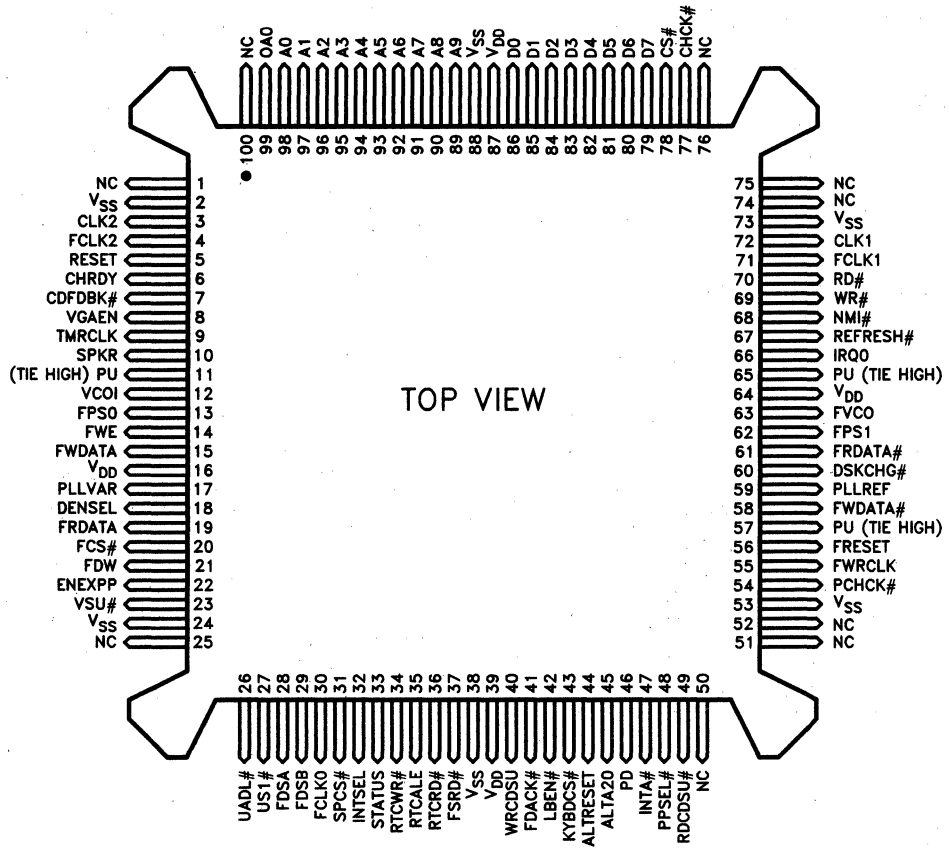
82306 Local Channel Support Chip Pin Definitions (Continued)

Signal Name	Pin Number	I/O	Description
ALTA20	45	O	Alternate A20 bit-Controls address bit A20 in a manner similar to the way it is controlled by the 8742. (Optimized for switching between Real-mode and Protected-mode tasks).
PD	46	O	POS Decode output. When the system board is in setup mode, this output acts as an (active high) chip select for system board POS ports 100H, 101H, and 103H through 107H. (POS port 102H is integrated on the Local Channel Support.)
INTA#	47	I	Interrupt acknowledge generated by the Bus controller.
PPSEL#	48	O	Parallel port chip select. Can be programmed to map the parallel port to LPT1, LPT2, or LPT3.
PCHCK#	54	I	DRAM Parity Error. It is driven by the Bus Controller upon detection of a motherboard DRAM parity error.
IRQ0	66	O	System Timer 0 timeout Interrupt Request.
NMI#	68	O	NMI request to the CPU. This is an open drain output that allows for an external wire "OR" with other NMI sources.
CHCK#	77	I	Micro Channel channel check indicator, for reporting adapter errors.
FPS0, FPS1	13, 62	I	Low and high order pre-compensation select bits. They are driven by the 8272A floppy disk controller. (Note that the pre-compensation logic is integrated on the Local Channel Support). Tied to GND when using 82072.
FWE	14	I	Write Enable for floppy. Generated by the FDC to enable the write data stream to disk.
FWDATA	15	I	FDC output write data stream. It goes through the LCS integrated pre-compensation logic, and then is fed to the drive over the LCS WRDATA# output. In 82072, the FWDATA is inverted and fed into the drive controller.
FWDATA#	58	O	Pre-compensated write data stream to disk for 8272. For 82072 it is simply an inverted output of FWDATA
FRDATA#	61	I	Read data stream from disk.
FRDATA	19	O	Buffered read data output to the FDC. No connect for 82072.
FDSA, FDSB	28, 29	O	Drive select/motor enable outputs.
DENSEL	18	O	Density Select.
FCS#	20	O	Device select for the FDC.
FDACK#	41	I	DMA acknowledge to the FDC from the DMA/CACP.
FCLKO	30	O	8272A clock. It is 8 MHz for high density, or 4 MHz for low density. Not required for 82072.
FWRCLK	55	O	8272A write clock input. It oscillates at twice the data rate; i.e., 1 MHz for a rate of 500 Kbits/sec and 500 KHz for a rate of 250 Kbits/sec. No connect for 82072.
FRESET	56	O	FDC Reset.
DSKCHG#	60	I	Disk changed signal.
VCOI	12	I	Buffered output of the 4024 voltage controlled oscillator. Grounded for 82072.

82306 Local Channel Support Chip Pin Definitions (Continued)

Signal Name	Pin Number	I/O	Description
PLLVAR	17	O	Divided down version of VCOI. It is fed back and used for phase comparison against the PLLREF output. No connect for 82072.
PLLREF	59	O	Phase Lock Loop Reference Clock. No connect for 82072.
FVCO	63	I	Valid Read Data Stream Indicator. It is driven by the 8272A, and defines a valid read data stream. Grounded for 82072.
FDW	21	O	Data window input of 8272A. It defines the valid sample points in the read data stream. No connect for 82072.
OA0	99	O	Output A0 signal for use by the 82072 disk controller. No connect for 8272A.
UADL#	26	I	Micro Channel Address decode latch. An Active low signal used to latch US1# on the trailing edge for support of the OA0 signal. Grounded for 8272A.
US1#	27	I	Micro Channel status bit 1. Used to distinguish a write operation from a read operation for support of the OA0 signal. Grounded for 8272A.
PU	11, 57, 65	I	Pull Up
V_{DD}	16, 39, 64, 87		Power
V_{SS}	2, 24, 38, 53, 73, 88		Ground
NC	1, 25, 50, 51, 52, 74, 75, 76, 100		No Connect

82306 Local Channel Support Chip



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NOTES:
PU = Pull-Up
NC = No Connect
—Pull-Up Resistor Value = 2K to 10K
—No more than three nodes to a single pull-up resistor.

82306 PARAMETRICS

ABSOLUTE MAXIMUM RATINGS*

Case Temperature under Bias .... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage to Any Pin with Respect to Ground ..... −0.3V to (V_{CC}+0.3)V
DC Supply Voltage (V_{CC}) ..... −0.3V to +7.0V
DC Input Current ..... ±10 mA

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTICE: Specifications contained within the following tables are subject to change.

D.C. CHARACTERISTICS

T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Conditions
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	CLK1, CLK2
V_{IH}	Input High Voltage	V_{CC} − 0.8		V	CLK1, CLK2
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 2 mA
I_{CC}	Power Supply Current		180	mA	No DC Loads
I_{LI}	Input Leakage Current		±10	μA	$V_{SS} < V_{IN} < V_{CC}$
I_{OZ}	Tri-State Output Leakage Current		±10	μA	$V_{SS} < V_{OUT} < V_{CC}$

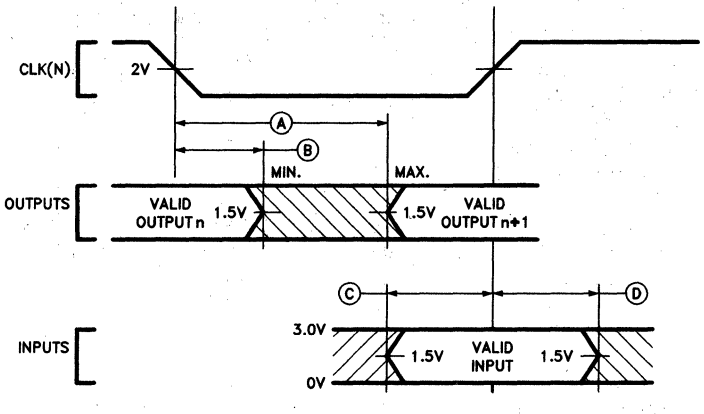
82306 LCS A.C. SPECS

T_C = 0°C to +70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Kit 16 MHz		Kit 20 MHz		Kit 25 MHz		C_L	Notes
		Min	Max	Min	Max	Min	Max	(pF)	
T1	CLK1, CLK2 LOW TIME	15		15		14			
T2	CLK1, CLK2 NON-OVERLAP	4		4		0			
T3	FCLK1, FCLK2 LOW TIME	10		10		10			
T4	FCLK1, FCLK2 NON-OVERLAP	10		10		10			
T5	RESET PULSE WIDTH	500		500		500			
T6	ALTRESET PULSE WIDTH	75	150	75	150	75	150	75	
T7	TMRCLK HIGH/LOW TIME	300		300		300			
T8	A9–A0, CS#, FDACK# SETUP	30		30		30			
T9	A9–A0, CS#, FDACK# HOLD	10		10		10			
T10	RD#, WR#, INTA# PULSE WIDTH	170		170		170			
T11	WRITE DATA SETUP	25		25		25			
T12	WRITE DATA HOLD	0		0		0			
T13	READ DATA VALID DELAY	0	50	0	50	0	50	75	
T14	READ DATA FLOAT DELAY	0	35	0	35	0	35	75	
T15	CHRDY DELAY	0	80	0	80	0	80	75	5
T16	CHRDY INACTIVE PULSE WIDTH	230		230		180		75	5, 10
T17	ADDRESS DECODE DELAYS	0	50	0	50	0	50	75	1
T18	WRITE STROBE DELAYS	0	40	0	33	0	30	75	2
T19	READ STROBE DELAYS	0	40	0	40	0	40	75	3
T20	RTCALE MIN PULSE WIDTH	120		120		110		75	10
T21	DATA SETUP TO INTA#	25		25		25			
T22	DATA HOLD FROM INTA#	5		5		5			
T23A	FCLKO HIGH TIME	45	63	45	63	45	63	75	6
T23B	FCLKO HIGH TIME	90	150	90	150	90	150	75	6
T23C	FCLKO VALID DELAY		35		35		35	75	
T24A	FWRCLK HIGH TIME	200	300	200	300	200	300	75	
T24B	FWRCLK VALID DELAY		35		35		35	75	
T25	FWDATA# PULSE WIDTH	350		350		350		75	
T26	FRDATA# PULSE WIDTH	40		40		40		75	
T27	FRDTA PULSE WIDTH	125		125		125		75	
T28A	FDW SAMPLE PERIOD	1 µs		1 µs		1 µs		75	4, 7
T28B	FDW SAMPLE PERIOD	2 µs		2 µs		2 µs		75	4, 7
T29	VCOI FREQUENCY	4 MHz		4 MHz		4 MHz			4
T30A	PLLVAR,PLLREF FREQUENCY	1 MHz		1 MHz		1 MHz		75	4, 7, 8
T30B	PLLVAR,PLLREF FREQUENCY	500 KHz		500 KHz		500 KHz		75	4, 7, 8
T31	US1# SETUP TO UADL#	25		25		25			9

NOTES:
1. Address decode delays include SPCS#, LBEN#, KYBDCS#, FCS#, PD, PPSEL#, and OA0. (OA0 supports 82072 interface.)
2. Write Strobe delays include RTCWR# and WRCDSU.
3. Read Strobe delays include RTCRD#, FSRD#, and RDCDSU#.
4. Typical values . . . not tested.
5. LCS extends cycles to the 8242 keyboard controller, serial port, real time clock, and 8272 Floppy Disk Controller.
6. T23A applies to FCLKO = 8 MHz (500 KBPS Data Rate).
   T23B applies to FCLKO = 4 MHz (250 KBPS Data Rate).
7. T28A and T30A apply to 500 KBPS. The T28B and T30B apply to 250 KBPS.
8. VCOI/4 for 500 KBPS. VCOI/8 for 250 KBPS. PLLREF applies only when PLL is locked.
9. 82072 Support.
10. Functional Spec . . . not tested.

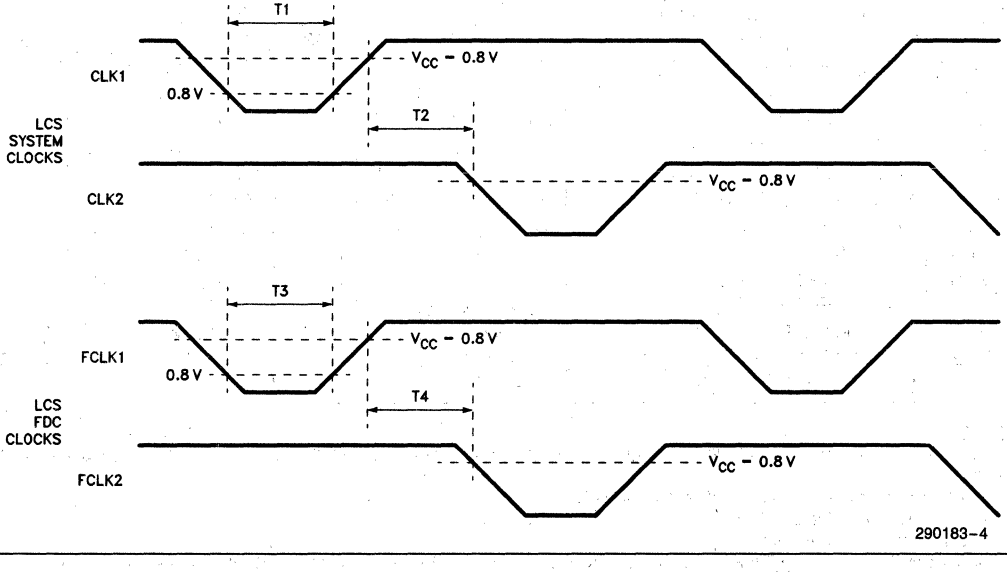
DRIVE LEVELS AND MEASUREMENT POINTS FOR A.C. SPECIFICATIONS



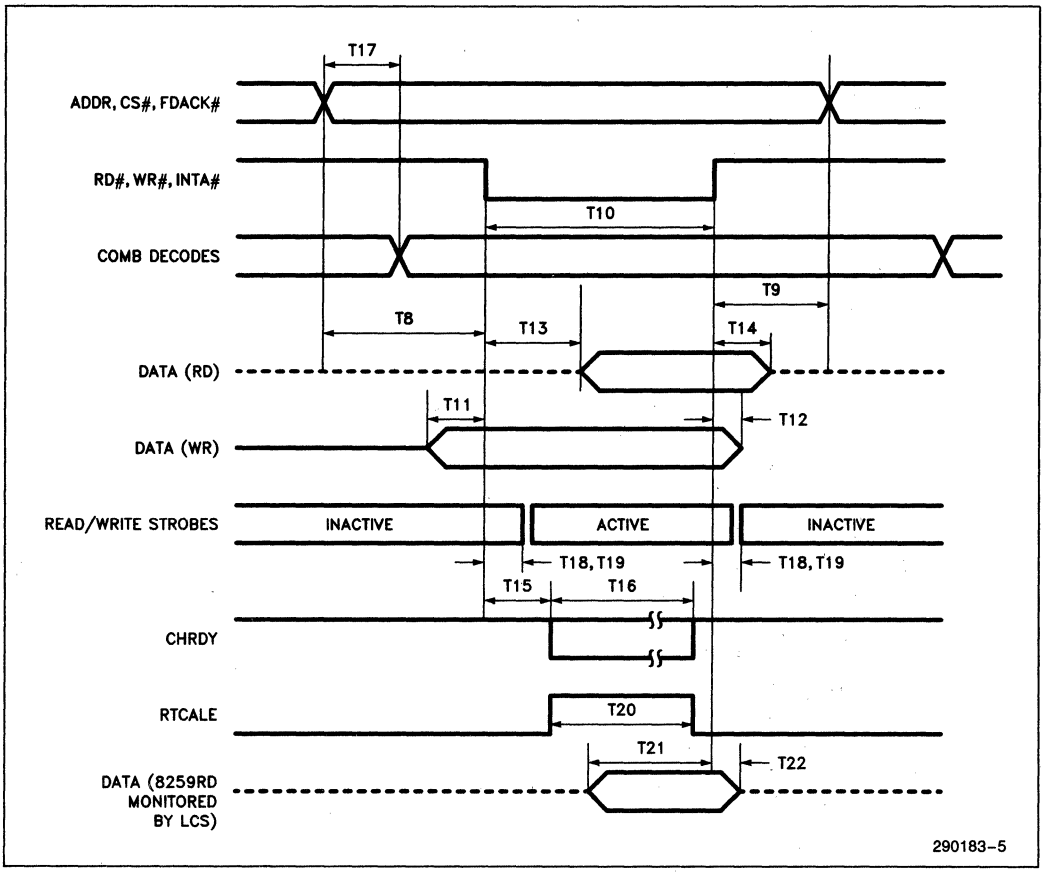
LEGEND:
A. Maximum Output Delay Specification.
B. Minimum Output Delay Specification.
C. Minimum Input Setup Specification.
D. Minimum Input Hold Specification.

Input waveforms have tr ≤ 2.0 ns from 0.8V to 2.0V.

LCS CLOCKS



SYSTEM INTERFACE



MISCELLANEOUS TIMINGS