IMISC4XX SYSTEM CLOCK CHIPS

January 1993

CMOS LSI
PLL FREQUENCY SYNTHESIZER

FEATURES

- Multiple PLL Clock Generators Provide All Essential Clock Signals for Computer CPU Boards.
- Supports 80286, 80386, and 80486 Based Designs.
- Up to 3 Buffered 0.5 NS Maximum Skew CPU Clock Outputs Available.
- 4V to 7V Operating Supply Range.
- Implements 486 Turbo Via Slow Frequency Shift.
- Integrates Clocks for CPU, Keyboard, Serial Port, FDC, Timer, ISA Bus, and Buffered Reference.
- Wide Range of Selectable CPU Frequencies Including 88, 80, 66.6, 50, 44, 40, 33.3, 32, 25, Etc.
- 1 NS Maximum Skew Between MCLK and MCLK/2 CPU Clock Outputs.
- Single Low Cost (14.318 Mhz) Crystal Used As Reference Frequency.
- Glitch-free Switching Between PLL Clock Generators.
- 50% Duty Cycle.
- Power Down and Reduced Power Modes.
- TTL and CMOS Compatible Outputs.
- Low Short and Long-Term Jitter.
- Available in Dip and SSOP (209 Mil Body) Packages.

IMCIS036

DESCRIPTION

The IMISC4XX Product Family is designed to economically replace crystal oscillators on CPU boards. These highly integrated products provide the clocking signals for the 80XX microprocessor, the chip set, and the peripheral chips commonly found on an IBM PC compatible main board. These signals are generated from several onboard independent VCO's, which are frequency calibrated from an inexpensive external 14.318 Mhz crystal. Select inputs determine which of several ROM-based frequencies appear on the CPU clock outputs. A slow walk frequency switching mode has been built into the SC4XX Family to make it easy to implement turbo on the 486.

Power reduction is supported by options for tristating outputs, turning off VCO's, and reducing VCO frequency. In standby mode, all outputs except reference clock are off and all phase detectors are tristated reducing power drain. Automatic frequency reduction controls are available on products targeted at laptop applications.

The IMISC4XX Family consists of a broad selection of products to meet the needs of each application. Double frequency CPU clocks and up to three CPU clock output drivers along with turbo control pins are available as options to meet the needs of some designs. The selection guide that follows can be used to select just the right product for your application.

INTERNATIONAL MICROCIRCUITS INC. 525 LOS COCHES ST.
MILPITAS, CA 95035 TEL :408-263-6300 FAX : 408-263-6571

PRODUCT SELECTION GUIDE

IMI PART #	PACKAGE INFORMATION			CPU CLOCK OUTPUTS (MHz)		ADDITIONAL CLOCK OUTPUTS (MHz)									BUFFER		TS
	# of Pins	Available Package Types	SSOP or SOIC Body (mils)	MCLK2	MCLK1 (MCLK2/2)	CPCK2	CPCK2/2	ISA 32	FDC 24	ISA 16	REF 14.318	KBRD 12	KBRD 7.159	AT 8	IN	OUT	
SC401	20	PDIP SSOP	209	24, 32, 40, 50, 66.6, 80, 88	√			√		√	√		√				√
SC402 (Turbo)	20	PDIP SSOP	209	8, 12, 16, 20, 25, 33.3, 40, 44 OR 24, 32, 40, 50, 66.6, 80, 88						√	√				*		
SC403	20	PDIP SSOP	209	12, 16, 20, 25, 33.3, 40, 44 OR 24, 32, 40, 50, 66.6, 80, 88				√		√	√		√				√
SC405 (Turbo)	28	PDIP SSOP	209	8, 12, 16, 20, 25, 33.3, 40, 44 OR 24, 32, 40, 50, 66.6, 80, 88	√			√		√	√		√		1 1	3 1	√
SC407	18	PDIP SOIC	300	24, 32, 40, 50, 66.6, 80, 88	√				√	√	2				**		√
SC409	24	PDIP SSOP	209	12, 16, 20, 25, 33.3, 40, 44 OR 24, 32, 40, 50, 66.6, 80, 88	√			√	√	√	√		√		1 1	1 1	√
SC417	20	PDIP SSOP	209	24, 32, 40, 50, 66.6, 80, 88	√			√	√	√	2	√					√
SC418	20	PDIP SSOP	209	24, 32, 40, 50, 66.6, 80, 88					√	√	2				1	3	
SC419	24	PDIP SSOP	209	12, 16, 20, 25, 33.3, 40, 44 OR 24, 32, 40, 50, 66.6, 80, 88	√			√	√	√	√	√			1 1	1 1	√
SC421	20	PDIP SSOP	209	16, 32, 33, 40, 50, 66, 80		CPCK2 = 32, 40, 50			√		2			√			
SC422	24	PDIP SSOP	209	16, 32, 33, 40, 50, 66, 80	√	CPCK2 = 32, 40, 50	√		√	√	2	√		√			
SC425	14	PDIP SOIC	300	12, 16, 20, 25, 33.3, 40, 50 OR 24, 32, 40, 50, 66.6, 80	√						√				1 1	3 1	√

* Available in 24 pin pack with buffers as SC406.

** Available in 28 pin pack with buffers as SC415.

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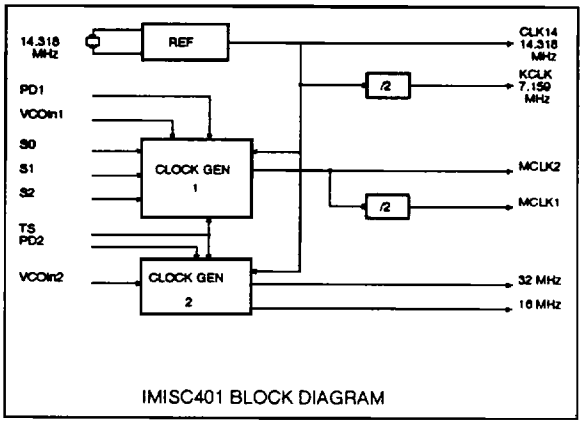
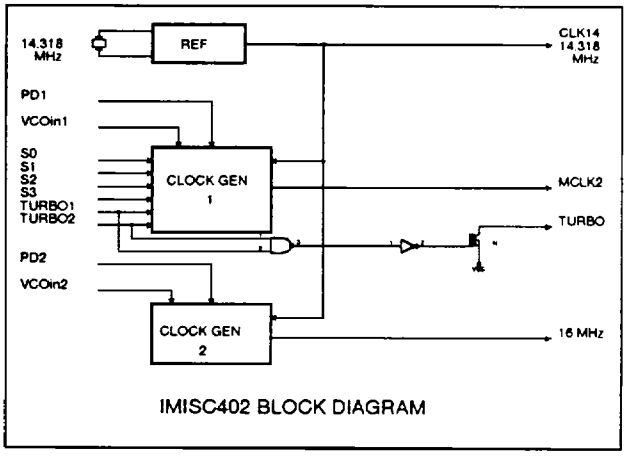
SC401 SYSTEM CLOCK CHIP



IMISC401 BLOCK DIAGRAM

MCLK2 FREQUENCY SELECTION			
INPUTS			OUTPUT
S2	S1	S0	MCLK2
0	0	0	24 MHz
0	0	1	32 MHz
0	1	0	40 MHz
0	1	1	50 MHz
1	0	0	66.6 MHz
1	0	1	80 MHz
1	1	0	88 MHz
1	1	1	Power Down

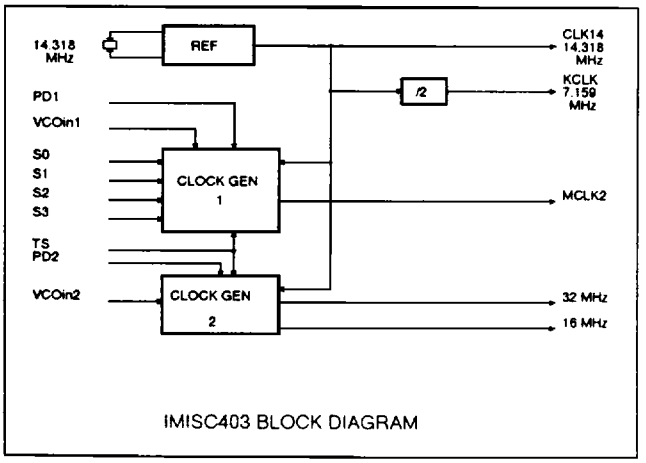
SC402 SYSTEM CLOCK CHIP



IMISC402 BLOCK DIAGRAM

MCLK2 FREQUENCY SELECTION							
INPUTS				MCLK2 (MHz)			
TURBO1	S2	S1	S0	TURBO2=1		TURBO2=0	
				S3=0	S3=1	S3=0	S3=1
0	X	X	X	8	16	8	16
1	0	0	0	12	24	8	16
1	0	0	1	16	32	12	24
1	0	1	0	20	40	16	32
1	0	1	1	25	50	20	40
1	1	0	0	33.3	66.6	25	50
1	1	0	1	40	80	33.3	66.6
1	1	1	0	44	88	40	80
1	1	1	1	Power Down	TEST	44	88

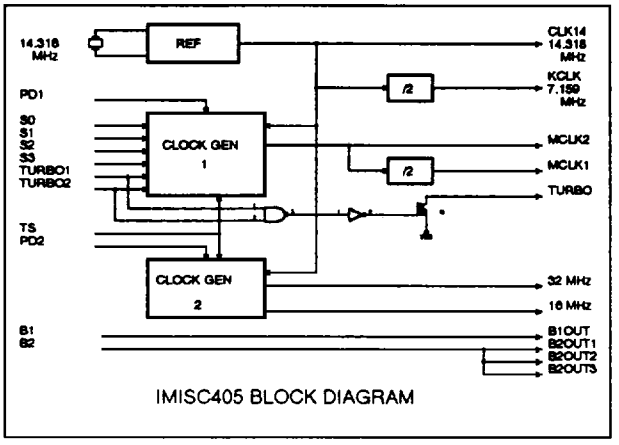
SC403 SYSTEM CLOCK CHIP



IMISC403 BLOCK DIAGRAM

MCLK2 FREQUENCY SELECTION				
INPUTS			MCLK2 OUTPUT	
S2	S1	S0	S3=0	S3=1
0	0	0	12 MHz	24 MHz
0	0	1	16 MHz	32 MHz
0	1	0	20 MHz	40 MHz
0	1	1	25 MHz	50 MHz
1	0	0	33.3 MHz	66.6 MHz
1	0	1	40 MHz	80 MHz
1	1	0	44 MH	88 MHz
1	1	1	Power Down	TEST

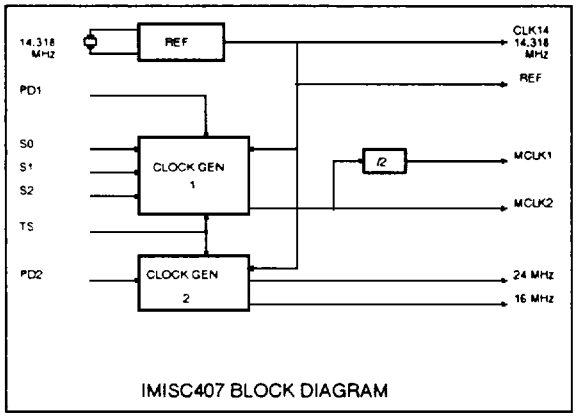
SC405 SYSTEM CLOCK CHIP



IMISC405 BLOCK DIAGRAM

MCLK2 FREQUENCY SELECTION							
INPUTS				MCLK2 (MHz)			
				TURBO2=1		TURBO2=0	
TURBO1	S2	S1	S0	S3=0	S3=1	S3=0	S3=1
0	X	X	X	8	16	8	16
1	0	0	0	12	24	8	16
1	0	0	1	16	32	12	24
1	0	1	0	20	40	16	32
1	0	1	1	25	50	20	40
1	1	0	0	33.3	66.6	25	50
1	1	0	1	40	80	33.3	66.6
1	1	1	0	44	88	40	80
1	1	1	1	Power Down	TEST	44	88

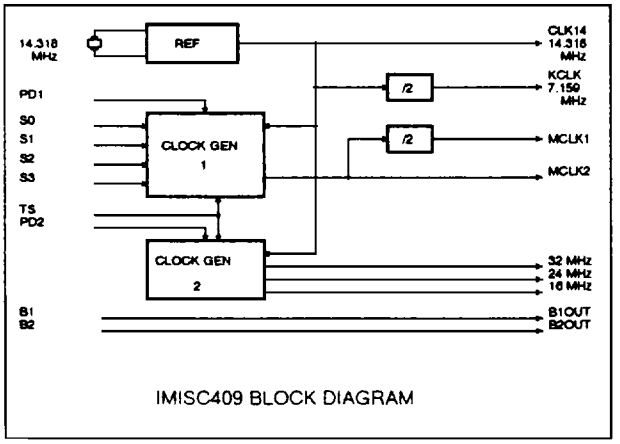
SC407 SYSTEM CLOCK CHIP



IMISC407 BLOCK DIAGRAM

MCLK2 FREQUENCY SELECTION			
INPUTS			OUTPUT
S2	S1	S0	MCLK2
0	0	0	24 MHz
0	0	1	32 MHz
0	1	0	40 MHz
0	1	1	50 MHz
1	0	0	66.6 MHz
1	0	1	80 MHz
1	1	0	88 MHz
1	1	1	Power Down

SC409 SYSTEM CLOCK CHIP



IMISC409 BLOCK DIAGRAM

MCLK2 FREQUENCY SELECTION				
INPUTS			MCLK2 OUTPUT	
S2	S1	S0	S3=0	S3=1
0	0	0	12 MHz	24 MHz
0	0	1	16 MHz	32 MHz
0	1	0	20 MHz	40 MHz
0	1	1	25 MHz	50 MHz
1	0	0	33.3 MHz	66.6 MHz
1	0	1	40 MHz	80 MHz
1	1	0	44 MH	88 MHz
1	1	1	Power Down	TEST

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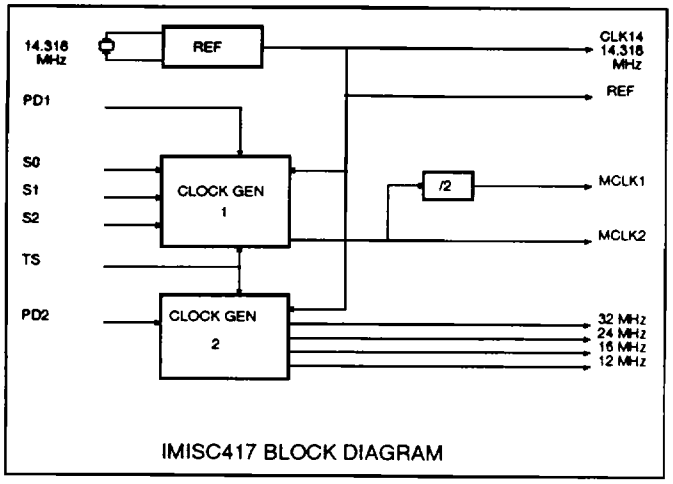
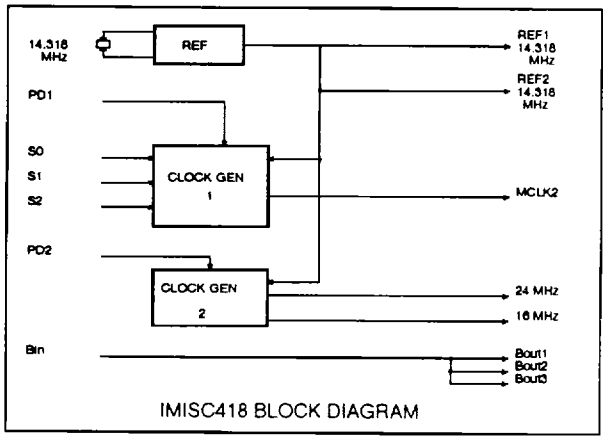
SC417 SYSTEM CLOCK CHIP



IMISC417 BLOCK DIAGRAM

MCLK2 FREQUENCY SELECTION			
INPUTS			OUTPUT
S2	S1	S0	MCLK2
0	0	0	24 MHz
0	0	1	32 MHz
0	1	0	40 MHz
0	1	1	50 MHz
1	0	0	66.6 MHz
1	0	1	80 MHz
1	1	0	88 MHz
1	1	1	Power Down

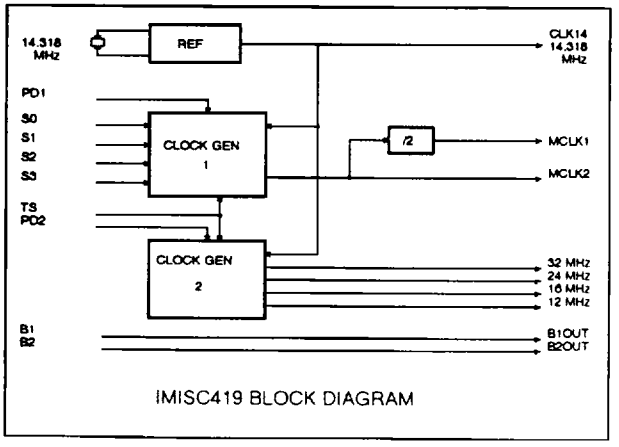
SC418 SYSTEM CLOCK CHIP



IMISC418 BLOCK DIAGRAM

MCLK2 FREQUENCY SELECTION			
INPUTS			OUTPUT
S2	S1	S0	MCLK2
0	0	0	24 MHz
0	0	1	32 MHz
0	1	0	40 MHz
0	1	1	50 MHz
1	0	0	66.6 MHz
1	0	1	80 MHz
1	1	0	88 MHz
1	1	1	Power Down

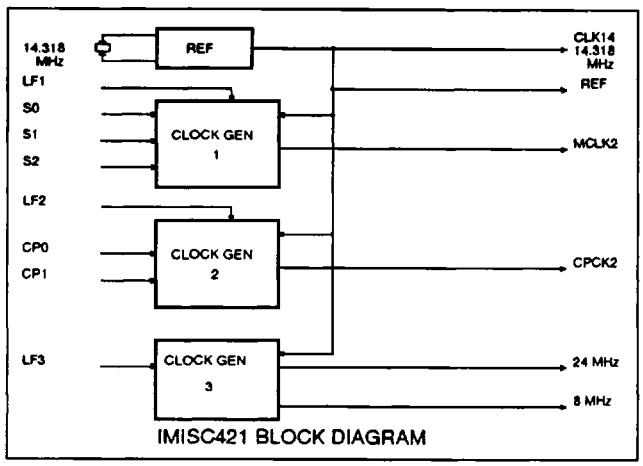
SC419 SYSTEM CLOCK CHIP



IMISC419 BLOCK DIAGRAM

MCLK2 FREQUENCY SELECTION				
INPUTS			MCLK2 OUTPUT	
S2	S1	S0	S3=0	S3=1
0	0	0	12 MHz	24 MHz
0	0	1	16 MHz	32 MHz
0	1	0	20 MHz	40 MHz
0	1	1	25 MHz	50 MHz
1	0	0	33.3 MHz	66.6 MHz
1	0	1	40 MHz	80 MHz
1	1	0	44 MH	88 MHz
1	1	1	Power Down	TEST

SC421 SYSTEM CLOCK CHIP

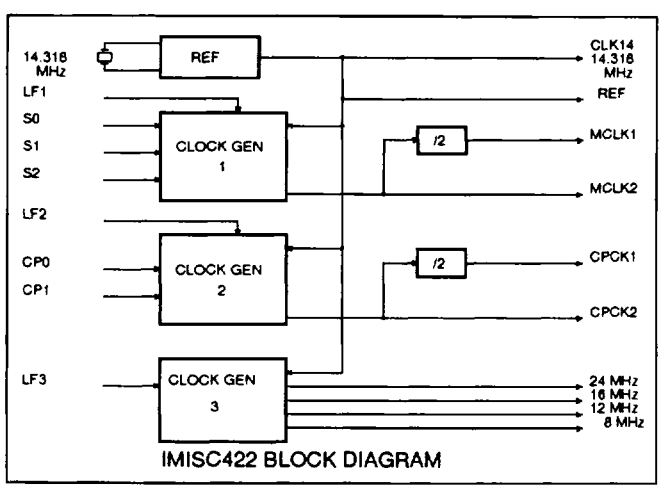


IMISC421 BLOCK DIAGRAM

MCLK2 FREQUENCY SELECTION			
INPUTS			OUTPUT
S2	S1	S0	MCLK2
0	0	0	16 MHz
0	0	1	32 MHz
0	1	0	33 MHz
0	1	1	40 MHz
1	0	0	50 MHz
1	0	1	66 MHz
1	1	0	80 MHz
1	1	1	Power Down

CPCK2 FREQUENCY SELECTION		
INPUTS		OUTPUT
CP1	CP0	CPCK2
0	0	32 MHz
0	1	40 MHz
1	0	50 MHz
1	1	Test Mode

SC422 SYSTEM CLOCK CHIP

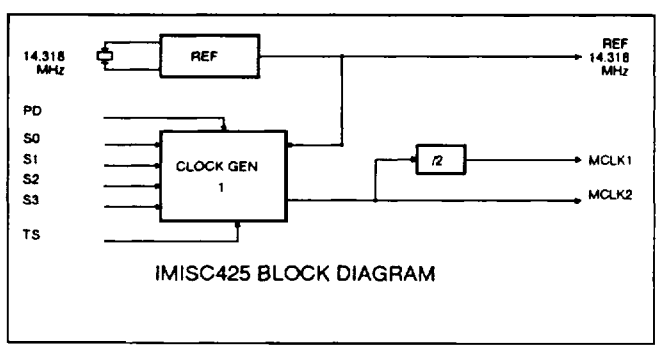


IMISC422 BLOCK DIAGRAM

MCLK2 FREQUENCY SELECTION				
INPUTS			OUTPUTS	
S2	S1	S0	MCLK2	MCLK1
0	0	0	16 MHz	8 MHz
0	0	1	32 MHz	16 MHz
0	1	0	33 MHz	16.5 MHz
0	1	1	40 MHz	20 MHz
1	0	0	50 MHz	25 MHz
1	0	1	66 MHz	33 MHz
1	1	0	80 MHz	40 MHz
1	1	1	Power Down	Power Down

CPCK2 FREQUENCY SELECTION			
INPUTS		OUTPUTS	
CP1	CP0	CPCK2	CPCK1
0	0	32 MHz	16 MHz
0	1	40 MHz	20 MHz
1	0	50 MHz	25 MHz
1	1	Test Mode	Test Mode

SC425 SYSTEM CLOCK CHIP



IMISC425 BLOCK DIAGRAM

MCLK2 FREQUENCY SELECTION				
INPUTS			MCLK2 OUTPUT	
S2	S1	S0	S3=1	S3=0
0	0	0	12 MHz	24 MHz
0	0	1	16 MHz	32 MHz
0	1	0	20 MHz	40 MHz
0	1	1	25 MHz	50 MHz
1	0	0	40 MHz	80 MHz
1	0	1	50 MHz	66.6 MHz
1	1	0	33.3 MH	66.6 MHz
1	1	1	Power Down	TEST

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