Integrated Device Technology, Inc.

128KB SECONDARY CACHE MODULE FOR THE INTEL™ i486™

PRELIMINARY
IDT7MB6091

FEATURES:

- Pin compatible with the Intel 485Turbocache™ 82485MB
- 128KB direct mapped, write-through, non-sectored, zero wait-state secondary cache module
- Ideal for use with i486-based systems with an Intel 485Turbocache socket
- Uses the IDT71589 32K x 9 CacheRAM™ with burst counter and self-timed write and the IDT71B74 cache-tag RAM
- Operates with external i486 speeds of up to 33MHz
- Concurrent snooping is supported
- 485Turbocache write protect strap feature is not supported
- 113 lead FR-4 QIP (Quad in-Line Package)
- Single 5V (±5%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

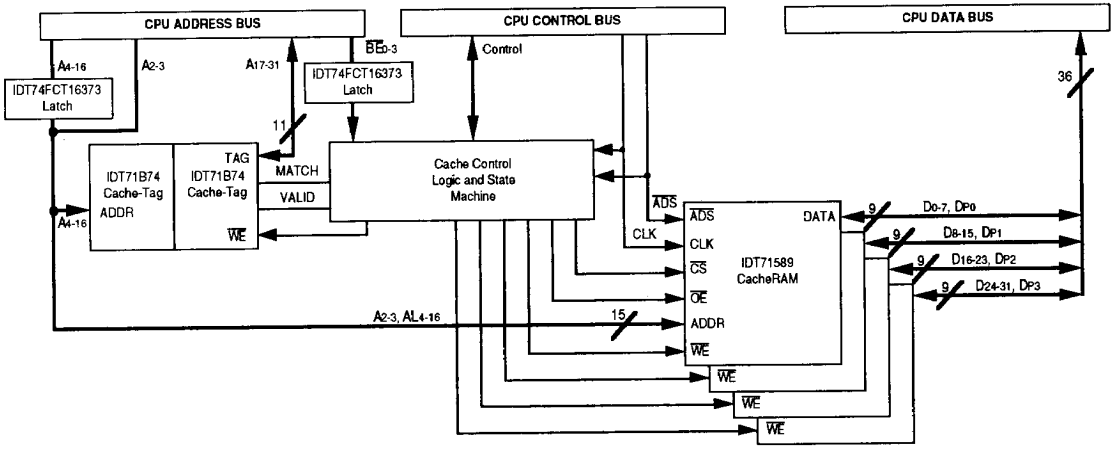
DESCRIPTION:

The IDT7MB6091 is a pin compatible replacement for the Intel 485Turbocache™ 82485MB. The module is a 128KB direct mapped, write-through, non-sectored, zero wait-state secondary cache and is ideal for use with many i486-based systems that have an Intel 485Turbocache socket. The IDT7MB6091 uses four IDT71589 32K x 9 CacheRAMs, two IDT71B74 8K x 8 cache-tag RAMs and two IDT74FCT16373 Double-Density™ 16-bit latches in plastic surface mount packages mounted on a multilayer epoxy laminate (FR-4) board along with logic for cache control. Extremely high speeds are achieved using IDT's high performance, high reliability BiCEMOS™ and CEMOS™ technologies.

An internal burst address counter accepts the first cycle address from the processor and then cycles through the adjacent four locations using the i486's burst refill sequence on appropriate rising edges of the system clock.

The quad in-line package (QIP) package configuration allows 113 leads to be placed on a package 2.9 inches long by 2.0 inches wide and 0.25 inches tall. All inputs and outputs of the IDT7MB6091 are TTL compatible and operate from a single 5V power supply.

FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION[1]

GND	A1	●	●	A2	RESET		$\overline{CS}$	A4	●	●	A5	GND
CLK	B1	●	●	B2	M/$\overline{IO}$		$\overline{CRDY}$	B4	●	●	B5	$\overline{CKEN}$
RESV	C1	●	●	C2	$\overline{FLUSH}$		$\overline{CBRDY}$	C4	●	●	C5	$\overline{BRDYO}$
$\overline{BLAST}$	D1	●	●	D2	$\overline{EADS}$		V_{CC}	D4	●	●	D5	$\overline{SKEN}$
$\overline{BOFF}$	E1	●	●	E2	V_{CC}		WP	E4	●	●	E5	$\overline{START}$
$\overline{ADS}$	F1	●	●	F2	W/$\overline{R}$		D_0	F4	●	●	F5	GND
GND	G1	●	●	G2	NC[2]		D_2	G4	●	●	G5	D_1
$\overline{BE_0}$	H1	●	●	H2	$\overline{BE_1}$		GND	H4	●	●	H5	D_3
$\overline{BE_2}$	I1	●	●	I2	$\overline{BE_3}$		D_5	I4	●	●	I5	D_4
A_2	J1	●	●	J2	GND		D_7	J4	●	●	J5	D_6
V_{CC}	K1	●	●	K2	A_3		D_8	K4	●	●	K5	GND
A_4	L1	●	●	L2	A_5		D_{10}	L4	●	●	L5	D_9
A_6	M1	●	●	M2	A_7		V_{CC}	M4	●	●	M5	D_{11}
A_9	N1	●	●	N2	A_8		D_{13}	N4	●	●	N5	D_{12}
A_{10}	O1	●	●	O2	V_{CC}		D_{15}	O4	●	●	O5	D_{14}
GND	P1	●	●	P2	A_{11}		D_{P0}	P4	●	●	P5	GND
A_{31}	Q1	●	●	Q2	A_{12}		D_{16}	Q4	●	●	Q5	D_{P1}
A_{14}	R1	●	●	R2	A_{13}		GND	R4	●	●	R5	D_{17}
A_{15}	S1	●	●	S2	GND		D_{19}	S4	●	●	S5	D_{18}
A_{17}	T1	●	●	T2	A_{16}		D_{21}	T4	●	●	T5	D_{20}
A_{19}	U1	●	●	U2	A_{18}		D_{22}	U4	●	●	U5	V_{CC}
V_{CC}	V1	●	●	V2	A_{20}		D_{24}	V4	●	●	V5	D_{23}
A_{22}	W1	●	●	W2	A_{21}		GND	W4	●	●	W5	D_{25}
A_{23}	X1	●	●	X2	V_{CC}		D_{27}	X4	●	●	X5	D_{26}
A_{25}	Y1	●	●	Y2	A_{24}		D_{29}	Y4	●	●	Y5	D_{28}
A_{27}	Z1	●	●	Z2	A_{26}		D_{30}	Z4	●	●	Z5	D_{31}
A_{29}	AA1	●	●	AA2	A_{28}		D_{P2}	AA4	●	●	AA5	D_{P3}
GND	BB1	●	●	BB2	A_{30}	$\overline{PRSN}$	BB3	●	V_{CC}	BB4	●	●	BB5	GND

QIP
TOP VIEW

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NOTE:
1. Pin G2 is $\overline{WPSTRP}$ on the Intel 485Turbocache. This signal is not used by the IDT7MB6091 and is N.C. (No Connect).

PIN NAMES

Symbol	Parameter	Type	Active	Description
CLK	CLOCK	Input	N/A	This input is the timing reference for all of the IDT7MB6091's functions. It is the same as the i486 CLK input.
RESET	RESET CACHE	Input	High	A synchronous positive-true reset input, which invalidates all cache locations and resets the cache control logic.
$\overline{ADS}$	ADDRESS STROBE	Input	Low	$\overline{ADS}$ is connected to the ADS# pin of the i486 CPU. It is used by the IDT7MB6091 to start any read or write cycle. $\overline{CS}$ must be asserted for $\overline{ADS}$ to be recognized.
M/$\overline{IO}$	MEMORY/IO	Input	N/A	This pin is used by the i486 to indicate whether the current cycle is a memory or I/O cycle. I/O cycles are not cacheable by the IDT7MB6091.
W/$\overline{R}$	WRITE/READ	Input	N/A	Write cycles are indicated by a high level on this pin, and read cycles are indicated by a low level.
$\overline{START}$	MEMORY START	Output	Low	During a cache read miss cycle or a write cycle, the $\overline{START}$ pin signals that the main memory system should service the current access.
$\overline{BRDYO}$	BURST READY OUT	Output	Low	This the IDT7MB6091's means of signaling to the i486 that cache data is ready to be sampled.
$\overline{CBRDY}$	CACHE BURST READY IN	Input	Low	This is the system input to the IDT7MB6091 to let the cache know that a main memory cache word is ready to be sampled by the CPU and the IDT7MB6091 during a burst access.
$\overline{CRDY}$	CACHE READY IN	Input	Low	$\overline{CRDY}$ signals to the IDT7MB6091 and the i486 that the main memory data is valid during a non-burst access. Another $\overline{ADS}$ must be generated by the CPU to fetch other words of that cache line from main memory.

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$\overline{BLAST}$	BURST LAST	Input	Low	This i486 output indicates to the IDT7MB6091 cache control logic that the current cycle is the last cycle of a cache burst.
$\overline{BOFF}$	BACKOFF	Input	Low	This signal is used to stall the IDT7MB6091. The IDT7MB6091 will also put its data bus into a high-impedance state. The IDT7MB6091 will only recognize invalidation cycles when $\overline{BOFF}$ is asserted.
$\overline{PRSN}$	PRESENCE	Output	Low	This pin is hardwired to ground. It tells the system logic that the IDT7MB6091 is plugged into the system.
A_2-A_{31}	PROCESSOR ADDRESSES	Input	N/A	These are the address inputs to the IDT7MB6091.
$\overline{BE_0}$-$\overline{BE_3}$	BYTE ENABLE	Input	Low	The byte enable inputs are sampled only during CPU write cycles and are only used to control byte writes to valid cache lines during write hit cycles. The timing is the same as for the address input pins.
$\overline{CS}$	CHIP SELECT	Input	Low	Chip select can be used for depth expansion. $\overline{CS}$ must be low for $\overline{EADS}$ or $\overline{ADS}$ to be recognized by the IDT7MB6091.
D_0-D_{31}	PROCESSOR DATA LINES	I/O	N/A	These are the data inputs from either the i486 or the system memory. D_0-D_7 define the least significant byte while D_{24}-D_{31} define the most significant byte.
DP_0-DP_3	DATA PARITY	I/O	N/A	These are the parity bits from either the i486 or the system memory. The timing requirements are the same as the data lines.
$\overline{CKEN}$	CACHE ENABLE TO CPU	Output	Low	This signal is the cache enable signal generated by the IDT7MB6091. The IDT7MB6091 will always assert $\overline{CKEN}$ during T1 cycles and during read hit cycles before the last $\overline{BRDYO}$. The IDT7MB6091 will not assert $\overline{CKEN}$ during read miss cycles.
$\overline{SKEN}$	SYSTEM CACHE ENABLE	Input	Low	This signal is generated by the system to indicate that a line is cacheable. The IDT7MB6091 will look for $\overline{SKEN}$ to be active during the cycle before the first word transfer and the cycle before the last word transfer of a line fill.
$\overline{FLUSH}$	FLUSH CACHE	Input	Low	This signal causes the IDT7MB6091 to invalidate its entire cache contents.
WP	WRITE PROTECT	Input	High	The write protect input is only sampled during write cycles. If this signal is asserted during a write hit cycle, the current cache data will not be overwritten.
$\overline{WPSTRP}$	WRITE PROTECT STRAP	N/A	N/A	This signal is not used by the IDT7MB6091.
$\overline{EADS}$	VALID EXTERNAL ADDRESS	Input	Low	This signal indicates that an invalidation address is present on the IDT7MB6091 address bus. $\overline{CS}$ must be low for $\overline{EADS}$ to be recognized by the IDT7MB6091.

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FUNCTIONAL DESCRIPTION:

BASIC OPERATION

The IDT7MB6091 is a complete secondary cache subsystem designed to replace the Intel Turbocache485. The IDT7MB6091 is designed to support zero wait state line reads, i.e. four words of data in five clocks. The IDT7MB6091 supports all of the following bus cycles: read hit, read miss, write hit, write miss, invalidation and backoff. The IDT7MB6091 also features single pin reset and cache flush capabilities.

The IDT7MB6091 latches the address at the input of the module at the beginning of any read, write or invalidation cycle. The address remains latched for one cycle after the initiation of a read or write, and the address remains latched for two cycles after the initiation of an invalidation.

RESET

The IDT7MB6091 is reset when RESET is asserted. Asserting RESET will invalidate the entire contents of the cache, and reset the control logic of the cache. The cache will be reset regardless of the state of other control signals when RESET is asserted.

FLUSH

The entire cache contents of the IDT7MB6091 is invalidated when the $\overline{FLUSH}$ input is asserted. The cache will be invalidated regardless of the state of other control signals when $\overline{FLUSH}$ is asserted. $\overline{FLUSH}$ will not reset the state of the cache control logic.

READ

The IDT7MB6091 recognizes the initiation of a read cycle when both $\overline{ADS}$ and $\overline{CS}$ are sampled low with M/$\overline{IO}$ high and W/$\overline{R}$ low. As soon as the address is valid at the input of the module, the IDT7MB6091 begins its tag look-up. If the input address is not contained in the cache, then a miss has occurred and the IDT7MB6091 will wait for the main memory system to service the current access. If the input address is present in the cache, then a hit has occurred and the IDT7MB6091 will burst back a line of data to the CPU.

If a read miss occurs the IDT7MB6091 asserts $\overline{START}$ in the first T2 cycle and then waits for the memory system to provide data. The IDT7MB6091 will consider the data returned from the memory system as cacheable if $\overline{SKEN}$ is sampled low at least one cycle before $\overline{CBRDY}$ or $\overline{CRDY}$ is first

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asserted. The IDT7MB6091 will load the data word returned from the memory system into the cache each time $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled low. However, the IDT7MB6091 will only validate the line of data returned from the memory system if $\overline{SKEN}$ is sampled low the cycle before the last data word is transferred from the memory system, i.e. the fourth time that $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled low. The line fill is aborted if $\overline{BLAST}$ is sampled low concurrent with $\overline{CBRDY}$ or $\overline{CRDY}$ being sampled low prior to the last data word transfer.

The IDT7MB6091 will consider the data returned as non-cacheable if $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled low before or concurrently with $\overline{SKEN}$. Therefore, to avoid a potential performance penalty, $\overline{SKEN}$ should not be asserted prior to $\overline{CBRDY}$ or $\overline{CRDY}$ if the data is considered non-cacheable, since the IDT7MB6091 will invalidate a line of data if $\overline{SKEN}$ is sampled low before $\overline{CBRDY}$ or $\overline{CRDY}$ is sampled low during a read miss.

The IDT7MB6091 requires that the read miss address (i.e. the address that was valid at the beginning of the read cycle) is present when $\overline{SKEN}$ is sampled low at the beginning of a line fill and again when $\overline{SKEN}$ is sampled at the end of a line fill. The address must be valid because it is latched at these times to invalidate a line at the beginning of the fill and then to validate the line at the end of the line fill. When the address is latched at the end of the line fill, it will remain latched until the last data word of the line is written to the cache.

If the IDT7MB6091 detects that the input address is contained in the cache, the IDT7MB6091 will supply data to the CPU. The IDT7MB6091 starts bursting data back to the CPU in the first T2 cycle. The IDT7MB6091 then transfers a new data word in each subsequent T2 cycle until $\overline{BLAST}$ is asserted to the cache. The IDT7MB6091 also forces $\overline{START}$ high and $\overline{BRDYO}$ low in the first T2 cycle. $\overline{CKEN}$ is asserted during the T1 cycle and again in the second and subsequent T2 cycles during a read hit.

WRITE

The IDT7MB6091 recognizes the initiation of a write cycle when both $\overline{ADS}$ and $\overline{CS}$ are sampled low with M/$\overline{IO}$ high and W/$\overline{R}$ high. As soon as the address is valid at the input of the module, the IDT7MB6091 begins its tag look-up. If the input address is contained in the cache then a write hit has occurred, and the cache contents are updated in the first T2 cycle if the WP input is low. If the WP input is high during a write hit, the line is seen as write protected and the write is ignored. If the input address is not contained in the cache then a write miss has occurred, the IDT7MB6091 ignores the write and the cache contents are not updated.

INVALIDATION

An invalidation is initiated by the simultaneous assertion of $\overline{EADS}$ and $\overline{CS}$. If $\overline{EADS}$ and $\overline{ADS}$ are asserted simultaneously, $\overline{ADS}$ is ignored since invalidations have priority. At the initiation of an invalidation, the IDT7MB6091 begins its tag look-up. If the line is found in the cache, the line will be invalidated. The IDT7MB6091 requires two cycles after the assertion of $\overline{EADS}$ to invalidate a line; therefore, invalidations can only occur every third cycle. The IDT7MB6091 ignores invalidations only if an address is currently latched in the address latch. Therefore, the IDT7MB6091 ignores invalidations at the following times: the cycle after the initiation of a read or write cycle, the cycle after $\overline{SKEN}$ is first sampled low during a line fill, the cycle(s) after sampling $\overline{SKEN}$ low concurrent with (or after) the third word transfer and prior to the fourth word transfer of a line fill, and the two cycles following a previous invalidation.

BACKOFF

A cache backoff is initiated by the assertion of $\overline{BOFF}$. $\overline{BOFF}$ interrupts any other cache cycle that the IDT7MB6091 is servicing. The cycle after $\overline{BOFF}$ is sampled low, the IDT7MB6091 will float its data bus, and the output control signals are driven to their idle levels, i.e. $\overline{CKEN}$ low, $\overline{START}$ high and $\overline{BRDYO}$ high. When $\overline{BOFF}$ is asserted, the IDT7MB6091 ignores all cache cycles except for invalidations; however, the IDT7MB6091 will still recognize the assertion of RESET or $\overline{FLUSH}$ when $\overline{BOFF}$ is asserted.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

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NOTE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Votage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

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NOTE:
1. VIL = –3.0V for pulse width less than 5ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 5%

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DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (A_2 - A_3)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	30	µA
$\|I_{LI}\|$	Input Leakage Current (Data, A_2 - A_3, $\overline{BE}_0$ - $\overline{BE}_3$)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LI}\|$	Input Leakage Current (CLK, $\overline{ADS}$)	V_{CC} = Max, V_{IN} = GND to V_{CC}	—	50	µA
$\|I_{IH}\|$	Input High Current (Control)	V_{CC} = Max, V_{IN} = V_{CC}	—	1.0	mA
$\|I_{IL}\|$	Input Low Current (Control)	V_{CC} = Max, V_{IN} = GND	—	260	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10	µA
V_{OLD}	Output Low Voltage (Data)	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OLC}	Output Low Voltage (Control)	I_{OL} = 12mA, V_{CC} = Min.	—	0.5	V
V_{OHD}	Output High Voltage (Data)	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V
V_{OHC}	Output High Voltage (Control)	I_{OH} = –2mA, V_{CC} = Min.	2.4	—	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$, f = f_{MAX}, Outputs Open	—	1900	mA

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CAPACITANCE[1]

(T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Condition	Max.	Unit
C_{IN}	Input Capacitance (A_2 - A_3)	V_{IN} = 0V	35	pF
C_{IN}	Input Capacitance (Data, A_{2-3}, $\overline{BE}_{0-3}$)	V_{IN} = 0V	15	pF
C_{IN}	Input Capacitance (Control)	V_{IN} = 0V	25	pF
C_{IN}	Input Capacitance ($\overline{ADS}$, CLK)	V_{IN} = 0V	45	pF
C_{OUT}	Output Capacitance ($\overline{BRDYO}$)	V_{IN} = 0V	40	pF
C_{OUT}	Output Capacitance (START, $\overline{SKEN}$)	V_{IN} = 0V	15	pF
$C_{I/O}$	Data I/O Capacitance	V_{OUT} = 0V	10	pF

NOTE:
1. These parameters are guaranteed by design but not tested.

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

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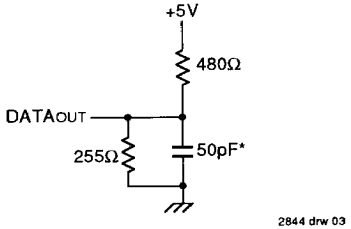

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Figure 1. Output Load

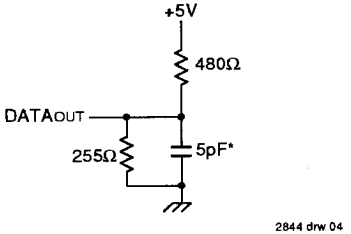

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Figure 2. Output Load (for t_{OHZ}, t_{CHZ}, t_{OLZ} and t_{CLZ})

*including scope and jig

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 0° to +70°C)

		7MB6091SxxK				
		33MHz		25MHz		
Symbol	Name	Min.	Max.	Min.	Max.	Unit
t_1	Clock Period	30	—	40	—	ns
t_2	Clock High Time	11	—	14	—	ns
t_3	Clock Low Time	11	—	14	—	ns
t_4	A_2-A_{31}, $\overline{BE_0}$-$\overline{BE_3}$ Setup Time	13	—	17	—	ns
t_5	A_2-A_{31}, $\overline{BE_0}$-$\overline{BE_3}$ Hold Time	10	—	10	—	ns
t_6	A_4-A_{31} Line Fill Setup Time	5	—	5	—	ns
t_7	$\overline{ADS}$, M/$\overline{IO}$, W/$\overline{R}$ Setup Time	13	—	20	—	ns
t_8	$\overline{ADS}$, M/$\overline{IO}$, W/$\overline{R}$ Hold Time	3	—	3	—	ns
t_9	$\overline{BLAST}$ Setup Time	9	—	10	—	ns
t_{10}	$\overline{BLAST}$ Hold Time	3	—	3	—	ns
t_{11}	$\overline{CRDY}$, $\overline{CBRDY}$ Setup Time	11	—	11	—	ns
t_{12}	$\overline{CRDY}$, $\overline{CBRDY}$ Hold Time	3	—	3	—	ns
t_{13}	$\overline{SKEN}$ Setup Time	9	—	9	—	ns
t_{14}	$\overline{SKEN}$ Hold Time	3	—	3	—	ns
t_{15}	D_0-D_{31}, DP_0-DP_3 Setup Time	5	—	5	—	ns
t_{16}	D_0-D_{31}, DP_0-DP_3 Hold Time	3	—	3	—	ns
t_{17}	$\overline{EADS}$ Setup Time	9	—	9	—	ns
t_{18}	$\overline{EADS}$ Hold Time	3	—	3	—	ns
t_{19}	A_4-A_{31} Setup Time (Snoop)	6	—	6	—	ns
t_{20}	A_4-A_{31} Hold Time (Snoop)	10	—	10	—	ns
t_{21}	RESET, $\overline{FLUSH}$ Setup Time	9	—	9	—	ns
t_{22}	RESET, $\overline{FLUSH}$ Hold Time	3	—	3	—	ns
t_{23}	RESET, $\overline{FLUSH}$ Pulse Width	80	—	80	—	ns
t_{24}	$\overline{BRDYO}$ Valid	—	16	—	22	ns
t_{25}	$\overline{CKEN}$ Valid	—	15	—	18	ns
t_{26}	$\overline{START}$ Valid	—	16	—	22	ns
t_{27}	D_0-D_{31}, DP_0-DP_3 Valid (Read Hit)	—	24	—	30	ns
t_{28}	WP Setup Time	15	—	15	—	ns
t_{29}	WP Hold Time	—	3	—	3	ns
t_{30}	$\overline{BOFF}$ Setup Time	9	—	10	—	ns
t_{31}	$\overline{BOFF}$ Hold Time	3	—	3	—	ns

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NOTE:
1. The address, M/$\overline{IO}$ and W/$\overline{R}$ inputs to the IDT7MB6091 must be held valid for the duration of the read, write or invalidation cycle.

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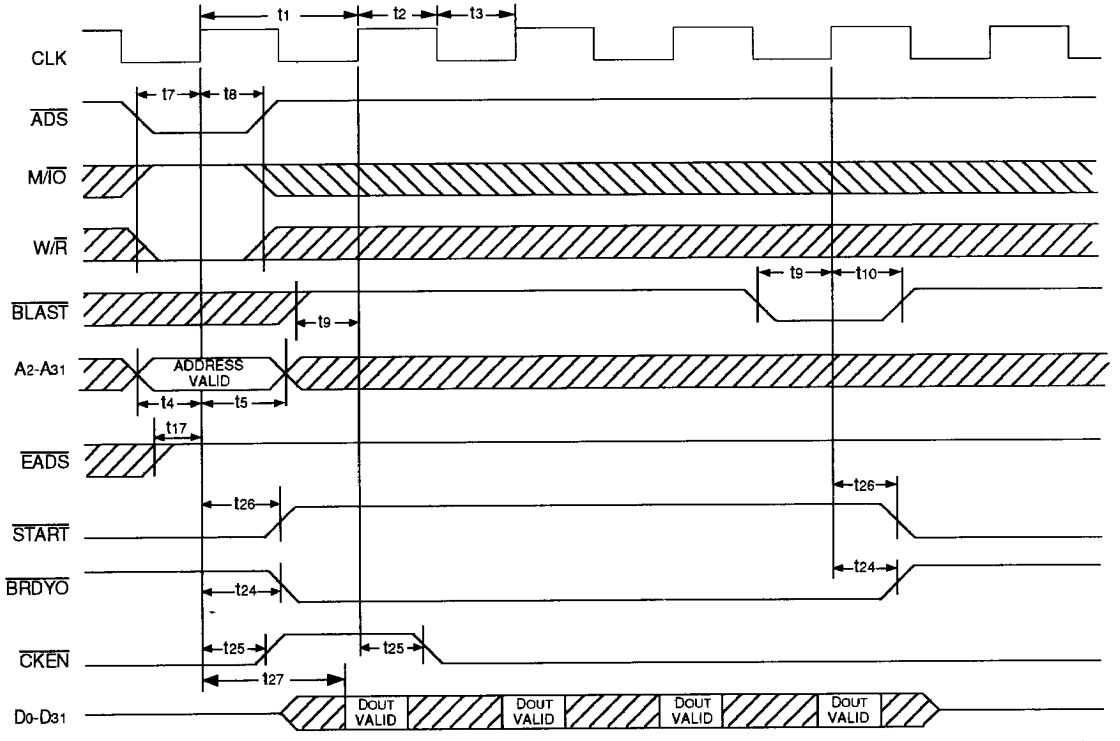
TIMING WAVEFORM OF A READ HIT CYCLE (READ LINE)(1)



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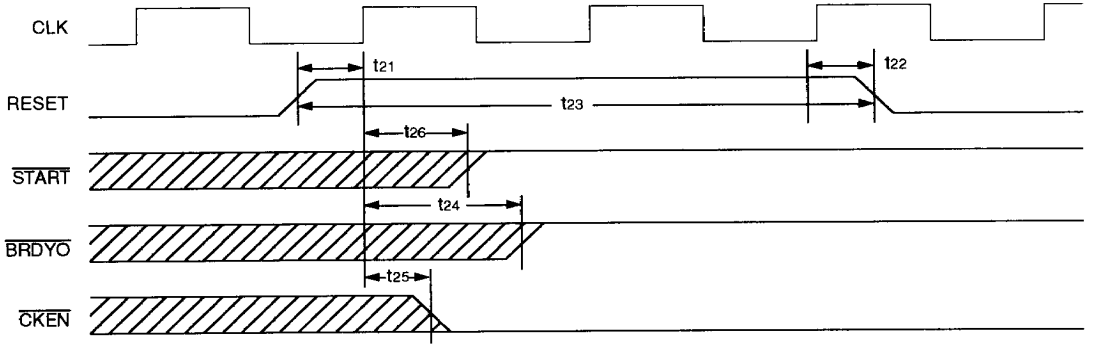
NOTE:
1. RESET is held LOW, $\overline{FLUSH}$ is held HIGH, $\overline{BOFF}$ is held HIGH.

TIMING WAVEFORM OF A RESET OPERATION



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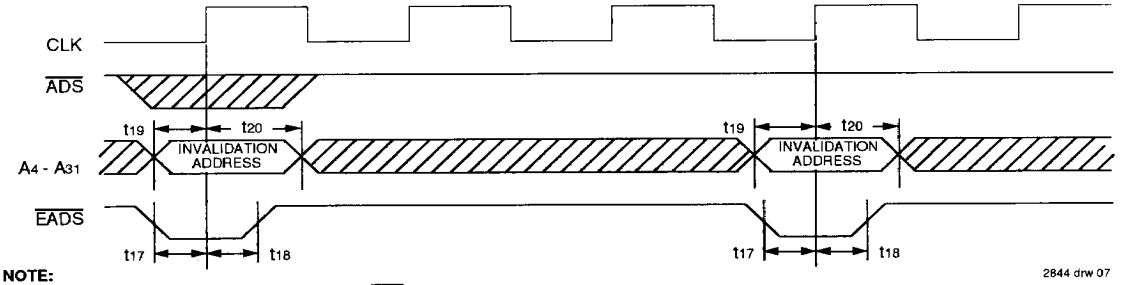
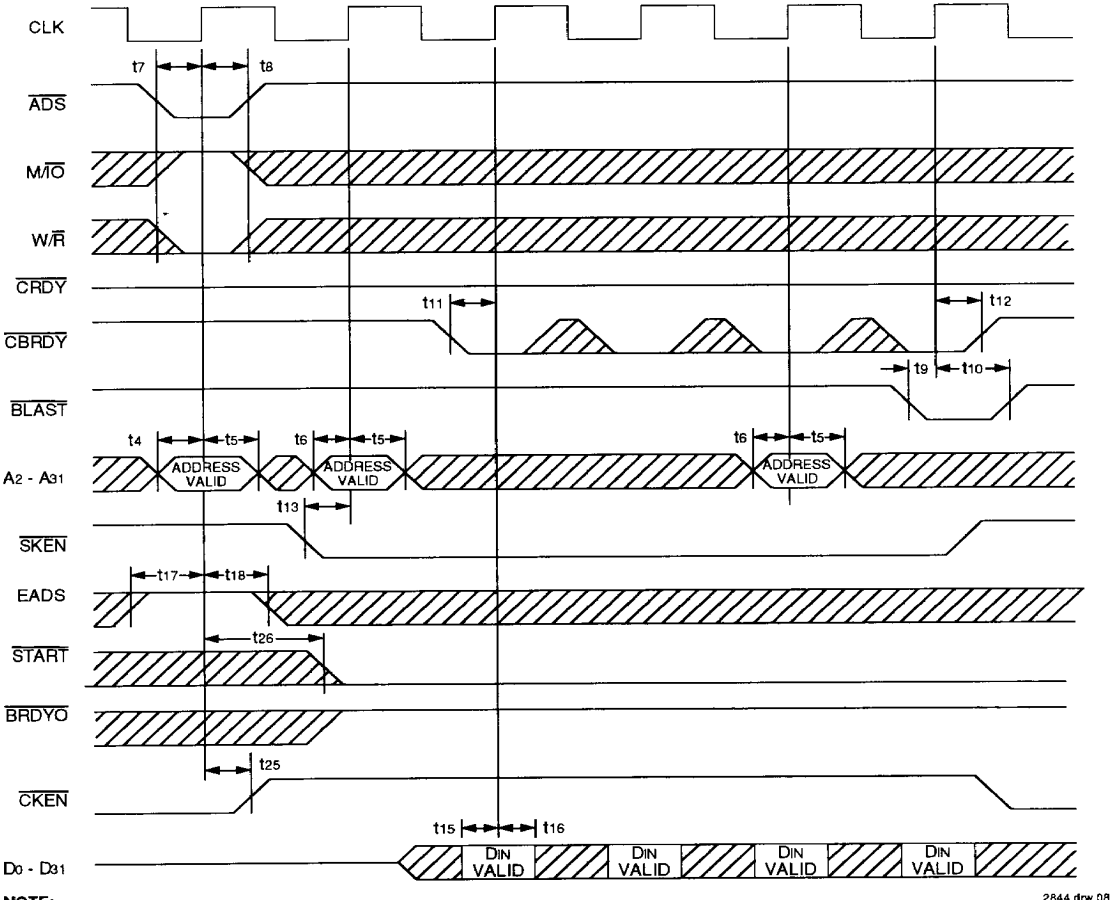
TIMING WAVEFORM OF A CACHE INVALIDATION(1)



NOTE:
1. If $\overline{EADS}$ and $\overline{ADS}$ are asserted simultaneously, $\overline{ADS}$ is ignored.

TIMING WAVEFORM OF A CACHEABLE BURST READ MISS CYCLE (WRITE LINE)(1)



NOTE:
1. RESET is held LOW, $\overline{FLUSH}$ is held HIGH, $\overline{BOFF}$ is held HIGH.

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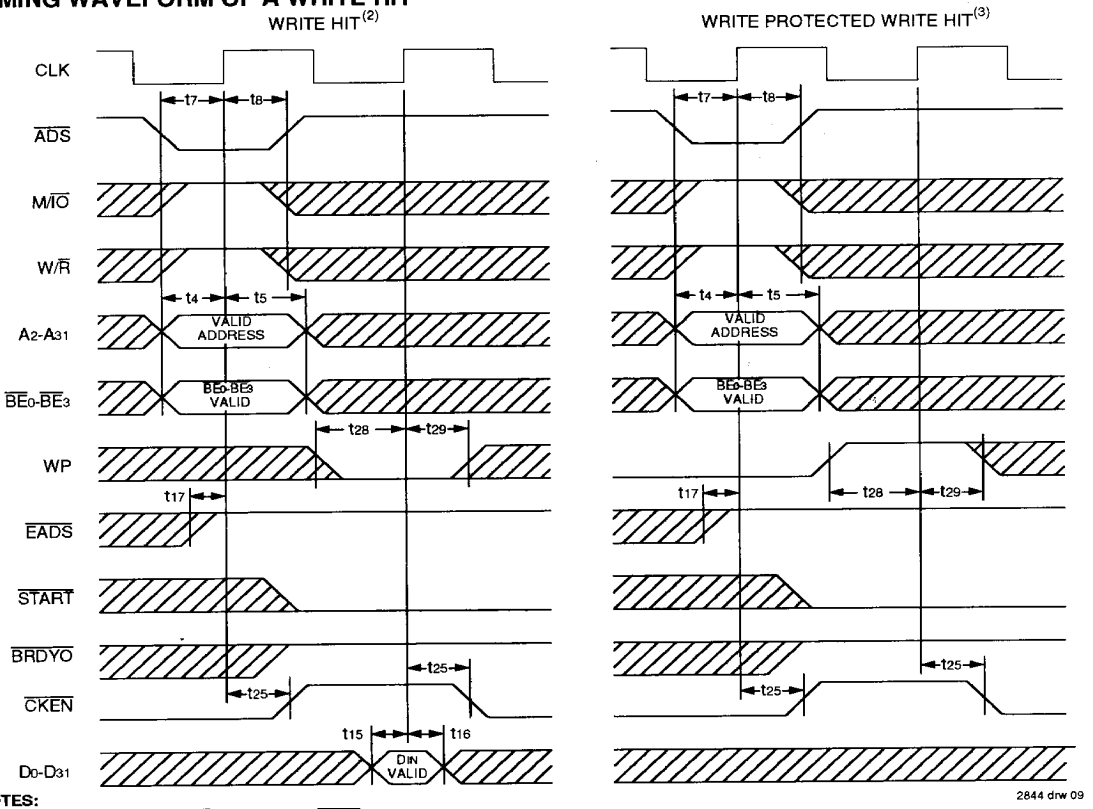
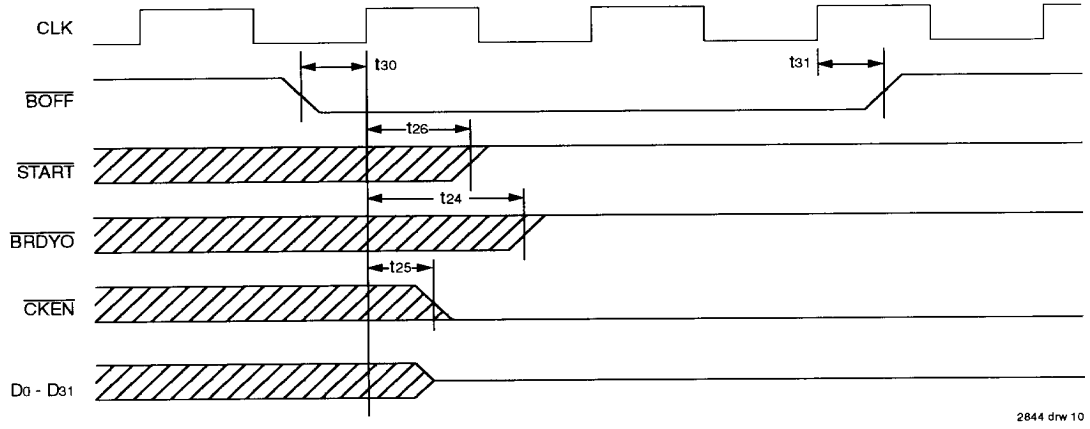
TIMING WAVEFORM OF A WRITE HIT[1]



NOTES:
1. RESET is held LOW, $\overline{FLUSH}$ is held HIGH, $\overline{BOFF}$ is held HIGH.
2. For a write hit, data in the IDT7MB6091 is updated.
3. For a write protected write hit, the data in the IDT7MB6091 is not updated.

TIMING WAVEFORM OF A BACKOFF OPERATION



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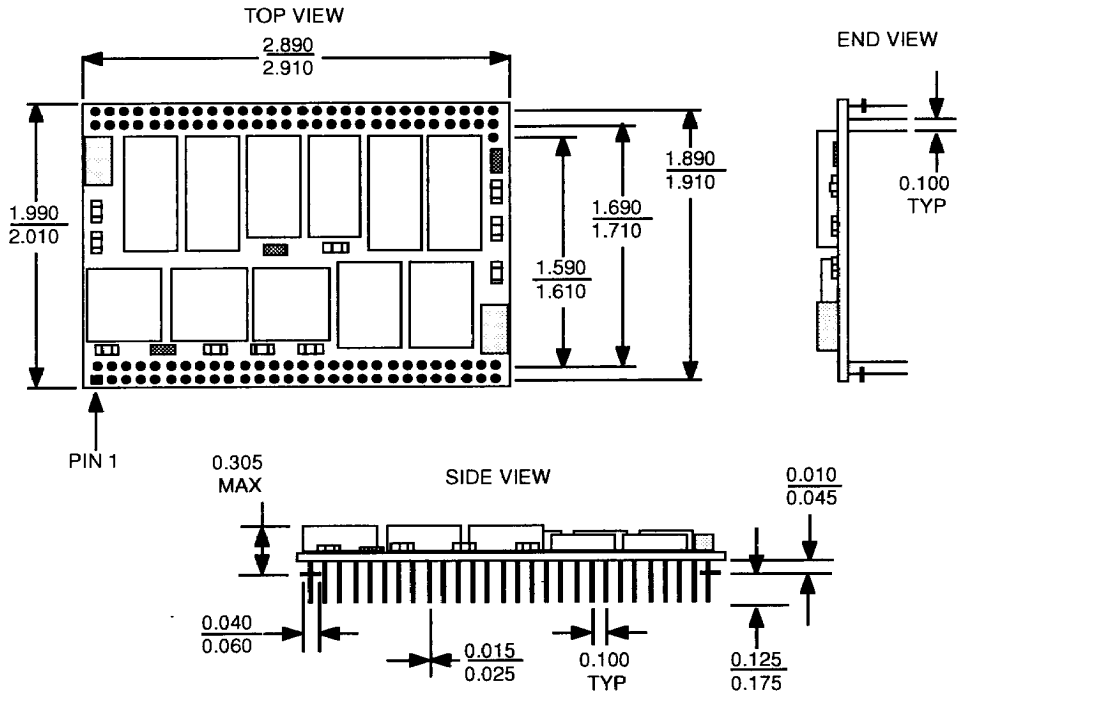
PACKAGE DIMENSIONS



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