256K Bit (32,768 X 8) Static CMOS ROM

Preliminary Data Sheet

GOULD *Electronics*

S63256

Features

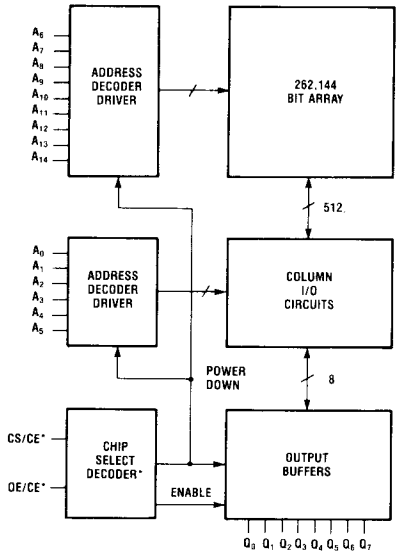
- Fast Access Time:
  S63256D—150ns (0°C to +70°C) Maximum
  S63256I—175ns (−40°C to +85°C) Maximum
  S63256M—200ns (−55°C to +125°C) Maximum
- Low Standby Power
  550 μW Maximum
- Fully Static Operation
- Single +5V ±10% Power Supply
- Directly TTL Compatible Inputs
- Three-State TTL Compatible Outputs
- EPROM Pin Compatible (27256)
- Late Mask Programmable
- Programmable Chip Enable/Select
- Programmable Output/Chip Enable

General Description

The Gould S63256 device is a 262,144 bit static mask programmable CMOS ROM organized as 32,768 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and uses a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

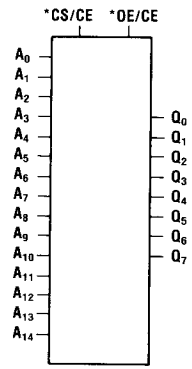
The S63256 is pin compatible with the 27256 UV EPROM making system development much easier and more cost effective. It is fully static, requiring no clocks for operation. The two control pins are mask programmable, the active level and function for each being specified by the user. When not enabled, the power supply current is reduced to a 100 μA maximum.

Block Diagram

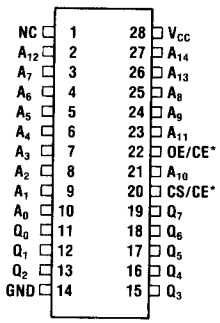


*THE USER DECIDES BETWEEN A CS OR CE FUNCTION AND OE OR CE FUNCTION AND THEN DEFINES THE ACTIVE LEVEL FOR CS/CE AND OE/CE

Logic Symbol



Pin Configuration



Pin Names

A_0–A_{14}	ADDRESS INPUTS
Q_0–Q_7	DATA OUTPUTS
CS/CE	CHIP SELECT/ENABLE
OE/CE	OUTPUT ENABLE/CHIP ENABLE
V_{CC}; GND; NC	5V; GROUND; NO CONTACT

MEMORY PRODUCTS

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Absolute Maximum Ratings

Ambient Temperature Under Bias—T_A (Standard part)	0°C to +70°C
(Industrial temperature part)	−40°C to +85°C
(Military temperature part)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Power Supply Voltage	−0.3V to +7V
Input or Output Voltages	−0.3V to V_{CC} +0.3V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to +70°C (Standard part); −40°C to +85°C (Industrial temperature part); −55°C to +125°C (Military temperature part)

Symbol	Parameter	Minimum	Maximum	Units	Conditions
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 3.2mA
V_{OH}	Output HIGH Voltage	2.4		V	I_{OH} = −1.0mA
V_{IL}	Input LOW Voltage	−0.3	0.8	V	
V_{IH}	Input HIGH Voltage	2.2	V_{CC} + 0.3	V	
I_{LI}	Input Leakage Current	−1.0	1.0	µA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current	−10	10	µA	V_O = 0V to V_{CC}, Chip Deselected
I_{CC1}	Power Supply Current—Active		40	mA	I_O = 0, TR = 150ns, duty = 100%**
I_{CC2}	Power Supply Current—CMOS Active		35	mA	I_O = 0, TR = 150ns, duty = 100%** V_I = GND or V_{CC}
I_{SB1}	Power Supply Current—Deselect		2	mA	Chip in Standby Mode, V_I = V_{IL} or V_{IH}
I_{SB2}	Power Supply Current—Standby		100	µA	Chip in Standby Mode, V_I = GND or V_{CC}

**Duty = 100%: CE =active level @ V_I

Capacitance: T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Minimum	Maximum	Units	Conditions
C_{IN}	Input Capacitance		7	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance		10	pF	V_{OUT} = 0V

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Switching Characteristics: V_{CC} = +5V ± 10%, T_A = 0°C to +70°C (Standard part); −40°C to +85°C (Industrial temperature part); −55°C to +125°C (Military temperature part)

Symbol	Parameter		Minimum	Maximum	Units	Conditions
t_{AA}	Address Access Time	S63256D S63256I S63256M		150 175 200	ns	See AC Timing Diagram and Test Load
t_{ACE}	Chip Enable Access Time	S63256D S63256I S63256M		150 175 200	ns	
t_{ACS}	Chip Select Access Time	S63256D S63256I S63256M	0 0 0	70 80 80	ns	
t_{OE}	Output Enable Access Time	S63256D S63256I S63256M	0 0 0	70 80 80	ns	
t_{OFF}	Chip Deselect Time	S63256D S63256I S63256M	0 0 0	50 70 70	ns	
t_{CEO}	Disable Time from Chip Enable	S63256D S63256I S63256M	0 0 0	50 70 70	ns	
t_{OEO}	Disable Time from Output Enable	S63256D S63256I S63256M	0 0 0	50 70 70	ns	
t_{OH}	Output-Hold Time	S63256D S63256I S63256M	0 0 0		ns	

Truth Table: (For simplicity, all control functions in the Truth Table are defined as active high).

CS/CE	OE/CE	Outputs	Power
$\overline{CE}$	X	HI-Z	STANDBY
X	$\overline{CE}$	HI-Z	STANDBY
$\overline{CS}$	$\overline{OE}$/CE	HI-Z	ACTIVE
CS/CE	$\overline{OE}$	HI-Z	ACTIVE
CS/CE	OE/CE	DATA OUT	ACTIVE

Pins	Control Functions Available
22	OE, $\overline{OE}$, CE, $\overline{CE}$, DC
20	CS, $\overline{CS}$, CE, $\overline{CE}$, DC

The user decides between a CS/CE and OE/CE function and then defines the active level. The function may also be defined as a Don't Care (DC). The chip is enabled when the inputs match the user defined states. Don't Care pins are still connected to input protection diodes and are subject to "Absolute Maximum Ratings".

The S63256 is fabricated using Gould's CMOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

ROM Code Data

Gould Semiconductor's preferred method of receiving ROM CODE DATA is in EPROM. Two EPROMs should be submitted. One is programmed to the desired code and the other is blank. Gould will read the programmed EPROM, transfer this data to disk and then program the blank EPROM from the stored information. This procedure guarantees that the EPROM has been properly entered into the Gould computer system. The Gould programmed EPROM is returned to the customer for verification of the ROM program. Unless otherwise requested Gould will not proceed until the customer verifies the program in the returned EPROM.

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EPROM Requirements
The following EPROMs should be used for submitted ROM Code Data:

PREFERRED 27256
Optional 2-27128
or 4-2764

If two or four EPROMs are used to specify one ROM pattern, an equal number of blank EPROMs must be submitted. In this instance, the programmed EPROMs must clearly state which of the EPROMs is for lower and upper address locations in the ROM. The preferred method is to mark each EPROM with the ROM address (in Hex) where the EPROM data is to be located.

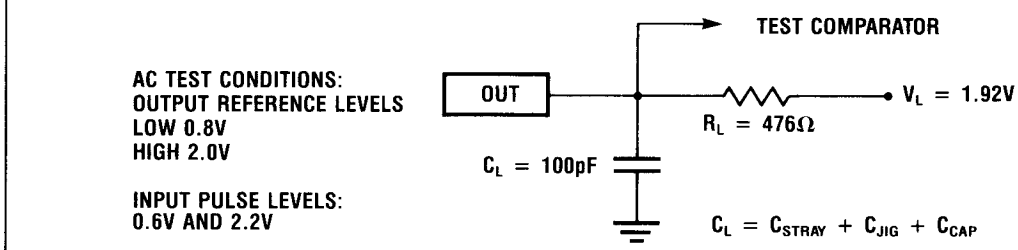
Pattern Data from ROMs
If a customer has ROMs produced by another supplier, these ROMs can be submitted for ROM pattern data instead of EPROMs. Obviously, these ROMs must be pin compatible with the Gould device. The programmable chip selects must be defined. (NOTE: In some cases a competitor's ROM may have a chip select or enable that is not customer defined. However, if this pin is customer defined for the Gould ROM, the required active logic level for this input must be specified.)

Optional Method of Supplying ROM Data*
If an EPROM or ROM cannot be supplied, the following other methods are acceptable.

- 9 Track NRZ Magnetic Tape
- Card Deck

*Consult Gould sales office for format.

Test Load



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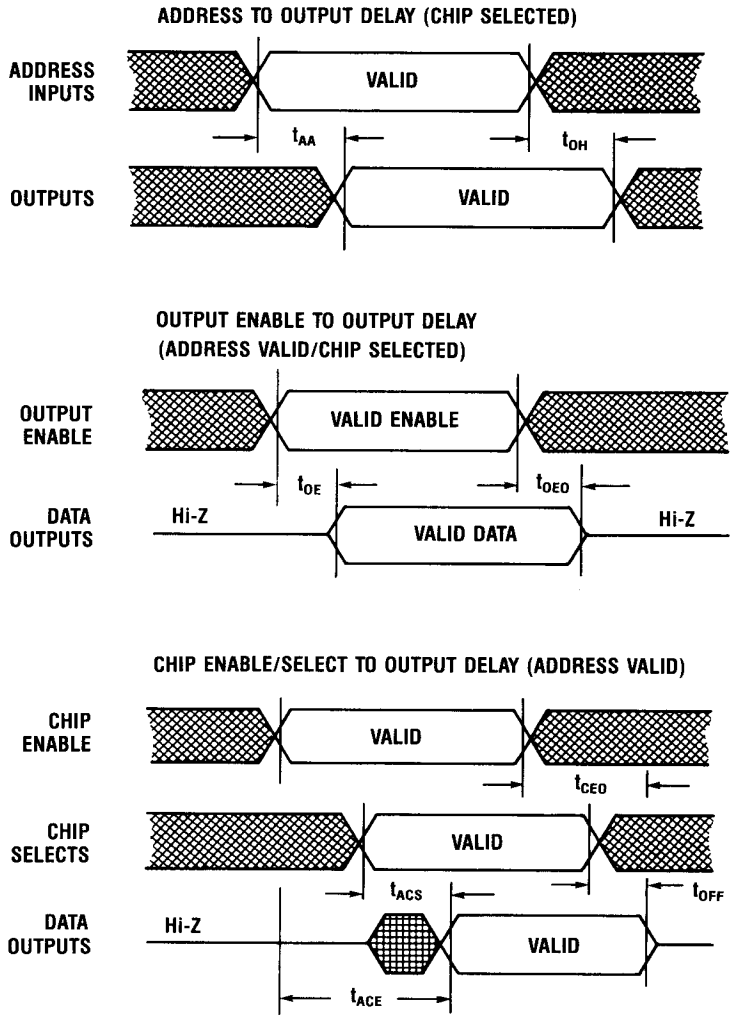
AC Timing Diagram



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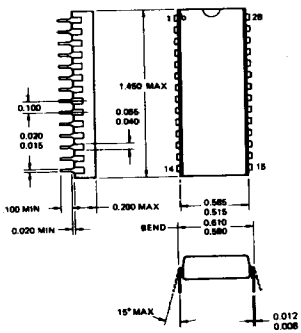
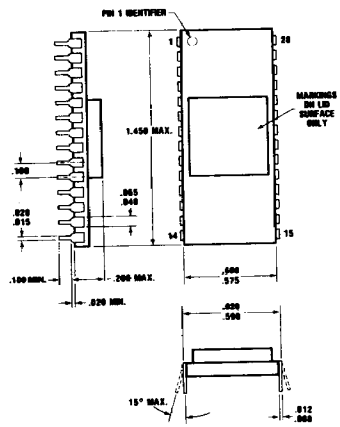
Package Outlines

28-Pin Plastic



28-Pin Ceramic



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