September 1990
Edition 1.0

FUJITSU

DATA SHEET

MB8298-25/-35
CMOS 256K-BIT HIGH-SPEED SRAM

1

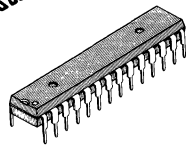
32K Words x 8 Bits High-Speed Static Random Access Memory

The Fujitsu MB8298 is a high-speed static random access memory organized as 32,768 words x 8 bits and fabricated with CMOS technology. To obtain a smaller chip size, the cells use NMOS transistors and resistors. The MB8298 is housed in 300 mil plastic DIP and SOJ packages and a 450-mil SOP package. All pins are TTL compatible and a single +5 V power supply is required.

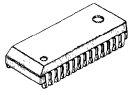
The MB8298 has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization: 32,768 words x 8 bits
- Static operation: no clocks or timing strobe required
- Access time: $t_{AA} = t_{ACS} = 25$ ns max. (MB8298-25)
  $t_{AA} = t_{ACS} = 35$ ns max. (MB8298-35)
- Low power consumption: 715 mW max. (Operating) for 25 ns
  605 mW max. (Operating) for 35 ns
  138 mW max. (TTL Standby)
  27.5 mW max. (CMOS Standby)
- Single +5 V power Supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capability
- Electrostatic protection for all inputs and outputs
- Standard 28-pin Plastic Packages:
  Skinny DIP (300 mil) MB8298-xxPSK
  SOP (450 mil) MB8298-xxPF
  SOJ (300 mil) MB8298-xxPJ

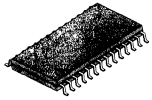
ADVANCE INFORMATION



Plastic Package
(DIP-28P-M04)

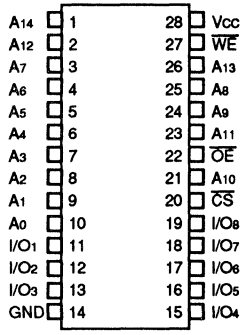


Plastic Package
(LCC-28P-M04)



Plastic Package
(FPT-28P-M02)

Pin Assignment
(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Absolute Maximum Ratings (See Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7	V
Input Voltage on any pin with respect to GND	V_{IN}	−3.5 to +7	V
Output Voltage on any I/O pin with respect to GND	V_{OUT}	−0.5 to +7	V
Output Current	I_{OUT}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias	T_{BIAS}	−10 to +85	°C
Storage Temperature Range	T_{STG}	−45 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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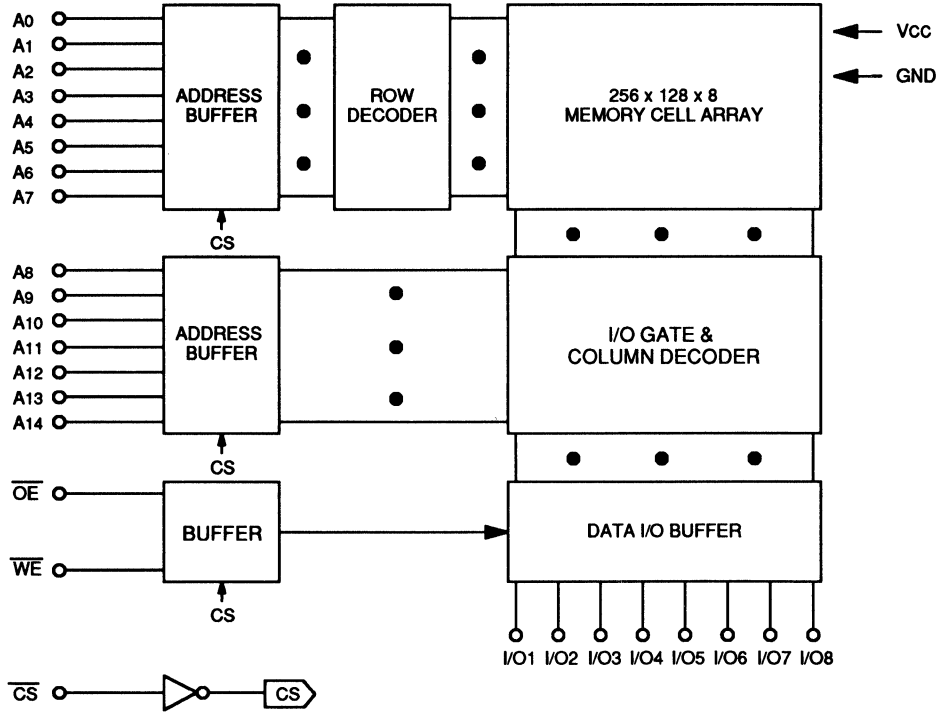
Fig. 1 – MB8298 BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	STANDBY	ISB	HIGH-Z
L	H	H	DOUT DISABLE	ICC	HIGH-Z
L	H	L	READ	ICC	DOUT
L	L	X	WRITE	ICC	DIN

CAPACITANCE (T_A= 25° C, f = 1MHz)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Input Capacitance ($\overline{CS}$, $\overline{OE}$, $\overline{WE}$)	VIN = 0V	CI1			8	pF
Input Capacitance (Other Input)	VIN = 0V	CI2			7	pF
I/O Capacitance	VI/O = 0V	CI/O			8	pF

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.5	5.0	5.5	V
Ambient Temperature	TA	0		70	°C

1

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

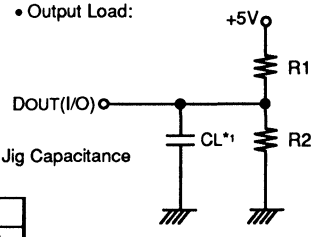
Parameter		Symbol	Test Condition	Min	Max	Unit
Standby Supply Current		ISB1	$\overline{CS} \geq VCC - 0.2V$ $VIN \geq VCC - 0.2V$ or $VIN \leq 0.2V$		5	mA
		ISB2	$VIN \leq 0.2V$ $\overline{CS} = VIH$		25	mA
Operating Supply Current	25ns	ICC	IOUT = 0mA, $\overline{CS}$ = VIL Cycle = Min.		130	mA
	35ns				110	
Input Leakage Current		ILI	VIN = 0V to VCC, VCC = Max.	–5	5	µA
Output Leakage Current		ILI/O	$\overline{CS}$ = VIH or $\overline{WE}$ = VIL or $\overline{OE}$ = VIH, VI/O = 0V to VCC	–5	5	µA
Input Low Voltage		VIL		–2.0*1	0.8	V
Input High Voltage		VIH		2.2	6.0	V
Output High Voltage		VOH	IOH = –4mA	2.4		V
Output Low Voltage		VOL	IOL = 8mA		0.4	V

Note: *1 –2.0V Min. for pulse width less than 20% of cycle time. (VIL min.=–0.5V at DC level)

Fig. 2 – AC TEST CONDITIONS

- Input Pulse Levels: 0V to 3.0V
- Input Pulse Rise & Fall Times: 3ns (Transient between 0.8V and 2.2V)
- Timing Reference Levels: Input :VIL=0.8V, VIH=2.2V
  Output :VOL=0.8V, VOH=2.2V

- Output Load:



*1 Including Scope and Jig Capacitance

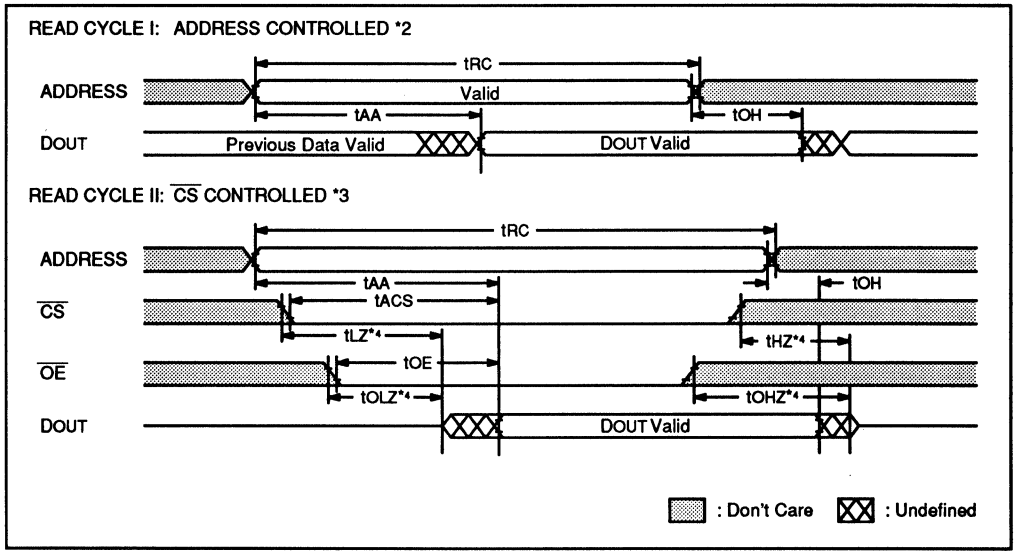
	R1	R2	CL	Parameters Measured
Load I	480kΩ	255Ω	30pF	except tLZ, tHZ, tWZ, tOW, tOLZ and tOHZ
Load II	480kΩ	255Ω	5pF	tLZ, tHZ, tWZ, tOW, tOLZ and tOHZ

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8298-25		MB8298-35		Unit
		Min	Max	Min	Max	
Read Cycle Time	tRC	25		35		ns
Address Access Time *2	tAA		25		35	ns
$\overline{CS}$ Access Time *3	tACS		25		35	ns
$\overline{OE}$ Access Time	tOE		12		14	ns
Output Hold from Address Change	tOH	3		3		ns
Output Low-Z from $\overline{CS}$ *4	tLZ	5		8		ns
Output Low-Z from OE *4	tOLZ	2		3		ns
Output High-Z from $\overline{CS}$ *4	tHZ	1	15	1	15	ns
Output High-Z from $\overline{OE}$ *4	tOHZ	1	15	1	15	ns

READ CYCLE TIMING DIAGRAM *1



Note: *1 $\overline{WE}$ is high for Read Cycle.
*2 Device is continuously selected, $\overline{CS}$ = VIL, and $\overline{OE}$=VIL.
*3 Address valid prior to or coincident with $\overline{CS}$ transition low.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

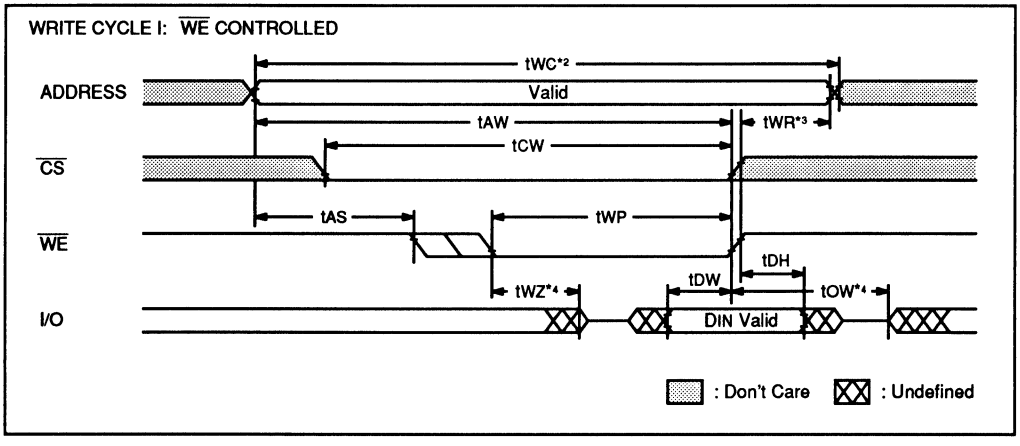
AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

WRITE CYCLE*1

Parameter	Symbol	MB8298-25		MB8298-35		Unit
		Min	Max	Min	Max	
Write Cycle Time*2	tWC	25		35		ns
Address Valid to End of Write	tAW	18		28		ns
$\overline{CS}$ to End of Write	tCW	16		26		ns
Data Setup Time	tDW	8		12		ns
Data Hold Time	tDH	0		0		ns
Write Pulse Width	tWP	15		20		ns
Write Recovery Time*3	tWR	0		0		ns
Address Setup Time	tAS	0		0		ns
Output Low-Z from $\overline{WE}$*4	tOW	0		0		ns
Output High-Z from $\overline{WE}$*4	tWZ	0	8	0	14	ns

WRITE CYCLE TIMING DIAGRAM *1



Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 tWR is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

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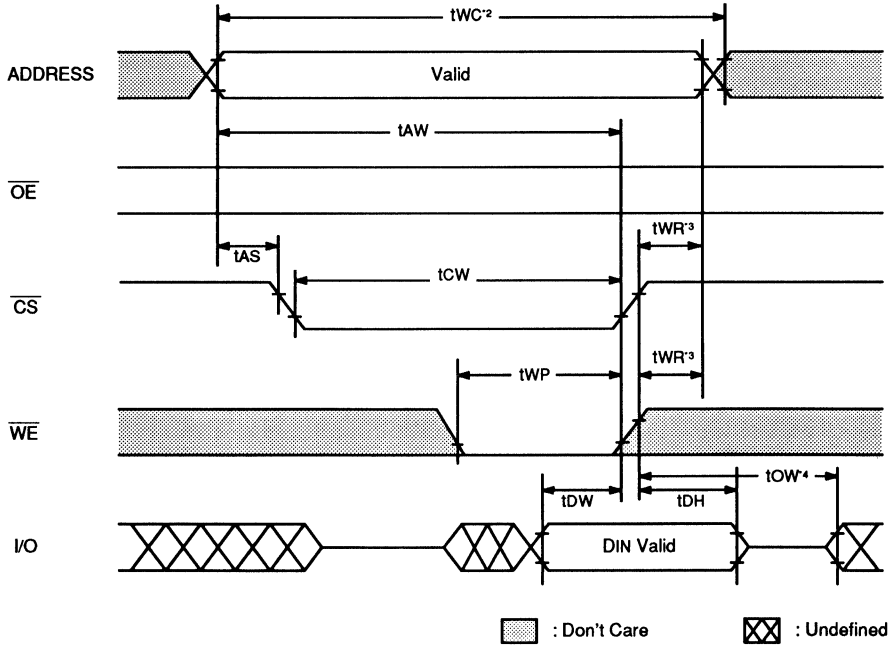
WRITE CYCLE TIMING DIAGRAM*1

WRITE CYCLE No. 2 ($\overline{CS}$ CONTROLLED)

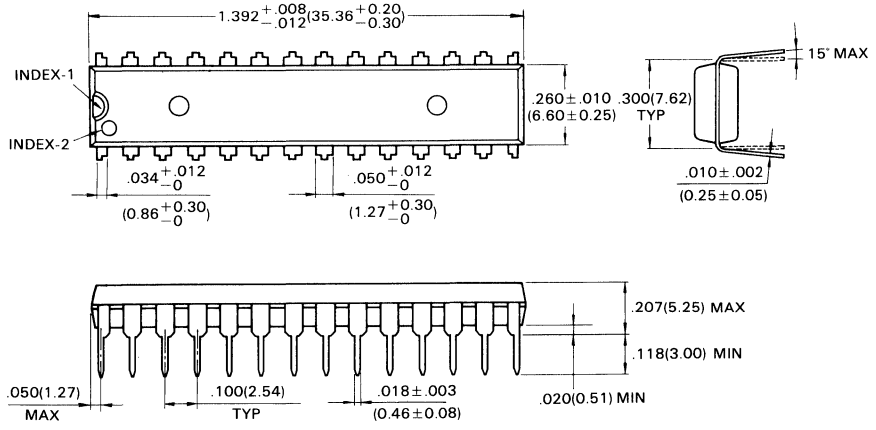


Note: *1 If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in high impedance state.
*2 All Write Cycles are determined from the last address transition to the first address transition of next address.
*3 tWR is defined from the end point of Write Mode.
*4 Transition is specified at the point of ±500mV from steady state voltage with specified Load II in Fig. 2.

PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: P-SK)

28-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-28P-M04)

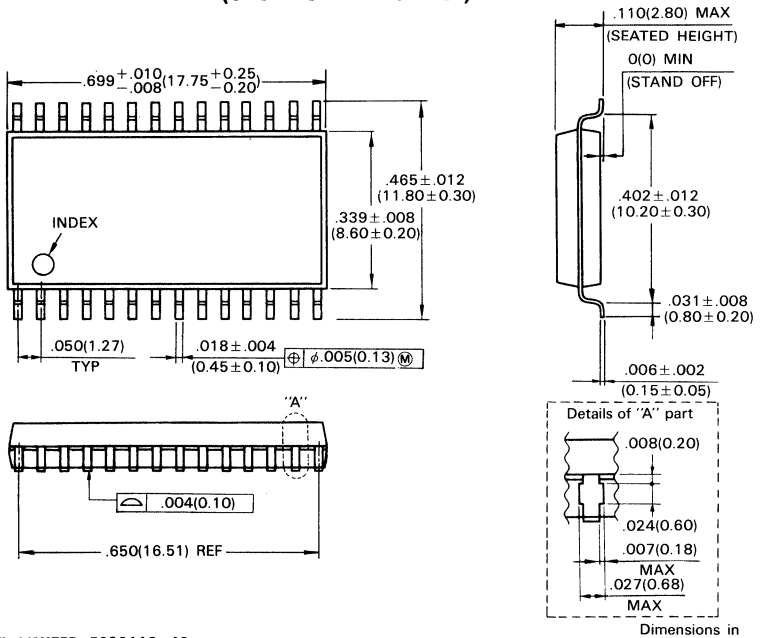


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

Plastic FPT (Suffix: PJ)

28-LEAD PLASTIC FLAT PACKAGE
(CASE NO.: FPT-28P-M02)

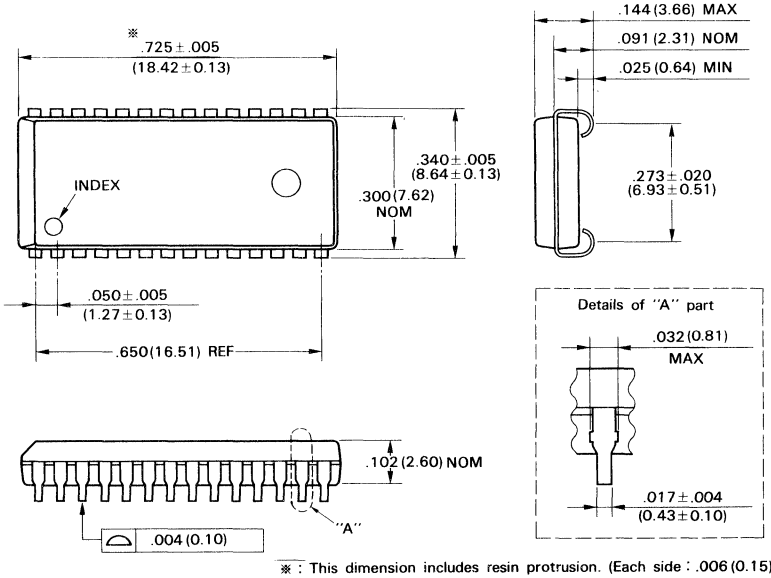


Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (Continued)

Plastic FPT (Suffix: PJ)

28-LEAD PLASTIC LEADED CHIP CARRIER
(CASE NO.: LCC-28P-M04)



※ : This dimension includes resin protrusion. (Each side : .006(0.15) MAX)

Dimensions in inches (millimeters)