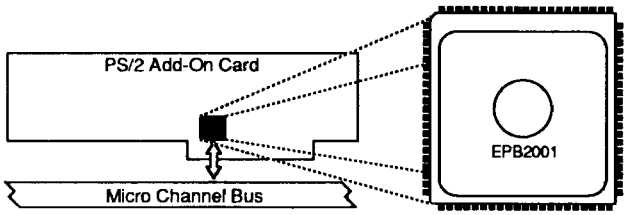
and the Micro Channel Bus (MC Bus). The EPB2001 is an ideal chip for manufacturers of IBM PS/2 add-on cards based on Micro Channel Architecture (MCA) since it allows programming of specific card characteristics for a specific application. The EPB2001's integrated functions can replace 18 or more MSI/TTL and standard PLD devices.

Although the EPB2001 occupies less than two square inches on the PC card (see Figure 2), its CMOS EPROM technology provides non-volatile storage of card ID, chip-select ranges, and POS I/O selection for reduced component count and added design security.

Figure 2. EPB2001 Single-Chip, Small Footprint Interface

The EPB2001 occupies less than two square inches on the PS/2 card.

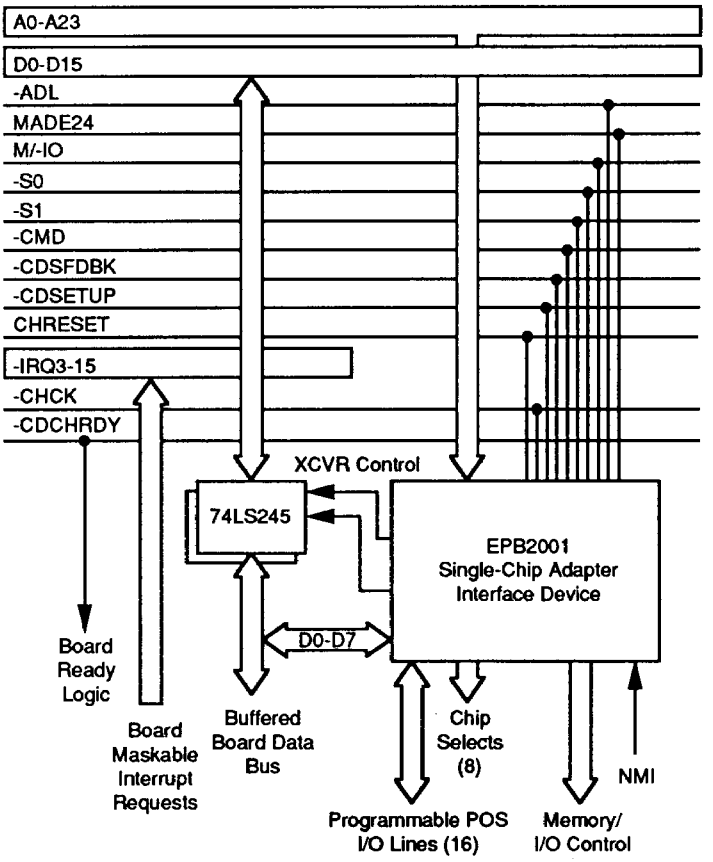


More specifically, the EPB2001 provides the following general-purpose interface functions: POS registers 0100-0105 (including card ID), access to POS register contents on card-accessible I/O lines (replacing jumpers and DIP switches on IBM PC and compatible add-on cards), card address remapping via programmable chip-select logic, and card control signals (e.g., -MEMWR, -IORD). Figure 3 shows the EPB2001 integrated into the Micro Channel environment.

The EPB2001 is available in both one-time-programmable plastic and erasable/reprogrammable ceramic J-lead chip carrier packages.

Figure 3. Micro Channel Interface Connection

The EPB2001 provides a convenient interface with the Micro Channel Bus.



MCMap, Altera's PC-based development software, makes designing with the EPB2001 quick and easy. This table-driven software guides the user through a series of menus to generate the desired design and convert it to a JEDEC file. MCMap also generates an Adapter Description File (ADF) for address decodes controlled by POS register bits. Finally, the converted design is programmed into the EPB2001 in seconds with the LP4 programming card, the PLE3-12A programming unit, and the PLEJ2001 device adapter.

Figure 4 shows the EPB2001 block diagram, with Micro Channel interface signals on the left and card interface signals on the right.

Figure 4. EPB2001 Block Diagram

The programmable elements of the EPB2001 allow it to be customized for a wide variety of applications. (Shading indicates programmable items.)

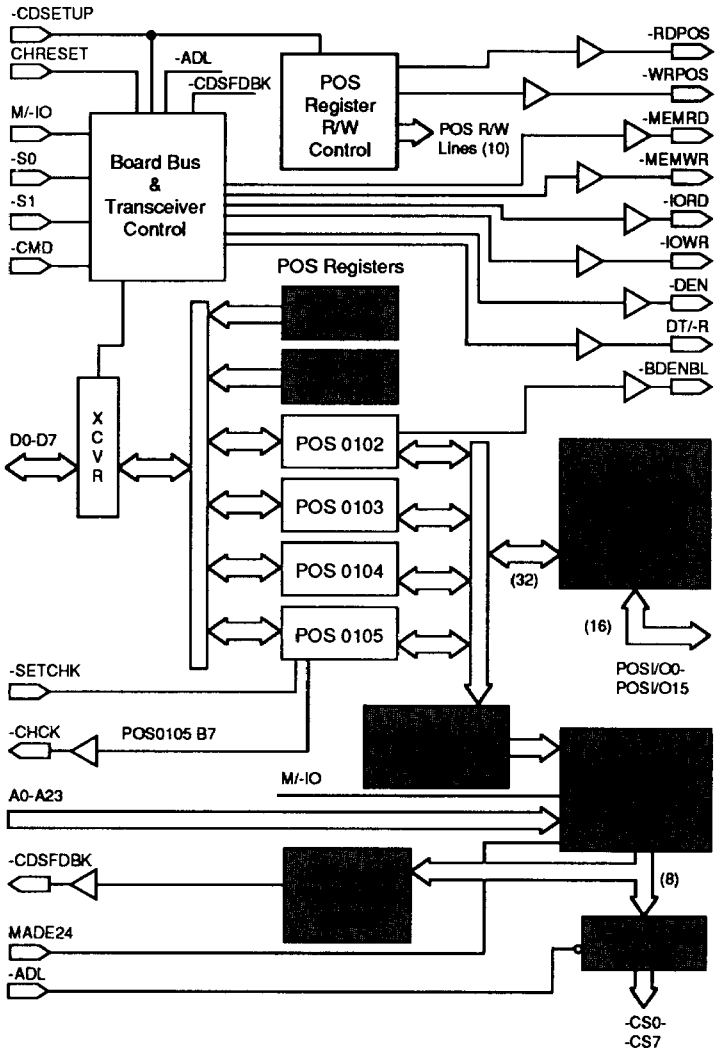


Table 1 summarizes the functions of EPB2001 pins. Note that active-low signals are prefixed with a dash (-).

Table 1. EPB2001 Pin Descriptions

Signal	Type*	Output Drive (mA) I_{OH}	Output Drive (mA) I_{OL}	Description
–CDSFDBK	TP	2	6	Active-low, bus-cycle acknowledge output generated by the EPB2001 for any I/O or memory cycle that activates one of the –CS outputs. Derived as a decode of unlatched chip selects.
–CHCK	OD		24	Active-low channel check output used to signal Non-Maskable Interrupt errors. Reflects the state of POS register 0105, bit 7. Activated by an active-low input pulse on the –SETCHK line.
D0-D7	TS	4	24	Tri-state bidirectional data bus lines. POS register Read/Write data access path. Enabled to the MC Bus only during a valid I/O Read cycle qualified by –CDSETUP.
–CDSETUP	I			Active-low set-up input. Signals a POST Read or Write cycle to the EPB2001's POS registers.
M/–IO	I			Memory/I/O cycle input from the MC Bus. High for memory cycles, low for I/O cycles.
–S0, –S1	I			Bus-cycle status input lines from the MC Bus. (Codings for various cycles are shown in Table 2.) Together with –CMD, used to generate card control lines (–MEMWR, –DEN, etc.).
–CMD	I			Active-low bus-cycle strobe input. Used to time data transfers during Read and Write operations.
CHRESET	I			Active-high channel reset input. The EPB2001 deasserts all active outputs a short time after CHRESET rises. POS register 0102, bit 0 is also reset by this input, deactivating –BDENBL.
MADE24	I			Active-high input indicating a 24-bit address is present on the MC Bus for the current cycle. When low, indicates that an extended address (32 bits) is present.
A0-A23	I			MC Bus address inputs. Valid while –ADL is low.
–ADL	I			Active-low address latch input. Leading edge of this signal is used to latch addresses and (optionally) chip-select lines.
–MEMRD	TP	4	24	Active-low Memory-Read strobe output. Generated as a decode of –S0=1, –S1=0, and M/–IO=1, timed by –CMD.
–MEMWR	TP	4	24	Active-low Memory-Write strobe output. Generated as a decode of –S0=0, –S1=1, and M/–IO=1, timed by –CMD.
–IORD	TP	4	24	Active-low I/O-Read strobe output. Generated as a decode of –S0=1,–S1=0, and M/–IO=0, timed by –CMD.
–IOWR	TP	4	24	Active-low I/O-Write strobe output. Generated as a decode of –S0=0,–S1=1, and M/–IO=0, timed by –CMD.
–DEN	TP	4	6	Active-low transceiver enable output. Low during data transfer portion of selected MC Bus cycles.
DT/–R	TP	4	6	Data transceiver direction control output. High during MC Bus Read cycles and low during bus Write cycles.
–CS0-7	TP	4	6	Active-low chip select outputs. Derived as a decode of addresses, M/–IO, and MADE24. May be individually latched by –ADL. Eight user-defined address ranges per output, enabled by groups of POS register bits.

* Signal Types:
I = Input
TP = Totem-Pole (Push-Pull) Output
OD = Open-Drain Output
TS = Bidirectional Tri-State I/O

Table 1. EPB2001 Pin Descriptions (Continued)

Signal	Type*	Output Drive (mA) I_{OH}	Output Drive (mA) I_{OL}	Description
POSI/O0 - POSI/O15	I/OD		6	Bidirectional POS I/O lines. Each open-drain output is driven by a user-defined POS register bit. State of POSI/O pin is reflected when corresponding POS bit is read through MC Bus port, allowing card logic status reporting when POS register contents equal 1 (default).
–WRPOS	TP	4	6	Active-low POS register Write strobe. Active for POS set-up cycle. Used to control optional POS functions external to the EPB2001.
–RDPOS	TP	4	6	Active-low POS register Read strobe. Active for POS set-up cycle. Used to control optional POS functions external to the EPB2001.
–BDENBL	OD		24	Active-low card enable output. Open-drain output reflects the state of POS register 0102, bit 0. Active low when this register bit is set to a "one." Deactivated by CHRESET.
–SETCHK	I			Active-low set channel-check input. A low pulse on this input resets POS register 0105, bit 7, and thereby activates the –CHCK output to the MC Bus.
V_{CC} (2 pins)				+5 V power supply.
V_{SS} (6 pins)				Ground.

* Signal Types:
I = Input
TP = Totem-Pole (Push-Pull) Output
OD = Open-Drain Output
TS = Bidirectional Tri-State I/O

Bus Control Section

The EPB2001 contains bus control logic, shown in the upper portion of Figure 4, which generates Read and Write signals for the internal POS registers, as well as card control signals such as -MEMWR and -IORD. This section consists of the -CDSETUP, -S0, -S1, -CMD, and M/-IO inputs on the Micro Channel side, and the -DEN, DT/-R, -IOWR, -IORD, -MEMWR, -MEMRD, -RDPOS, and -WRPOS outputs on the card side.

This section is activated by either an active -CDSETUP line together with an I/O Read or Write cycle from the processor (indicating a POS set-up configuration cycle), or a valid bus cycle (i.e., I/O Read or Write, Memory Read or Write). An active -CDSFDBK output indicates a bus cycle for the card, unless it occurs during setup. The card must have previously been enabled to activate the outputs of this bus control section. (See "POS Register Section" later in this data sheet.)

The bus control section interprets combinations of the -S0, -S1, and M/-IO signals as MC Bus cycles. The interpretation of each possible signal combination is shown in Table 2.

Table 2. Coding for MC Bus Cycles			
M/-IO	-S0	-S1	Cycle Type
0	0	0	No Operation
0	0	1	I/O Write
0	1	0	I/O Read
0	1	1	No Operation
1	0	0	No Operation
1	0	1	Memory Write
1	1	0	Memory Read

The states of the -S0, -S1, and M/-IO lines, like those of -CDSETUP and addresses A0-A23, are latched by the falling edge of -ADL for the duration of the cycle.

The -CMD signal, acting as a command strobe, times the generation of the appropriate control lines. Therefore, -MEMRD, -MEMWR, -IORD, and -IOWR are about as long as the -CMD signal.

DT/-R controls the direction of data flow through an external data transceiver. It changes after -ADL falls, and remains latched for the duration of the cycle. It is low for all Write cycles.

-DEN controls external data transceiver output enables. -DEN is active during a valid Read or Write cycle for about the same time as -CMD.

To minimize MC Bus loading, the EPB2001 data bus pins (D0-D7) should be connected to the card's buffered data bus rather than directly to the Micro Channel (see Figure 3). By locating the data bus pins behind the card bus transceiver, only one load per data pin is given to the Micro Channel. To support this operating mode, the EPB2001 -DEN output is active during -CDSETUP cycles. If, however, EPB2001 data pins are directly connected to the Micro Channel, the -DEN output *must* be externally disabled during set-up operations to ensure that there is no contention between the EPB2001 data pins and the card data transceiver.

The card setup procedure, which is part of the Power-On System Test (POST), can occur only when -CDSETUP is active on the rising edge of -ADL followed by an I/O Read or Write cycle. The falling edge of -ADL may be used to latch addresses for any type of cycle, and is used during setup to latch A0-A2 to select the correct POS registers.

The -RDPOS and -WRPOS signals control optional external POS register functions. They are active for any POS Read or Write operation accompanied by -CDSETUP. Timing for these signals is similar to that of -IOWR and -IORD.

If CHRESET is asserted, any bus cycle in progress is immediately halted, and the D0-D7 outputs of the EPB2001 chip are tri-stated. In addition, the card control lines immediately become inactive.

The -MEMRD, -MEMWR, -IORD, and -IOWR outputs have 24-mA push-pull output drivers. The -DEN, DT/-R, -RDPOS, and -WRPOS outputs have 6-mA push-pull drivers.

The EPB2001's internal transceiver (connected to D0-D7) is only enabled to the MC Bus during an I/O Read qualified by -CDSETUP.

POS Register Section

The POS registers, shown in the middle of Figure 4, are accessible through the dedicated transceiver associated with pins D0-D7 on the EPB2001. Data is transferred to the selected POS register in a Write operation while -CMD is low. The rising edge of -CMD then latches the input data into the register. Data is read from the POS registers while -CMD is low, and becomes valid at the D0-D7 pins after the -CMD falling edge. Refer to Figures 7 and 8 later in this data sheet for -CMD timing information.

The required POS registers reside in a block at I/O addresses 0100-0105 Hex for all cards. All registers are byte-wide. Locations 0100 and 0101, which are Read-only, non-volatile EPROM locations, contain the card ID. POS registers 0102-0105 are user-defined, with the exception of the following three bit locations:

Bit 0 of register 0102 This bit is used as a card enable bit. It is reset by CHRESET or by the processor writing a "zero" to this bit during a -CDSETUP cycle. When the bit is set to "zero," the EPB2001 (and card) will not respond to any normal bus cycles. Only setup Reads and Writes are allowed. When the processor sets the bit to a "one," the card is enabled. This card-enable bit may not be written to location 0102 by normal I/O Write operations. The -BDENBL signal on the card interface reflects the state of this bit for on-card use. The -BDENBL pin uses a 24-mA open-drain output structure.

Bit 7 of register 0105 This bit is used as a channel-check flag. A card reports Non-Maskable Interrupts (NMI) to the processor by asserting the -CHCK (channel check) line, which is wire-ORed to all cards. On the EPB2001, a pulse on the -SETCHK input resets this bit to a -CHCK output on the MC Bus. This bit may also be reset by a Write to 0105 with "zero" in the bit 7 location. The channel-check flag bit is set by a CHRESET or by writing a "one" to the bit 7 position.

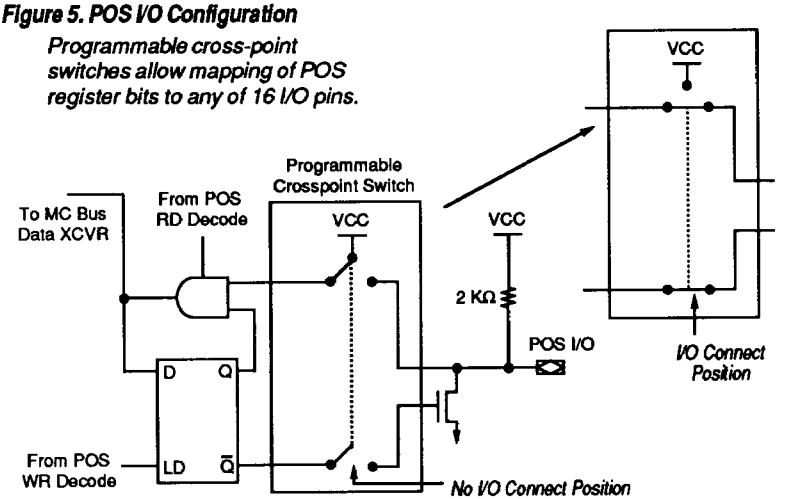
Bit 6 of register 0105 This bit may be used if bit 7 is set to "one." It flags availability of channel-check exception status in optional POS registers 0106 and 0107. (These registers, if used, are typically implemented in components such as 74LS374s.) If channel-check exception status is provided in POS registers 0106 and 0107, a "zero" will be found in the bit 6 location; if not, a "one" will be found. If bit 6 is used, one of the programmable POS I/O pins on the card interface may be used to force the appropriate value.

All remaining bits are user-definable. These bits may be used for address remapping control (i.e., software-controlled "jumpers") or simply for general input or output port functions on the card. Each POS I/O pin can be used for input or output, and may be assigned to any POS register bit. The remapping function is discussed in "Chip-Select Logic."

The connection of any of the 31 POS register bits (locations 0102-0105, exclusive 0102 bit 0) with the 16 dedicated POS I/O pins on the card interface is controlled by a user-programmable cross-point switch arrangement (see Figure 5). Each POS I/O pin has a 6-mA open-drain output structure as well as an input path. On the output side, a programmable matrix takes the output of any of the POS register bits and assigns it to any of the 16 output lines. Since the pins are open drain, if a "one" is written to a given POS register bit from the MC Bus, the associated I/O pin is not driven. The I/O pin can therefore be driven by an external signal source, and its value may be read through the corresponding POS register bit location. However, forcing a value from the POS I/O pins does not change the value in the POS register location. All POS I/O pins should either be driven by an external signal source or connected to external pull-up resistors. Resistors should have a value between 2 K and 10 K ohms.

Figure 5. POS I/O Configuration

Programmable cross-point switches allow mapping of POS register bits to any of 16 I/O pins.

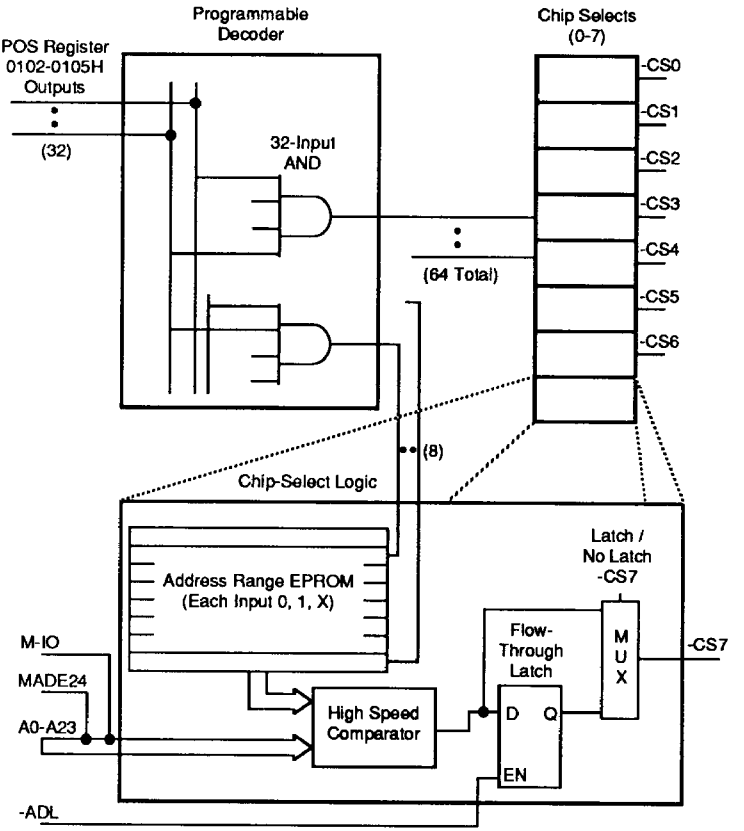


Chip-Select Logic

The chip-select logic on the EPB2001 (Figure 6) provides up to 8 user-programmable chip selects. Each chip-select output (-CS0 through -CS7) has a 6-mA push-pull driver and is active-low. Each may also have up to 8 pre-programmed address ranges over which it is active. The granularity of these chip selects may range from one location to the entire 24-bit (16-Mbyte) physical address range. Each may be defined for either memory or I/O mapping. All 24 MC Bus addresses and the M/-IO input enter the programmable chip-select logic.

Figure 6. Chip Select Logic

EPROM arrays allow programmable address range decoding.



An additional input to the programmable chip-select arrays may act as an enable for the chip selects. Typically, this input would be connected to the MADE24 MC Bus signal to qualify chip selects when 32-bit addressing is involved.

Normally, chip-select outputs are not latched, and are valid only during a valid address/M/-IO combination on the bus. Optionally, the chip-select outputs may be individually latched by user-programmable, flow-through latches enabled by -ADL. This latching causes the affected chip-select output(s) to become active a short time after -ADL has become active-low (the A0-A23 address lines and M/-IO input having stabilized well before -ADL falls). The outputs are latched on the -ADL falling edge and remain active until the next bus cycle, when -ADL goes low again. Latched/non-latched operation for each chip-select output is determined by the user when the device is programmed.

The chip-select logic is implemented as 8 distinct logic blocks, with 1 block per chip select. Each block consists of an 8-word by 52-bit programmable memory (416 bits) feeding a comparator along with the address and other required inputs. Each word corresponds to a desired chip-select active range. Any input bit may be compared for "zero," "one," or "don't care" in determining an address match. Thus, 2 bits per input (26 inputs * 2 = 52 bits) are needed to encode these possibilities.

The selection of one of the eight available chip-select ranges to be used for a particular chip-select output (corresponding to one of the eight words in each of the blocks) is determined by user-defined combinations of POS register bits. The user may define the POS register bits and bit combinations that will activate a given chip-select range. This information is then coded into a programmable decoder on the device that generates an enable for each range. The PS/2 operating system may remap address ranges during the POST setup if there is a conflict, i.e., two or more cards responding to the same address range. The address ranges are remapped by changing the POS register bits controlling the chip selects, thus enabling a new address range.

All of the unlatched, active-low chip-select outputs are available to be logically ANDed to form the -CDSFDBK signal presented to the MC Bus. MCMap allows the user to choose any combination of the eight chip selects to include for -CDSFDBK. The resulting output, acting as a "cycle acknowledge" line, signals a valid bus cycle for the card to the MC Bus. -CDSFDBK is active-low and has a 6-mA push-pull driver.

If CHRESET is active, all chip select latches are immediately cleared to the inactive (high) state.

Design Guidelines

The EPB2001 will be permanently damaged if it is operated under conditions that surpass those listed under "Absolute Maximum Ratings." This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability. The EPB2001 contains circuitry to protect device pins from high static voltages or electric fields; however, normal precautions should be taken to avoid application of any voltage higher than maximum rated voltages.

For proper operation, input and output pins must be constrained to the range GND < (V_{IN} or V_{OUT}) < V_{CC}. Unused inputs must always be tied to an appropriate logic level (either V_{CC} or GND). Each set of V_{CC} and GND pins must be connected directly at the device. Power supply decoupling capacitors of at least 0.2 µF must be connected between V_{CC} and GND. For the most effective decoupling, each V_{CC} pin should be separately decoupled to GND, directly at the device.

Latch-Up and ESD Protection

The EPB2001 input, output, and I/O pins are designed to resist electrostatic discharge (ESD) and latch-up damage. Each device pin will withstand voltage energy levels exceeding those specified by MIL STD 883C. Pins will not latch up for input voltages between -1 V and V_{CC} + 1 V with currents up to 100 mA. During transitions the inputs may undershoot to -2.0 V for periods less than 20 ns. Additionally, the programming pin is designed to resist latch-up to the 13.5 V maximum device limit.

Device Erasure

The EPB2001 begins to erase when exposed to light wavelengths shorter than 4000 Å. Since fluorescent lighting and sunlight fall into this range, opaque labels should be placed over the EPB2001 window to ensure long-term reliability. (Plastic packaged devices are, of course, protected). Constant exposure to room-level fluorescent lighting could erase an EPB2001 in about three years, and direct sunlight could erase it in about one week.

To ensure proper erasure, the EPB2001 must be exposed to ultraviolet light with a wavelength of 2537 Å. The integrated erasure dose should be a minimum of 30 Wsec/cm². The erasure time with this dosage is about 1 hour using an ultraviolet lamp with a 12,000 µW/cm² power rating. During erasure, the EPB2001 should be placed within 1 inch of the lamp tubes. The maximum integrated exposure dose for an EPB2001 is 7,000 Wsec/cm². This dose is equivalent to 1 week at 12,000 µW/cm². Exposure of the windowed EPB2001 to high-intensity ultraviolet light for long periods of time may cause permanent damage.

The EPB2001 may be erased and reprogrammed as often as necessary within the limits described and using the recommended procedure.

Design Security

The EPB2001 contains a programmable Security Bit that controls access to programmed information. If this Security Bit is used, the custom pattern in the device is secured from external interrogation and possible reverse engineering. The Security Bit, which is set by the user during design entry, may be erased with ultraviolet light as described in "Device Erasure."

MCMap Development System

Altera provides MCMap, a PC-based design development system, to support efficient design and use of the EPB2001. It is an interactive, table-driven software package. The designer is prompted for information concerning the programmable portions of a design: card ID, chip-select ranges, POS register bit combinations used as enables, etc. Real-time error checking reports any errors as they are entered. When entry is complete, MCMap compiles a JEDEC programming file for the EPB2001 in seconds. MCMap also generates an Adapter Description File (ADF) for address decodes controlled by POS register bits.

The JEDEC file may then be submitted to LogicMap software to program the EPB2001 on the PC. Altera's LP4 programming card, PLE3-12A Master Programming Unit, and PLEJ2001 Programming Adapter are the required hardware. The PLEJ2001 provides an interface between the LP4 and PLE3-12A and the 84-lead EPB2001 chip carrier package. For more information concerning Development Systems, please contact Altera's Marketing Department at (408) 984-2805 ext. 101.

The recommended PC system requirements for Altera's MCMap software and hardware are:

- ❒ IBM XT, AT, or compatible PC
- ❒ EGA,VGA, or Hercules Graphics Adapter
- ❒ 640 KBytes RAM
- ❒ 10-MByte hard disk and 5.25 inch floppy drive
- ❒ DOS Version 3.3 or a later version

Ordering Information

Development Systems

Part Number	Description
PLDS-MCMAP	Stand-alone Programmable Logic Development System. Contains MCMap Programmable Logic Development software and documentation, PL-ASAP programming hardware, PLEJ2001 adapter, and sample EPB2001JC.
PLS-MCKIT	Software only from PLDS-MCMAP system. Also contains PLEJ2001 adapter and sample EPB2001JC.

Components

Part Number	Description
EPB2001JC	Windowed ceramic J-lead chip carrier
EPB2001LC	One-time-programmable plastic J-lead chip carrier

Reference

Altera's Applications Department can be reached at (408) 984-2805 ext. 102 for technical support. Technical information on the EPB2001 is available in the following aritcles provided in the ***Applications Handbook***:

Application Note 14 (IBM PS/2 Add-On Card Interfacing)

Application Note 15 (IBM PS/2 Add-On Card Software Design)

Application Brief 72 (IBM PS/2 Master and Slave Adapter Design)

The following magazine article also contains information about the EPB2001:

"Hands-on Experience Paves the Way for Future MCA Designs." *EDN* (November 9, 1989), p. 233.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND	-2.0	7.0	V
V_{PP}	Programming supply voltage	*See Note (2)*	-2.0	14.0	V
V_I	DC input voltage	*See Note (2)*	-2.0	V_{CC} + 1.0	V
I_{MAX}	DC V_{CC} or GND current		-500	+500	mA
I_{OUT}	DC output current, per pin		-50	+50	mA
P_D	Power dissipation			1000	mW
T_{STG}	Storage temperature	No bias	-65	+150	° C
T_{AMB}	Ambient temperature	Under bias	-65	+135	° C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
T_A	Operating temperature		0	+70	° C
t_R	Input rise time			250	ns
t_F	Input fall time			250	ns

DC Operating Characteristics

V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	High level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	Low level input voltage		-0.3		0.8	V
V_{OH}	High level TTL output voltage	See Tables above	2.4			V
V_{OL}	Low level output voltage	See Tables above			0.50	V
I_I	Input leakage current	V_I = V_{CC} or GND	-10		+10	µA
I_{OZ}	Output high-Z leakage current	V_O= V_{CC} or GND	-10		+10	µA
I_{CC}	V_{CC} supply current (standby)	V_I = V_{CC} or GND, No load		20	30	mA

Capacitance

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input capacitance (except –CDSETUP) *See Note (3)*	V_{OUT} = 0 V, f = 1.0 MHz *See Note (4)*		15	pF
$C_{I/O}$	I/O capacitance			15	pF
C_{OD}	Output capacitance			15	pF

AC Operating Characteristics

V_{CC} = 5 V ± 5%, T_A = 0° C to 70° C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T1	–ADL width		40			ns
T2	–ADL high to –S0, –S1 high		25			ns
T3	–S0, –S1 low to –ADL low		12			ns
T4	–ADL low to –CMD low		40			ns
T5	MADE24, M/–IO, A0-A23 valid to –S0, –S1 low		10			ns
T6	–S0, –S1 low to –CMD low		55			ns
T7	–CMD low to –S0, –S1 high		30			ns
T8	–CMD width		90			ns
T9	– CMD low to –MEMRD, –MEMWR, –IORD, –IOWR, –RDPOS, –WRPOS low				18	ns
T10	– CMD high to –MEMRD, –MEMWR, –IORD, –IOWR, –RDPOS, –WRPOS high				18	ns
T11	–ADL low to DT/–R high				20	ns
T12	–ADL low to DT/–R low				20	ns
T13	–CMD low to –DEN low				15	ns
T14	–CMD high to –DEN high				15	ns
T15	DT/–R low to –DEN low		20			ns
T16	–ADL low to latched –CS0-7 low				20	ns
T17	MADE24, M/–IO, A0-A23 valid to –ADL low		45			ns
T18	MADE24, M/–IO, A0-A23 hold from –ADL high		25			ns
T19	MADE24, M/–IO, A0-A23 valid to –CS0-7 low				25	ns
T20	MADE24, M/–IO, A0-A23 valid to –CDSFDBK low				40	ns
T21	MADE24, M/–IO, A0-A23 invalid to –CDSFDBK high				45	ns
T22	–CMD low to D0-D7 valid (Read)				60	ns
T23	–CMD high to D0-D7 high-Z				40	ns
T24	D0-D7 valid to –CMD low (Write)		0			ns
T25	D0-D7 hold from –CMD high (Write)		30			ns
T26	POS I/O input valid to POS data valid				175	ns
T27	–CMD low to POSI/O valid				130	ns
T28	CHRESET width		100			ns
T29	–SETCHCK low to –CHK low				30	ns
T30	CHRESET high to –DEN , –MEMWR , –MEMRD, –IOWR, –IORD high				30	ns
T31	CHRESET high to D0-D7 high-Z				30	ns
T32	CHRESET high to –CHCK, –BDENBL high-Z				30	ns

AC Output Capacitance Loadings

Output Pins	Load Capacitance
–CS0-7, –DEN, POSI/O0-15, –WRPOS, –RDPOS	50 pF
–BDENBL, –MEMRD, –MEMWR, –IORD, –IOWR	200 pF
–CDSFDBK, –CHCK, D0-D7	240 pF

Notes to tables:
(1) Typical values are for $T_A = 25°$ C and $V_{CC} = 5$ V.
(2) Minimum DC input is -0.3 V. During transitions, inputs may undershoot to -2.0 V for periods less than 20 ns.
(3) Pin 39 (high-voltage pin during programming) has capacitance of 35 pF max.
(4) Capacitances measured at 25° C. Sample tested only.

Figure 7. EPB2001 Waveforms

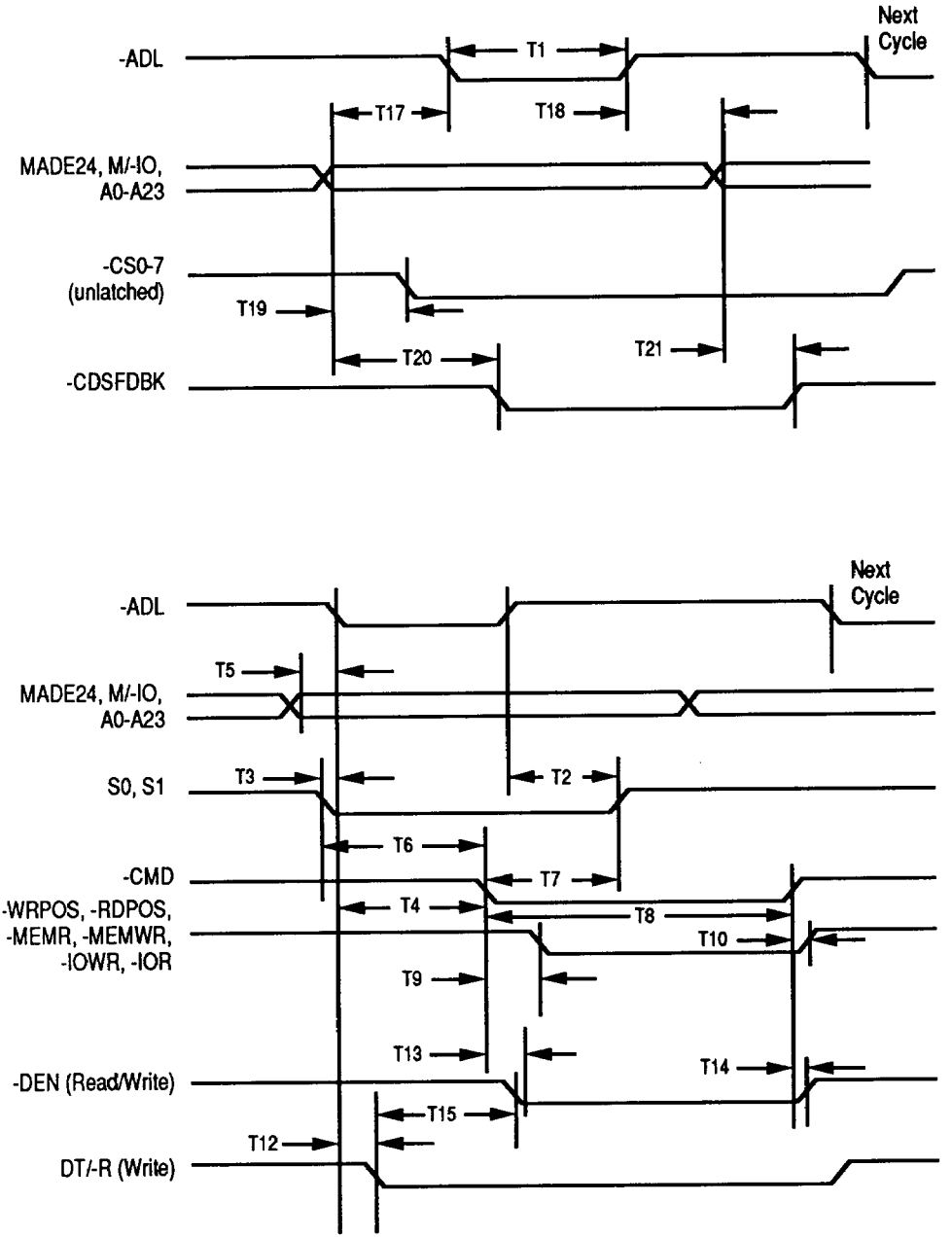
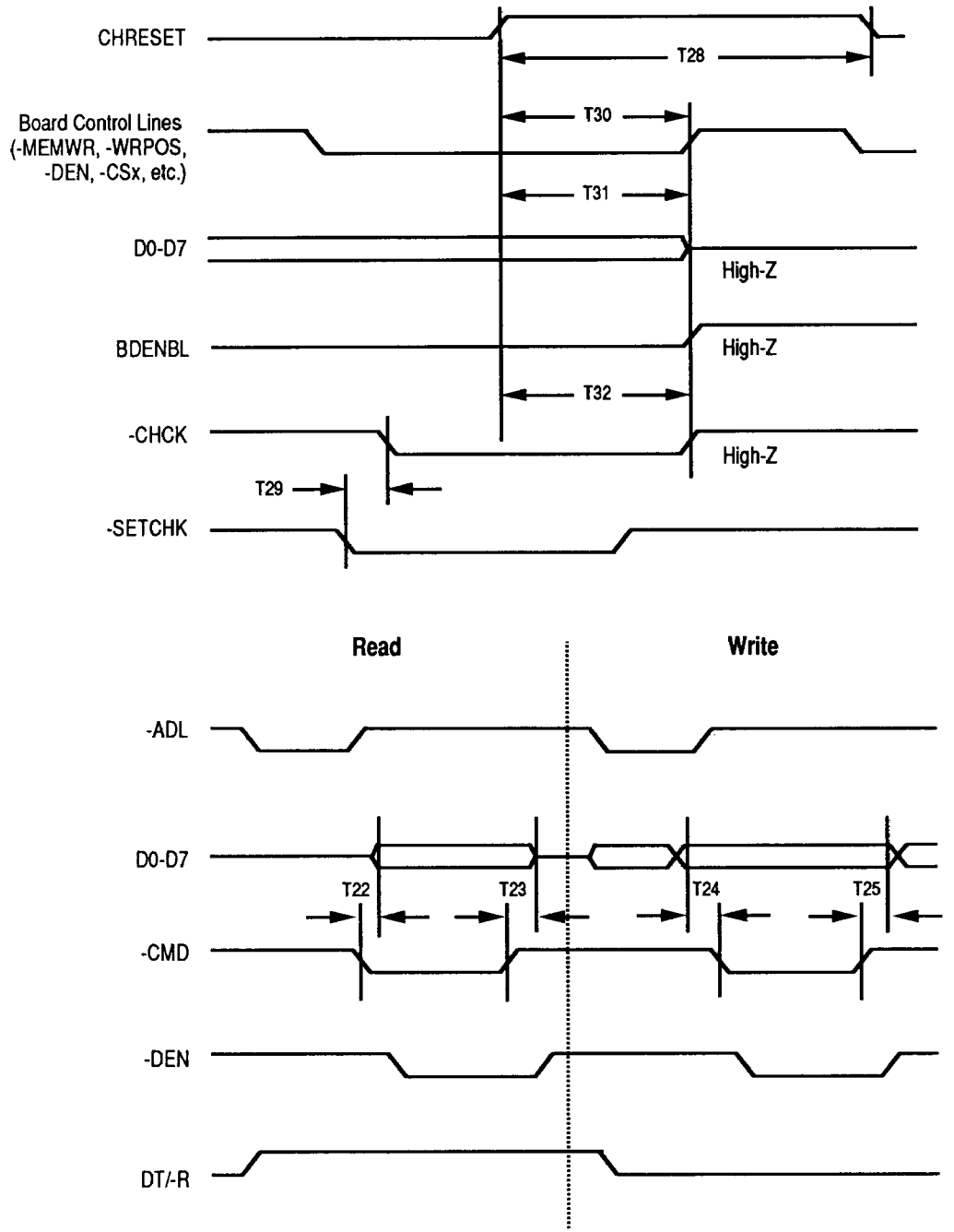


Figure 8. EPB2001 Waveforms (Continued)



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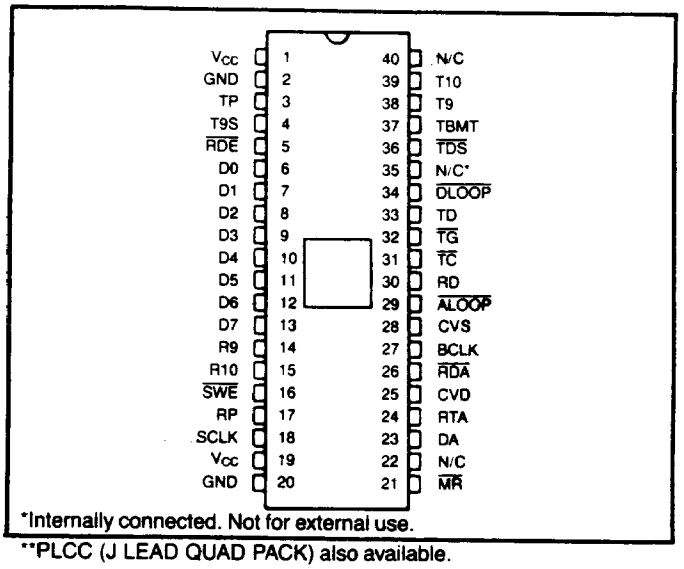
COM90C84
PRELIMINARY

IBM® 3274/3276 Compatible COAX Receiver/Transmitter

FEATURES

- ☐ Conforms to the IBM® 3270 Interface Display System Standard
- ☐ Transmits and Receives Manchester II Code
- ☐ Detects and Generates Line Quiesce, Code Violation, Sync, Parity, and Ending Sequence (Mini Code Violation)
- ☐ Multi Byte or Single Byte Transfers
- ☐ Double Buffer Receiver and Transmitter
- ☐ Separate Data and Status Select
- ☐ Operates at 2.3587 MHz
- ☐ TTL Compatible Inputs and Outputs
- ☐ **Low Power 1.6 Micron CMOS Technology**

PIN CONFIGURATION**



*Internally connected. Not for external use.

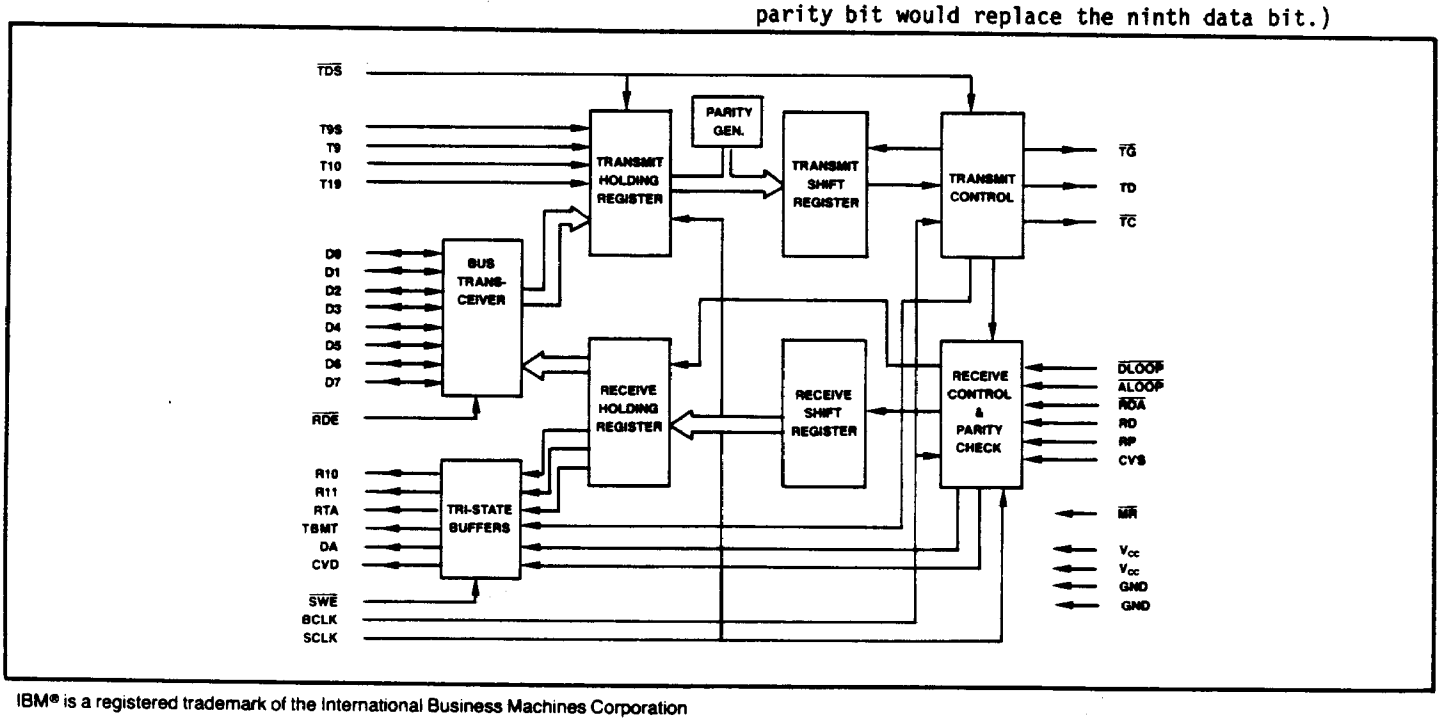
**PLCC (J LEAD QUAD PACK) also available.

GENERAL DESCRIPTION

The COM90C84 COAX Receiver/Transmitter is a CMOS device that performs the communications interface between the IBM 3270 family control units and terminals units. The receiver and transmitter sections of the COM90C84 are separate and may be used independently of one another.

The COM90C84 generates and detects the line quiesce, code violation, parity, and mini code violation bit patterns.

The on-chip parity logic is capable of generating and checking either even or odd parity for the entire 10 bit data word. In addition, parity may be generated for the least significant 8 bits of the data word (this parity bit would replace the ninth data bit.)



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