Preliminary

Am7984A

FDDI ENcoder DECoder (ENDEC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Implements 4B/5B encoding/decoding as specified by the ANSI X3T9.5 Fiber Distributed Data Interface (FDDI) standard**
- **100 Mbps, 125 MBaud serial data-rate**
- **Byte-clock and nibble-clock output**
- **Selectable loopback and repeat modes**
- **Elasticity Buffer**
- **Smoother**
- **Repeat filter**
- **Single +5-V supply**

GENERAL DESCRIPTION

The Am7984A ENDEC (ENcoder DECoder) performs 4B/5B encoding on data to be transmitted from an FDDI station. The chip also performs 4B/5B decoding of received data. It has an elasticity buffer which allows a station to compensate for small differences between receive and transmit clock frequencies. There is a smoother present in the receive path to ensure with a very high probability that a minimum of 6 bytes of IDLE are received before a frame. It also decodes line state information from data that has been received from the network media, and enables line states to be forced onto the media for connection management purposes. A repeat filter replaces any invalid symbols with other symbols that are determined by the repeat filter state machine. The ENDEC interfaces to the FORMAC through two 11-bit transmit buses and one 11-bit receive bus. Data is serially transferred to an optical transmitter by a differential driver. The ENDEC interfaces to the Node Processor (NP) through a 3-bit bus and associated handshake lines. It also supplies the master clock for the network interface of the station.

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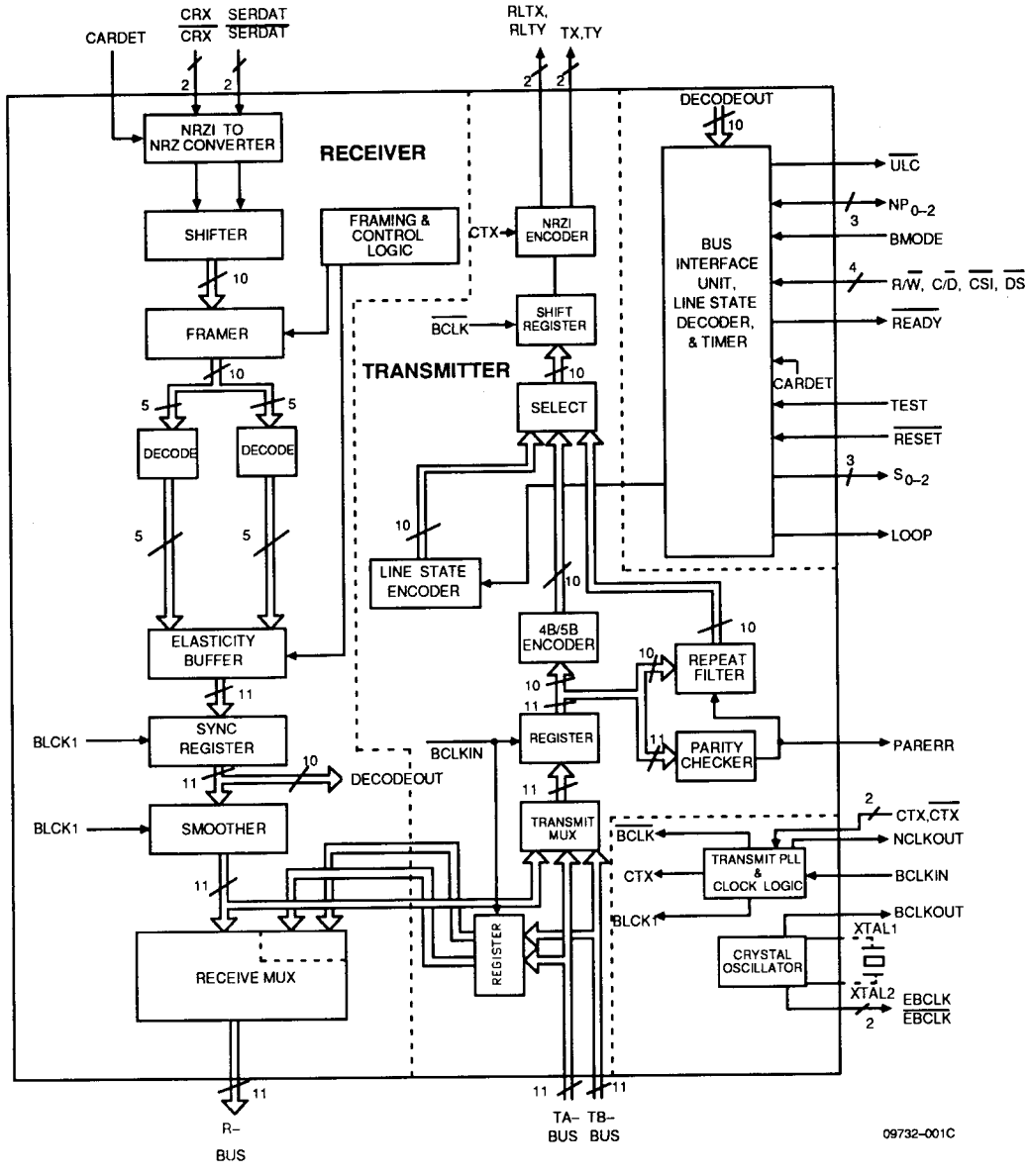
BLOCK DIAGRAM



NOTE

The word "frame" is used in the SUPERNET data sheets to describe two different groups of information.

1) One group is passed over the network media and is structured as follows:

Frame Preamble	Start Delimiter	Frame Control	Destination Address	Source Address	Information	Frame Check Sequence	End Delimiter	Frame Status

2) The others are stored in buffer memory and structured as follows:

A) Transmit frame

Descriptor	Frame Control	Destination Address	Source Address	Information	Frame Check Sequence	Pointer

B) Receive frame

Descriptor	Frame Control	Destination Address	Source Address	Information	Frame Check Sequence

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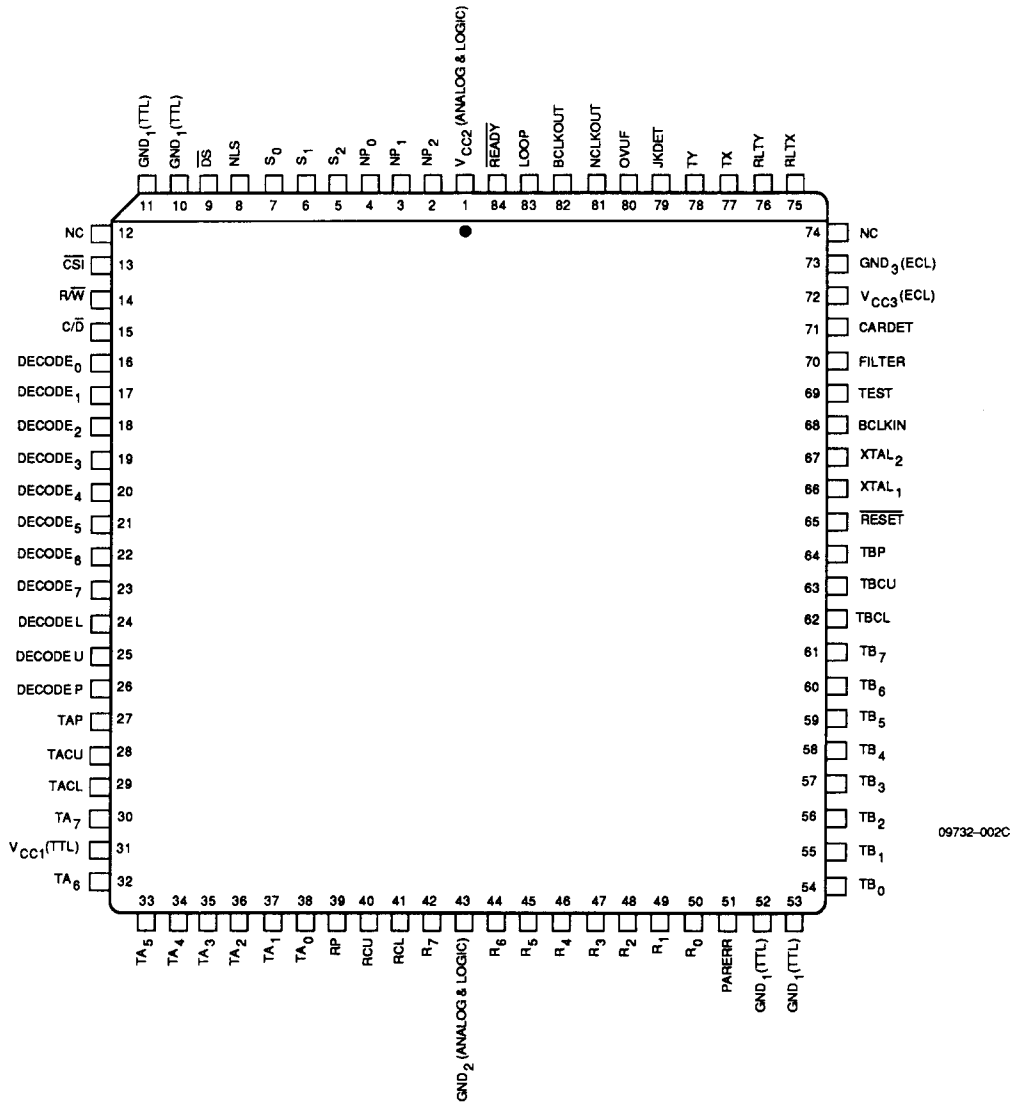
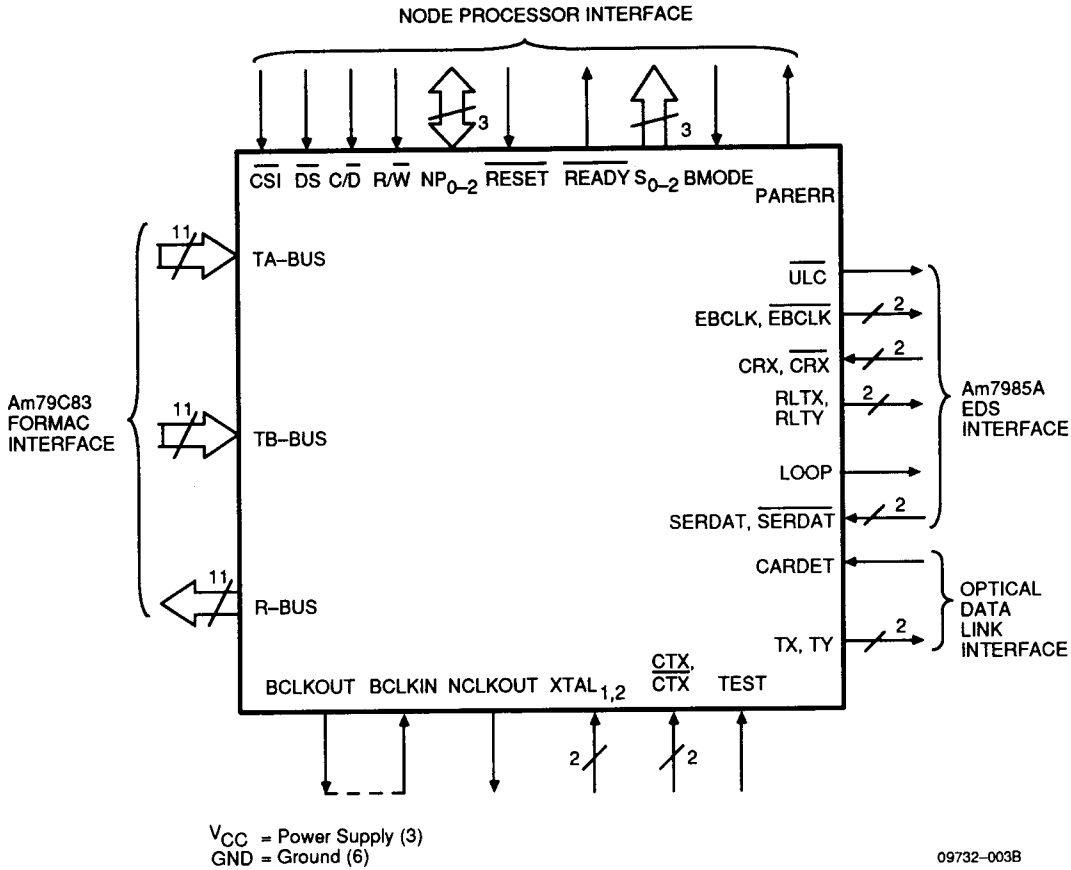
CONNECTION DIAGRAM (Top View)
PL084



09732-002C

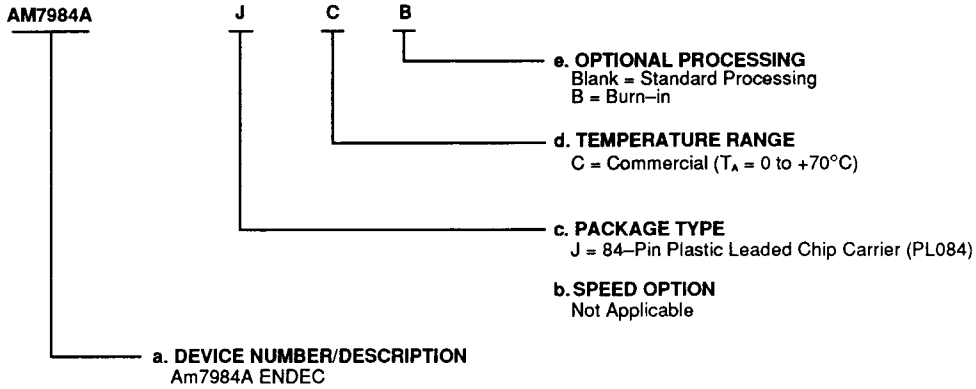
LOGIC SYMBOL



ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM7984A	JC, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Parallel Buses

This section describes the pins used to interface the Am7984A ENDEC with a FORMAC or another ENDEC. All of the signals are synchronous with BCLKIN. There are two transmit buses and one receive bus. The higher order nibble is transmitted first.

R_{0-7}
Receive Bus (TTL Outputs)

The R-bus output sends information being decoded from the serial receive input of the ENDEC to either the FORMAC or the transmit bus of another ENDEC in the station.

RCL
Receive Control Lower (TTL Output; Active HIGH)

The RCL signal is used to identify the type of information being presented on the lower nibble (R_{0-3}) of the ENDEC receive bus output. If RCL is HIGH, then the lower nibble is a network control character; if LOW, the lower nibble is data.

RCU
Receive Control Upper (TTL Output; Active HIGH)

The RCU signal is used to identify the type of information being presented on the upper nibble (R_{4-7}) of the ENDEC receive bus output. If RCU is HIGH, then the upper nibble is a network control character; if LOW, the upper nibble is data.

RP
Receive Bus Parity (TTL Output; Active HIGH)

The RP signal ensures odd parity on RCU, RCL, and lines R_{0-7} of the ENDEC receive bus. If the number of "1s" on these pins is odd, then RP will be logic "0".

TA_{0-7}
Transmit Bus A (TTL Inputs)

This is one of two input buses used to accept transmit data and control information from either the FORMAC or the other ENDEC (if one exists) at the station.

TACL
"Transmit Bus A" Control Lower (TTL Input; Active HIGH)

The TACL signal is used to identify the type of information being presented on the lower nibble (TA_{0-3}) of transmit bus A. When TACL is HIGH, the lower nibble is interpreted as a network control character; otherwise, it is interpreted as data.

TACU
"Transmit Bus A" Control Upper (TTL Input; Active HIGH)

The TACU pin is similar in function to TACL except that it identifies the type of information being presented on the upper nibble (TA_{4-7}) of transmit bus A.

TAP
"Transmit Bus A" Parity (TTL Input; Active HIGH)

The TAP signal ensures odd parity of signals TA_{0-7}, TACL, and TACU. If the number of logic "1s" on these pins is odd, then TAP will be logic "0". Data with a parity error will be processed by the repeat filter state machine inside the ENDEC.

TB_{0-7}
"Transmit Bus B" (TTL Inputs)

This is one of two input buses used to accept transmit data and control characters from the FORMAC or the other ENDEC (if one exists) in the station.

TBCL
"Transmit Bus B" Control Lower (TTL Input; Active HIGH)

TBCL is similar in function as TACL except that it identifies the type of information being presented on the lower nibble of transmit bus B. If TBCL is HIGH, the nibble TB_{0-3} is a control character.

TBCU
"Transmit Bus B" Control Upper (TTL Input; Active HIGH)

The TBCU signal provides an identical function as TBCL for the upper nibble of transmit bus B. If TBCU is HIGH, then the nibble TB_{4-7} is a control character.

TBP
"Transmit Bus B" Parity (TTL Input; Active HIGH)

The TBP signal ensures odd parity of signals TB_{0-7}, TBCL, and TBCU (see pin TAP). If the number of logic "1s" on these pins is odd, then TBP will be logic "0". Data with a parity error will be processed by the repeat filter inside the Am7984A.

EDS Interface

The following section describes the pins which connect to Am7985A EDS.

CRX, $\overline{CRX}$

Clock Receive+, Clock Receive- (Differential CML/ECL Input)

The bit rate clock derived from the received serial data (RX, RY or RLTX, RLTY) is sent to the ENDEC from the receive PLL in the EDS using CRX, $\overline{CRX}$.

EBCLK, $\overline{EBCLK}$

ECL Byteclock+, ECL Byteclock- (Differential Pseudo ECL Output)

The crystal oscillator on the ENDEC generates the byte rate (12.5 MHz) frequency reference for use by the EDS. This signal is synchronous to BCLKOUT.

LOOP

(Pseudo-ECL Output; Active HIGH)

The LOOP signal is active when the ENDEC is in loop-back mode. When the LOOP pin is active, it causes the RLTX, RLTY outputs of the ENDEC to be looped back through the RLTX, RLTY inputs of the EDS.

RLTX, RLTY

Receive Loop Transmit+, Receive Loop Transmit– (Differential Pseudo-ECL Outputs)

RLTX, RLTY are an alternate set of serial outputs from the ENDEC, used to loop back through the EDS. They contain the same data as TX, TY except when the ENDEC is in loopback mode.

SERDAT, $\overline{SERDAT}$

Serial Data+, Serial Data– (Differential CML/ECL Input)

SERDAT, $\overline{SERDAT}$ are NRZI data coming from the EDS. They are synchronized with the rising edge of CRX.

$\overline{ULC}$

Use Local Clock (Single Ended Pseudo ECL Output; Active LOW)

The $\overline{ULC}$ signal is active whenever CARDET goes inactive, or when in Quiet Line State (QLS). $\overline{ULC}$ is also controlled by the noise timer inside the ENDEC. The noise timer forces $\overline{ULC}$ to be active for a period of 128 BCLK cycles (10.24 µsec @ 100 Mbps) after NLS has been active for at least one byteclock. After 128 BCLK cycles, the noise timer releases $\overline{ULC}$ for the next 128 BCLK cycles. After the end of this second 128 BCLK cycle interval, if NLS is still active, then the noise timer becomes active again, forcing $\overline{ULC}$ active.

Node Processor (NP) Interface

C/$\overline{D}$

Command/$\overline{Data}$ (TTL Input)

When C/$\overline{D}$ is HIGH, the data on the NP_{0-2} (NP_{0-2}) is written into the 3-bit pointer register in the ENDEC. When C/$\overline{D}$ is LOW, data on NP_{0-2} is written into one of the control registers or read from one of the control/status registers inside the ENDEC, as pointed to by the pointer register.

$\overline{CSI}$

$\overline{Chip\ Select}$ (TTL Input; Active LOW)

$\overline{CSI}$, when LOW, indicates that the NP has selected the ENDEC to write into the control registers inside the ENDEC or to read either the control registers or the line state status register. It should stay LOW until the $\overline{READY}$ signal from the ENDEC goes LOW (in asynchronous mode).

$\overline{DS}$

$\overline{Data\ Strobe}$ (TTL Input; Active LOW)

The $\overline{DS}$ is used for defining the presence of data on the NP_{0-2}. $\overline{DS}$ is LOW whenever the data to be written is valid in the case of write operation, or when the NP is ready to read in the case of a read operation. It should stay LOW until the $\overline{READY}$ signal from the ENDEC goes active (LOW).

NP_{0-2}

Node Processor Bus (TTL Input/Output; Three State)

Data from the NP_{0-2} is written into the control register of the ENDEC when $\overline{CSI}$, $\overline{DS}$, and R/$\overline{W}$ are all LOW. The contents of any of the control registers or of the line state status register inside the ENDEC may be read onto the NP_{0-2} when $\overline{CSI}$ and $\overline{DS}$ are LOW and R/$\overline{W}$ is HIGH. The NP operates synchronously with the ENDEC when the BMODE pin is HIGH, or operates asynchronously if the BMODE pin is LOW. The NP_{0-2} is three-stated whenever either $\overline{CSI}$ or $\overline{DS}$ is HIGH.

PARERR

Parity Error (TTL Output; Active HIGH)

PARERR indicates that there is a parity error on data which is coming in from the selected transmit bus.

$\overline{READY}$

$\overline{READY}$ (TTL Output; Open Collector, Active LOW)

The $\overline{READY}$ signal is a handshake signal for use with an asynchronous NP. When the BMODE pin is HIGH, as in the case of a synchronous NP, $\overline{READY}$ is also HIGH and

is typically not used in the system. When BMODE is LOW, the NP runs asynchronous to BCLKIN and the ENDEC indicates that data is being acted upon by bringing $\overline{\text{READY}}$ LOW. During a write operation, $\overline{\text{READY}}$ goes LOW after data from the NP is clocked into the ENDEC. In the case of a read operation, $\overline{\text{READY}}$ goes LOW after the ENDEC supplies valid data on the NP_{0-2}. Typically, the ENDEC takes between two and three BCLKIN cycles to force $\overline{\text{READY}}$ LOW after NP asserts $\overline{\text{DS}}$. $\overline{\text{READY}}$ stays LOW as long as $\overline{\text{DS}}$ and $\overline{\text{CSI}}$ stay LOW.

$\overline{\text{RESET}}$

$\overline{\text{Reset}}$ (TTL Input; Active LOW)

This is a hardware reset that initializes the internal logic in the ENDEC. Reset can be activated asynchronously with BCLKIN but must be held LOW for at least three BCLKIN cycles.

R/$\overline{\text{W}}$

Read/$\overline{\text{Write}}$ (TTL Input)

When R/$\overline{\text{W}}$ is HIGH, the NP reads data from one of the control/status registers. When R/$\overline{\text{W}}$ is LOW, the NP writes data into one of the control registers or the pointer register.

S_{0-2}

Line Status (TTL Outputs)

These signals indicate the line states of the medium as seen at the R_{0-7}, RCL, RCU, and RP outputs of the ENDEC. The meaning of the status lines is detailed in Table 2.

BMODE

Bus Mode (TTL Input)

The BMODE pin is strapped HIGH for synchronous operation of the NP_{0-2} or LOW for asynchronous operation of the NP_{0-2}.

Clock Signals

BCLKIN

Byte Clock (TTL Input)

BCLKIN is the main clock that runs the ENDEC. It must be driven from a TTL clock source such as the chip's own BCLKOUT pin or from that of another nearby ENDEC. The transmit PLL uses BCLKIN as a reference to generate the transmit bit clock. The transmit bit clock is ten times the frequency of BCLKIN.

BCLKOUT

Byte Clock (TTL Output)

BCLKOUT is derived from an internal oscillator which uses an external crystal operating in its fundamental mode of operation. It is the main clock running the station. All SUPERNET devices use this clock. When there are two ENDECs in a station, as in a dual attachment station (DAS), only one clock source is used; BCLKIN of all ENDECs in the station must be driven from the same clock source.

NCLKOUT

Nibble Clock (TTL Output)

NCLKOUT is derived from the internal PLL and is twice the frequency of BCLKIN and synchronous to BCLKIN.

$XTAL_1$, $XTAL_2$

Crystal 1, Crystal 2 (Inputs)

These two crystal inputs connect to an oscillator which operates at the fundamental frequency of a parallel resonant crystal. During normal operation, the byte rate is set by the crystal frequency. If these pins are not used, ground $XTAL_1$. If an external TTL clock source is used to drive $XTAL_1$, then $XTAL_2$ should be grounded.

Optical Data Link Interface

CARDET

Carrier Detect (Pseudo-ECL Input; Active HIGH)

The CARDET signal is received from the optical receiver. When HIGH, it indicates the presence of data in the fiber. When LOW, this signal is used to force a quiet line state (QLS) in the line state status register and quiet into the decoder. CARDET is ignored in loopback mode.

TX, TY

Transmit+, Transmit- (Differential Pseudo-ECL Outputs)

These output pins provide a differential ECL NRZI output from the ENDEC. These ECL signals drive the optical transmitter input. They are referenced to +5 volts and are capable of driving lines which are terminated with 50 ohms resistance connected to V_{CC} - 2 volts.

Test Signals

TEST

Test (Input; Active HIGH)

When the TEST pin is connected to V_{CC}, the internal PLL is disabled and instead an external bit clock is input through the CTX, $\overline{\text{CTX}}$ pins. When in TEST mode, we recommend that an external clock source provide BCLKIN. The TEST pin must be grounded for normal operation.

CTX $\overline{\text{CTX}}$

Clock Test+, Clock Test- (Differential Pseudo-ECL Inputs)

CTX, $\overline{\text{CTX}}$ are used during outgoing inspection, when the TEST pin is tied to V_{CC}. They are used to supply the bit clock to the ENDEC.

Power Supply

GND_1, GND_2, GND_3
Ground Pins

GND_1 is the TTL ground, GND_2 is the logic and analog ground, and GND_3 is the ECL ground.

V_{CC1}, V_{CC2}, V_{CC3}
Power Supply

These are +5.0-volt nominal power supply pins. V_{CC1} powers TTL, V_{CC2} powers logic and analog, and V_{CC3} powers ECL circuitry.

FUNCTIONAL DESCRIPTION

User-Accessible Resources

Programmable Resources

The ENDEC can be programmed for various modes of operation by the NP using NP data and control status lines. There are four control registers and one status register, each 3 bits wide, inside the ENDEC. Data is written into the control register and read from control/status registers using the NP_{0-2}. The NP interface is used to configure the ENDEC in the following ways:

1) A string of quiet symbols, halt symbols, master line states (halt- quiet symbol pairs), idle-quiet symbol pairs, idle symbols, or a JK pair followed by idle symbols may be forced onto the network by the ENDEC by setting the appropriate bits in the control register CR_0 (see Table 3-2);
2) The repeat filter state machine may be enabled by programming control register CR_0 (see Table 3-2). It is disabled by resetting the ENDEC;
3) Either the TA- or TB-bus may be selected for transmission onto the network by programming register CR_1;
4) Repeat, short loopback, or through mode for the ENDEC, or loopback for the ENDEC/EDS combination may be selected by programming register CR_1;
5) By programming the PARCON bit in register CR_2, parity error may be converted into halt followed by idle symbols by the repeat filter state machine;
6) The ENDEC can be reset using control register CR_2;
7) Information stored in control and status registers may be read;
8) Even/Odd parity mode of operation can be chosen by using control register CR_2.
9) Smoother can be reset through use of control register CR_3 and smoother extension status can be read through control register CR_3.

Hardwired Resources

The following are the hardwired resources in the ENDEC:

1) The TEST pin;
2) The presence of various line states in the decoded data stream is indicated by the ENDEC on pins S_{0-2};
3) The $\overline{\text{RESET}}$ pin operates asynchronously and resets the internal logic of the ENDEC;
4) The CARDET pin may be used to force a quiet line state (QLS); (logic "1"s will also be forced onto the R-bus.)
5) The PARERR pin indicates the occurrence of parity errors in data to be sent out from the transmit bus;
6) The nibble clock is brought out on pin NCLKOUT for possible use by the system;
7) The main clock for the station, running at the byte rate, may be generated by the crystal oscillator inside the ENDEC and is available for other chips in the station on the BCLKOUT pin. The BCLKIN pin accepts this byte-rate clock, distributes it to the internal logic associated with data transmission, and uses it to generate a bit-rate clock,
8) The $\overline{\text{ULC}}$ pin is used to disable the input data going to the EDS and change the frequency reference for the receive PLL inside the EDS to the transmit byte clock (EBCLK or $XTAL_1$);
9) The BMODE pin can be used to select the asynchronous or synchronous mode of operation for the NP bus.

Block Diagram Description

Transmitter

The transmitter section is divided into eight sub-blocks: transmit mux, register, 4B/5B encoder, select, shift register, NRZI encoder, repeat filter, and parity checker.

The transmit mux is used to select the source of data to be transmitted. The source could be either of the two transmit buses (TA or TB), or the output of the smoother. The selected data is clocked into the register on the rising edge of BCLKIN. The data then goes simultaneously to the encoder, parity checker, and repeat filter. The register is forced to a quiet byte (QQ) during reset.

The parity checker circuit detects the presence of parity error in data coming from the transmit bus. If an error is found, this circuit flags the error to the repeat filter and drives the PARERR pin HIGH.

The purpose of the repeat filter is to detect the presence of invalid symbols such as halt, quiet, violation, isolated J or K, or parity error, and to force four symbols of halt followed by a string of idles onto the medium once any of these symbols is detected. The repeat filter implements the state machine shown in Figure 1.

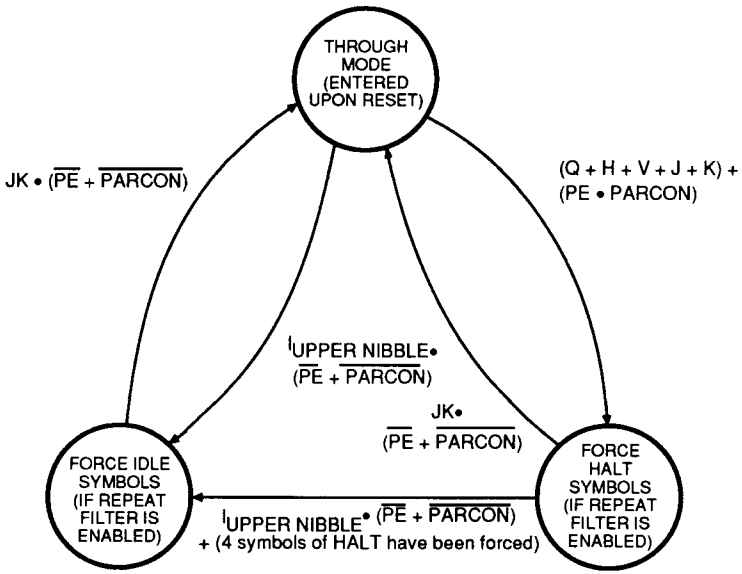
The 4B/5B encoder performs the data conversion (binary to 4B/5B) for both the upper and lower nibbles of the register contents as shown in Table 1A.

The select circuit is used to choose symbols from either the 4B/5B encoder, the line state encoder, or the repeat filter for transmission. The select circuit chooses the encoder output only when either the control register (CR_0) enables the repeat filter and the repeat filter does not force any control symbols, or when the repeat filter is

not enabled and the line state encoder is not forcing any line state symbols.

The 10-bit parallel data from select is serialized using the shift register. This is a 10-bit parallel-to-serial shift register which is parallel loaded with the output of select on the falling edge of BCLKIN and shifted out using the transmit bit clock. The most significant bit of the upper nibble is transmitted first.

The output from the shift register is clocked into the NRZI encoder using the bit clock. Its output is logic "0" whenever the ENDEC is reset or when quiet symbols are forced onto the network. In loopback and short loop-back modes, TX is held at logic "0" (RLTX and RLTY remain unaffected).



Abbreviations:

PE:	Parity Error
PARCON:	Parity Error Convert (CR2, bit 0)
Q:	Quiet Symbol
H:	Halt Symbol
V:	Violation (any bit pattern not defined in Table 1)
J,K:	Start Delimiters
+:	Logical "OR" function
•:	Logical "AND" function

09732-004B

Figure 1. Repeat Filter State Machine

Table 1A. FDDI Encoding Table

Transmit Bus C	Transmit Bus Data	NRZ CODE Symbol	NRZ CODE 12345
0	0000	0	11110
0	0001	1	01001
0	0010	2	10100
0	0011	3	10101
0	0100	4	01010
0	0101	5	01011
0	0110	6	01110
0	0111	7	01111
0	1000	8	10010
0	1001	9	10011
0	1010	A	10110
0	1011	B	10111
0	1100	C	11010
0	1101	D	11011
0	1110	E	11100
0	1111	F	11101
1	0100	H	00100
1	0111	I	11111
1	1100	J	11000
1	0011	K	10001
1	0000	Q	00000
1	0001	R	00111
1	1001	S	11001
1	1101	T	01101

Notes:

1) Any unused combination including H, Q, V, and isolated J, Ks are treated according to Figure 1.
2) Order of NRZI code transmission: 1, 2, 3, 4, 5.
3) When the ENDEC is in the unfiltered encoded mode, these unused combinations are encoded as shown.

1	0010	00000 (Q)
1	0101	00101 (V)
1	0110	01000 (H)
1	1000	00110 (V)
1	1010	11000 (J)
1	1011	11001 (S)
1	1110	11000 (J)
1	1111	11111 (I)

Symbol Notation:

0,1....F = Hexadecimal digits
H, I, J, K, Q, R, S, T = Network control symbols
H = Halt symbol
I = Idle symbol
J = First-Half Start Delimiter
K = Second-Half Start Delimiter
Q = Quiet symbol
R = Reset
S = Set
T = Terminate

Table 1B. FDDI Decoding Table

NRZ CODE	SYMBOL	DECODER OUTPUT C	DECODER OUTPUT DATA
11110	0	0	0000
01001	1	0	0001
10100	2	0	0010
10101	3	0	0011
01010	4	0	0100
01011	5	0	0101
01110	6	0	0110
01111	7	0	0111
10010	8	0	1000
10011	9	0	1001
10110	A	0	1010
10111	B	0	1011
11010	C	0	1100
11011	D	0	1101
11100	E	0	1110
11101	F	0	1111
00100	H	1	0100
10000	H	1	0100
01000	H	1	0100
00010	H	1	0100
00001	H	1	0100
11111	I	1	0111
11000	J	1	1100
10001	K	1	0011
00000	Q	1	0000
00111	R	1	0001
11001	S	1	1001
01101	T	1	1101
00011	V	1	1000
00101	V	1	1000
00110	V	1	1000
01100	V	1	1000

Symbol Notation:

0, 1....F = Hexadecimal digits
H, I, J, K, Q, R, S, T, V: = Network Control Symbols

Note:

Overflow/Underflow in the elasticity buffer causes violation (11000) symbols to be sent out to the sync register. Also, line state conditions QLS, HLS, MLS, NLS in the line state decode logic cause PHY invalid (11111) symbols to be sent out on the R-bus.

Table 2. Line State Identification

S2	S1	S0	STATE	DEFINITION
0	0	0	LSU	**Line State Unknown.** The criteria for entering or remaining in any other line state have not been met.
0	0	1	NLS	**Noise Line State** is entered upon the occurrence of 16 potential noise events without satisfying the criteria for entry into another line state. Potential noise events are the decoding of symbol pairs (with CARDET active) containing at least one Q,H,J,K, or V symbol or the detection of elasticity buffer overflow/underflow. Decoding of data R, S,and T when the last known state is not ALS or ILS is also considered a noise event. NLS is exited when the criteria for entry into any other line state is satisfied.
0	1	0	MLS	**Master Line State** is entered upon the reception of eight or nine consecutive HQ or QH symbol pairs when CARDET is HIGH. MLS is exited upon receipt of any symbol pair other than HQ or QH, or when CARDET goes LOW.
0	1	1	ILS	**Idle Line State** is entered upon receipt of four or five consecutive idle symbols while CARDET is HIGH. ILS is exited upon receipt of any symbol other than idle or when CARDET goes LOW.
1	0	0	HLS	**Halt Line State** is entered upon receipt of 16 or 17 consecutive H symbols while CARDET is HIGH. HLS is exited upon receipt of any symbol other than H when CARDET is HIGH.
1	0	1	QLS	**Quiet Line State** is entered upon receipt of 16 or 17 consecutive Q symbols, or whenever CARDET goes LOW. QLS is exited upon receipt of any symbol other than Q when CARDET is HIGH.
1	1	0	ALS	**Active Line State** is entered upon receipt of a JK symbol pair while CARDET is HIGH. ALS is exited whenever CARDET goes LOW, ILS is entered, or when any control symbol other than I, R, S, or T is received.
1	1	1	OVUF	**Elasticity Buffer Overflow/ Underflow.**

Line State Decoder, Timer, and Bus Interface Unit

The purpose of line state decoder logic is to detect the presence of quiet, halt, master, idle, active, or noise line states at the sync register output. An 8-to-3 priority encoder decides the priority of line states indicated on pins $S_{0\text{-}2}$. A table showing the output is shown in Table 2. OVUF indicates overflow/underflow of the elasticity buffer present inside the ENDEC. OVUF gets the highest priority followed by ALS, QLS, HLS, ILS, MLS, and finally NLS. When two line states are simultaneously reached, the one with the higher priority is flagged.

The function of the bus interface unit is to provide the ENDEC with an interface to the NP for the purpose of:

1) Connection management;
2) Selecting various loopback and repeat modes for the ENDEC/EDS combination;
3) Enabling either the TA or TB bus for transmission;
4) Forcing quiet, master, idle, or halt symbols onto the medium;
5) Enabling the repeat filter;
6) Enabling conversion of parity errors by the repeat filter;
7) Indicating line state status and the contents of control registers;
8) Monitoring the smoother extensions;
9) Software reset of the ENDEC and/or smoother;
10) Selecting odd or even parity of the transmit input.

Data from the 3-bit $NP_{0\text{-}2}$ may be written into the four control registers (described in the "User-Accessible Registers" section) in the ENDEC. These control registers are used to help perform items 1-10 listed above. Communication is established with the NP through the use of the $\overline{CSI}$, $\overline{DS}$, $\overline{READY}$ and C/$\overline{D}$. The Bus Interface Unit also synchronizes the $\overline{RESET}$ signal with BCLKIN before distributing it to the rest of the chip.

Receiver

Decoder

The decoder section consists of an NRZI to NRZ converter, a shifter, two 4B/5B decoders,and a parity generator. Data is first processed by the NRZI to NRZ converter. Then the shifter performs serial-to-10-bit parallel conversion of the NRZ data. The shifted symbol pair is then parallel-loaded into a register in the 4B/5B decoder; this transfer is timed by the framing and control logic. The decoder then performs 4B/5B decoding for the two nibbles of data and parity is generated for the 10-bit decoded output.

Framing and Control Logic

The purpose of the framing and control logic is to generate timing pulses to load data into the decoder and to write data into the elasticity buffer. The timing of these pulses is based on the byte boundary information provided by the Start Delimiter (SD) of each frame.

Elasticity Buffer

The purpose of the elasticity buffer is to provide temporary storage for the decoded data before it is loaded into the sync. register and clocked out to the receive mux. This temporary storage is necessary because of the difference in frequency that may exist between the transmit clock and the receive clock which is recovered from the received bit stream. The maximum difference allowed by ANSI X3T9.5 is 100 parts per million.

The elasticity buffer also provides an indication of overflow/underflow and JK (Start Delimiter) detection to the line state decoder logic. These signals are synchronous to BCLKIN. Whenever overflow/underflow occurs, the elasticity buffer is allowed to modify up to three bytes of input to recenter correctly. Violation symbols are flagged during overflow/underflow.

Sync. Register

Data is clocked out from the elasticity buffer through the sync. register using delayed BCLKIN. The sync register is constructed in two stages to reduce the effects of metastability. It forces violation symbols (11000) into the receive mux under two conditions. The first is elasticity buffer overflow/underflow. The second case is when the noise line state (NLS) as described in the line state decoder section goes active. The sync. register will send violation symbols for 160 byte clock cycles once NLS goes active. The sync register will resume sending receive data from the elasticity buffer to the receive mux after 160 byte-clock cycles, even if NLS is still active. It is allowed 96 byte times to examine this data and decide whether NLS still exists. If so, the ENDEC will continue holding NLS active, and the sync. register will force violation symbols for another 160 byte-time period.

Smoother

The smoother is included in the ENDEC to ensure with a very high probability that at least 6 bytes of preamble precede a frame. The station that originates a frame initially has 8 bytes of preamble. If the next station is a slower station, the elasticity buffer could delete a byte of Idle if the elasticity buffer implementation is bytewide. If succeeding stations are also slower, they could also delete an additional 2 bytes of Idle, causing the number of deleted bytes to be 3. This 5-byte interframe gap could prove inadequate for a station to copy its addressed frames because of the handshaking that goes on at the end of frames. The smoother helps to reduce the number of lost frames.

Receive Mux

This circuit is used to send data from the smoother, TA-, or TB-bus to the FORMAC on the R-bus. The selection is made by the TMUXSEL bit and the $LPBK_1$ and $LPBK_0$ bits in control register 1 (CR_1). When any of QLS, HLS, NLS or MLS exists, this mux sends a pair of Phy Invalid symbols (11111) out on the R-bus. The Smoother output has a 0-, 1-, or 2- byte delay depending whether it is in extension 0,1,2, respectively. When data from the TA- or TB-bus is selected, it is sent through a register clocked using BCLKIN.

Crystal Oscillator

A parallel-mode oscillator operating at the fundamental frequency of an external crystal generates the transmit byte-rate clock (BCLKOUT). This is the master clock which synchronizes the other members of the SUPERNET chip-set. Some applications require more than one ENDEC to be used in a station; in these cases, BCLKOUT from only one of the local ENDECs is used.

Transmit PLL and Clock Logic

An internal PLL is used to generate a transmit bit clock. The PLL is referenced to BCLKIN, which is intended to be driven by BCLKOUT (described above). This section also drives a nibble clock, operating at twice the frequency of BCLKIN.

Operational Modes

The ENDEC can operate any of the four modes listed in Table 3-3 and as shown in Figure 2. Bits $LPBK_1$ and $LPBK_0$ of control register CR_1 (located in the ENDEC) define the mode of operation.

In "through" mode, data from the FORMAC is transmitted onto the serial link, and the data received from the network is passed onto the FORMAC. In "loopback" mode, data from the transmit output is directly looped back to the receive input (RLTX, RLTY) of the EDS. This is useful for self-diagnostics. In "short loopback" mode, data from one of the transmit bus inputs to the ENDEC is directly looped back to the receive bus output, without going through the rest of the transmit path. In "repeat" mode, receive data is repeated onto the transmit path without being sent to the FORMAC. Also in "repeat" mode, the selected transmit bus input is looped back to the receive bus output as in "short loopback" mode. This is useful in connection management and station reconfiguration. Quiet symbols are sent out on pins TX and TY in "short loopback" or "loopback" modes.

User-Accessible Registers

There are four control registers (CR_0, CR_1, CR_2, and CR_3) and one pointer register (CR pointer) in the ENDEC. Each of these is 3 bits wide as shown in Table 3-1. Their contents are cleared to logic "0" when the Am7984A ENDEC is reset.

Table 3-1. Control Register and Pointer Bit Assignments

Register	Bit 2	Bit 1	(LSB) Bit 0
CR_0	C2	C1	C0
CR_1	TMUXSEL	LPBK1	LPBK0
CR_2	RESET	EVEN/ODD	PARCON
CR_3	EXTENSION 2	EXTENSION 1	SMRESET
CR Pointer	REGSEL2	REGSEL1	REGSEL0

(All bits = 0 after reset.SMRESET and RESET are cleared once set)

Table 3-2. CR_0 (Force Line States)

C2	C1	C0	Function	Description
0	0	0	Force Quiet	Q bytes continually forced
0	0	1	Force Master	QH bytes continually forced
0	1	0	Force Halt	Halt bytes continually forced
0	1	1	Force Idle	Idle bytes continuously forced
1	0	0	Enable Repeat Filter	Repeat filter enabled
1	0	1	Force JKILS	JK followed by continuous Idle bytes
1	1	0	Force IQ	IQ bytes continuously forced
1	1	1	Unfiltered Encode	Input bytes to encoder without repeat filtering.

Control Register 0 – (CR_0) programs the ENDEC to transmit data or various line states as described in Table 3-2. These line states are used for connection management and station reconfiguration.

Control Register 1– (CR_1) selects either the TA-bus or the TB-bus inputs to the ENDEC for transmission onto the media. This is accomplished by setting the TMUX-SEL bit. Logic "0" selects the TB-bus and logic "1" chooses the TA-bus. CR_1 also forces the ENDEC and EDS into one of the operational modes described earlier and shown in Table 3-3.

Table 3-3. CR_1 (Loopback Modes)

$LPBK_1$	$LPBK_0$	Function
0	0	Through
0	1	Loopback
1	0	Short Loopback
1	1	Repeat

Control Register 2 – (CR_2) contains the RESET, EVEN/ODD and PARCON bits. When RESET is set to 1, the ENDEC gets reset and the bit gets cleared. When EVEN/ODD is 1, the even parity mode of operation is chosen for the ENDEC. When EVEN/ODD is 0, odd parity mode of operation is chosen for the ENDEC. PARCON, when set to logic "1", enables the conversion of parity by the repeat filter state machine.

Control Register 3 – (CR_3) is used to reset the smoother (smoother is not extended) by means of SMRESET bit and can also be used to read the status of the smoother through EXTENSION2 and EXTENSION1 bits. When the EXTENSION2 bit is logic "1", the smoother is extended by two bytes. When the EXTENSION1 bit is logic "1", the smoother is extended by one byte.The SMRESET bit, once it resets the smoother, gets cleared to "0".

Pointer Register (CR pointer) – selects one of the control registers to be written or read by the NP as shown in Table 3-1. It can also select the line status of the decoded data as indicated by the S_{0-2} pins by choosing CR Pointer = 011. This register can be written, but not read.

Table 3-4. Pointer Register (CR Pointer)

REGSEL2	REGSEL1	REGSEL0	Enable
0	0	0	CR_0
0	0	1	CR_1
0	1	0	CR_2
0	1	1	Status
1	0	0	CR_3

Loading and reading these registers is done using the C/$\overline{D}$, $\overline{DS}$, $\overline{CSI}$, R/$\overline{W}$, and NP_{0-2} pins. C/$\overline{D}$ is analogous to the $INST_{0-3}$ lines on the RBC, DPC, and FORMAC. Since the RESET and SMRESET bits are automatically cleared, it is not meaningful to read them.

Diagnostic Features

The ENDEC and EDS together can operate in various loopback modes. These are described in the "Operational Modes" section of this data sheet. The ENDEC also has a TEST pin which disables the internal VCO in the "PLL and clock" section of the ENDEC. The CTX/$\overline{CTX}$ pins can then be used to bring in the transmit bit clock for test purposes. When the TEST pin is floating, the on-chip crystal oscillator can be used as a bit rate oscillator.

Global Issues

Following are the global objectives for the ENDEC.

1) Frequency Stability of bit clock: better than ±50 parts per million.
2) Maximum latency through ENDEC with Smoother unextended: 65 bits.
3) Maximum latency through ENDEC with Smoother extended once: 75 bits.
4) Maximum latency through ENDEC with Smoother extended twice: 85 bits.

Crystal Specifications

Frequency (fundamental)	12.5MHz
Resonant Mode	Parallel
Load Capacitor (Correlation)	75pF
Operating Temperature Range	0 to 70°C
Temperature Stability (Including calibration tolerance)	± 25 parts per million
Drive Level (Correlation)	2 mW
Effective Series Resistance	25 ohms (max)
Holder Type	Low Profile
Aging for 10 years	± 10 parts per million

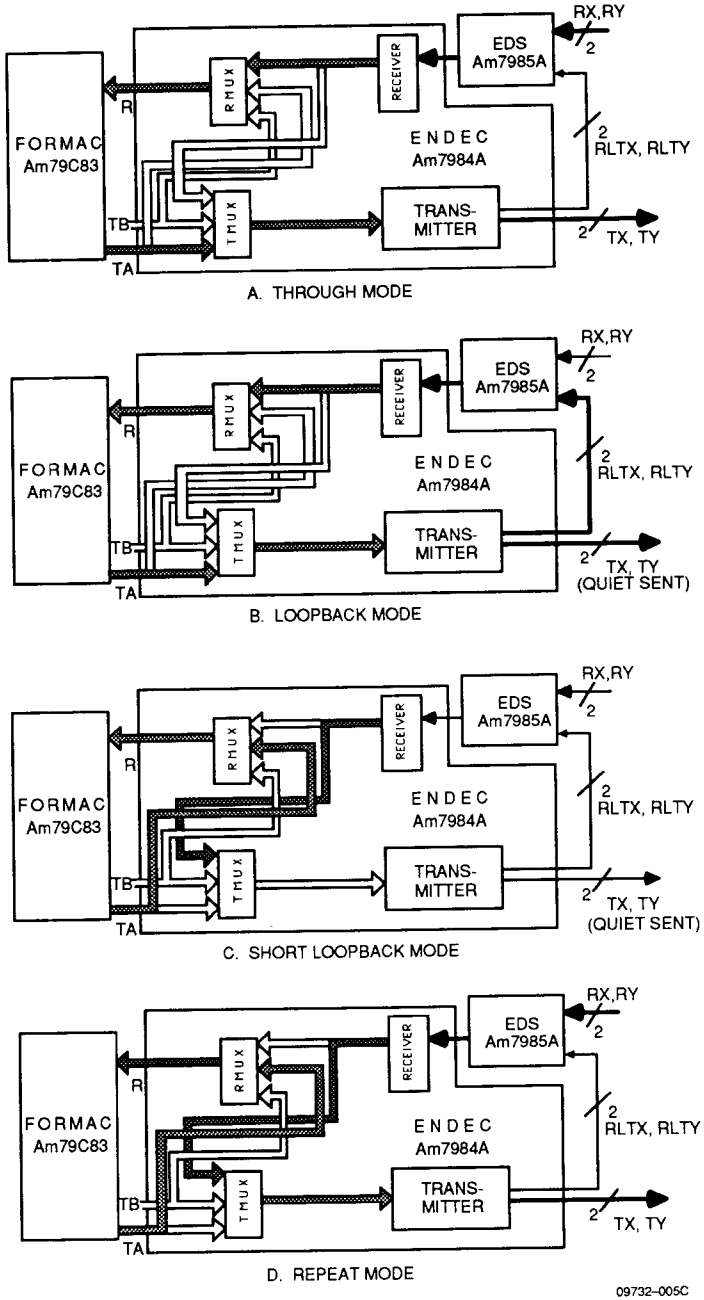


Figure 2. Loopback Paths
(Active data paths are highlighted)

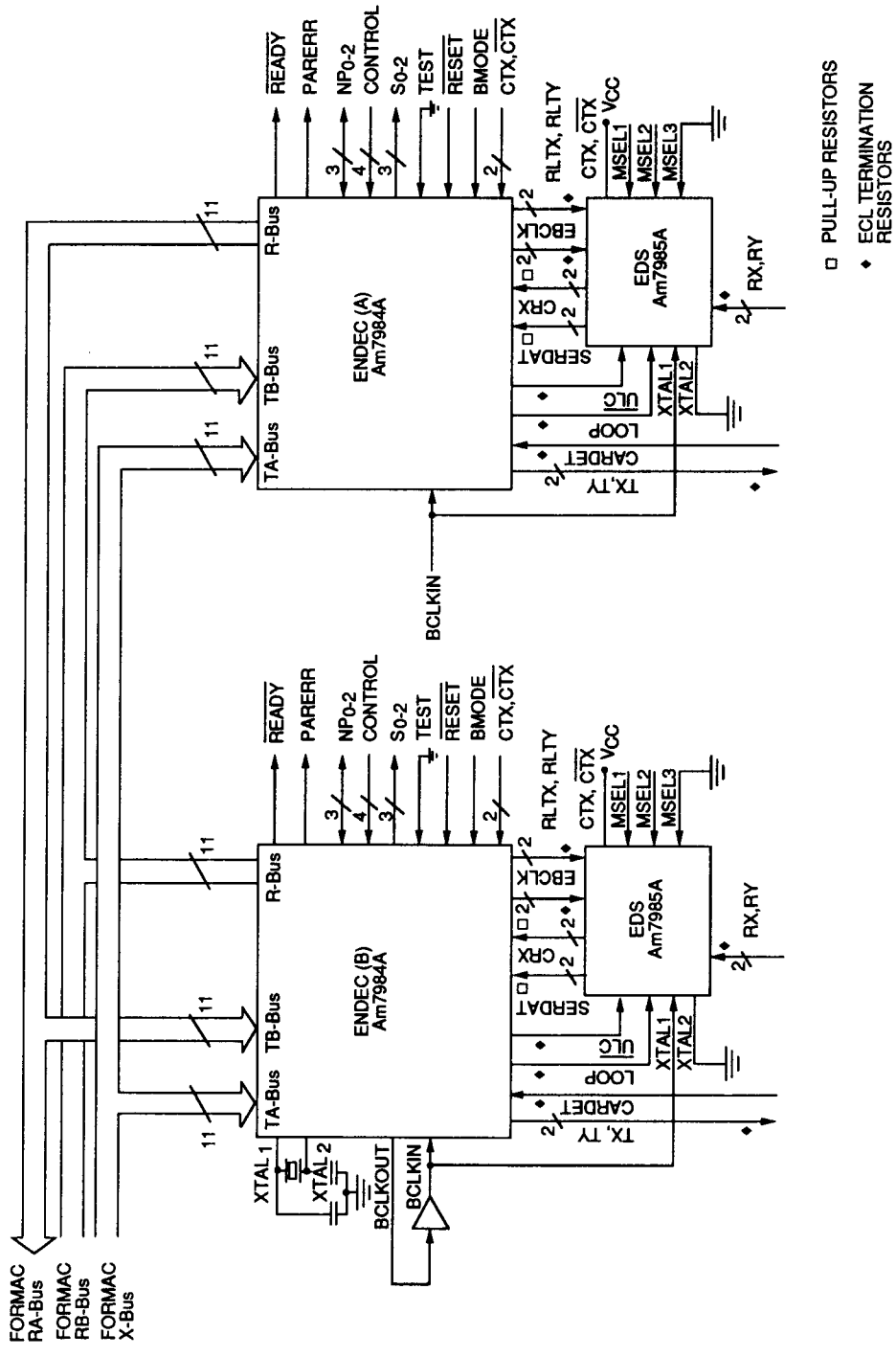


Figure 3: ENDEC-EDS Interconnections in a Dual-attach Station

09732-006C

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65 to +150°C
Ambient Temperature Under Bias	-55 to +125°C
Supply Voltage to Ground Potential Continuous	-0.5 to + 7.0 V
DC Voltage Applied to Outputs	-0.5 to V_{CC} Max.
DC Input Voltage	-0.5 to +5.5 V
DC Output Current	±100 mA
DC Input Current	-30 to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V

Extended Commercial (E) Devices

Case Temperature (T_C)	-55 to +125°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions (Notes 1 & 5)		Min.	Max.	Unit
TTL INPUT PINS (Note7)						
V_{IH}	Input HIGH Voltage	V_{CC} = Max (note 6).		2.0		V
V_{IL}	Input LOW Voltage	V_{CC} = Max. (Note 6)			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min. I_{IN} = -18 mA			–1.5	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4 V	All Except NP_{0-2}, $\overline{CSI}$, $\overline{DS}$, R/$\overline{W}$		–400	µA
			NP_{0-2}, $\overline{CSI}$, $\overline{DS}$, R/$\overline{W}$		–550	µA
I_{IH}	Input HIGH Current	V_{CC} = Max.,	All Except NP_{0-2}		50	µA
		V_{IN} = 2.7 V	NP_{0-2}		100	µA
I_I	Input Leakage Current	V_{CC} = Max.,	All Except NP_{0-2}		50	µA
		V_{IN} = 5.5 V	NP_{0-2}		100	µA
TTL OUTPUT PINS (Note8)						
V_{OH}	Output HIGH Voltage (All Outputs Except $\overline{READY}$)	V_{CC} = Min.	I_{OH} = -1 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 4 mA		0.5	V
I_{SC}	Output Short-Circuit Current	V_{CC} = Max. (Note 4)	All outputs except $\overline{READY}$ and NP_{0-2}	-15	–85	mA
			NP_{0-2}	-15	-100	mA
I_{CEX}	Output Leakage Current ($\overline{READY}$ pin only)	V_{IN} = 2.4 V			50	µA
CML/ECL INPUT PINS (SERDAT, $\overline{SERDAT}$, CRX, $\overline{CRX}$, CTX, $\overline{CTX}$)						
I_{IL}	Input LOW Current	V_{CC} = Max V_{IN} = V_{CC} - 1.81		0.5		µA
I_{IH}	Input HIGH Current	V_{CC} = Max V_{IN} = V_{CC}			500	µA
V_{DIFF}	Differential Input Voltage	V_{CC} = Max		0.2	1.1	V
V_{ICM}	Input Common Mode Voltage	(Note 9)		3.05	V_{CC} - 1/2 (V_{DIFF})	V

DC CHARACTERISTICS (Continued)

Parameter Symbol	Parameter Description	Test Conditions (Notes 1 and 5)		Min.	Max.	Unit
ECL INPUT PINS (CARDET)						
V_{IHS}	Input HIGH Voltage	V_{CC} = Max. (Note 6)		V_{CC} - 1.165	V_{CC} - 0.88	V
V_{ILS}	Input LOW Voltage	V_{CC} = Max. (Note 6)		V_{CC} - 1.81	V_{CC} - 1.475	V
I_{IL}	Input LOW Current	V_{CC} = Max, V_{IN} = V_{CC} - 1.81V		0.5		µA
I_{IH}	Input HIGH Current	V_{CC} = Max, V_{IN} = V_{CC} - 0.88 V			220	µA
ECL OUTPUT PINS (TX, TY, RLTX, RLTY, EBCLK, $\overline{\text{EBCLK}}$, $\overline{\text{ULC}}$, LOOP)						
V_{OH}	Output HIGH Voltage	V_{CC} = Min., ECL Load		V_{CC} - 1.025	V_{CC} - 0.88	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., ECL Load		V_{CC} - 1.81	V_{CC} - 1.62	V
CRYSTAL PINS ($XTAL_1$, $XTAL_2$)						
I_{ILX}	Input LOW Current $XTAL_1$	V_{IN} = 0 V			-1	mA
I_{IHX}	Input HIGH Current $XTAL_1$	V_{IN} = 3.5 V			+1	mA
POWER SUPPLY PINS (V_{CC1}, V_{CC2}, V_{CC3})						
I_{CC}	Supply Current (Note 10)	V_{CC1} = V_{CC2} = V_{CC3} = Max., T_A = +25°C	Pin V_{CC1} (TTL)			mA
			Pin V_{CC2} (CML)			mA
			Pin V_{CC3} (ECL)			mA
		V_{CC1} = V_{CC2} = V_{CC3} = Max	Total @ + 125°C			mA
			Total @ +25°C		930	mA
			Total @ - 55°C			mA

SWITCHING CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified (Notes 4 & 11)

No.	Parameter	Signal Name	Min.	Max.	Unit
1	Clock Period	BCLKIN	80		ns
2	HIGH Pulse Width	BCLKIN	35		ns
3	LOW Pulse Width	BCLKIN	35		ns
4	Setup Time Before BCLKIN ↑	$\overline{CSI}$, $\overline{DS}$, C/$\overline{D}$, R/$\overline{W}$	36		ns
5	Hold Time After BCLKIN ↑	$\overline{CSI}$, R/$\overline{W}$	8		ns
6	Hold Time After BCLKIN ↑	$\overline{DS}$	8		ns
7	Hold Time After BCLKIN ↑	C/$\overline{D}$	8		ns
8	Hold Time After BCLKIN ↑	NP_{0-2}	11		ns
9	Setup Time Before BCLKIN ↑	NP_{0-2}	25		ns
10	R/$\overline{W}$ ↑, $\overline{CSI}$ ↓, $\overline{DS}$ ↓ (Whichever Occurs Last) Until NP_{0-2} is Enabled (Synchronous Mode)	NP_{0-2}	0		ns
11	Signal Valid After BCLKIN ↑	NP_{0-2}		(0.05 x T1) + 41	ns
12	Signal Invalid After BCLKIN ↑	NP_{0-2}	(-.05 x T1) + 10		ns
13	R/$\overline{W}$ ↓, $\overline{DS}$ ↑, or $\overline{CSI}$ ↑ (Whichever Occurs First at the End of a Synchronous Read Cycle) to Bus Inactive	NP_{0-2}		30	ns
14	Signal Invalid After $\overline{DS}$ ↑, $\overline{CSI}$ ↑, or R/$\overline{W}$ ↓ (Whichever Occurs First at the End of a Synchronous Read Cycle)	NP_{0-2}	4		ns
15	Hold Time After $\overline{DS}$ ↑ or $\overline{CSI}$ ↑ (Whichever Occurs First in Asynchronous Write)	NP_{0-2}	0		ns
16-19	Unused				
20	Setup Time Before $\overline{CSI}$ ↓ $\overline{DS}$ ↓ (Whichever Occurs Last in Asynchronous Read/Write)	R/$\overline{W}$ ↓ (Write) or R/$\overline{W}$ ↑ (Read), C/$\overline{D}$	0		ns
21	Unused				
22	Pulse Width HIGH (Asynchronous Read or Write, From the First of these Signals to go HIGH to the Last to go LOW)	$\overline{CSI}$, $\overline{DS}$	(1.5 x T1)		ns
23	Hold Time After $\overline{DS}$ ↑ or $\overline{CSI}$ ↑ (Whichever Occurs First at the End of Asynchronous Read/Write)	R/$\overline{W}$,C/$\overline{D}$	0		ns
24	Delay Time From $\overline{DS}$ ↓	$\overline{READY}$	(2 x T1)	(3 x T1) + 40	ns
25	Delay Time From $\overline{DS}$ ↑	$\overline{READY}$		40	ns
26	Bus Enabled After $\overline{DS}$ ↓ or $\overline{CSI}$ ↓ (Whichever Occurs Last in Asynchronous Read)	NP_{0-2}	0		ns

SWITCHING CHARACTERISTICS (Continued)

No.	Parameter	Signal Name	Min.	Max.	Unit
27	Bus Valid After $\overline{DS}$ ↓ or $\overline{CSI}$ ↓ (Whichever Occurs Last in Asynchronous Read)	NP_{0-2}		(2 x T1) + 60	ns
28	Signal Invalid After $\overline{DS}$ ↑ or $\overline{CSI}$ ↑ (Whichever Occurs First in Asynchronous Read)	NP_{0-2}	2		ns
29	Bus Disabled After $\overline{DS}$ ↑ or $\overline{CSI}$ ↑ (Whichever Occurs First in Asynchronous Read)	NP_{0-2}		30	ns
30	Setup Time Before $\overline{DS}$ ↓ or $\overline{CSI}$ ↓ (Whichever Occurs Last in Asynchronous Write)	NP_{0-2}	(-2 x T1) - 6		ns
31	Setup Time Before BCLKIN ↑	TA_{0-7}, TACL, TACU, TAP, TB_{0-7}, TBCL, TBCU, TBP	7		ns
32	Hold Time After BCLKIN ↑	TA_{0-7}, TACL, TACU, TAP, TB_{0-7}, TBCL, TBCU, TBP	10		ns
33	Signal Valid After BCLKIN ↑	R_{0-7}, RCL, RCU, RP		(0.05 x T1) + 36	ns
34	Signal Invalid After BCLKIN ↑	R_{0-7}, RCL, RCU, RP	(– 0.05 x T1) + 19		
35	Signal Valid After BCLKIN ↑	S_{0-2}		(0.05 x T1) + 32	ns
36	Signal Invalid After BCLKIN ↑	S_{0-2}	(-0.05 x T1) + 6		ns
37	Signal Valid After BCLKIN ↑	PARERR		50	ns
38	Signal Invalid After BCLKIN ↑	PARERR	2		ns
39	Pulse Width LOW	$\overline{RESET}$	(3 x T1)		ns
40	Unused				ns
41	Pulse Width HIGH	BCLKOUT	35		ns
42	Unused				
43	Pulse Width LOW	BCLKOUT	35		ns
44	Skew From BCLKIN ↑	NCLKOUT ↑		(0.05 x T1) + 25	ns
45	Unused				
46	Unused				
47	Unused				
48A	Setup time Before CRX ↑	SERDAT, $\overline{SERDAT}$	2		ns
48B	Hold Time After CRX ↑	SERDAT, $\overline{SERDAT}$	0		ns
49	Signal Valid After BCLKIN ↑	LOOP		35	ns
50	Signal Valid After BCLKIN ↑	$\overline{ULC}$		(0.05 x T1) + 20	ns
51	CARDET ↓ or ↑ to $\overline{ULC}$ ↓ or ↑			30	ns
52	Pulse Width HIGH	EBCLK, $\overline{EBCLK}$	35		ns
53	Pulse Width LOW	EBCLK, $\overline{EBCLK}$	35		ns
54	Unused				
55	Unused				
56	Rise Time (See note 2)	TX, TY	0.8	3	ns

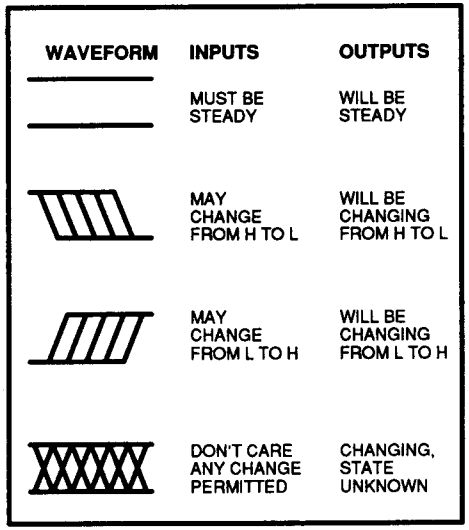
SWITCHING CHARACTERISTICS (Continued)

No.	Parameter	Signal Name	Min.	Max.	Unit
57	Fall Time (See note 2)	TX, TY	0.8	3	ns
58	Duty Cycle Distortion (peak to peak)	TX, TY		0.4	ns
59	Unused				
60	Unused				
61	Unused				
62	Delay from BCLKIN ↑	TX, TY, RLTX, RLTY		0.75 x T1	ns
63	Transition Interval	TX, TY	8	80	ns
64	Setup time before CTX ↑ (Test Mode)	BCLKIN	1		ns
65	Hold time after CTX ↑ (Test Mode)	BCLKIN	1		ns

Notes:

1. For conditions shown as Min. or Max., use the appropriate value specified under operating range.
2. Rise and fall time measurements are made at 20% and 80% points.
3. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.
4. All timing references are made with respect to +1.5 V for TTL-level signals, to the 50% point between V_{OH} and V_{OL} for ECL signals and CML/ECL signals. ECL input rise and fall times must be 2 ns ± 0.2 ns between 20% and 80% points. TTL input rise and fall times must be 2 ns ± 0.2 ns between 1 V and 2 V. Output-enabled and disabled times are referenced to 0.5 V above V_{OL} or below VOH.
5. Nominal input voltages are 0 or 3 V on TTL pins, V_{CC} - 0.9 or V_{CC} - 1.7 V on ECL input pins. Nominal input voltages on CML/ECL input pins are load dependent. For a load of 50 ohms connected to V_{CC} and 30 pF to ground, CML/ECL nominal voltages are between V_{CC} and V_{CC} - 0.25 Volts.
6. Measured with device in test mode while monitoring output logic states.
7. TTL Input Pins: $\overline{\text{RESET}}$, BCLKIN, $TA_{0\text{-}7}$, TACL, TACU, $TB_{0\text{-}7}$, TBCL, TBCU, TAP, TBP, $\overline{\text{CSI}}$, $\overline{\text{DS}}$, C/$\overline{\text{D}}$, R/$\overline{\text{W}}$, $NP_{0\text{-}2}$, and BMODE.
8. TTL Output Pins: $R_{0\text{-}7}$, RCL, RCU, RP, PARERR, $S_{0\text{-}2}$, BCLKOUT, NCLKOUT, $NP_{0\text{-}2}$, and $\overline{\text{READY}}$
9. Voltages applied to either of the differential inputs should not be above V_{CC} or below + 2.5 V to assure proper operation.
10. I_{CC} is measured with TX, TY, RLTX, RLTY, EBCLK, $\overline{\text{EBCLK}}$, $\overline{\text{ULC}}$, and LOOP pins connected to an ECL output load. I_{CC} is pulse tested at the stated ambient temperature.
11. T1 is specified to be 80 ns ± 50 ppm.

Key to Switching Waveforms



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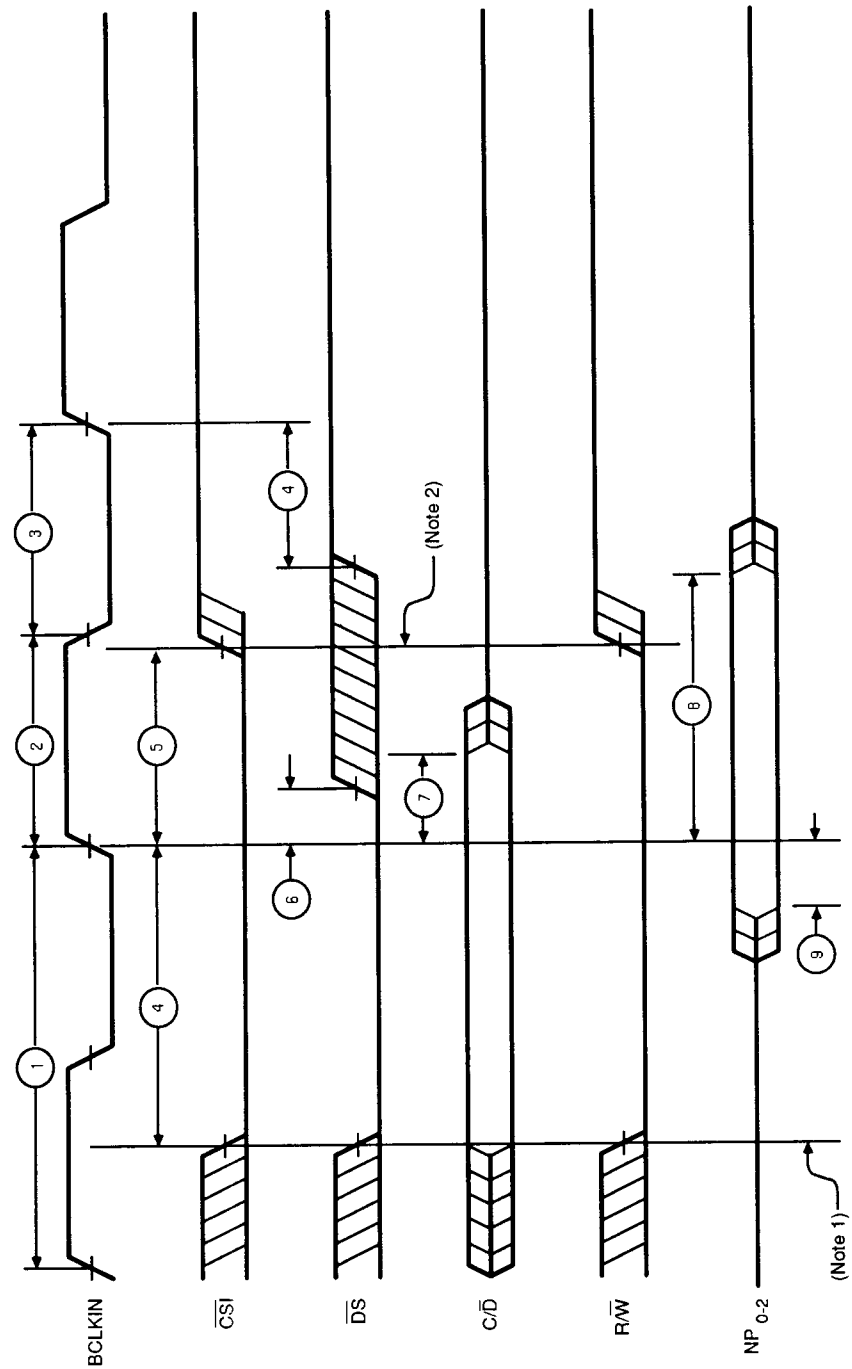
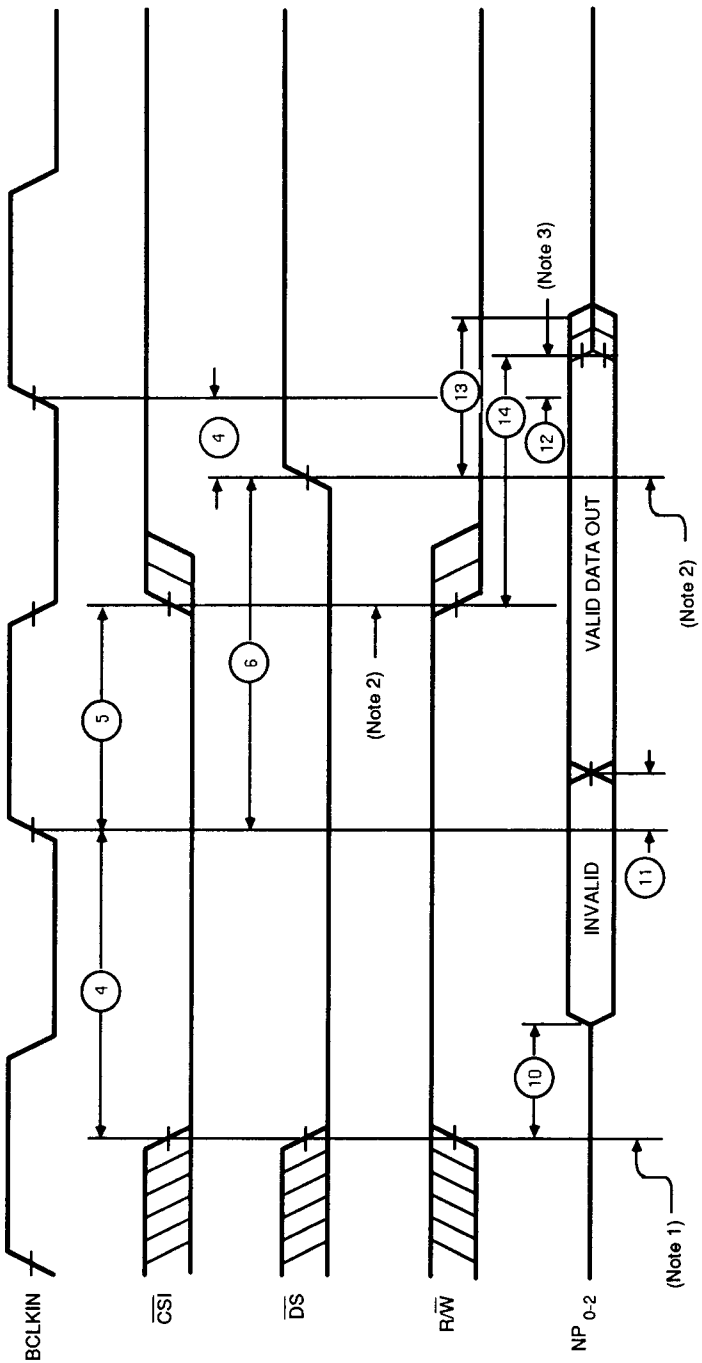
SWITCHING WAVEFORMS



Notes:
1. Timing measured from falling edge of CSI, DS, or R/W or the assertion of C/D, whichever occurs last.
2. Timing is measured from the rising edge of CSI or R/W, whichever occurs first.

09732-010B

NP-bus Synchronous Write Timing



Notes:
1. Timing measured from falling edge of $\overline{CSI}$ or $\overline{DS}$, or the rising edge of R/$\overline{W}$, whichever occurs last.
2. Timing is measured from the rising edge of $\overline{CSI}$, $\overline{DS}$, or the falling edge of R/$\overline{W}$, whichever occurs first.
3. NP_{0-2} may be updated on each rising edge of BCLKIN. Parameter #12 pertains to the situation where $\overline{CSI}$ and $\overline{DS}$ remain LOW and R/$\overline{W}$ remains HIGH for several BCLKIN periods. It does not define when NP_{0-2} becomes three-stated.

NP-bus Synchronous Read Timing

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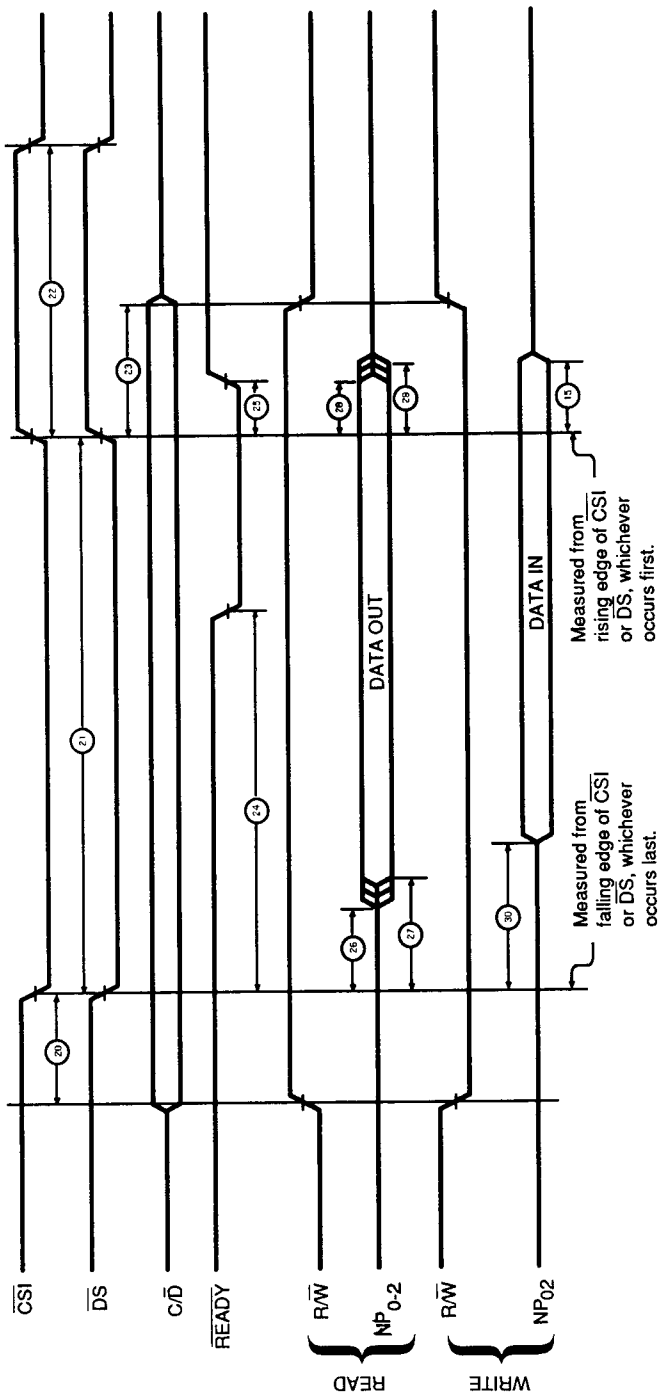

NP-bus Asynchronous Read/Write Timing

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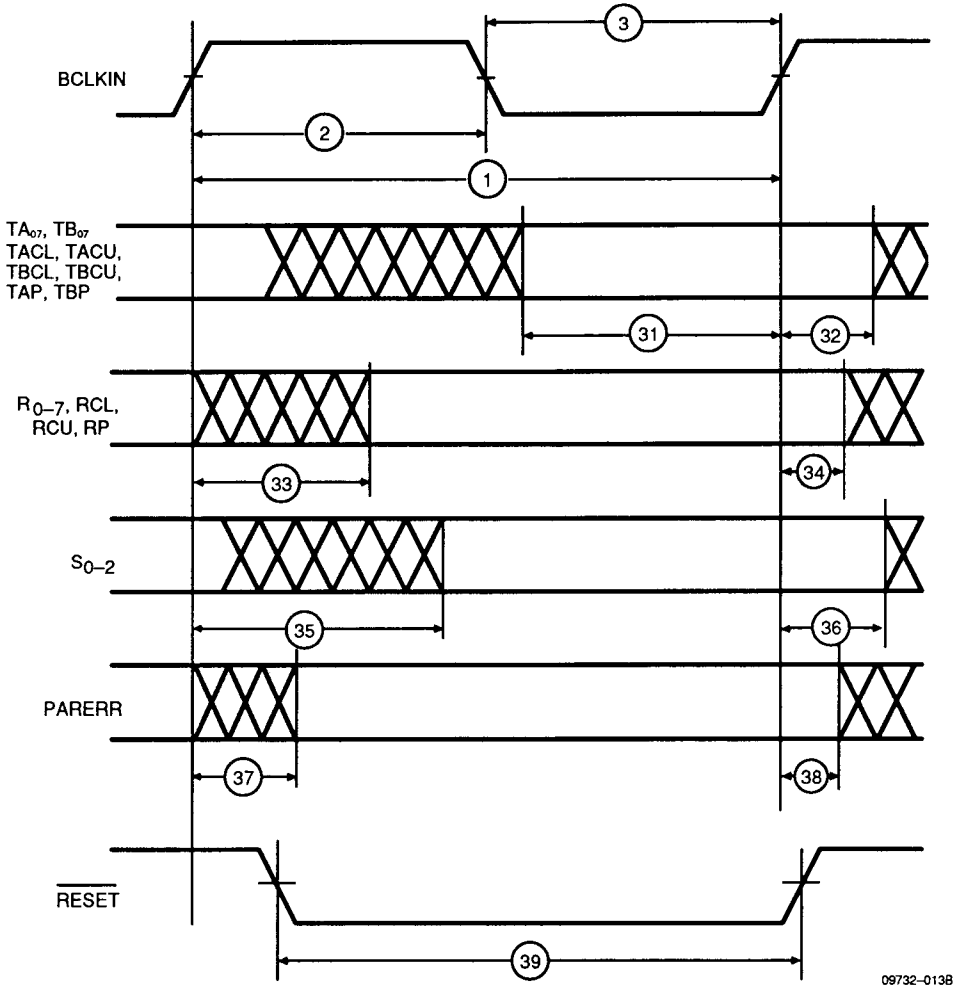
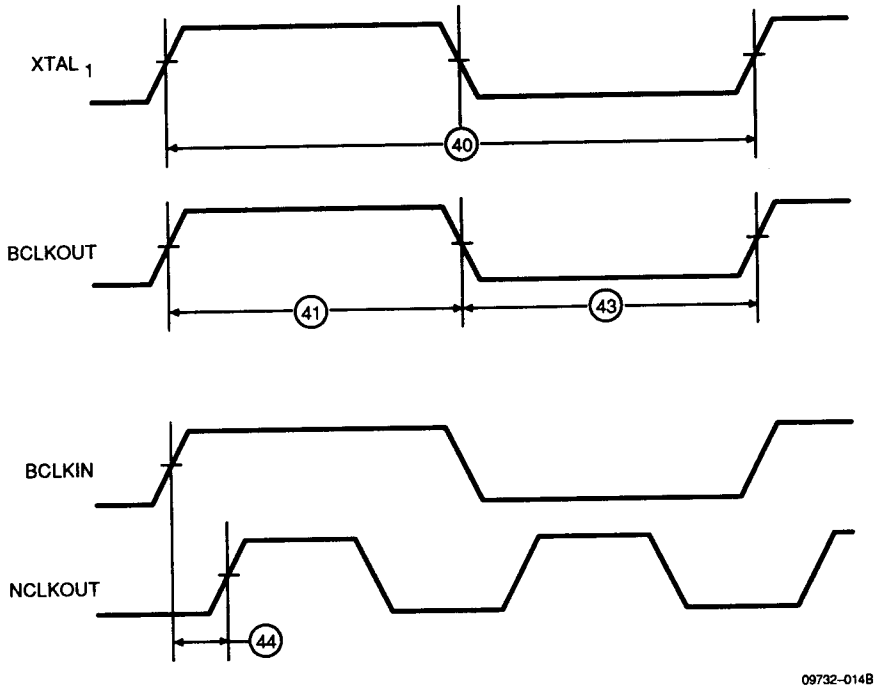
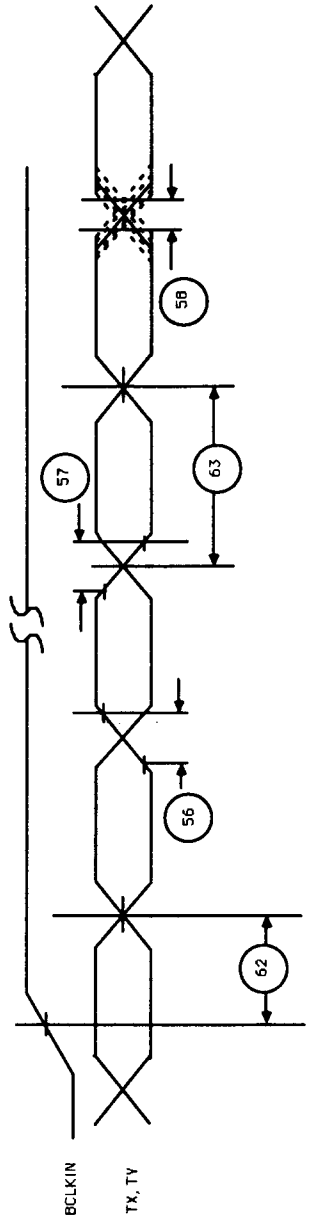
R-bus, T-bus, and Line State Timing



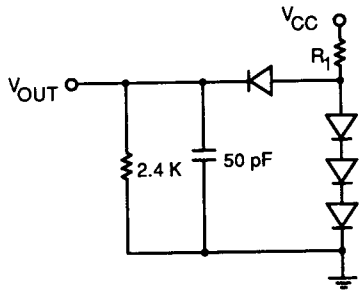

XTAL 1
40
BCLKOUT
41
43
BCLKIN
NCLKOUT
44
09732-014B

TX,TY Timing



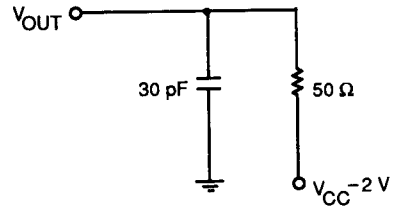
09732-06C

SWITCHING TEST CIRCUITS

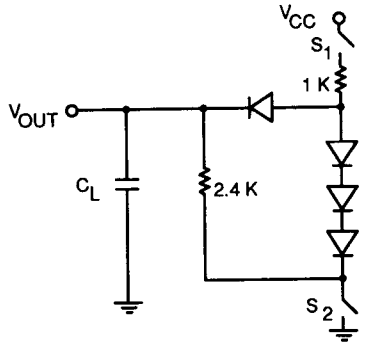


R_1 = 500 Ω for IOL = 8 mA and
R_1 = 1 K Ω for IOL = 4 mA

A. TTL Output Load



B. ECL Output Load

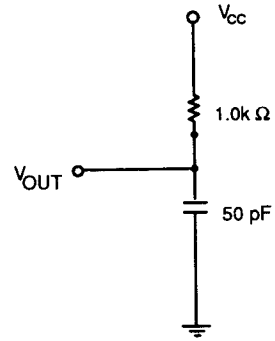


Circuit Configuration

Measurement	S_1	S_2	C_L	Threshold
ZH	O	X	50 pF	1.5 V
ZL	X	O	50 pF	1.5 V
HZ	X	X	5 pF	V_{OH}–0.5
LZ	X	X	5 pF	V_{OL}+0.5

X = Switch closed
O = Switch open

C. Three–State Outputs

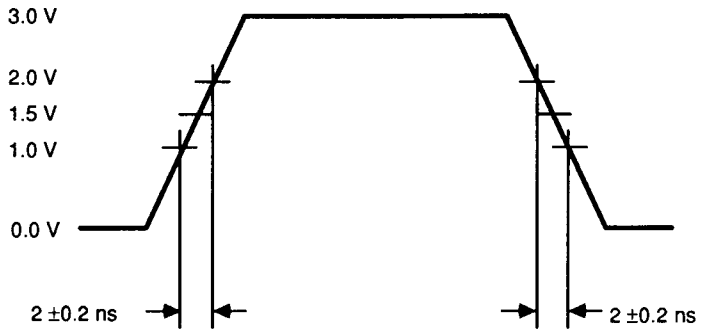


D. Open Collector Output Load

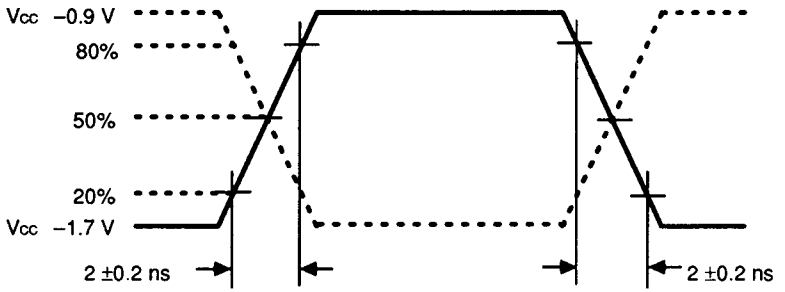
Notes: 1. All diodes 1N916 or 1N3064, or equivalent.
2. C = 50 pF includes scope probe, wiring and stray capacitances without device in test fixture.
3. AMD uses ATE load configurations and forcing functions. This figure is for reference only.

09732–008B

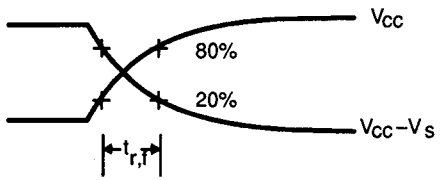
SWITCHING TEST WAVEFORMS



TTL Input Waveform



ECL Input Waveform



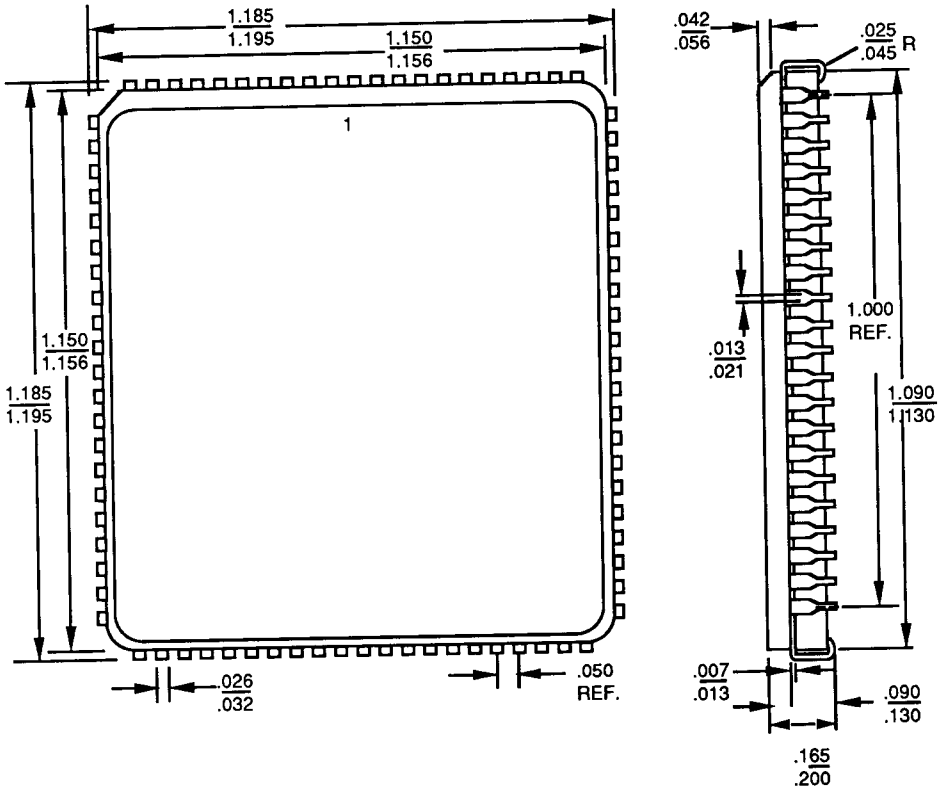
V_S = 250 mV

t_r, t_f = 2.2 ± 0.7ns

CML Input Waveform

09732-009B

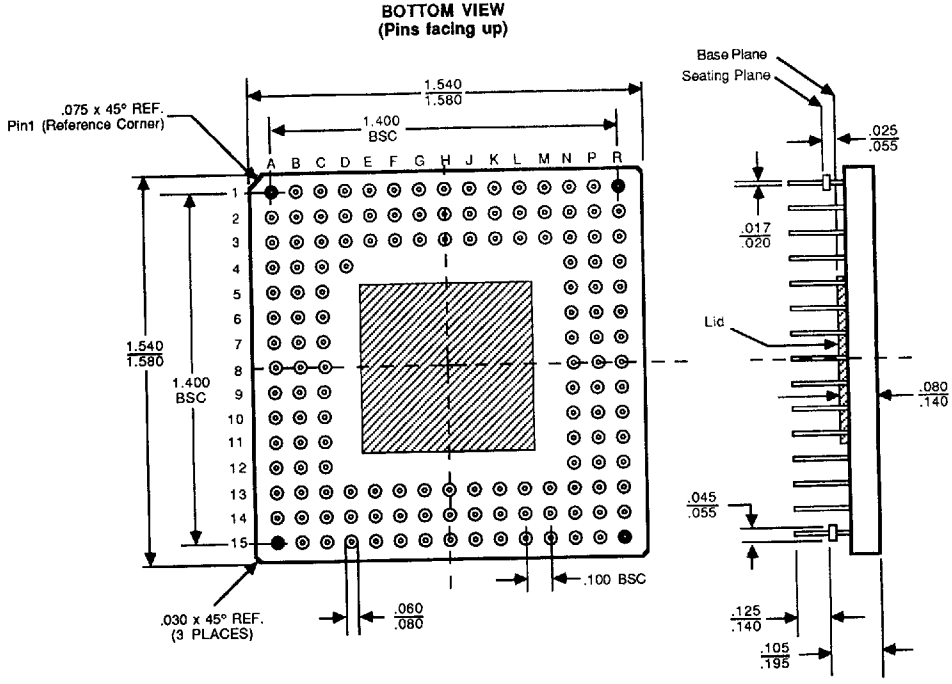
PHYSICAL DIMENSIONS
PL 084



09980-001A

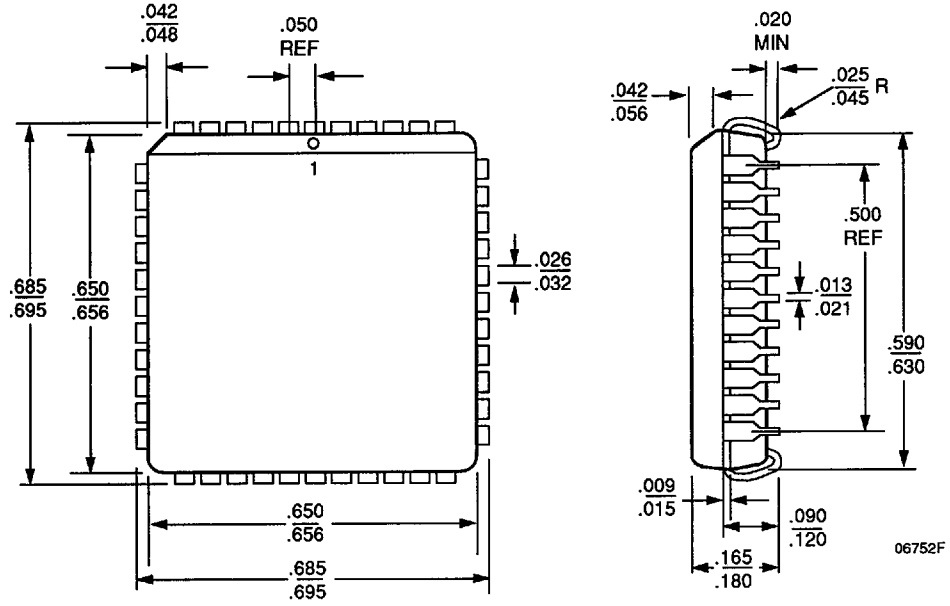
T-90-20

CGX145
145-Lead Pin Grid Array without Heat Sink

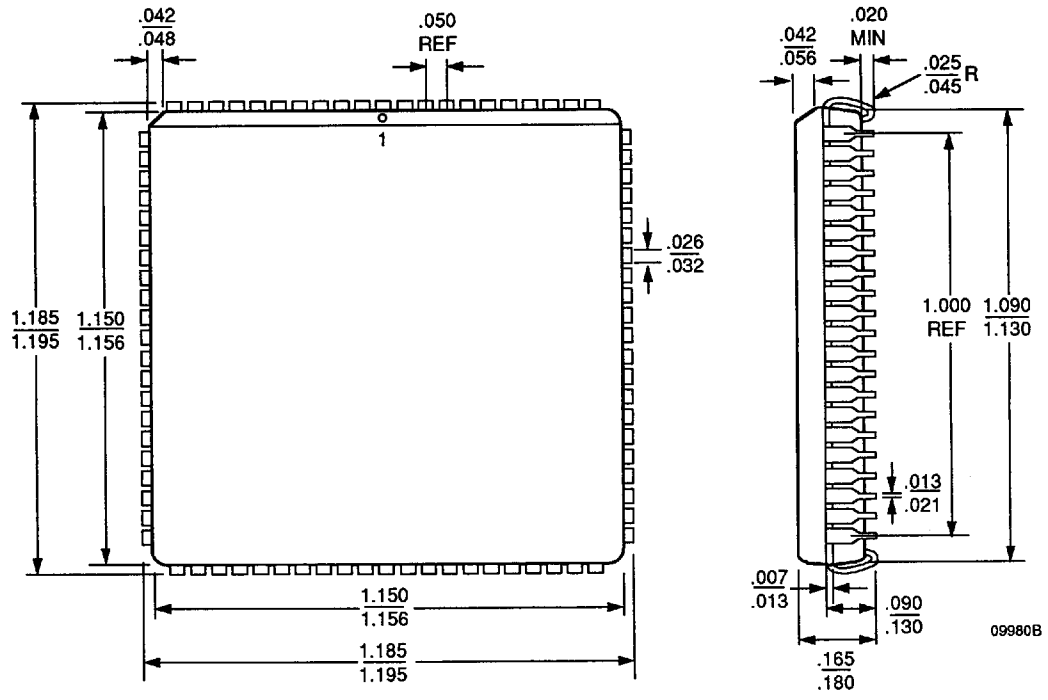


PID # 09691B

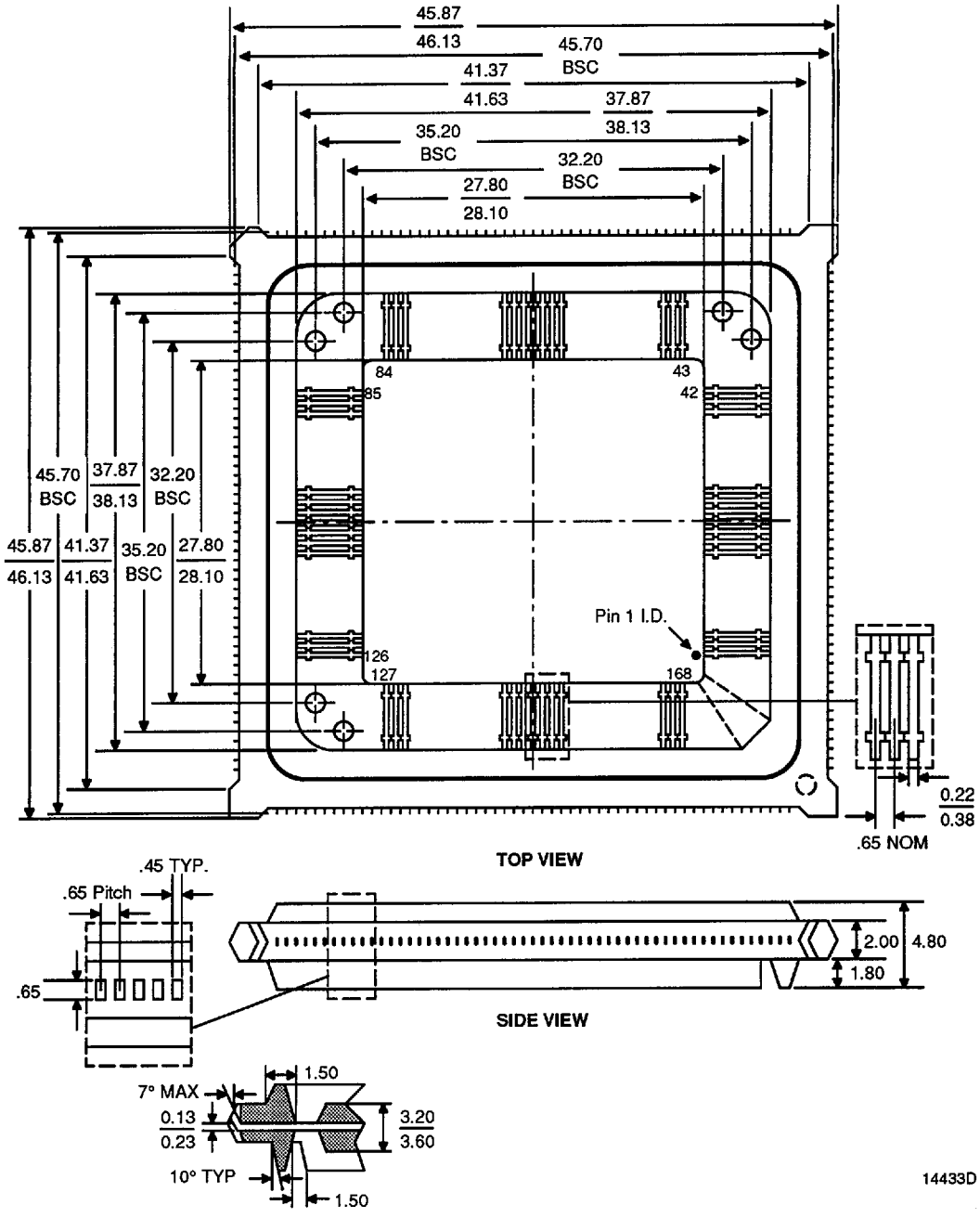
PL 044
44-Pin Plastic Leaded Chip Carrier



PL 084
84-Pin Plastic Leaded Chip Carrier

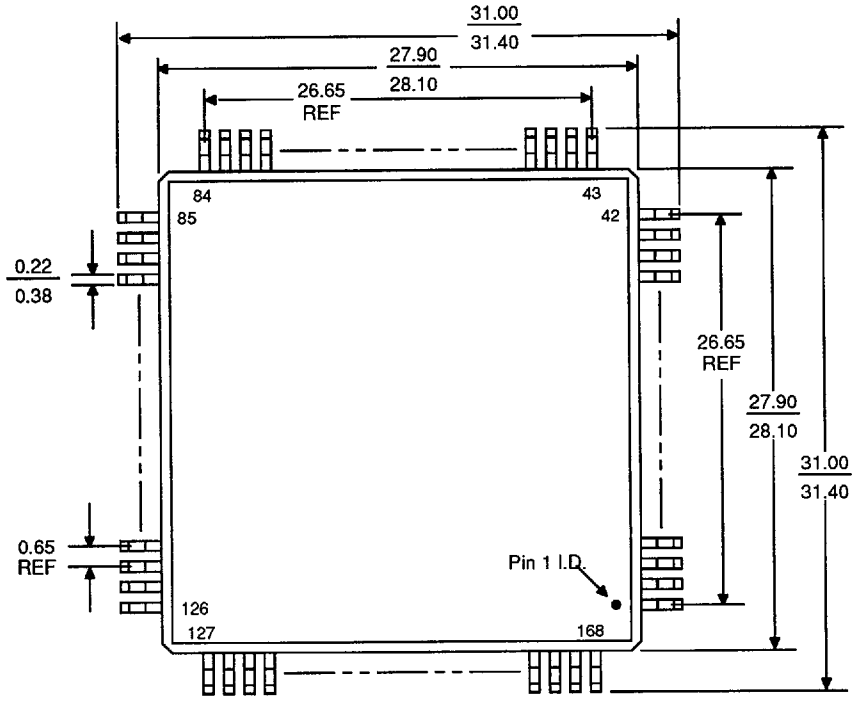


PQR168**
168-Pin Plastic Quad Flat Pack (Tape Pak)

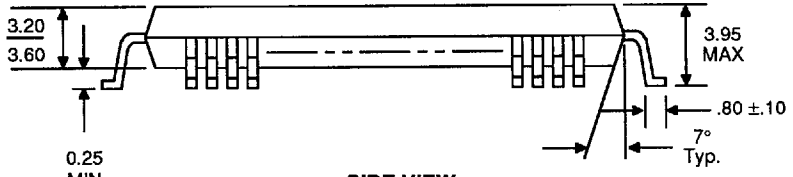


**Measured in Millimeters

PQJ168**
168-Pin Plastic Quad Flat Pack (Trimmed and Formed)



TOP VIEW



SIDE VIEW

**Measured in Millimeters