WARRANTY INFORMATION

Qua Tech Inc. warrants the **QS-2000/QS-3000** to be free of defects for **one (1) year** from the date of purchase. Qua Tech Inc. will repair or replace any board that fails to perform under normal operating conditions and in accordance with the procedures outlined in this document during the warranty period. Any damage that results from improper installation, operation, or general misuse voids all warranty rights.

Although every attempt has been made to guarantee the accuracy of this manual, Qua Tech Inc. assumes no liability for damages resulting from errors in this document. Qua Tech Inc. reserves the right to edit or append to this document at any time without notice.

Please complete the following information and retain for your records. Have this information available when requesting warranty service.

DATE OF PURCHASE:

MODEL NUMBER: **QS-2000/QS-3000**

PRODUCT DESCRIPTION: **FOUR CHANNEL RS-422/RS-485 ASYNC. COMMUNICATIONS ADAPTER**

SERIAL NUMBER:

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I. INTRODUCTION

The Qua Tech QS-2000 provides four independent asynchronous RS-422 serial communication channels for systems utilizing the MicroChannel architecture. The QS-3000 is an RS-485 version of the adapter. Each port may be accessed individually from the predefined addresses of Serial 1 through Serial 8 or the four channels may be grouped together and located anywhere within the available I/O address range of the system. Two output options increase flexibility by allowing connection to a 37-pin 'D' connector or an abbreviated 6-wire RJ-11 'modular' phone jack style connector.

The QS-2000/QS-3000 serial interface is realized through four 16550 ACEs (Asynchronous Communication Elements). The 16550 is compatible with the 8250 and 16450 ACEs used in the PC/XT/AT models. In addition, the 16550 supports a FIFO mode to reduce CPU overhead at higher data rates.

Address and interrupt selections are accessed through the Programmable Option Select using the IBM installation utilities. In addition, jumpers are provided to select input clock frequency and control of the data exchanged on the auxiliary channel.

II. BOARD DESCRIPTION

A component diagram of the QS-2000/QS-3000 showing the locations of the 16550 ACEs, clock frequency jumper, auxiliary channel control jumpers, and D-37 and RJ-11 output connectors is shown in figure 1. Channel 1 is controlled by the ACE labeled U5 and jumper J1. Channels 2 - 4 are controlled by ACEs U12, U6, and U13 and jumpers J2, J3, and J4 respectively. The input clock frequency for all channels is selected using jumper J5. All channels are output via the D-37 connector CN1 or the RJ-11 connector CN2 depending on the option selected.

On the QS-2000, the driver circuit consists of two RS-422 drivers (U25 and U32), two RS-422 receivers (U30 and U31) and eight 100_ termination resistors (R5 - R12). On the QS-3000, these are replaced by RS-485 drivers and receivers and 120_ termination resistors.

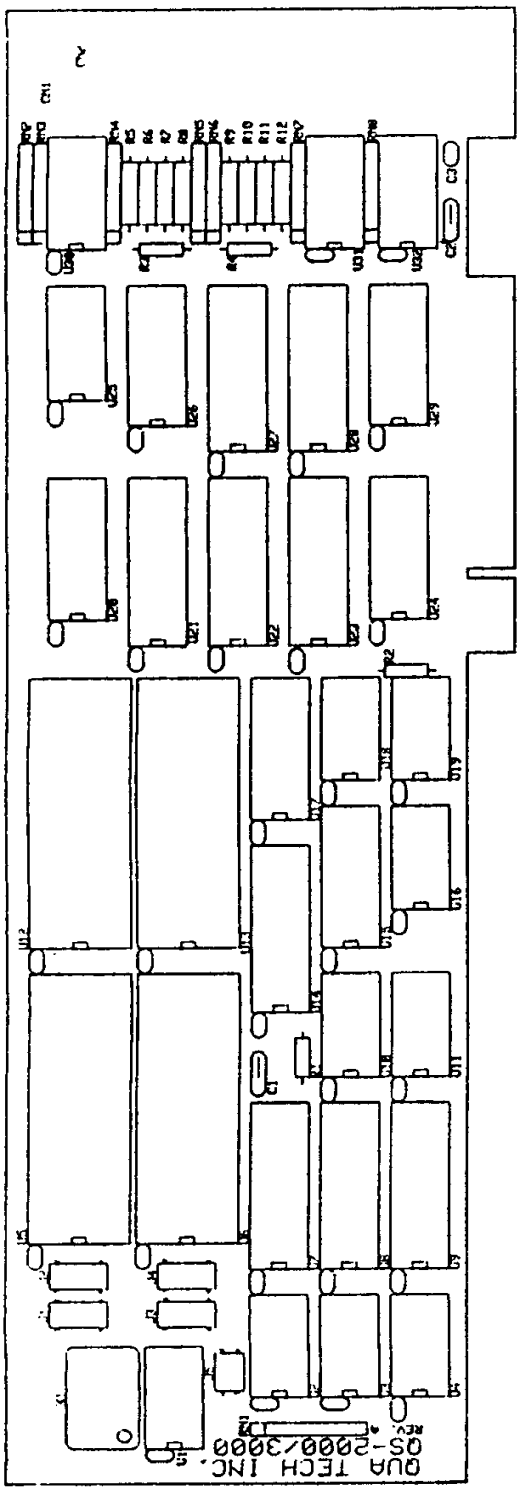


Figure 1. QS-2000/QS-3000 board layout.

III. 16550 FUNCTIONAL DESCRIPTION

The 16550 is an upgrade of the standard 16450 Asynchronous Communications Element (ACE). Designed to be compatible with the 16450, the 16550 enters the character mode on reset and in this mode will appear as a 16450 to user software. An additional mode, FIFO mode, can be selected to reduce CPU overhead at high data rates. The FIFO mode increases performance by providing two internal 16-byte FIFOs (one transmit and one receive) to buffer data and reduce the number of interrupts issued to the CPU.

Other features include:

Programmable baud rate, character length, parity, and number of stop bits

Automatic addition and removal of start, stop, and parity bits

Independent and prioritized transmit, receive and status interrupts

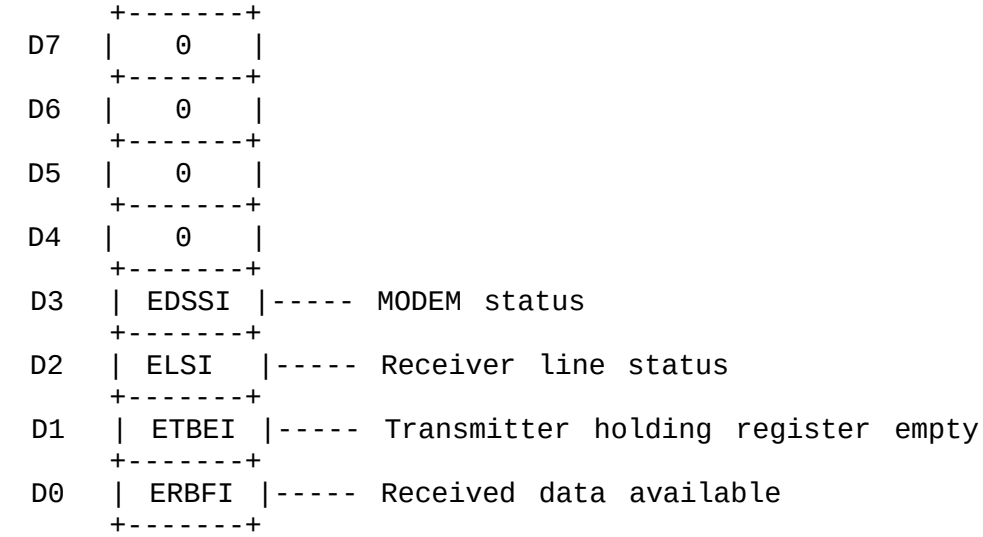
Transmitter clock output to drive receiver logic

The following pages provide a brief summary of the internal registers available within the 16550 ACE. The registers are addressed as shown in figure 2 below.

DLAB	A2	A1	A0	REGISTER DESCRIPTION
0	0	0	0	Receive buffer (read only)
				Transmit holding register (write only)
0	0	0	1	Interrupt enable
x	0	1	0	Interrupt identification (read only)
				FIFO control (write only)
x	0	1	1	Line control
x	1	0	0	MODEM control
x	1	0	1	Line status
x	1	1	0	MODEM status
x	1	1	1	Scratch
1	0	0	0	Divisor latch (least significant byte)
1	0	0	1	Divisor latch (most significant byte)

Figure 2. Internal register map for 16550 ACE. DLAB is accessed through the Line Control Register.

IIIA. INTERRUPT ENABLE REGISTER



CAUTION:
To maintain compatibility with earlier personal computer systems, the user defined output, OUT 2, is used as an external interrupt enable and must be set active for interrupts to be acknowledged. OUT 2 is accessed through the 16550's MODEM control register.

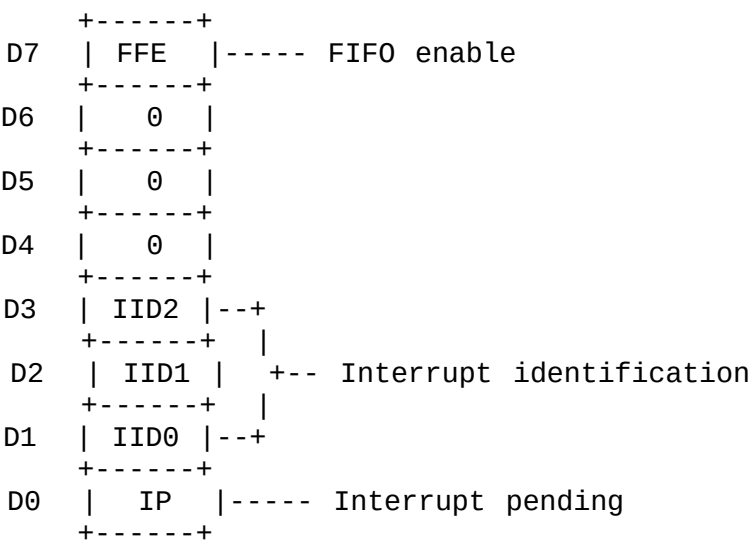
EDSSI - MODEM Status Interrupt:
When set (logic 1), enables interrupt on clear to send, data set ready, ring indicator, and data carrier detect.

ELSI - Receiver Line Status Interrupt:
When set (logic 1), enables interrupt on overrun, parity, and framing errors, and break indication.

ETBEI - Transmitter Holding Register Empty Interrupt:
When set (logic 1), enables interrupt on transmitter register empty.

ERBFI - Received Data Available Interrupt:
When set (logic 1), enables interrupt on received data available or FIFO trigger level.

IIIB. INTERRUPT IDENTIFICATION REGISTER



FFE - FIFO Enable:
When logic 1, indicates FIFO mode enabled.

IIDx - Interrupt Identification:
Indicates highest priority interrupt pending if any. See IP and figure 3. NOTE: IID2 is always a logic 0 in character mode.

IP - Interrupt Pending:
When logic 0, indicates that an interrupt is pending and the contents of the interrupt identification register may be used to determine the interrupt source. See IIDx and figure 3.

IID2	IID1	IID0	IP	Priority	Interrupt Type
x	x	x	1	N/A	None
0	1	1	0	Highest	Receiver Line Status
0	1	0	0	Second	Received Data Ready
1	1	0	0	Second	Character Timeout (FIFO only)
0	0	1	0	Third	Transmitter Holding Register Empty
0	0	0	0	Fourth	MODEM Status

Figure 3. Interrupt identification bit definitions.

Receiver Line Status:
Indicates overrun, parity, or framing errors or break interrupts. The interrupt is cleared by reading the line status register.

Received Data Ready:
Indicates receiver data available. The interrupt is cleared by reading the receiver buffer register

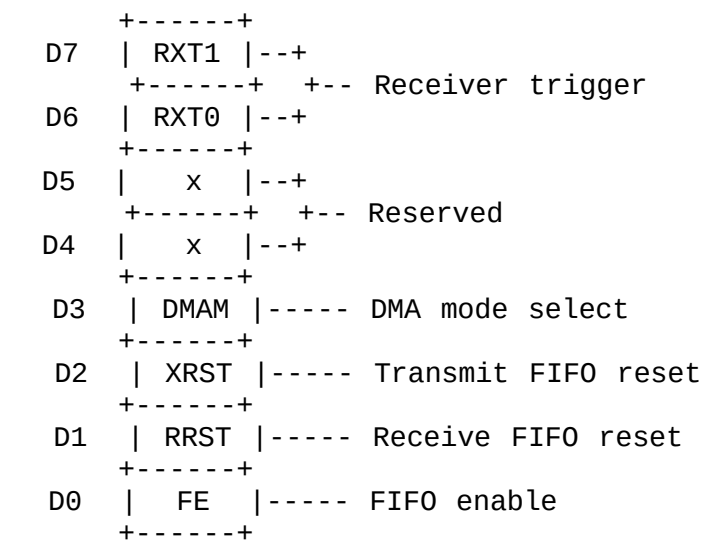
FIFO mode:
Indicates the receiver FIFO trigger level has been reached. The interrupt is reset when the FIFO drops below the the trigger level.

Character Timeout: (FIFO mode only)
Indicates no characters have been removed from or input to the receiver FIFO for the last four character times and there is at least one character in the FIFO during this time. The interrupt is cleared by reading the receiver FIFO.

Transmitter Holding Register Empty:
Indicates the transmitter holding register is empty. The interrupt is cleared by reading the interrupt identification register or writing to the transmitter holding register.

MODEM Status:
Indicates clear to send, data set ready, ring indicator, or data carrier detect have changed state. The interrupt is cleared by reading the MODEM status register.

IIIC. FIFO CONTROL REGISTER



RXTx - Receiver FIFO Trigger Level:
Determines the trigger level for the FIFO interrupt as given in figure 4 below.

RXT1	RXT0	RCVR FIFO Trigger level (bytes)
0	0	1
0	1	4
1	0	8
1	1	14

Figure 4. FIFO trigger levels.

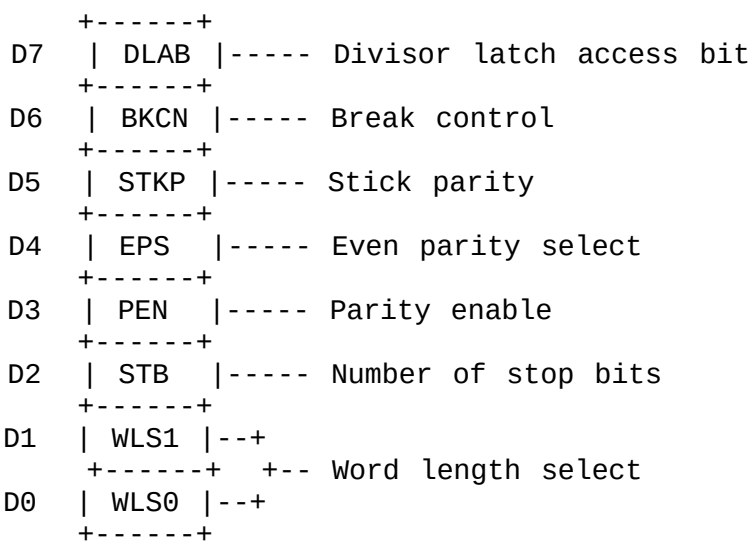
DMAM - DMA Mode Select:
When set (logic 1), RxRDY and TxRDY change from mode 0 to mode 1. (DMA mode is not supported on the QS-2000/QS-3000.)

XRST - Transmit FIFO Reset:
When set (logic 1), all bytes in the transmitter FIFO are cleared and the counter is reset. The shift register is not cleared. XRST is self-clearing.

RRST - Receive FIFO Reset:
When set (logic 1), all bytes in the receiver FIFO are cleared and the counter is reset. The shift register is not cleared. RRST is self-clearing.

FE - FIFO Enable:
When set (logic 1), enables transmitter and receiver FIFOs. When cleared (logic 0), all bytes in both FIFOs are cleared. This bit must be set when other bits in the FIFO control register are written to or the bits will be ignored.

IIID. LINE CONTROL REGISTER



DLAB - Divisor Latch Access Bit:
DLAB must be set to logic 1 to access the baud rate divisor latches. DLAB must be set to logic 0 to access the receiver buffer, transmitting holding register and interrupt enable register.

BKCN - Break Control:
When set (logic 1), the serial output (SOUT) is forced to the spacing state (logic 0).

STKP - Stick Parity:
Forces parity to logic 1 or logic 0 if parity is enabled. See EPS, PEN, and figure 5.

EPS - Even Parity Select:
Selects even or odd parity if parity is enabled. See STKP, PEN, and figure 5.

PEN - Parity Enable:
Enables parity on transmission and verification on reception. See EPS, STKP, and figure 5.

STKP	EPS	PEN	Parity
x	x	0	None
0	0	1	Odd
0	1	1	Even
1	0	1	Logic 1
1	1	1	Logic 0

Figure 5. 16550 parity selections.

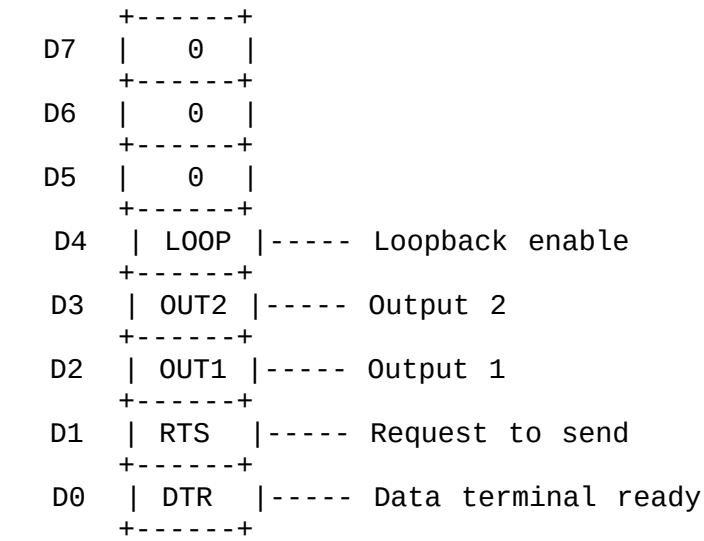
STB - Number of Stop Bits:
Sets the number of stop bits transmitted. See WLSx and figure 6.

WLSx - Word Length Select:
Determines the number of bits per transmitted word. See STB and figure 6.

STB	WLS1	WLS0	Word length	Stop bits
0	0	0	5 bits	1
0	0	1	6 bits	1
0	1	0	7 bits	1
0	1	1	8 bits	1
1	0	0	5 bits	1½
1	0	1	6 bits	2
1	1	0	7 bits	2
1	1	1	8 bits	2

Figure 6. Word length and stop bit selections.

IIIE. MODEM CONTROL REGISTER



LOOP - Loopback Enable:
When set (logic 1), the transmitter shift register is connected directly to the receiver shift register. The MODEM control inputs are internally connected to the MODEM control outputs and the outputs are forced to the inactive state.

Bits OUT2, OUT1, RTS, and DTR perform identical functions on their respective outputs. When these bits are set (logic 1) in the register, the associated output is forced to a logic 0. When cleared (logic 0), the output is forced to logic 1.

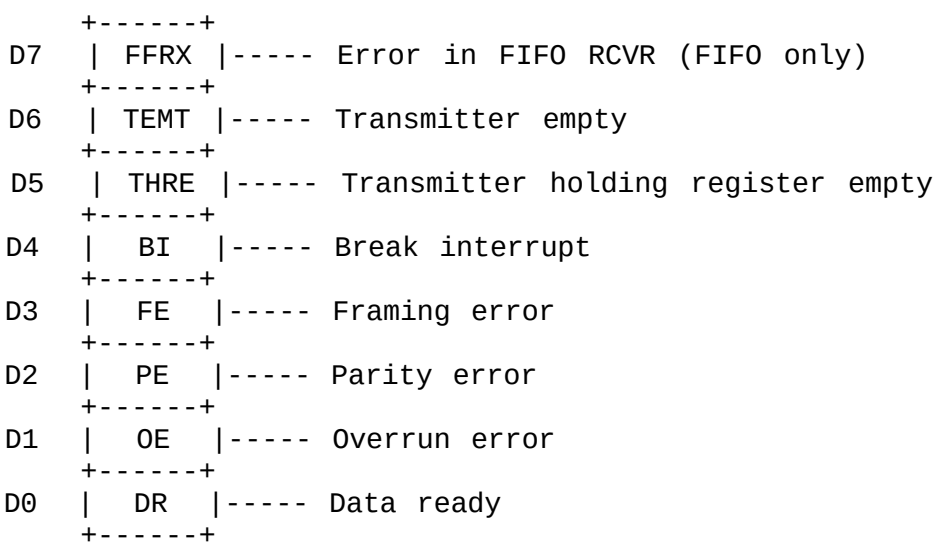
OUT2 - Output 2:
Controls the OUT2 output as described above. To maintain compatibility with earlier personal computer systems, OUT2 is used as an external interrupt enable and must be set active for interrupts to be acknowledged.

OUT1 - Output 1:
Controls the OUT1 output as described above.

RTS - Request To Send:
Controls the RTS output as described above.

DTR - Data Terminal Ready:
Controls the DTR output as described above. This bit is used to control the line drivers for half duplex operation. See section IX.

IIIF. LINE STATUS REGISTER



FFRX - FIFO Receiver Error:
Always logic 0 in character mode.
FIFO mode:
Indicates one or more parity errors, framing errors, or break indications in the receiver FIFO. FFRX is reset by reading the line status register.

TEMT - Transmitter Empty:
Indicates the transmitter holding register (or FIFO) and the transmitter shift register are empty and are ready to receive new data. TEMT is reset by writing a character to the transmitter holding register.

THRE - Transmitter Holding Register Empty:
Indicates the transmitter holding register (or FIFO) is empty and it is ready to accept new data. THRE is reset by writing data to the transmitter holding register (or FIFO).

Bits BI, FE, PE, and OE are the sources of receiver line status interrupts. The bits are reset by reading the line status register. In FIFO mode, these bits are associated with a specific character in the FIFO and the exception is revealed only when that character reaches the top of the FIFO.

BI - Break Interrupt:
Indicates the receive data input has been in the spacing state (logic 0) for longer than one full word transmission time.
FIFO mode:
Only one zero character is loaded into the FIFO and transfers are disabled until SIN goes to the mark state (logic 1) and a valid start bit is received.

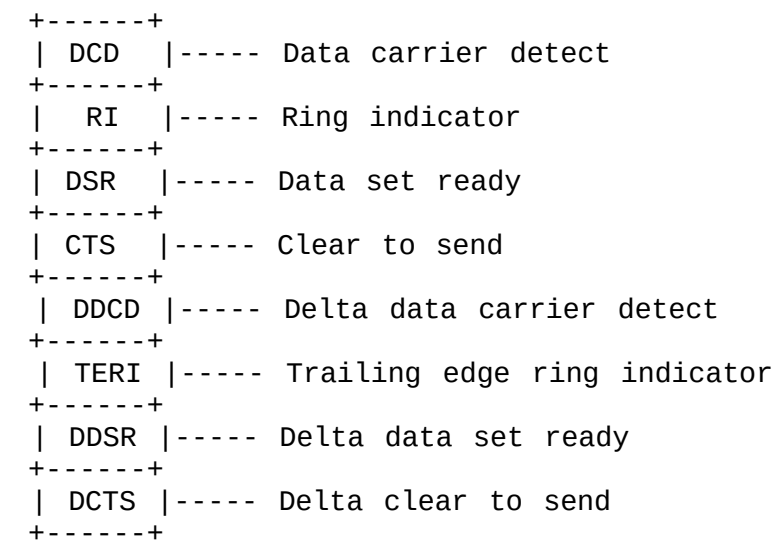
FE - Framing Error:
Indicates the received character had an invalid stop bit. The stop bit following the last data or parity bit was a 0 bit (spacing level).

PE - Parity Error:
Indicates that the received data does not have the correct parity.

OE - Overrun Error:
Indicates the receive buffer was not read before the next character was received and the character is destroyed.
FIFO mode:
Indicates the FIFO is full and another character has been shifted in. The character in the shift register is destroyed but is not transferred to the FIFO.

DR - Data ready:
Indicates data is present in the receive buffer or FIFO. DR is reset by reading the receive buffer register or receiver FIFO.

IIIG. MODEM STATUS REGISTER



DCD - Data Carrier Detect:
Complement of the DCD input.

RI - Ring Indicator:
Complement of the RI input.

DSR - Data Set Ready:
Complement of the DSR input.

CTS - Clear To Send:
Complement of the CTS input.

Bits DDCD, TERI, DDSR, and DCTS are the sources of MODEM status interrupts. These bits are reset when the MODEM status register is read.

DDCD - Delta Data Carrier Detect:
Indicates the Data Carrier Detect input has changed state.

TERI - Trailing Edge Ring Indicator:
Indicates the Ring Indicator input has changed from a low to a high state.

DDSR - Delta Data Set Ready:
Indicates the Data Set Ready input has changed state.

DCTS - Delta Clear To Send:
Indicates the Clear to Send input has changed state.

IIIH. SCRATCHPAD REGISTER

This register is not used by the 16550. It may be used by the programmer for data storage.

IV. FIFO INTERRUPT MODE OPERATION

1. The receive data interrupt is issued when the FIFO reaches the trigger level. The interrupt is cleared as soon as the FIFO falls below the trigger level.

CAUTION:
To maintain compatibility with earlier personal computer systems, the user defined output, OUT 2, is used as an external interrupt enable and must be set active for interrupts to be acknowledged. OUT 2 is accessed through the 16550's MODEM control register.

2. The interrupt identification register's receive data available indicator is set and cleared along with the receive data interrupt above.

3. The data ready indicator is set as soon as a character is transferred into the receiver FIFO and is cleared when the FIFO is empty.

V. BAUD RATE SELECTION

The 16550 ACE determines the baud rate of the serial output from a combination of the clock input frequency and the value written to the divisor latches. Standard PC, PC/XT, PC/AT, and PS/2 serial interfaces use an input clock of 1.8432 MHz. To increase versatility, the QS-2000/QS-3000 uses an 18.432 MHz clock and a frequency divider circuit to produce the standard clock frequency.

Jumper block J5 is used to set the input frequency to the 16550. It may be connected to divide the clock input by 1, 2, 5, or 10. To maintain compatibility with adapters using a 1.8432 MHz input, J5 should be configured to divide by 10 as shown in figure 7(d). A table of divisor latch values for various input frequencies is given in figure 8.

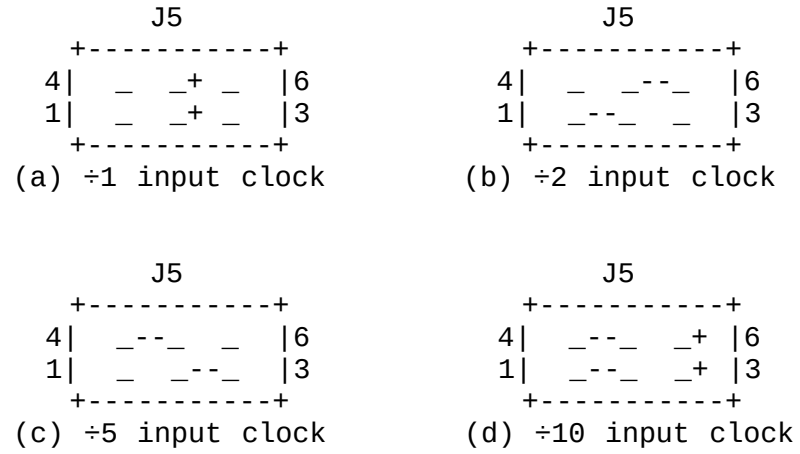


Figure 7. Input clock frequency options. For compatibility, the jumper should be set at ÷10 (18.432 MHz ÷ 10 = 1.8432 MHz).

Baud Rate	Divisor latch value ÷10	÷5	÷2	÷1
110	1,047	2,094	5,236	10,473
300	384	768	1,920	3,840
600	192	384	960	1,920
1,200	96	192	480	960
2,400	48	96	240	480
3,600	32	64	160	320
4,800	24	48	120	240
9,600	12	24	60	120
19,200	6	12	30	60

Figure 8. Divisor latch settings for common baud rates using an 1.8432 MHz input clock. For compatibility, connect jumper in the divide by 10 configuration (figure 7(d)).

VI. ADDRESSING

Each channel of the QS-2000/QS-3000 uses eight consecutive I/O address locations beginning on any even eight byte boundary (xxx0H - xxx7H) or (xxx8H - xxxFH). The 16550 uses these addresses as shown in figure 2.

Two addressing modes are available: discrete addressing and block addressing. Each of these modes will be discussed separately.

Discrete Addressing Mode

In the discrete addressing mode, each port may choose an individual base address. This mode allows maximum compatibility with software supporting the pre-defined addresses for Serial 1 through Serial 8. Channels 1 and 2 may select from Serial 1 through Serial 7, Channels 3 and 4 may choose from Serial 2 through Serial 8. Each channel may be individually disabled.

Block Addressing Mode

In block addressing mode, the four serial channels are arranged to form a continuous 32-byte block of I/O addresses. This mode offers more compact addressing for software applications supporting communications beyond the Serial 1 - Serial 8 limitations. The block may be placed anywhere in the available I/O address range on an even 32-byte boundary (e.g. 400H-41FH, 620-63FH, 4980H-499FH) using the IBM installation utilities and the Qua Tech address installation utility QTINSTAL.EXE.

WARNING:
In block mode, each channel may be individually disabled, but the I/O space assigned to that channel is still considered in use and may not be used by another device.

Channel	Address range
1	Base+ 0 --> Base+ 7
2	Base+ 8 --> Base+15
3	Base+16 --> Base+23
4	Base+24 --> Base+31

Figure 9. Block mode address assignments.

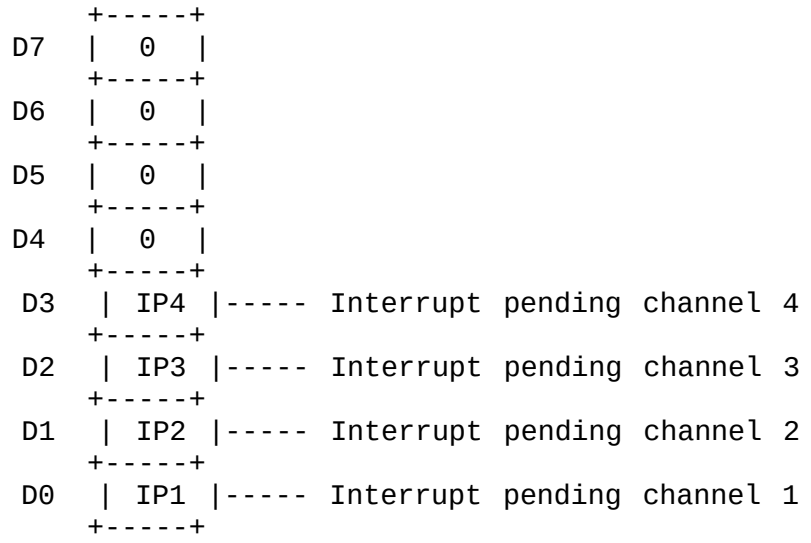
VII. INTERRUPTS

The QS-2000/QS-3000 has support for three interrupt levels: IRQ 3, IRQ 4, and IRQ 9. During the installation process, one pair of interrupts must be selected, either IRQ 3 and IRQ 4, or IRQ 3 and IRQ 9. Each channel may then choose an interrupt from the selected pair. If interrupts are being shared, the interrupt pending bit in the 16550's interrupt identification register or the interrupt pending bits in the interrupt status register should be used to test for the source of the interrupt.

CAUTION:

To maintain compatibility with earlier personal computer systems, the user defined output, OUT 2, is used as an external interrupt enable and must be set active for interrupts to be acknowledged. OUT 2 is accessed through the 16550's MODEM control register.

Interrupt Status Register



An interrupt status register has been implemented to ease software burden associated with the interrupt sharing process. An interrupt status bit (IPx) will be set (logic 1) if there is an interrupt pending in the 16550 and the associated OUT 2 line (interrupt enable) is active.

When selected during the configuration process, the interrupt status register is accessed by reading any of the 16550 scratchpad registers. The interrupt status register is read only.

NOTE:
When enabled, the interrupt status register will override the 16550's internal scratchpad register. Since the BIOS tests the scratchpad register during initialization, the channels may not appear in the system's equipment list on power-up. If the equipment list is updated through user software, the operating system should accept and use the channel.

VIII. PROGRAMMABLE OPTION SELECT

The IBM PS/2 family of computers using the Micro-Channel bus structure utilize on board registers referred to as the Programmable Option Select (POS) registers to hold the adapter's configuration information. The first two POS registers hold a unique adapter identification number that has been issued to Qua Tech for the QS-2000/QS-3000. This number is defined in hardware and can not be changed. These registers are read only.

The remaining POS registers are used for address and interrupt selections. Three additional POS registers are implemented on the QS-2000/QS-3000. These registers are programmed by the user through the IBM installation utility supplied with the PS/2 and the Qua Tech address installation software QTINSTAL.EXE. These registers are read/write but should not be written to by user software. The bit definitions of the registers are given in figure 10.

PROGRAMMABLE OPTION SELECT

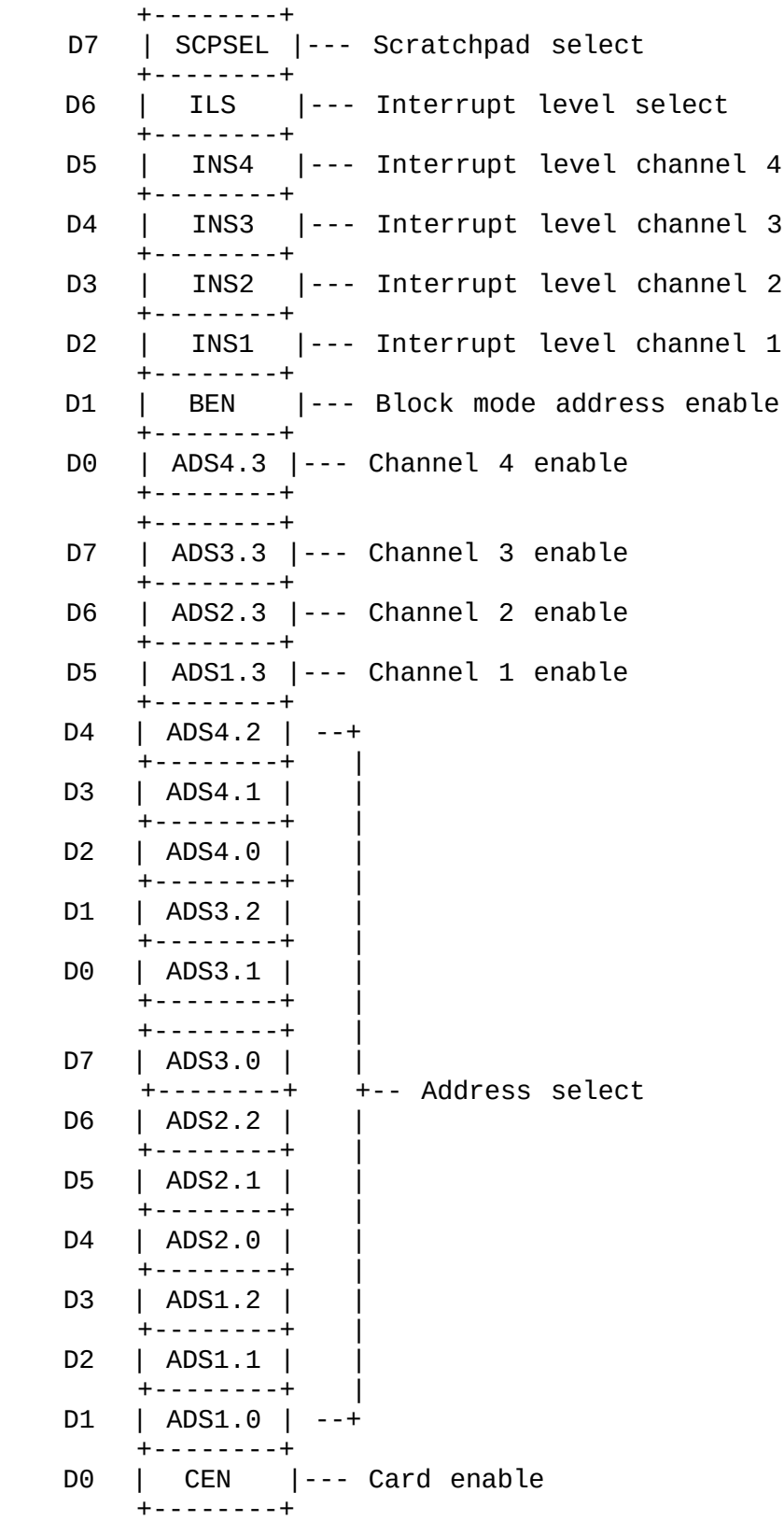


Figure 10. QS-2000/QS-3000 POS implementation.

ADSx.3	ADSx.2	ADSx.1	ADSx.0	Base address
0	x	x	x	Disabled
1	0	0	0	03F8H (Serial 1)
1	0	0	1	02F8H (Serial 2)
1	0	1	0	3220H (Serial 3)
1	0	1	1	3228H (Serial 4)
1	1	0	0	4220H (Serial 5)
1	1	0	1	4228H (Serial 6)
1	1	1	0	5220H (Serial 7)
1	1	1	1	5228H (Serial 8)

Figure 11. QS-2000/QS-3000 discrete mode address options.

ILS INSx	Interrupt
0 0	IRQ 3
0 1	IRQ 4
1 0	IRQ 3
1 1	IRQ 9

Figure 12. QS-2000/QS-3000 interrupt options.

The bits labeled ADSx.x in figure 10 contain the address decoding information. In discrete addressing mode, these bits form a three bit code for each channel as defined in figure 11. In block addressing mode, bits ADS4.1 - ADS1.0 directly correspond to address lines A15 - A5. For example, if the adapter is in block addressing mode with a base address of 5620H, the POS would appear as follows:

5	6	2	0H
0101	0110	0010	0000B

ADS4.2	-->	unused			ADS2.3	-->	A10	= 1
ADS4.1	-->	A15	=	0	ADS2.2	-->	A9	= 1
ADS4.0	-->	A14	=	1	ADS2.1	-->	A8	= 0
ADS3.2	-->	A13	=	0	ADS2.0	-->	A7	= 0
ADS3.1	-->	A12	=	1	ADS1.2	-->	A6	= 0
ADS3.0	-->	A11	=	0	ADS1.1	-->	A5	= 1

Once the addressing has been established, POS bits ADS1.3, ADS2.3, ADS3.3, and ADS4.3 are used to enable or disable channels 1 - 4 respectively. In discrete addressing mode, the addresses allocated for the disabled channel may be issued to another device. In block addressing mode, however, the address locations used by the disabled channel are still allocated to the QS-2000/QS-3000 and may not be used by another device.

Interrupt levels are assigned independently for each channel of the QS-2000/QS-3000. A channel's interrupt level is determined by first selecting an interrupt pair for the adapter using the ILS bit and then selecting the channel interrupt using bits INS1 - INS4 for channels 1 - 4 respectively. The interrupt choices for each channel are listed in figure 12.

The final POS option is the Scratchpad/Interrupt status register selection. When SCPSEL is set to logic 0, the 16550 internal scratchpad registers are enabled for complete serial port compatibility. When set to logic 1, the scratchpad registers are overridden by the interrupt status register as described in section VII.

NOTE:

When enabled, the interrupt status register will override the 16550's internal scratchpad register. Since the BIOS tests the scratchpad register during initialization, the channels may not appear in the system's equipment list on power-up. If the equipment list is updated through user software, the operating system should accept and use the channel.

IX. OUTPUT CONFIGURATIONS

Four sets of jumpers are implemented on the QS-2000/QS-3000 to control the auxiliary driver/receiver set. J1 through J4 perform the identical functions on channels 1 through 4 respectively.

Auxiliary Channel Configuration

The following discussion pertains to the control of the information exchanged on the auxiliary channel of the QS-2000/QS-3000. Since the auxiliary channel is not supported with the RJ-11 connector option, these users should set jumpers J1-J4 to loopback all of the auxiliary channel signals (figures 14 and 17) and skip to "Half Duplex Operation" on page 23.

The function of J1 through J4 is to control the source of the information exchanged on the auxiliary communication lines. The output sources are request to send (RTS), transmit clock (XCLK), and the auxiliary input (AUX IN). The inputs are clear to send (CTS) and receive clock (RCLK).

Transmission of RTS, when combined with reception of CTS, allows for handshaking between the 16550 and a peripheral device. RTS is transmitted by connecting pins 5 and 6 of the jumper block (figure 15). CTS is received by connecting pins 1 and 2 (figure 15). The RTS/CTS handshake can be defeated by looping the RTS output back to the CTS input. This is accomplished by connecting pins 1 and 5 (figures 16 and 17).

RCLK is the input to the 16550 that controls the shift rate of the receiver portion of the chip. Generally, this input is provided by connecting it to the transmit clock, XCLK, output from the ACE. This is accomplished by connecting pins 3 and 7 of the jumper (figures 15 and 17). RCLK may be received from an external source by connecting pins 2 and 3 (figure 16).

Transmission of XCLK can be used to synchronize communications with a peripheral or to provide a shift clock to a receiver. XCLK is transmitted by connecting pins 6 and 7 of the jumper block (figure 16).

AUX IN is the auxiliary input from a peripheral device. Connecting AUX IN to AUX OUT provides a loopback mode of operation. That is, whatever is transmitted by the peripheral will be fed back to the peripheral. This is implemented by connecting pins 2 and 6 of the jumper block (figure 17).

Half Duplex Operation

The other function of J1 through J4 is to configure the communication channel in half or full duplex mode. Half duplex operation is achieved by connecting pins 4 and 8 of the jumper block (figure 17). This connection allows the transmitter to be enabled and disabled by using the data terminal ready (DTR) output controlled through the modem control register of the 16550. When DTR is set (logic 1), the transmitter driver is enabled for both the data and auxiliary channel output. When cleared (logic 0), both outputs enter a high impedance state. Full duplex communication is restored by removing the jumper on pins 4 and 8 (figures 15 and 16).

CAUTION: When operating in half duplex mode, the transmitter must be disabled before receiving any information. Failure to do so will result in two output drivers being connected together which may cause damage to the adapter, the computer, and/or the peripheral equipment.

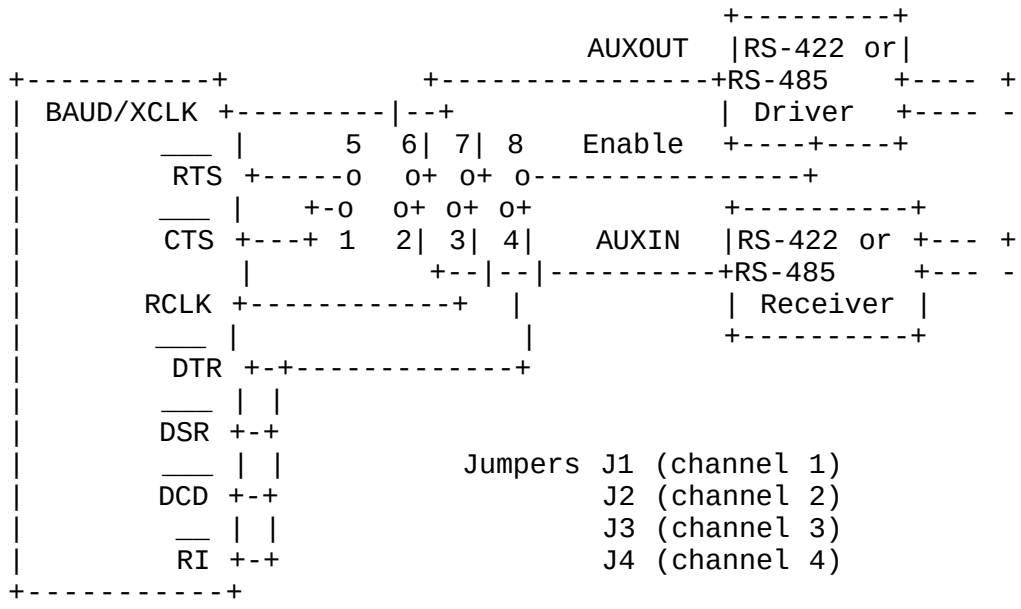
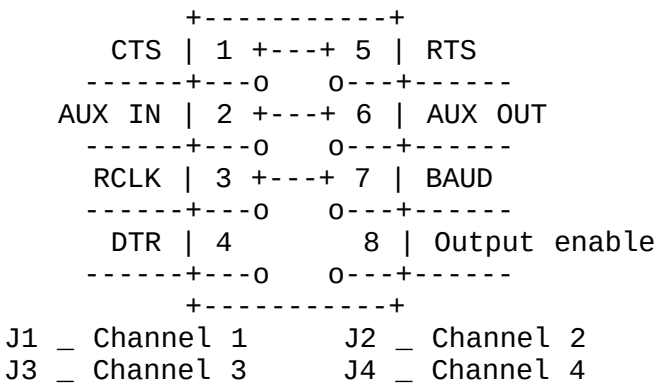


Figure 13. Output Control Block Diagram. (Pin numbers are for all channels.)



Function	Connect	Disconnect
RTS/CTS loopback *	1-5	1-2
Transmit RTS	5-6	6-7
Receive CTS	1-2	2-3
RCLK/XCLK loopback *	3-7	2-3
Transmit XCLK	6-7	5-6
Receive RCLK	2-3	1-2
AUX OUT/AUX IN loopback *	2-6	5-6,6-7
Half duplex	4-8	
Full duplex *		4-8

*Indicates factory jumper settings.

Figure 14. J1 - J4 Jumper Layout and Settings.

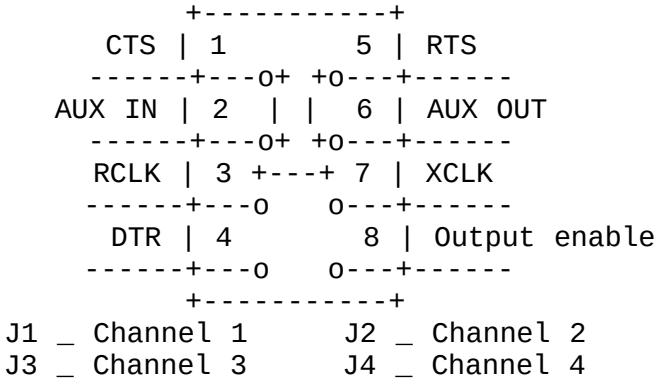


Figure 15. Jumper configuration showing:
(1) RTS transmission
(2) CTS reception
(3) XCLK/RCLK loopback
(4) Full duplex operation

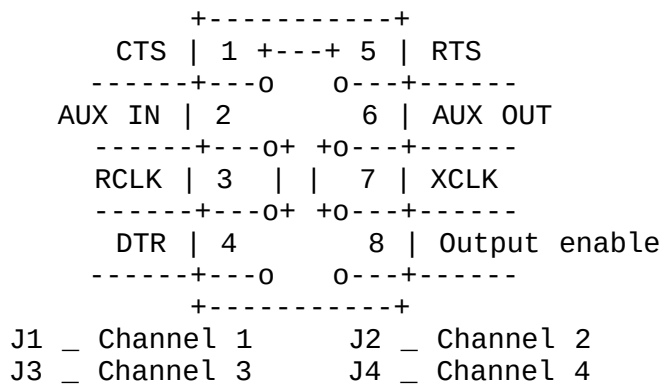


Figure 16. Jumper configuration showing:
(1) RTS/CTS loopback
(2) XCLK transmission
(3) RCLK reception
(4) Full duplex operation

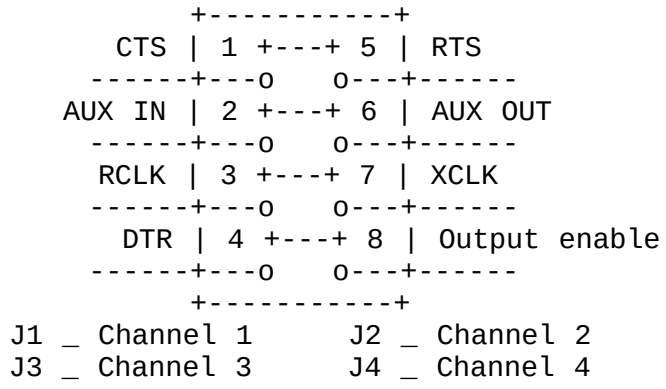


Figure 17. Jumper configuration showing:
(1) RTS/CTS loopback
(2) XCLK/RCLK loopback
(3) AUX OUT/AUX IN loopback
(4) Half duplex operation

NOTE: Since the auxiliary channel is not supported with the RJ-11 connector option, these users should set jumpers J1-J4 to loopback all of the auxiliary channel signals (figures 14 and 17). Half duplex operation is still supported for the data channel output.

X. EXTERNAL CONNECTIONS

The QS-2000/QS-3000 is available with two output configurations. The first option uses a female D-37 connector labeled CN1 on the circuit board. This configuration provides all of the signals for each channel. The second option uses a quad 6-wire RJ-11 phone jack style connector labeled CN2 on the circuit board. This configuration provides only transmit and receive. Both output configurations have optional adapter cables to provide D-25 connectors for each channel. The various connectors and pinouts are given in the figures below.

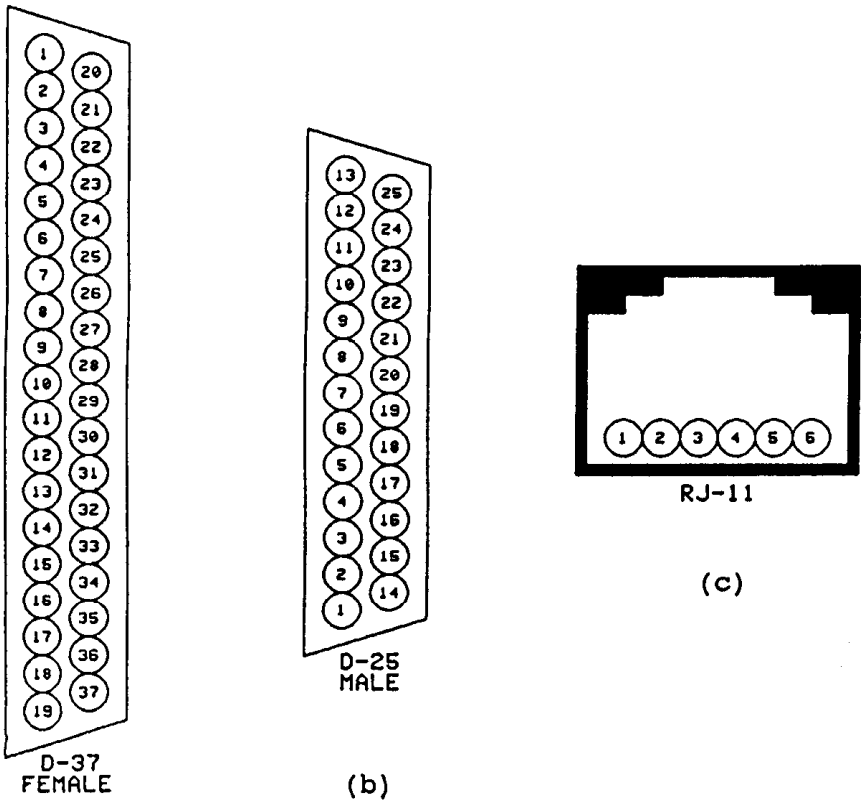


Figure 18. QS-2000/QS-3000 output connectors.

	CHANNEL 1			CHANNEL 2		
SIGNAL	D-37	RJ-11	D-25	D-37	RJ-11	D-25
TxD+	24	1	2	10	1	2
TxD-	5	2	3	28	2	3
RxD+	23	4	4	9	4	4
RxD-	4	5	5	27	5	5
AUXOUT+	21	---	20	7	---	20
AUXOUT-	22	---	6	8	---	6
AUXIN+	20	---	22	6	---	22
AUXIN-	2	---	8	25	---	8
GND	3	3,6	7	26	3,6	7

	CHANNEL 3			CHANNEL 4		
SIGNAL	D-37	RJ-11	D-25	D-37	RJ-11	D-25
TxD+	33	1	2	19	1	2
TxD-	14	2	3	37	2	3
RxD+	32	4	4	18	4	4
RxD-	13	5	5	36	5	5
AUXOUT+	30	---	20	16	---	20
AUXOUT-	31	---	6	17	---	6
AUXIN+	29	---	22	15	---	22
AUXIN-	11	---	8	34	---	8
GND	12	3,6	7	35	3,6	7

Figure 19. Connector definitions. Pins not listed are not connected.

NOTE: Since the auxiliary channel is not supported with the RJ-11 connector option, these users should set jumpers J1-J4 to loopback all of the auxiliary channel signals (figures 14 and 17). Half duplex operation is still supported for the data channel output.

XI. HARDWARE INSTALLATION

Make sure there is a back-up copy of the original IBM PS/2 reference diskette available. A copy of the reference disk must be used for the installation process as the diskette must be modified to accept any option adapters.

1. Turn system on and allow to boot.
2. Insert the QS-2000/QS-3000 distribution disk into drive A and change the default drive to A.
3. Execute:
   QS-2000 BLOCK for block address mode
   QS-2000 DISCRETE for discrete address mode
   See section VI for descriptions of addressing modes.
4. Turn unit off.
5. Remove system cover as instructed in the IBM Quick Reference Guide.
6. Insert adapter into any vacant slot following the guidelines for installing an optional adapter in the IBM Quick Reference Guide.
7. Replace system cover.
8. Turn unit on and insert a COPY of the IBM PS/2 reference diskette into drive A.
9. Respond "N" at automatic configuration prompt.
10. Select "Copy an option diskette" and follow copying instructions.
11. Select "Set configuration"
12. Select "Change configuration" or "Run automatic configuration" and follow installation instructions.

NOTE: When installing the QS-2000/QS-3000 for block mode addressing, if the desired address is not available in the configuration routine, select any non-conflicting address and continue with Additional Block Mode Addressing (section XIII).

After the initial installation, the copy of the reference diskette will contain the configuration file for the QS-2000/QS-3000. Subsequent re-installation may omit step 10 and a "Y" response may be given during step 9 (automatically configure system) if desired.

XII. CHANGING ADDRESSING MODES

Make sure there is a copy of the original IBM PS/2 reference diskette available. This diskette must be modified to accept any option adapters.

The QS-2000/QS-3000 may be addressed in discrete or block addressing modes as discussed in section VI. If the addressing mode is to be changed, the existing configuration must be purged from the configuration memory. The alternate addressing information may then be entered into configuration memory. The procedure is as follows:

1. Turn unit off.
2. Remove system cover as instructed in the IBM Quick Reference Guide.
3. Remove the adapter from the system following the guidelines for removing an option adapter in the IBM Quick Reference Guide.
4. Turn unit on and insert a COPY of the IBM PS/2 reference diskette into drive A.
5. Respond "Y" at automatic configuration prompt.
6. Exit the IBM installation procedure and restart the computer.

At this point the QS-2000/QS-3000 configuration has been purged from the configuration memory. The installation procedure (section XI of this document) may now be used to select the addressing mode and enter the new configuration information.

XIII. ADDITIONAL BLOCK MODE ADDRESSES

The QS-2000/QS-3000 block addressing mode supports the entire I/O address range of the PS/2 occupying 32 consecutive I/O locations. This produces 2K possible choices for base address location. Since it would not be feasible or practical to provide all of these choices in the configuration file, 25 addresses have been selected for inclusion in the file. An address installation utility (QTINSTAL.EXE) has been included on the distribution diskette to facilitate the address installation process. QTINSTAL should be used ONLY if the desired block mode base address cannot be found through the IBM installation utilities.

WARNING:
QTINSTAL must only be used when the QS-2000/QS-3000 has been installed and configured for BLOCK addressing mode. Executing QTINSTAL in discrete mode will cause unpredictable results and may destroy the contents of the adapter description file.

1. Insert the QS-2000/QS-3000 distribution disk in drive A.
2. Execute QTINSTAL.
3. Select the QS-2000/QS-3000 by using the cursor keys to highlight the selection and press <enter>. See figure 20.
4. At the prompt, insert the back-up copy of the IBM PS/2 reference in drive A.
5. Select an address to change by using the cursor keys to highlight the address and press <enter>. (Addresses will appear in ascending order.) See figure 21.
6. Enter the desired address in hex, decimal, or binary (hex is the default radix). See figure 22.
7. Repeat steps 5 and 6 as necessary.
8. Press <esc> to exit the address menu.
9. Press <enter> to save configuration changes. (A back-up copy of the configuration file will be generated.)
   - OR -
Press <esc> to exit without saving changes.
10. Press <esc> to exit the board selection menu.
11. Press <esc> to return to DOS. The configuration file is modified but the system configuration is not updated.
    - OR -
Press <enter> to enter the IBM installation utilities and update the system configuration.

XIV. SPECIFICATIONS

Bus interface: IBM MicroChannel 16-bit bus
Controller: NS-16550-A
Interface: Female D-37 connector
Quad 6-wire RJ-11 (optional)
Transmit drivers: MC3487
Receive buffers: MC3486
I/O Address range
Discrete mode: Serial 1 - Serial 8 Interrupt levels: IRQ 3,4,9

Block mode: 0000H - FFFFH

Power requirements:

D-37 option		RJ-11 option		
IT	IMS	IT	IMS	Supply
1425mA	1618mA	1372mA	1566mA	+5 Volts
--	--	--	--	+12 Volts
--	--	--	--	-12 Volts

I_T - Typical adapter current
I_{MS} - Maximum statistical adapter current

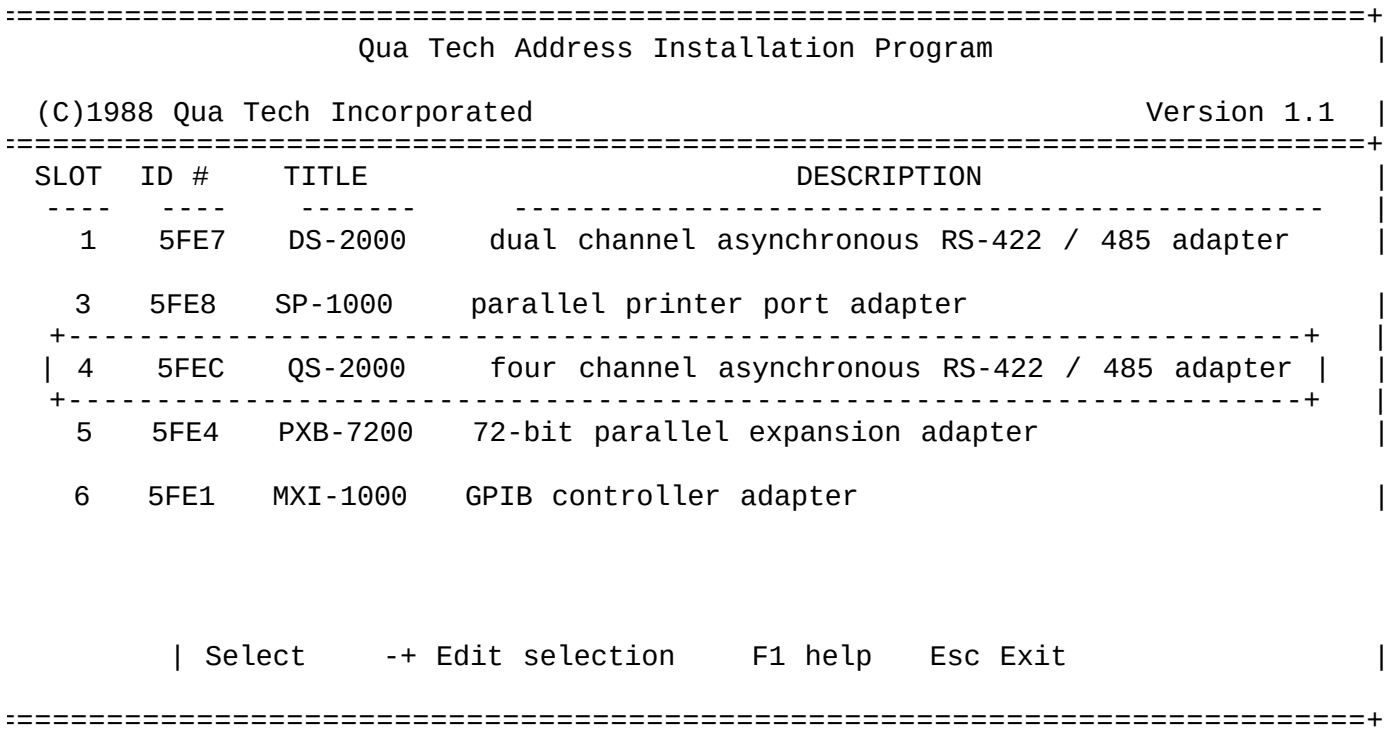


Figure 20. QTINSTAL.EXE opening menu. Outline indicates QS-2000/QS-3000 selected.

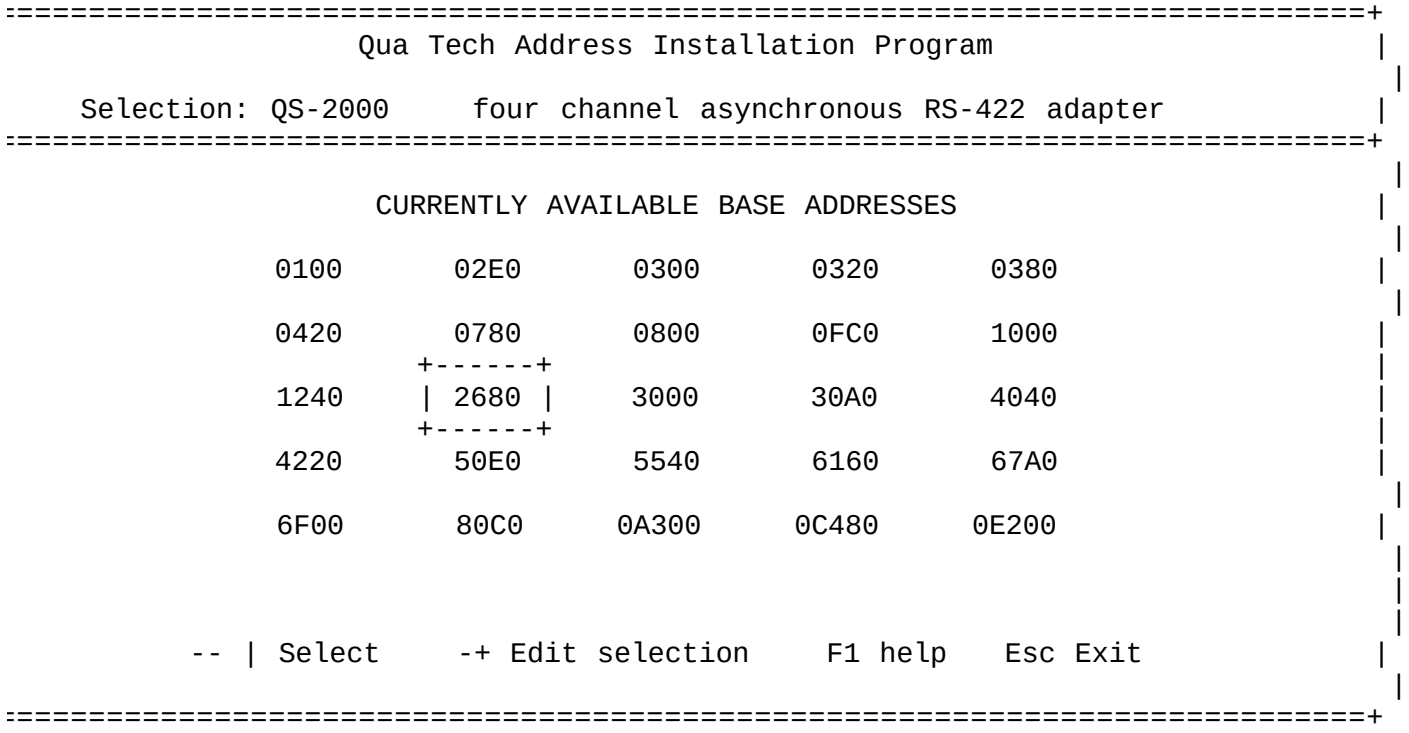


Figure 21. QTINSTAL.EXE address selection menu. Outline indicates address 2680H selected for change.

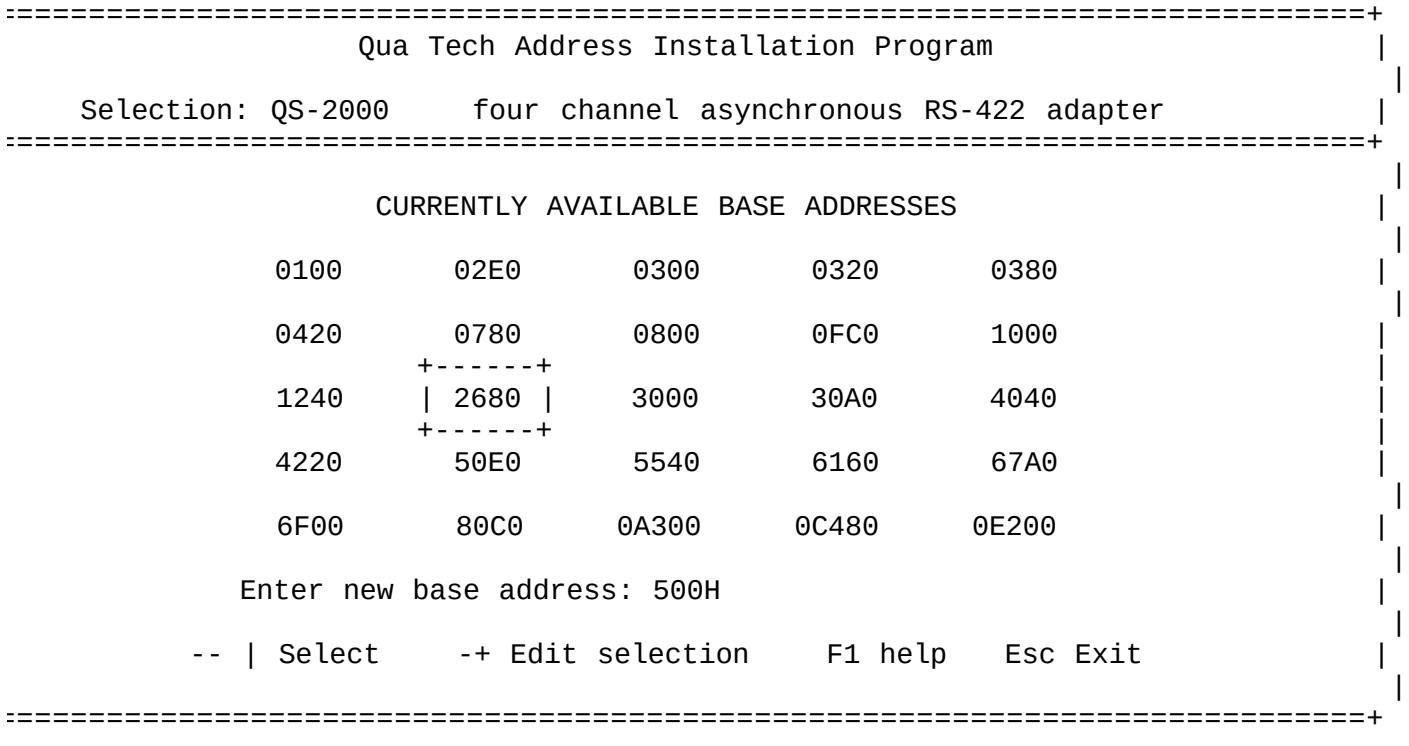


Figure 22. Address selection menu showing input prompt. Input indicates 500H being substituted for 2680H.

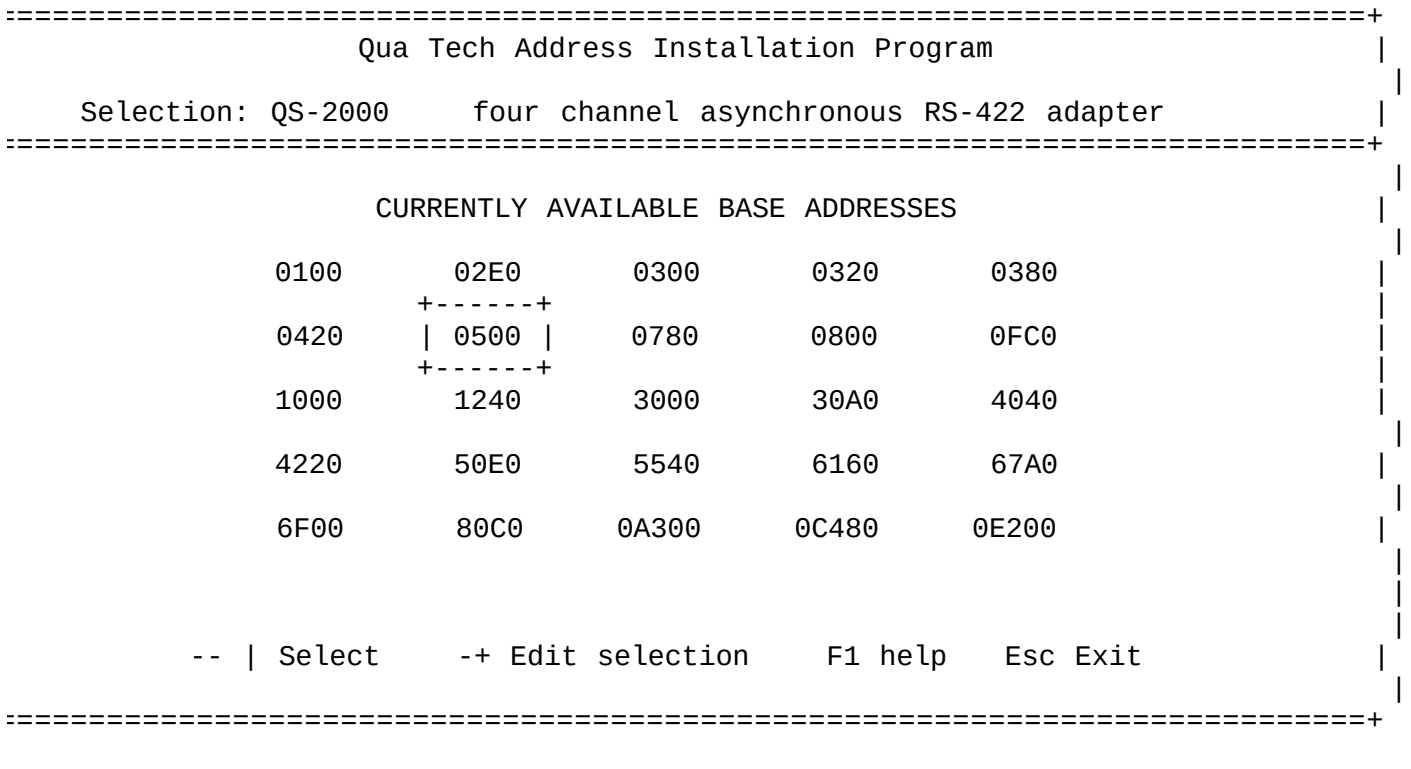


Figure 23. Address selection menu after modifications. Outline highlights the new selection.