P55C Micro-Architecture – The First Implementation of the MMX™ Technology

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August 20, 1996

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Outline

- **Micro Architecture Overview**
  - Instruction Decode
  - Pairing
  - MMX™ Technology Execution Units
  - Pipeline
- **Performance**
- **Summary**

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Implementation Goals and Challenges

- **Significant performance improvement of multimedia and communications applications**

- **No impact on device speed**

- **Maximize usage of existing micro-architecture**
  - New instructions to decode
  - Unique execution units

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MMX™ Technology Implementation
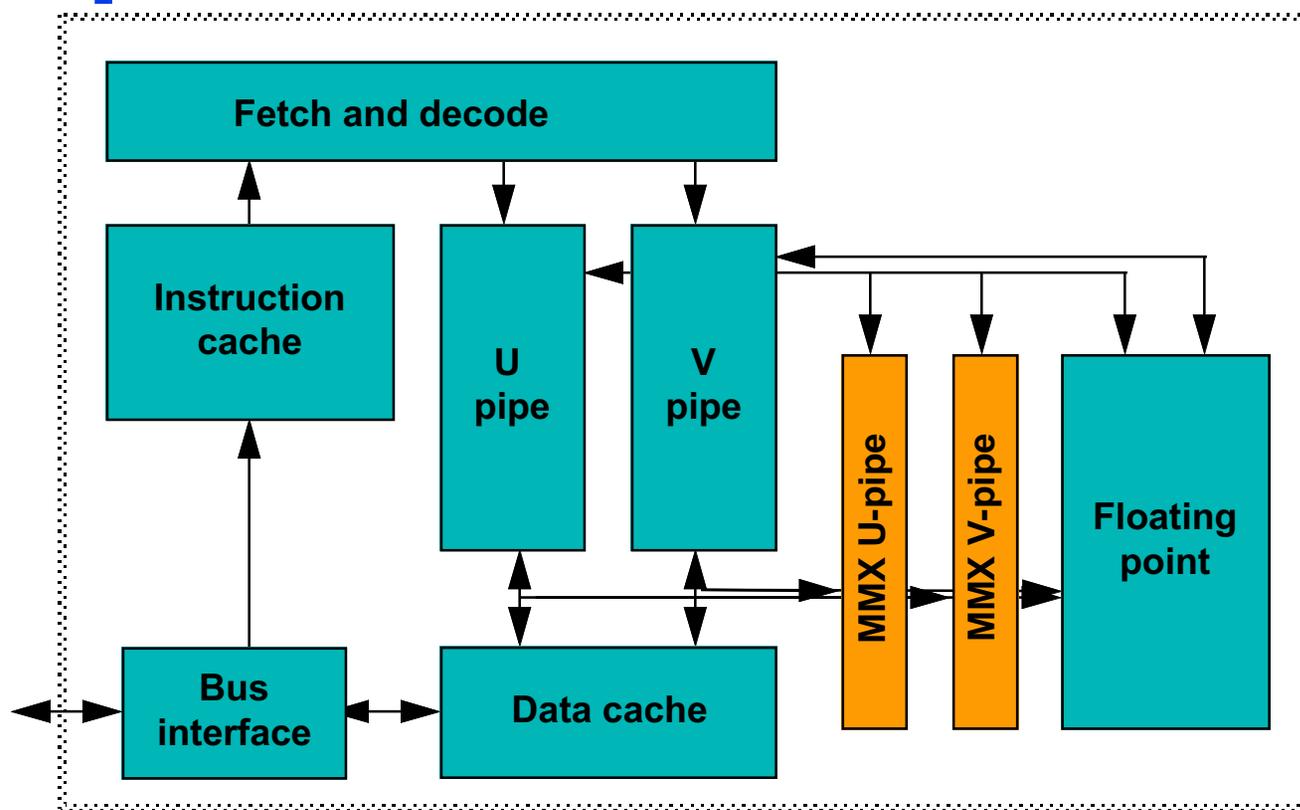
MMX™ Technology Added in Parallel to the Existing Integer and FP H/W

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Decoding MMX™ Technology Instructions

- **0F prefix becomes a mainstream opcode**
  - All MMX™ technology instructions start with 0F
- **Length decoder extended to 4 bytes**
  - Quadruple 0F decode bandwidth
- **Capable of issuing two MMX technology instructions per cycle**

Decoder Supports Full Bandwidth for New Instructions

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MMX™ Technology Execution Pipe

- **MMX™ technology instructions use the integer pipe**

- **After the Execute stage the MMX technology pipe continues to the Mex and WM stage**

  – Multiply instructions continue in the MMX technology pipe to the M2, M3 and WMul stages

Mex	WM/M$_2$	M$_3$	WMul

PF	F	D1	D2	E	WB

E$_1$	E$_2$

E$_1$	E$_2$	E$_3$

- MMX stages
- Integer with MMX
- Integer stages

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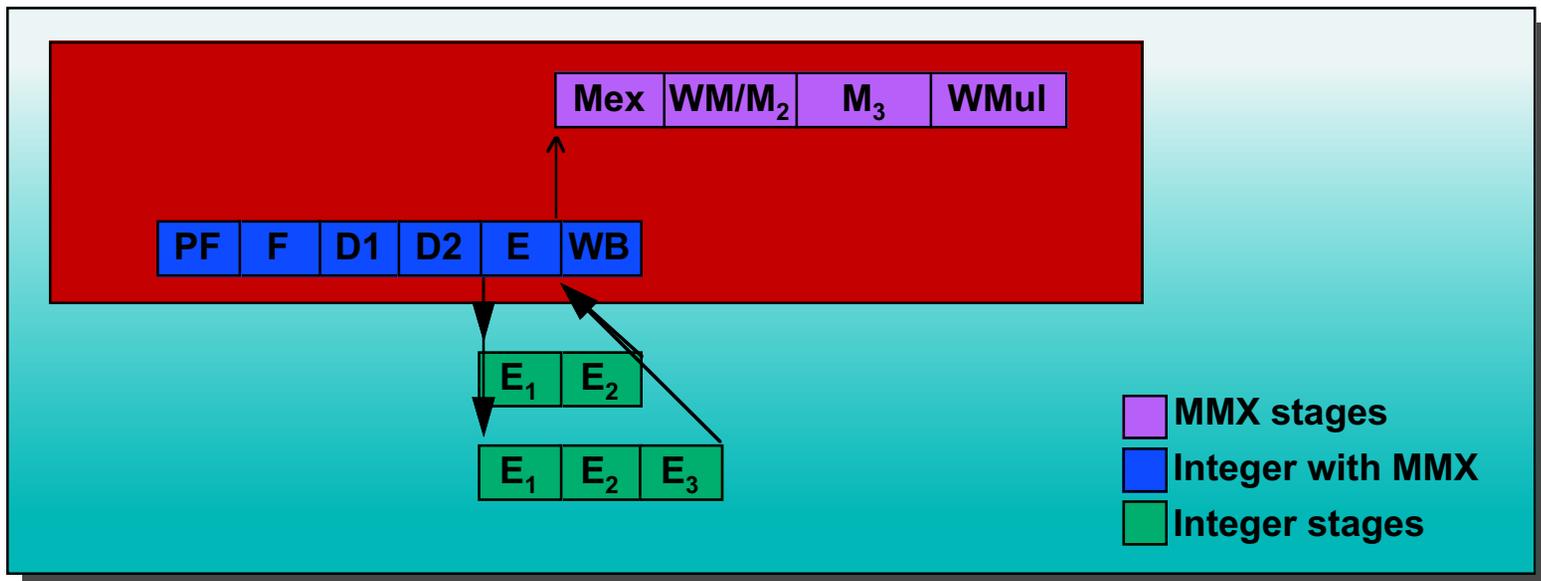
MMX™ Technology Execution Units

- **All MMX™ technology Instructions can be issued every clock**

Operation	# Of Units	Latency	Throughput	Pipes
ALU	2	1	1	U and V
Multiplier	1	3	1	U or V
Shift/Pack/Unpack	1	1	1	U or V
Memory Access	1	1	1	U
Integer Register Access	1	1	1	U

**Maximum Throughput for New Instructions
Most Instructions Can Be Paired**

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MMX™ Technology Instructions Execution

IDCT Inner Loop Execution

Paring			**Bypass**

Movq   mm4, [edi]   /* load 1st 4 values   `PF | F | D1 | D2 | E | Mex | WM`

Movq   mm7, [edx]   /* load 2nd 4 values   `PF | F | D1 | D1 | D2 | E | Mex | WM`

Movq   mm0, mm4   /* Copy 1st values   `PF | F | D1 | D2 | E | Mex | WM`

Psubw   mm4, mm7   /* O1[0-3] = I0[0-3] - I1[0-3]   `PF | F | D1 | D2 | E | Mex | WM`

Paddw   mm7, mm0   /* O0[0-3] = I0[0-3] + I1[0-3]   `PF | F | D1 | D2 | E | Mex | WM`
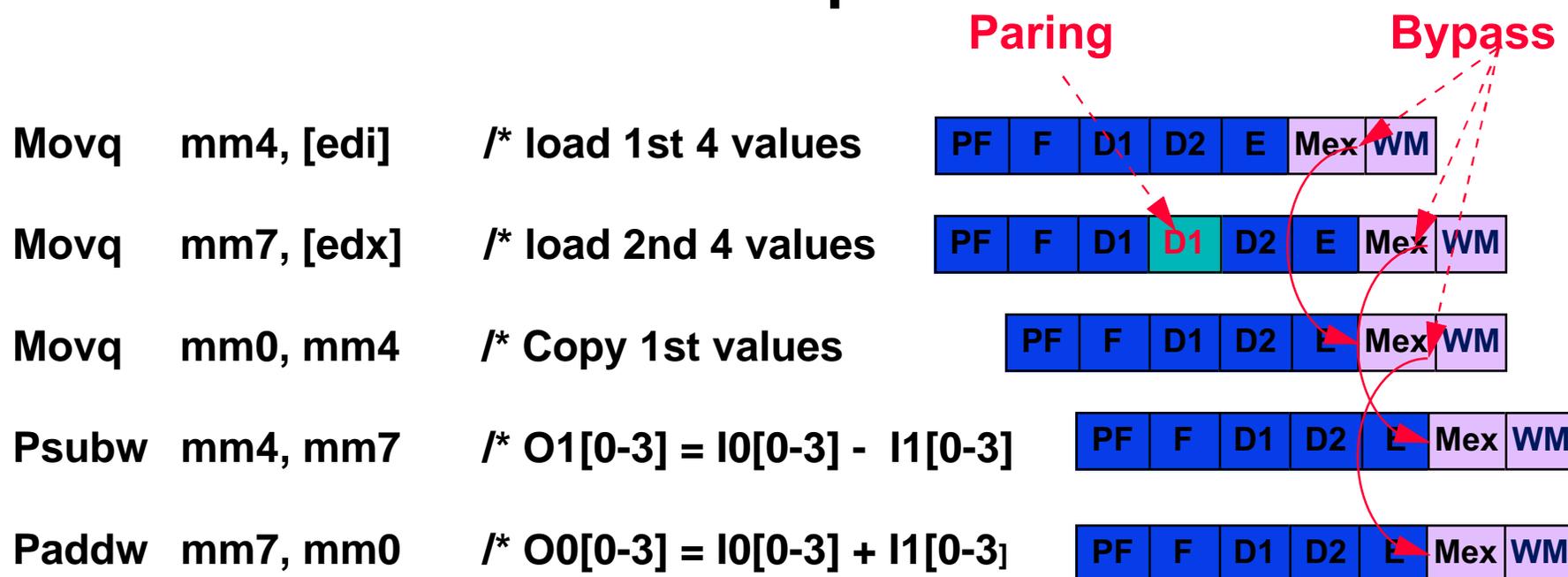
Utilize SIMD and Micro-Architecture Parallelism To Achieve Performance

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P55C Multimedia Kernels Performance

	12
	10
	8
	6
	4
	2
	0

Complex FIR   Complex FFT   Inverse DCT   Motion estimat.   Lag search   Analysis filter

DSP   **Video**   **Voice**

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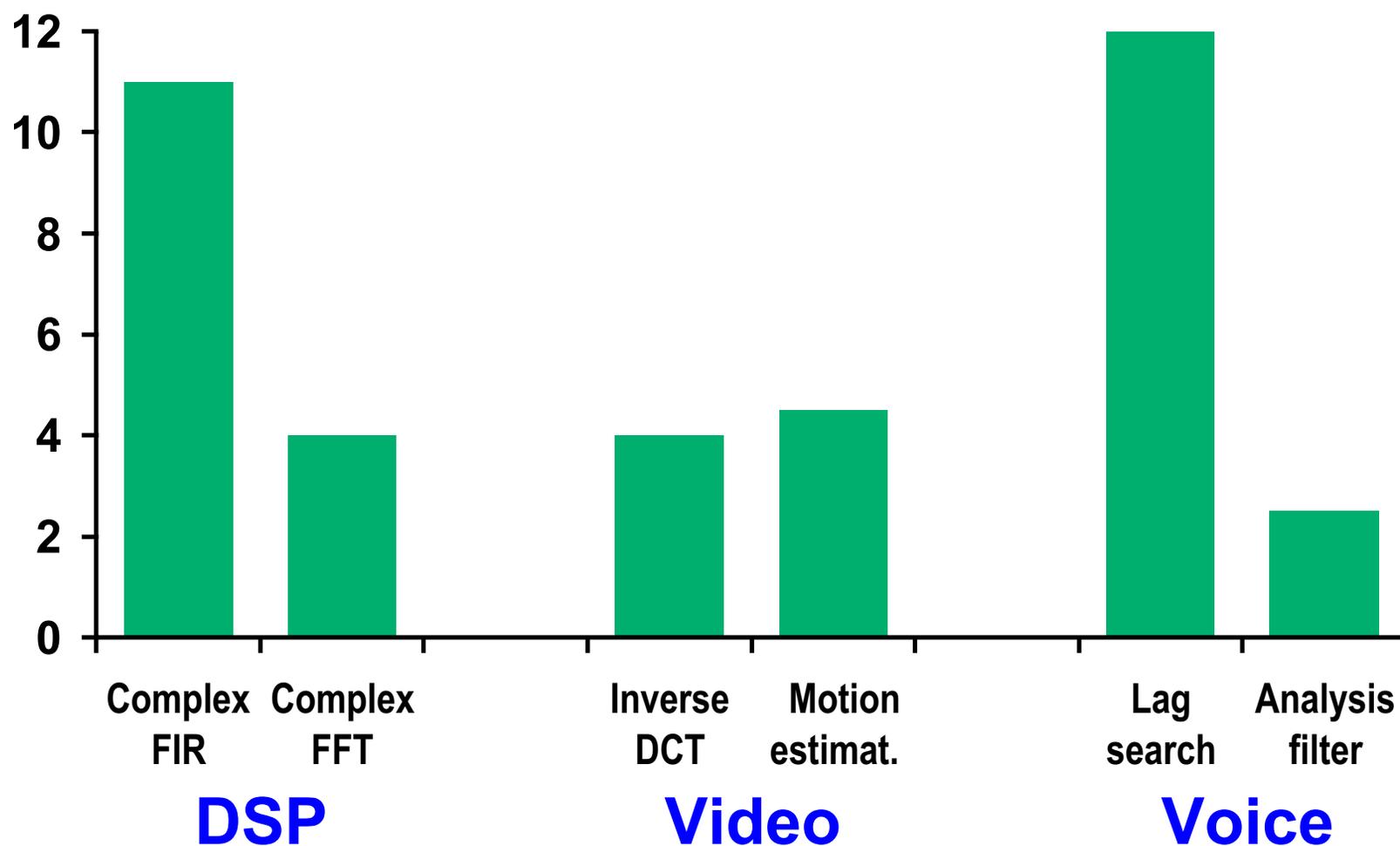
Summary

- **P55C with MMX™ technology will provide significant performance improvement for multimedia and communications applications**

- **Clean MMX technology implementation without sacrificing device speed**

- **P55C maximizes usage of existing Pentium® Processor micro-architecture**

- **Product introduction expected in Q1'97**

**Intel's MMX technology --
For the next generation of multimedia
and communications**

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