12.0 Low-power Embedded Pentium® Processor with MMX™ Technology Electrical Specifications

This section contains preliminary information on new products in production. The specifications are subject to change without notice.

12.1 Absolute Maximum Ratings

Warning: The following values are stress ratings only. Functional operation at the maximum ratings is not implied nor guaranteed. Functional operating conditions are given in the AC and DC specification tables. Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage.

Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the Pentium processor with MMX technology contains protective circuitry to resist damage from Electrostatic Discharge (ESD), always take precautions to avoid high static voltages or electric fields.

Table 83. Absolute Maximum Ratings

Parameter	Maximum Rating
Case temperature under bias	–65° C to 110° C
Storage temperature	–65° C to 150° C
V_{CC3} supply voltage with respect to V_{SS}	–0.5 V to +3.2 V
V_{CC2} supply voltage with respect to V_{SS}	–0.5 V to +2.8 V
2.5 V only buffer DC input voltage	–0.5 V to V_{CC3}+0.5 V (not to exceed V_{CC3} max)

12.2 DC Specifications

Tables 85, 86, 87 and 88 list the DC specifications which apply to the low-power embedded Pentium processor with MMX technology.

12.2.1 Power Sequencing

There is no specific sequence required for powering up or powering down the V_{CC2} and V_{CC3} power supplies. However, it is recommended that the V_{CC2} and V_{CC3} power supplies be either both ON or both OFF within one second of each other.

The I/O voltage V_{CC3} is 2.5 V. The core voltage V_{CC2} is 1.9 V for PPGA. The core voltage V_{CC2} for the HL-PBGA package type is 1.8 V (166 MHz) or 2.0 V (266 MHz).

Table 84. V_{CC} and T_{CASE} Specifications

Package	T_{CASE}	Supply	Min Voltage	Max Voltage	Voltage Tolerance	Frequency
PPGA	0°C to 85°C	V_{CC2}	1.750 V	2.04 V	1.9 V ± 7.5%	166/266 MHz
		V_{CC3}	2.375 V	2.625 V	2.5 V ± 5%	166/266 MHz
HL-PBGA	0°C to 95°C	V_{CC2}	1.665 V	1.935 V	1.8 V ± 7.5%	166 MHz
		V_{CC2}	1.85 V	2.15 V	2.0 V ± 7.5%	266 MHz
		V_{CC3}	2.375 V	2.625 V	2.5 V ± 5%	166/266 MHz

Table 85. DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL3}	Input Low Voltage	–0.3	0.5	V	
V_{IH3}	Input High Voltage	$V_{CC3} - 0.7$	$V_{CC3} + 0.3$	V	TTL Level
V_{OL3}	Output Low Voltage		0.4	V	TTL Level, (1)
V_{OH3}	Output High Voltage	$V_{CC3} - 0.4$ $V_{CC3} - 0.2$		V V	TTL Level, (2) TTL Level, (3)

NOTES:
1. Parameter measured at -4 mA.
2. Parameter measured at 3 mA.
3. Parameter measured at 1 mA; not 100% tested, guaranteed by design.

The values in Table 86 should be used for power supply design. The values were determined using a worst case instruction mix and maximum V_{CC}. Power supply transient response and decoupling capacitors must be sufficient to handle the instantaneous current changes occurring during transitions from Stop Clock to full Active modes.

Table 86. I_{CC} Specifications

Symbol	Parameter	Min	Max	Unit	Notes
I_{CC2}	Power Supply Current		2.35 (HL-PBGA) 2.5 (PPGA) 4.00	A A A	166 MHz 166 MHz 266 MHz
I_{CC3}	Power Supply Current		0.38 0.38	A A	166 MHz 266 MHz

Table 87. Power Dissipation Requirements for Thermal Design

Parameter	Typical(1)	Max(2)	Unit	Frequency
Thermal Design Power		4.1 (HL-PBGA) 4.5 (PPGA) 7.6	Watts Watts Watts	166 MHz 166 MHz 266 MHz
Active Power(3)	2.9 4.5		Watts Watts	166 MHz 266 MHz
Stop Grant/Auto Halt Powerdown Power Dissipation(4)		0.70 0.70	Watts Watts	166 MHz 266 MHz
Stop Clock Power(5)		0.06 0.06	Watts Watts	166 MHz 266 MHz

NOTES:
1. This is the typical power dissipation in a system. This value is expected to be the average value that will be measured in a system using a typical device at the specified voltage running typical applications. This value is dependent upon the specific system configuration. Typical power specifications are not tested.
2. Systems must be designed to thermally dissipate the maximum thermal design power unless the system uses thermal feedback to limit processor's maximum power. The maximum thermal design power is determined using a worst-case instruction mix and also takes into account the thermal time constant of the package.
3. Active power is the average power measured in a system using a typical device running typical applications under normal operating conditions at nominal V_{CC} and room temperature.
4. Stop Grant/Auto Halt Powerdown Power Dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction. When in this mode, the processor has a new feature which allows it to power down additional circuitry to enable lower power dissipation. This is the power without snooping at the specified voltage and with TR12 bit 21 set. In order to enable this feature, TR12 bit 21 must be set to 1 (the default is 0 or disabled). Stop grant/Auto Halt Powerdown power dissipation without TR12 bit 21 set may be higher. The Max rating may be changed in future specification updates.
5. Stop Clock Power Dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input. This is specified at a T_{CASE} of 50 °C.

Table 88. Input and Output Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Capacitance		15	pF	(4)
C_O	Output Capacitance		20	pF	(4)
$C_{I/O}$	I/O Capacitance		25	pF	(4)
C_{CLK}	CLK Input Capacitance		15	pF	(4)
C_{TIN}	Test Input Capacitance		15	pF	(4)
C_{TOUT}	Test Output Capacitance		20	pF	(4)
C_{TCK}	Test Clock Capacitance		15	pF	(4)
I_{LI}	Input Leakage Current		±15	µA	$0<V_{IN}<V_{IL}$, $V_{IH}< V_{IN}<V_{CC3}$, (1)
I_{LO}	Output Leakage Current		±15	µA	$0<V_{IN}<V_{IL}$, $V_{IH}< V_{IN}<V_{CC3}$, (1)
I_{IH}	Input High Leakage Current		200	µA	$V_{IN} = V_{CC3} – 0.4$ V, (3)
I_{IL}	Input Low Leakage Current		–400	µA	V_{IN} = 0.4 V (2, 5)

NOTES:
1. This parameter is for inputs/outputs without an internal pull up or pull down.
2. This parameter is for inputs with an internal pull up.
3. This parameter is for inputs with an internal pull down.
4. Guaranteed by design.
5. This specification applies to the HITM# pin when it is driven as an input (e.g., in JTAG mode).

12.3 AC Specifications

The AC specifications of the low-power embedded Pentium processor with MMX technology consist of setup times, hold times, and valid delays at 0 pF.

12.3.1 Power and Ground

For clean on-chip power distribution, the PPGA has 25 V_{CC2} (core power), 28 V_{CC3} (I/O power) and 53 V_{SS} (ground) inputs. For the HL-PBGA package, there are 42 V_{CC3}, 37 V_{CC2} and 72 V_{SS} inputs.

Power and ground connections must be made to all external V_{CC2}, V_{CC3} and V_{SS} pins. On the circuit board, all V_{CC2} pins must be connected to a proper voltage V_{CC2} plane or island (core voltage determined by package type/frequency). All V_{CC3} pins must be connected to a 2.5 V V_{CC3}, plane. All V_{SS} pins must be connected to a V_{SS} plane. Please refer to Table 68 on page 4 for the list of V_{CC2}, V_{CC3} and V_{SS} pins.

12.3.2 Decoupling Recommendations

Liberal decoupling capacitance should be placed near the processor. The processor's large address and data buses can cause transient power surges, particularly when driving large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the processor and decoupling capacitors as much as possible. These capacitors should be evenly distributed around each component on the power plane. Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

Power transients also occur as the processor rapidly transitions from a low level power consumption to a high level one (or high to low power transition). A typical example would be entering or exiting the Stop Grant state. Another example would be executing a HALT instruction, causing the processor to enter the Auto HALT Powerdown state, or transitioning from HALT to the Normal state. All of these examples may cause abrupt changes in the power being consumed by the processor.

Note that the Auto HALT Powerdown feature is always enabled even when other power management features are not implemented.

Bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 to 100 µf range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel.

These capacitors should be placed near the processor on both V_{CC2} plane and V_{CC3} plane to ensure that the supply voltages stay within specified limits during changes in the supply current during operation.

12.3.3 Connection Specifications

All NC/INC pins must remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC3}. Unused active high inputs should be connected to ground.

12.3.4 AC Timings

The AC specifications given in Table 89 consist of output delays, input setup requirements and input hold requirements for the standard 66 MHz external bus. All AC specifications (with the exception of those for the TAP signals and APIC signals) are relative to the rising edge of the CLK input.

All timings are referenced to V_{CC3}/V_{CC2} for both “0” and “1” logic levels unless otherwise specified. Within the sampling window, asynchronous inputs must be stable for correct operation.

Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling to account for signal flight time delays. Do not select a bus fraction and clock speed which will cause the processor to exceed its internal maximum frequency.

The following specifications apply to all standard TTL signals used with the Pentium processor family:

- TTL input test waveforms are assumed to be 0 to 2.5 V transitions with 1.0 V/ns rise and fall times.
- 0.3 V/ns ≤ input rise/fall time ≤ 5 V/ns.
- All TTL timings are referenced from V_{CC3}/V_{CC2}.

Table 89. Low-Power Embedded Pentium® Processor with MMX™ Technology AC Specifications (Sheet 1 of 3)
(See Table 84 for V_{CC} and T_{CASE} assumptions.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes (see Table 91)
	CLK Frequency	33.33	66.6	MHz		(1)
t_{1a}	CLK Period	15.0	30.0	ns	56	
t_{1b}	CLK Period Stability		±250	ps		(2, 3)
t_2	CLK High Time	4.0		ns	56	@V_{CC3} – 0.7 V, (2)
t_3	CLK Low Time	4.0		ns	56	@0.5 V, (2)
t_4	CLK Fall Time	0.15	1.5	ns	56	V_{CC3} – 0.7 V to 0.5 V, (2, 4)
t_5	CLK Rise Time	0.15	1.5	ns	56	0.5 V to V_{CC3} –0.7 V, (2, 4)
t_{6a}	PWT, PCD, CACHE# Valid Delay	1.0	7.0	ns	57	
t_{6b}	AP Valid Delay	1.0	8.5	ns	57	
t_{6c}	LOCK#, Valid Delay	0.9	7.0	ns	57	
t_{6d}	ADS# Valid Delay	1.0	6.2	ns	57	
t_{6e}	A31–A3 Valid Delay	0.8	6.4	ns	57	
t_{6f}	M/IO# Valid Delay	0.8	6.2	ns	57	
t_{6g}	BE7#–BE0#, D/C#, W/R#, SCYC Valid Delay	0.8	7.0	ns	57	
t_7	ADS#, AP, A31–A3, PWT, PCD, BE7#–BE0#, M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK# Float Delay		10.0	ns	58	(2)
t_{8a}	APCHK#, IERR#, FERR# Valid Delay	1.0	8.3	ns	57	(5)
t_{8b}	PCHK# Valid Delay	1.0	7.0	ns	57	(5)
t_{9a}	BREQ Valid Delay	1.0	8.0	ns	57	(5)
t_{9b}	SMIACT# Valid Delay	1.0	7.3	ns	57	(5)
t_{9c}	HLDA Valid Delay	1.0	6.8	ns	57	(5)
t_{10a}	HIT# Valid Delay	1.0	6.8	ns	57	
t_{10b}	HITM# Valid Delay	0.9	6.0	ns	57	
t_{11a}	PM1–PM0, BP3–BP0 Valid Delay	1.0	10.0	ns	57	
t_{11b}	PRDY Valid Delay	1.0	8.0	ns	57	
t_{12}	D63–D0, DP7–DP0 Write Data Valid Delay	1.0	7.7	ns	57	
t_{13}	D63–D0, DP3–0 Write Data Float Delay		10.0	ns	58	(2)
t_{14}	A31–A5 Setup Time	6.0		ns	59	(6)
t_{15}	A31–A5 Hold Time	1.0		ns	59	
t_{16a}	INV, AP Setup Time	5.0		ns	59	
t_{16b}	EADS# Setup Time	5.0		ns	59	
t_{17}	EADS#, INV, AP Hold Time	1.0		ns	59	

Table 89. Low-Power Embedded Pentium® Processor with MMX™ Technology AC Specifications (Sheet 2 of 3)
(See Table 84 for V_{CC} and T_{CASE} assumptions.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes (see Table 91)
t_{18a}	KEN# Setup Time	5.0		ns	59	
t_{18b}	NA#, WB/WT# Setup Time	4.5		ns	59	
t_{19}	KEN#, WB/WT#, NA# Hold Time	1.0		ns	59	
t_{20}	BRDY# Setup Time	4.75		ns	59	
t_{21}	BRDY# Hold Time	1.0		ns	59	
t_{22}	AHOLD, BOFF# Setup Time	5.5		ns	59	
t_{23}	AHOLD, BOFF# Hold Time	1.0		ns	59	
t_{24a}	BUSCHK#, EWBE#, HOLD, Setup Time	5.0		ns	59	
t_{24b}	PEN# Setup Time	4.8		ns	59	
t_{25a}	BUSCHK#, EWBE#, PEN# Hold Time	1.0		ns	59	
t_{25b}	HOLD Hold Time	1.5		ns	59	
t_{26}	A20M#, INTR, STPCLK# Setup Time	5.0		ns	59	(7, 8)
t_{27}	A20M#, INTR, STPCLK# Hold Time	1.0		ns	59	(9)
t_{28}	INIT, FLUSH#, NMI, SMI#, IGNNE# Setup Time	5.0		ns	59	(8, 10, 17)
t_{29}	INIT, FLUSH#, NMI, SMI#, IGNNE# Hold Time	1.0		ns	59	(9)
t_{30}	INIT, FLUSH#, NMI, SMI#, IGNNE# Pulse Width, Async	2.0		CLKs	59	(10, 11)
t_{31}	R/S# Setup Time	5.0		ns	59	(7, 8, 10)
t_{32}	R/S# Hold Time	1.0		ns	59	(9)
t_{33}	R/S# Pulse Width, Async.	2.0		CLKs	59	(10, 11)
t_{34}	D63–D0, DP7–0 Read Data Setup Time	2.8		ns	59	
t_{35}	D63–D0, DP7–0 Read Data Hold Time	1.5		ns	59	
t_{36}	RESET Setup Time	5.0		ns	59	(7, 8)
t_{37}	RESET Hold Time	1.0		ns	60	(9)
t_{38}	RESET Pulse Width, V_{CC} & CLK Stable	15.0		CLKs	60	(10)
t_{39}	RESET Active After V_{CC} & CLK Stable	1.0		mS	60	Power up

Table 89. Low-Power Embedded Pentium® Processor with MMX™ Technology AC Specifications (Sheet 3 of 3)
(See Table 84 for V_{CC} and T_{CASE} assumptions.)

Symbol	Parameter	Min	Max	Unit	Figure	Notes (see Table 91)
t_{40}	Reset Configuration Signals (INIT, FLUSH#) Setup Time	5.0		ns	60	(7, 8, 10)
t_{41}	Reset Configuration Signals (INIT, FLUSH#) Hold Time	1.0		ns	60	(9)
t_{42a}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	60	To RESET falling edge, (8)
t_{42b}	Reset Configuration Signals (INIT, FLUSH#) Setup Time, Async.	2.0		CLKs	60	To RESET falling edge
t_{43a}	BF2–BF0 Setup Time	1.0		mS	60	To RESET falling edge, (10)
t_{43b}	BF2–BF0 Hold Time	2.0		CLKs	60	To RESET falling edge, (12)
t_{43c}	APICEN, BE4# Setup Time	2.0		CLKs	60	To RESET falling edge
t_{43d}	APICEN, BE4# Hold Time	2.0		CLKs	60	To RESET falling edge
t_{44}	TCK Frequency	—	16.0	MHz		
t_{45}	TCK Period	62.5		ns	56	
t_{46}	TCK High Time	25.0		ns	56	@V_{CC3} –0.7 V, (2)
t_{47}	TCK Low Time	25.0		ns	56	@0.5 V, (2)
t_{48}	TCK Fall Time		5.0	ns	56	V_{CC3} –0.7 V to 0.5 V (2, 13, 14)
t_{49}	TCK Rise Time		5.0	ns	56	0.5 V to V_{CC3} –0.7 V, (2, 13, 14)
t_{50}	TRST# Pulse Width	40.0		ns	62	Asynchronous, (2)
t_{51}	TDI, TMS Setup Time	5.0		ns	62	(15)
t_{52}	TDI, TMS Hold Time	13.0		ns	62	(15)
t_{53}	TDO Valid Delay	3.0	20.0	ns	62	(13)
t_{54}	TDO Float Delay		25.0	ns	62	(2, 13)
t_{55}	All Non-Test Outputs Valid Delay	3.0	20.0	ns	62	(13, 16, 17)
t_{56}	All Non-Test Outputs Float Delay		25.0	ns	62	(2, 13, 16, 17)
t_{57}	All Non-Test Inputs Setup Time	5.0		ns	62	(15, 16, 17)
t_{58}	All Non-Test Inputs Hold Time	13.0		ns	62	(15, 16, 17)

Table 90. APIC AC Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{60a}	PICCLK Frequency	2	16.66	MHz		
t_{60b}	PICCLK Period	60	500	ns	56	
t_{60c}	PICCLK High Time	15		ns	56	
t_{60d}	PICCLK Low Time	15		ns	56	
t_{60e}	PICCLK Rise Time	0.15	2.5	ns	56	
t_{60f}	PICCLK Fall Time	0.15	2.5	ns	56	
t_{60g}	PICD0–1 Setup Time	3		ns	59	To PICCLK
t_{60h}	PICD0–1 Hold Time	2.5		ns	59	To PICCLK
t_{60i}	PICD0–1 Valid Delay (L to H)	4	38	ns	57	From PICCLK, (18)
t_{60j}	PICD0–1 High Time (H to L)	4	22	ns	57	From PICCLK, (18)
t_{61}	PICCLK Setup Time	5.0			59	To CLK
t_{62}	PICCLK Hold Time	2.0			59	To CLK
t_{63}	PICCLK Ratio (CLK/PICCLK)	4				(19)

Table 91. Notes to Tables 89 and 90

1. CLK input frequency must be either 33.33 MHz (+1 MHz) or 66.6 MHz (–1 MHz). Operation in the range between 33.33 MHz and 66.6 MHz is not supported.
2. Not 100 percent tested. Guaranteed by design.
3. These signals are measured on the rising edge of adjacent CLKs at V_{CC3}/V_{CC2}. To ensure a 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 KHz and 1/3 of the CLK operating frequency. The amount of jitter present must be accounted for as a component of CLK skew between devices. The internal clock generator requires a constant frequency CLK input to within +250 ps, and therefore the CLK input cannot be changed dynamically.
4. 0.87 V/ns ≤ CLK input rise/fall time ≤ 8.7 V/ns.
5. APCHK#, FERR#, HLDA, IERR#, LOCK#, and PCHK# are glitch-free outputs. Glitch-free signals monotonically transition without false transitions.
6. Timing (t_{14}) is required for external snooping (e.g., address setup to the CLK in which EADS# is sampled active).
7. Setup time is required to guarantee recognition on a specific clock.
8. This input may be driven asynchronously.
9. Hold time is required to guarantee recognition on a specific clock.
10. When driven asynchronously, RESET, NMI, FLUSH#, R/S#, INIT, and SMI# must be de-asserted (inactive) for a minimum of two clocks before being returned active.
11. To guarantee proper asynchronous recognition, the signal must have been de-asserted (inactive) for a minimum of two clocks before being returned active and must meet the minimum pulse width.
12. BF2–BF0 should be strapped to V_{CC3} or V_{SS}.
13. Referenced to TCK falling edge.
14. 1 ns can be added to the maximum TCK rise and fall times for every 10 MHz of frequency below 33 MHz.
15. Referenced to TCK rising edge.
16. Non-test outputs and inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO, and TMS). These timings correspond to the response of these signals due to boundary scan operations.
17. During probe mode operation, do not use the boundary scan timings (t_{55}–t_{58}).
18. This assumes an external pull-up resistor to V_{CC} and a lumped capacitive load. The pull-up resistor must be between 300 Ω and 1 KΩ, the capacitance must be between 20 pF and 120 pF, and the RC product must be between 6 ns and 36 ns.
19. The CLK to PICCLK ratio has to be an integer and the ratio (CLK/PICCLK) cannot be smaller than 4.

Figure 56. Clock Waveform

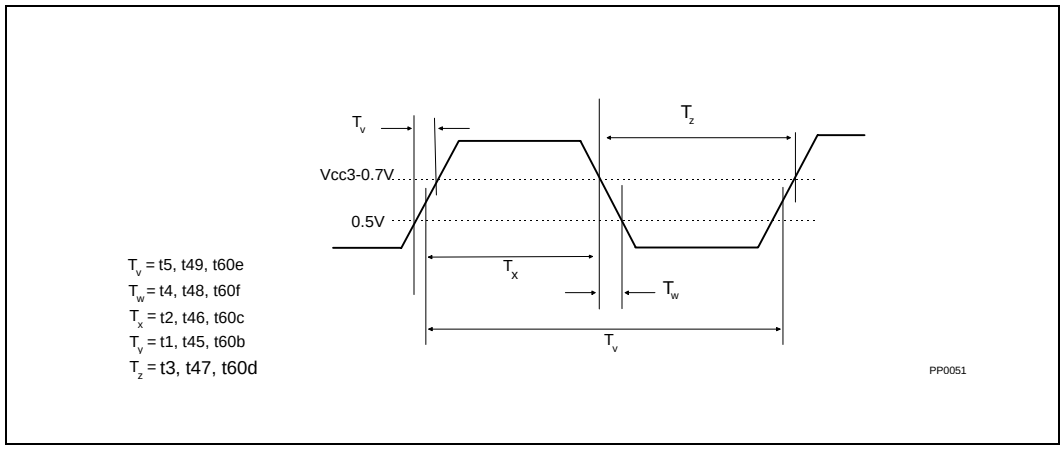


Figure 57. Valid Delay Timings

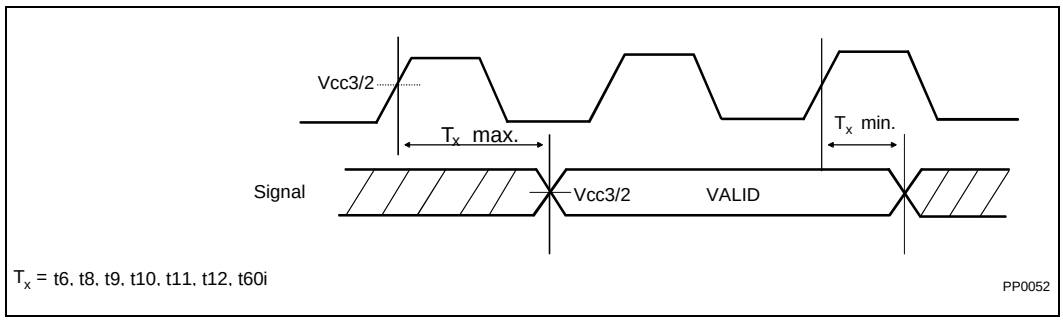


Figure 58. Float Delay Timings

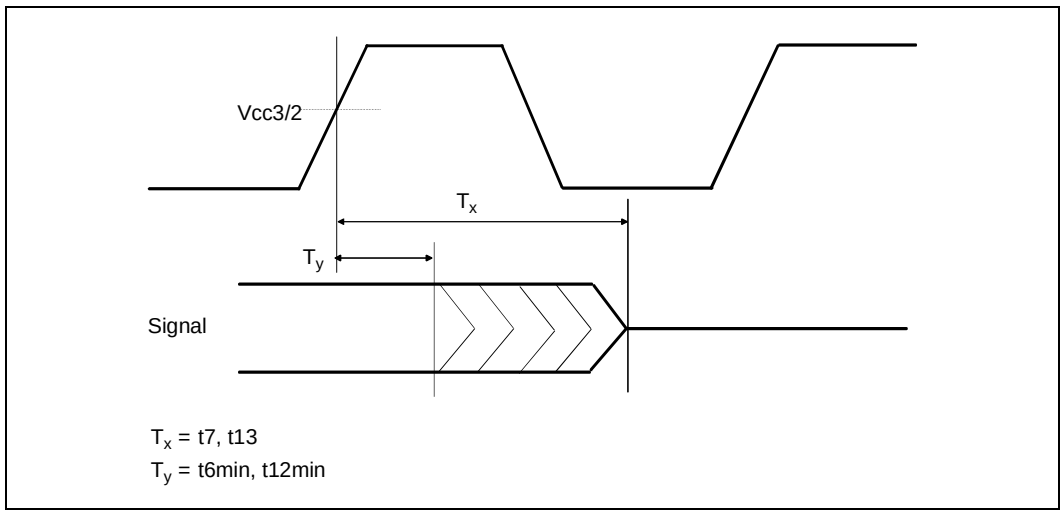
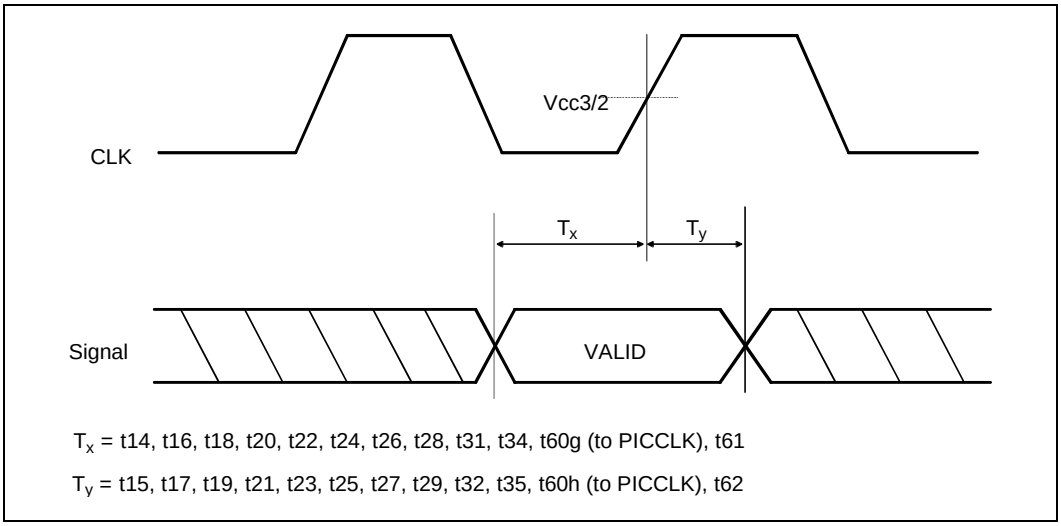


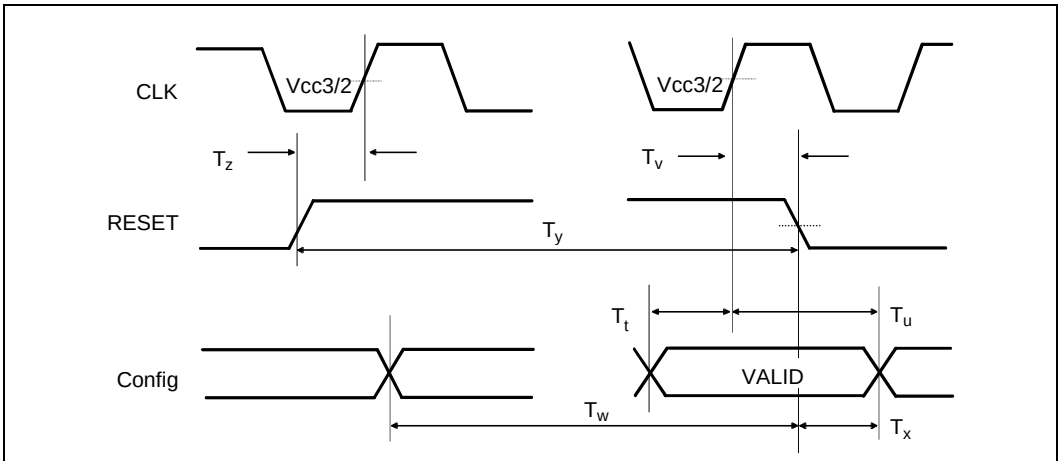
Figure 59. Setup and Hold Timings



T_x = t14, t16, t18, t20, t22, t24, t26, t28, t31, t34, t60g (to PICCLK), t61

T_y = t15, t17, t19, t21, t23, t25, t27, t29, t32, t35, t60h (to PICCLK), t62

Figure 60. Reset and Configuration Timings



T_t = t40

T_u = t41

T_v = t37

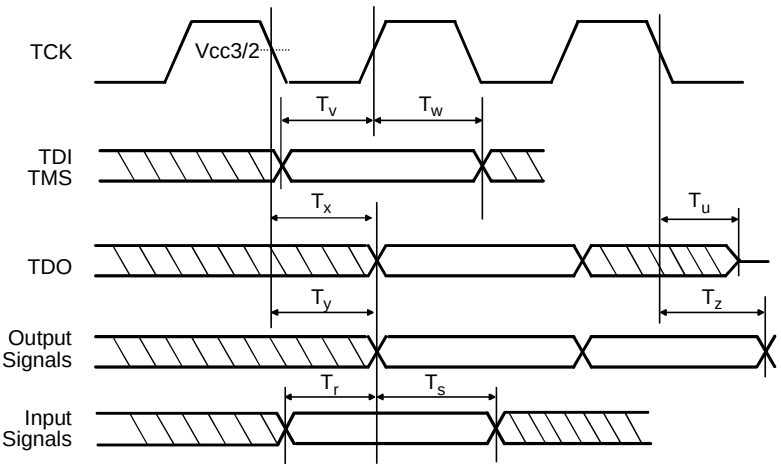
T_w = t42, t43c, t43e, t87

T_x = t43b, t43d, t43f, t88

T_y = t38, t39

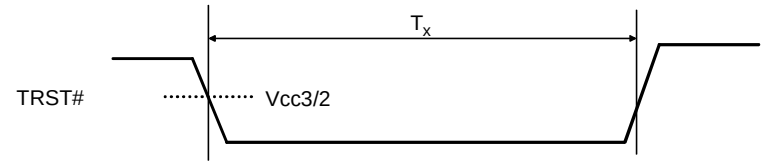
T_z = t36

Figure 61. Test Timings



T_r = t57
T_s = t58
T_u = t54
T_v = t51
T_w = t52
T_x = t53
T_y = t55
T_z = t56

Figure 62. Test Reset Timings



T_x = t50

12.4 I/O Buffer Models

This section describes the I/O buffer models of the low-power embedded Pentium processor with MMX technology.

The first order I/O buffer model is a simplified representation of the complex input and output buffers used. Figure 63 shows the structure of the input buffer model and Figure 64 shows the output buffer model. Table 92 and 93 show the parameters used to specify these models.

Although simplified, these buffer models will accurately model flight time and signal quality. For these parameters, there is very little added accuracy in a complete transistor model.

In addition to the input and output buffer parameters, input protection diode models are provided for added accuracy. These diodes have been optimized to provide ESD protection and provide some level of clamping. Although the diodes are not required for simulation, it may be more difficult to meet specifications without them.

Note, however, some signal quality specifications require that the diodes be removed from the input model. The series resistors (R_S) are a part of the diode model. Remove these when removing the diodes from the input model.

Figure 63. First Order Input Buffer Model

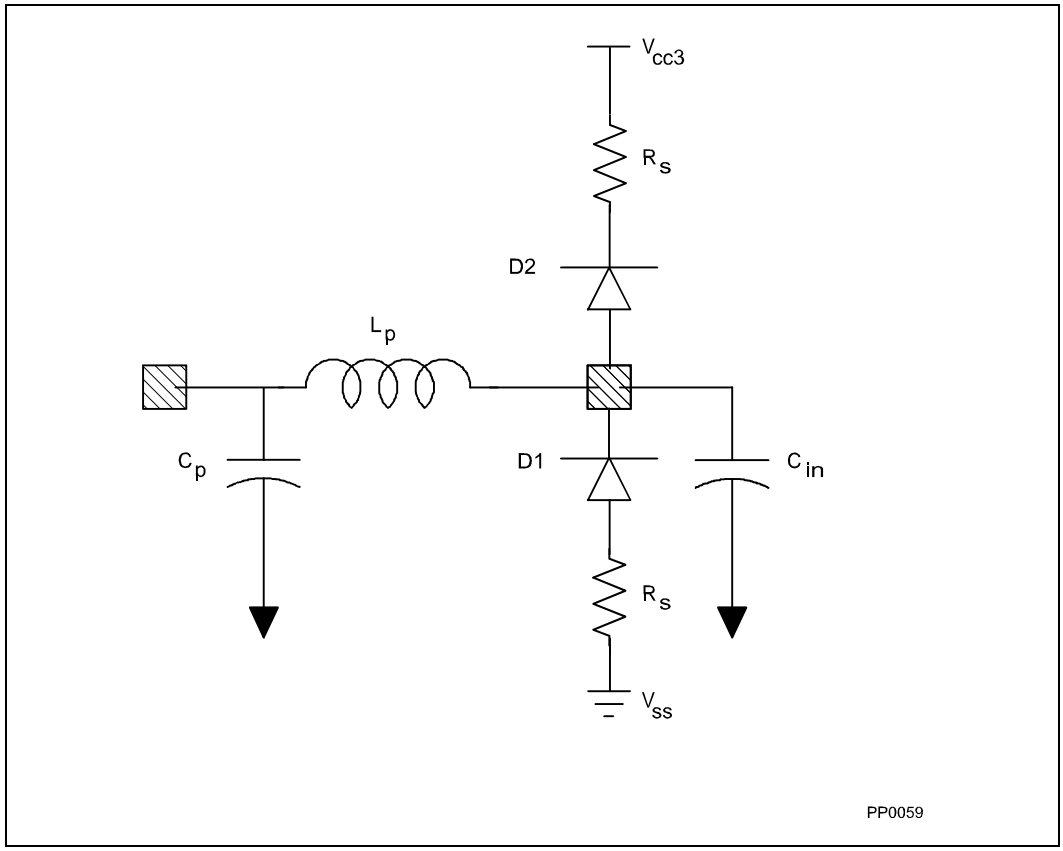


Table 92. Parameters Used in the Specification of the First Order Input Buffer Model

Parameter	Description
C_{in}	Minimum and Maximum value of the capacitance of the input buffer model
L_p	Minimum and Maximum value of the package inductance
C_p	Minimum and Maximum value of the package capacitance
R_S	Diode Series Resistance
D1, D2	Ideal Diodes

Figure 64. First Order Output Buffer Model

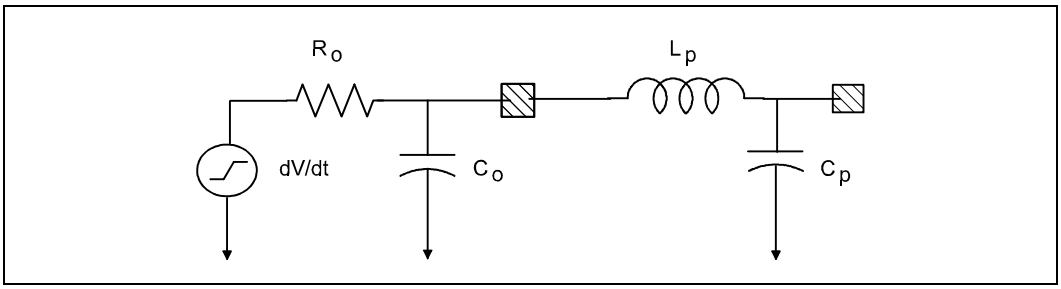


Table 93. Parameters Used in the Specification of the First Order Output Buffer Model

Parameter	Description
dV/dt	Minimum and maximum value of the rate of change of the open circuit voltage source used in the output buffer model
R_O	Minimum and maximum value of the output impedance of the output buffer model
C_O	Minimum and Maximum value of the capacitance of the output buffer model
L_P	Minimum and Maximum value of the package inductance
C_P	Minimum and Maximum value of the package capacitance

12.4.1 Buffer Model Parameters

This section gives the parameters for each input, output and bidirectional buffers.

The input, output and bidirectional buffer values of the processor are listed in Table 95. These tables contain listings for all three types, do not get them confused during simulation. When a bidirectional pin is operating as an input, use the C_{IN}, C_P and L_P values; if it is operating as a driver, use all of the data parameters.

Please refer to Table 94 for the groupings of the buffers.

The input, output and bidirectional buffer's values are listed below. These tables contain listings for all three types. When a bidirectional pin is operating as an input, just use the C_{IN}, C_P and L_P values, if it is operating as a driver use all the data parameters.

Table 94. Signal to Buffer Type

Signals	Type	Driver Buffer Type	Receiver Buffer Type
A20M#, AHOLD, BF, BOFF#, BRDY#, BUSCHK#, EADS#, EWBE#, FLUSH#, HOLD, IGNNE#, INIT, INTR, INV, KEN#, NA#, NMI, PEN#, PICCLK, R/S#, RESET, SMI#, STPCLK#, TCK, TDI, TMS, TRST#, WB/WT#	I		ER1
APCHK#, BE7–BE5#, BP3–BP2, BREQ, FERR#, IERR#, PCD, PCHK#, PM0/BP0, PM1/BP1, PRDY, PWT, SMIACT#, TDO	O	ED1	
A31–A3, AP, BE4#–BE0#, CACHE#, D/C#, D63–D0, DP8–DP0, HLDA, LOCK#, M/IO#, SCYC, ADS#, HITM#, HIT#, W/R#, PICD0, PICD1	I/O	EB1	EB1

Table 95. Input, Output and Bidirectional Buffer Model Parameters for PPGA Package

Buffer Type	Transition	dV/dt (V/nsec)		R_O (Ohms)		C_P (pF)		L_P (nH)		C_O/C_{IN} (pF)	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
ER1	Rising					1.1	5.3	7.7	15.3	0.8	1.2
(input)	Falling					1.1	5.3	7.7	15.3	0.8	1.2
ED1	Rising	2.2/2.2	2.7/0.15	21.6	65	1.1	5.8	8.1	16.3	2.0	2.6
(output)	Falling	2.2/2.9	2.7/0.22	17.5	75	1.1	5.8	8.1	16.3	2.0	2.6
EB1	Rising	2.2/2.2	2.7/0.15	21.6	65	1.3	7.0	8.2	18.4	2.0	2.6
(bidir)	Falling	2.2/2.9	2.7/0.22	17.5	75	1.3	7.0	8.2	18.4	2.0	2.6

Table 96. Preliminary Input, Output and Bidirectional Buffer Model Parameters for HL-PBGA Package

Buffer Type	Transition	dV/dt (V/nsec)		R_O (Ohms)		C_P (pF)		L_P (nH)		C_O/C_{IN} (pF)	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
ER1	Rising					0.2	0.4	6.4	11.3	0.8	1.2
(input)	Falling					0.2	0.4	6.4	11.3	0.8	1.2
ED1	Rising	2.2/2.2	2.7/0.15	21.6	65	0.2	0.5	5.4	11.7	2.0	2.6
(output)	Falling	2.2/2.9	2.7/0.22	17.5	75	0.2	0.5	5.4	11.7	2.0	2.6
EB1	Rising	2.2/2.2	2.7/0.15	21.6	65	0.2	0.4	5.2	10.3	2.0	2.6
(bidir)	Falling	2.2/2.9	2.7/0.22	17.5	75	0.2	0.4	5.2	10.3	2.0	2.6

NOTE: The data in this table is based on preliminary design information. Input, output and bidirectional buffer values are being characterized at this time.

Table 97. Input Buffer Model Parameters: D (Diodes)

Symbol	Parameter	D1	D2
I_S	Saturation Current	1.4e–14A	2.78e–16A
N	Emission Coefficient	1.19	1.00
R_S	Series Resistance	6.5 Ω	6.5 Ω
T_T	Transit Time	3 ns	6 ns
V_J	PN Potential	0.983 V	0.967 V
C_{J0}	Zero Bias PN Capacitance	0.281 pF	0.365 pF
M	PN Grading Coefficient	0.385	0.376

12.5 Signal Quality Specifications

Signals driven by the system into the low-power embedded Pentium processor with MMX technology must meet signal quality specifications to guarantee that the components read data properly and to ensure that incoming signals do not affect the reliability of the component.

12.5.1 Overshoot

The maximum overshoot and overshoot threshold duration specifications for inputs to the low-power embedded Pentium processor with MMX technology are described as follows:

- Maximum overshoot specification: The maximum overshoot of the CLK/PICCLK signals should not exceed V_{CC2}, nominal +0.6 V. The maximum overshoot of all other input signals should not exceed V_{CC3}, nominal +1.0 V.
- Overshoot threshold duration specification: The overshoot threshold duration is defined as the sum of all time during which the input signal is above V_{CC3}, nominal +0.3 V, within a single clock period. The overshoot threshold duration must not exceed 20% of the period.

Refer to Table 98 for a summary of the overshoot specifications for the low-power embedded Pentium processor with MMX technology.

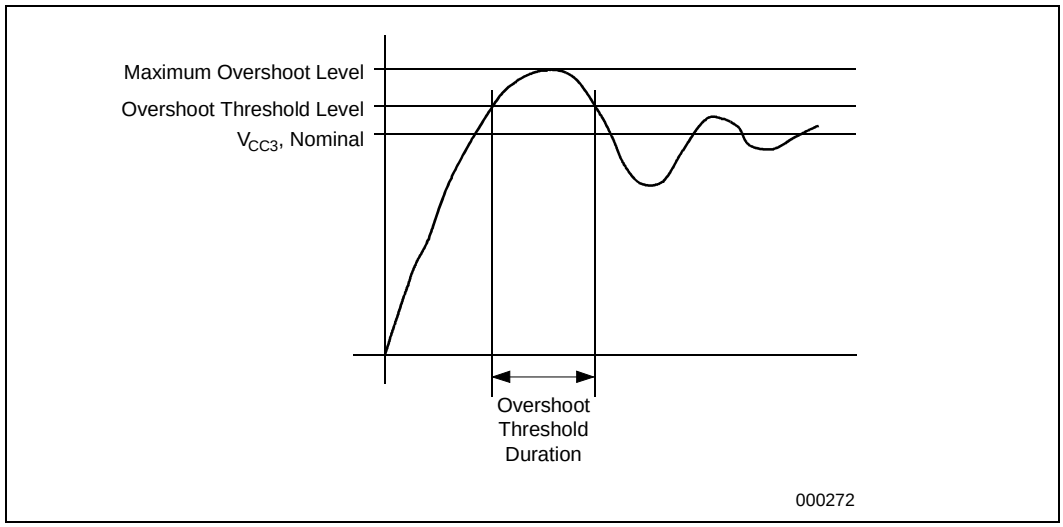
Table 98. Overshoot Specification Summary

Specification Name	Value	Units	Notes
Threshold Level	V_{CC3}, nominal +0.3	V	(1, 2)
Maximum Overshoot Level (CLK and PICCLK)	V_{CC3}, nominal +0.6	V	(1, 2)
Maximum Overshoot Level (all other inputs)	V_{CC3}, nominal +1.0	V	(1, 2)
Maximum Threshold Duration	20% of clock period above threshold voltage	ns	(2)
Maximum Ringback	V_{CC3}, nominal –0.7	V	(1, 2)

NOTES:

1. V_{CC3}, nominal refers to the voltage measured at the V_{CC3} pins.
2. See Figure 65 and Figure 67.

Figure 65. Maximum Overshoot Level, Overshoot Threshold Level and Overshoot Threshold Duration



12.5.2 Undershoot

The maximum undershoot and undershoot threshold duration specifications for inputs to the low-power embedded Pentium processor with MMX technology are described as follows:

- Maximum undershoot specification: The maximum undershoot of the CLK/PICCLK signals must not drop below –0.6 V. The maximum undershoot of all other input signals must not drop below –1.0 V.
- Undershoot threshold duration specification: The undershoot threshold duration is defined as the sum of all time during which the input signal is below –0.3 V within a single clock period. The undershoot threshold duration must not exceed 20% of the period.

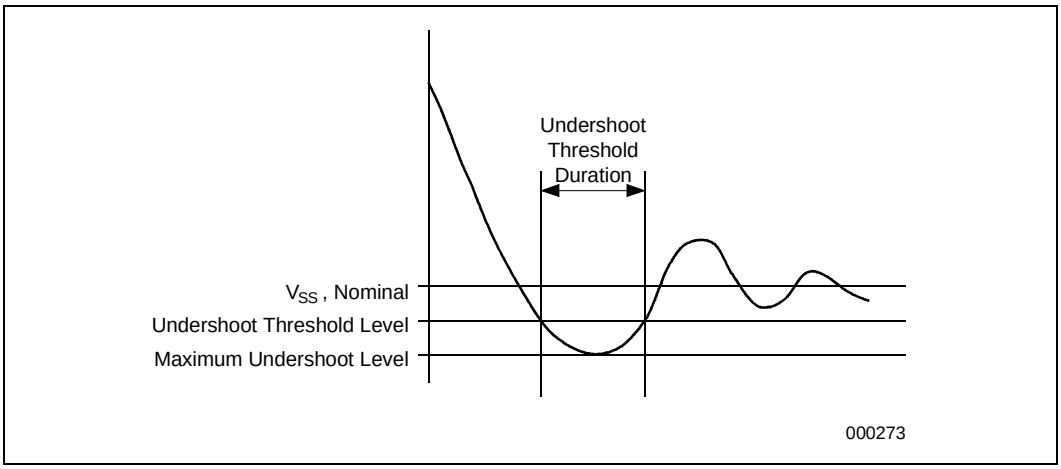
Refer to Table 99 for a summary of the undershoot specifications for the low-power embedded Pentium processor with MMX technology.

Table 99. Undershoot Specification Summary

Specification Name	Value	Units	Notes
Threshold Level	–0.3	V	(1)
Minimum Undershoot Level (CLK and PICCLK)	–0.6	V	(1)
Minimum Undershoot Level (all other inputs)	–1.0	V	(1)
Maximum Threshold Duration	20% of clock period below threshold voltage	ns	(1)
Maximum Ringback	0.5	V	(1)

NOTE:
1. See Figure 66 and Figure 68.

Figure 66. Maximum Undershoot Level, Undershoot Threshold Level and Undershoot Threshold Duration



12.5.3 Ringback

Excessive ringback can contribute to long-term reliability degradation of the low-power embedded Pentium processor with MMX technology, and can cause false signal detection. Ringback is simulated at the input pin of a component using the input buffer model. Ringback can be simulated with or without the diodes that are in the input buffer model.

Ringback is the absolute value of the maximum voltage at the receiving pin below V_{CC3} (or above V_{SS}) relative to the V_{CC3} (or V_{SS}) level after the signal has reached its maximum voltage level. The input diodes are assumed present.

If simulated without the input diodes, follow the Maximum Overshoot/Undershoot specifications. By meeting the overshoot/undershoot specifications, the signal is guaranteed not to ringback excessively.

If simulated with the diodes present in the input model, follow the maximum ringback specification. The maximum ringback specification for inputs to the low-power embedded Pentium processor with MMX technology is described as follows:

- Maximum ringback specification: The maximum ringback of inputs associated with their high states (overshoot) must not drop below V_{CC3} –1.0 V as shown in Figure 67. Similarly, the maximum ringback of inputs associated with their low states (undershoot) must not exceed 0.5 V as shown in Figure 68.
- Overshoot (undershoot) is the absolute value of the maximum voltage above V_{CC} (below V_{SS}). The guideline assumes the absence of diodes on the input.

Figure 67. Maximum Ringback Associated with the Signal High State

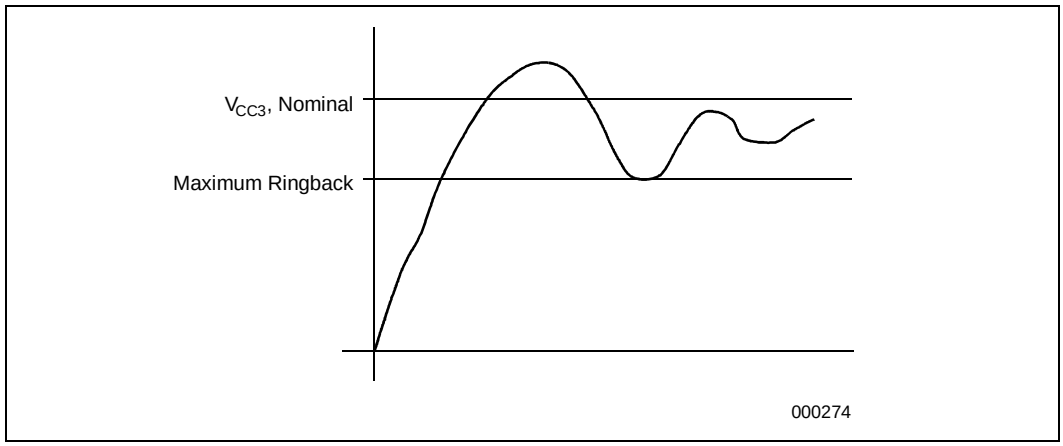
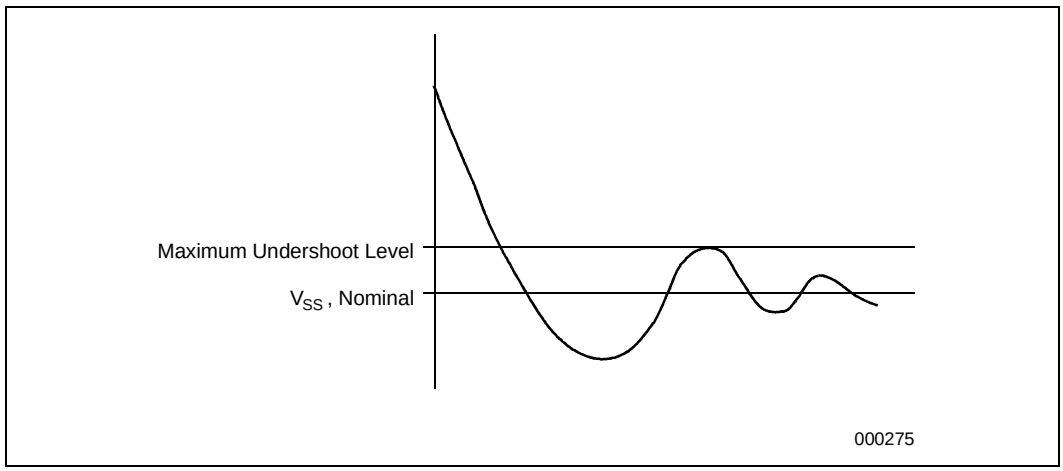


Figure 68. Maximum Ringback Associated with the Signal Low State



12.5.4 Settling Time

The settling time is defined as the time a signal requires the receiver to settle within 10 percent of V_{CC3} or V_{SS}. Settling time is the maximum time allowed for a signal to reach within 10 percent of its final value.

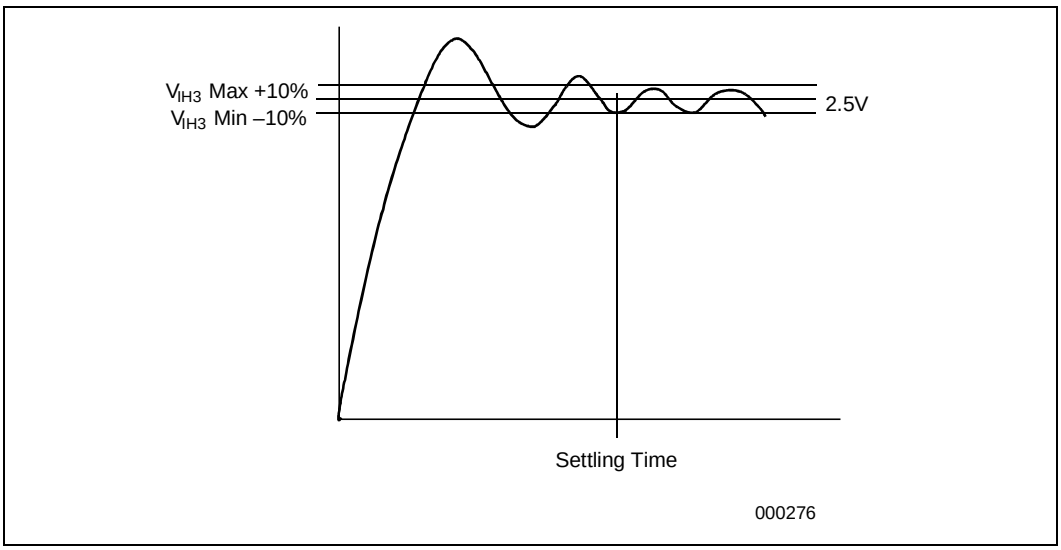
Most available simulation tools are unable to simulate settling time so that it accurately reflects silicon measurements. Second order, and other, effects on a physical board serve to dampen the signal at the receiver. Because of these concerns, settling time is a recommendation or a tool for layout tuning and not a specification.

To make sure that there is no impact on the flight times of the signals if the waveform has not settled, settling time is simulated at the slow corner. Settling time may be simulated with the diodes included or excluded from the input buffer model. If diodes are included, settling time recommendations will be easier to meet.

Although simulated settling time has not shown good correlation with physical, measured settling time, settling time simulations can still be used as a tool to tune layouts. Use the following procedure to verify board simulation and tuning with concerns for settling time:

1. Simulate settling time at the slow corner for a particular signal.
2. If settling time violations occur (signal requires more than 12.5 ns to settle to ±10% of its final value), simulate signal trace with DC diodes in place at the receiver pin. The DC diode behaves almost identically to the actual (non-linear) diode on the part as long as excessive overshoot does not occur.
3. If settling time violations still occur, simulate flight times for five consecutive cycles for that particular signal.
4. If flight time values are consistent over the five simulations, settling time should not be a concern. If, however, flight times are not consistent over the five consecutive cycles, tuning of the layout is required.
5. Note that, for signals that are allocated two cycles for flight time, the recommended settling time is doubled. Maximum Settling Time to within 10 percent of V_{IH} or V_{IL} is 12.5 ns at 66 MHz.

Figure 69. Settling Time



12.5.5 Measurement Methodology

The waveform of the input signals should be measured at the processor pins using an oscilloscope with a 3 dB bandwidth of at least 20 MHz (100 ms/s digital sampling rate). There should be a short isolation ground lead attached to a processor pin on the bottom side of the board. A 1-MΩ probe with loading of less than 1 pF is recommended. The measurement should be taken at the input pins and their nearest V_{SS} pins.

12.6 Measuring Maximum Overshoot, Undershoot and Ringback

The display should show continuous sampling (e.g., infinite persistence) of the waveform at 500 mV/div and 5 ns/div (for CLK) or 20 ns/div (for other inputs) for a recommended duration of approximately five seconds. Adjust the vertical position to measure the maximum overshoot and associated ringback with the largest possible granularity. Similarly, readjust the vertical position to measure the maximum undershoot and associated ringback. There is no allowance for crossing the maximum overshoot, maximum undershoot or maximum ringback specifications.

12.7 Measuring Overshoot Threshold Duration

A snapshot of the input signal should be taken at 500 mV/div and 500 ps/div (for CLK) or 2 ns/div (for other inputs). Adjust the vertical position and horizontal offset position to view the threshold duration. The overshoot threshold duration is defined as the sum of all time during which the input signal is above V_{CC3} nominal + 0.3 V within a single clock period. The overshoot threshold duration must not exceed 20% of the period.

12.8 Measuring Undershoot Threshold Duration

A snapshot of the input signal should be taken at 500 mV/div and 500 ps/div (for CLK) or 2 ns/div (for other inputs). Adjust the vertical position and horizontal offset position to view the threshold duration. The undershoot threshold duration is defined as the sum of all time during which the clock signal is below –0.3 V within a single clock period. The undershoot threshold duration must not exceed 20% of the period.