Low-Power Pentium® Processor with MMX™ Technology

Evaluation Platform Manual

February 1999

Order Number: 273235-001

Contents

Figures

Tables

About This Manual 1

This manual tells you how to set up and use the Low-Power Pentium® Processor with MMX™ Technology Evaluation Platform.

1.1 Content Overview

Chapter 1, “About This Manual” - This chapter contains a description of conventions used in this manual. The last few sections tell you how to obtain literature and contact customer support.

Chapter 2, “Getting Started” - Provides complete instructions on how to configure the board by setting jumpers, connecting peripherals, providing power, and configuring the BIOS.

Chapter 3, “Theory Of Operation” - This chapter provides information on the system design.

Chapter 4, “Hardware Reference” - This chapter provides a description of jumper settings and functions, and pinout information for each connector.

Chapter 5, “BIOS Quick Reference” - This chapter describes how to configure the BIOS for your system configuration. A summary of all BIOS menu options is provided.

Appendix A, “PLD Code Listing” - This appendix includes a sample code listing for the Post Code Debugger.

Appendix B, “Bill of Materials” - This appendix contains the bill of materials for the development platform.

Appendix C, “Schematics” - This appendix contains schematics for selected connectors and subsystems for the evaluation platform.

1.2 Text Conventions

The following notations may be used throughout this manual.

#	The pound symbol (#) appended to a signal name indicates that the signal is active low.
Variables	Variables are shown in italics. Variables must be replaced with correct values.
Instructions	Instruction mnemonics are shown in uppercase. When you are programming, instructions are not case-sensitive. You may use either upper- or lowercase.

Numbers Hexadecimal numbers are represented by a string of hexadecimal digits followed by the character *H*. A zero prefix is added to numbers that begin with *A* through *F*. (For example, *FF* is shown as *0FFH*.) Decimal and binary numbers are represented by their customary notations. (That is, 255 is a decimal number and 1111 1111 is a binary number. In some cases, the letter *B* is added for clarity.)

Units of Measure The following abbreviations are used to represent units of measure:

A	amps, amperes
Gbyte	gigabytes
Kbyte	kilobytes
KΩ	kilo-ohms
mA	milliamps, milliamperes
Mbyte	megabytes
MHz	megahertz
ms	milliseconds
mW	milliwatts
ns	nanoseconds
pF	picofarads
W	watts
V	volts
µA	microamps, microamperes
µF	microfarads
µs	microseconds
µW	microwatts

Signal Names Signal names are shown in uppercase. When several signals share a common name, an individual signal is represented by the signal name followed by a number, while the group is represented by the signal name followed by a variable (*n*). For example, the lower chip-select signals are named CS0#, CS1#, CS2#, and so on; they are collectively called CS*n*#. A pound symbol (#) appended to a signal name identifies an active-low signal. Port pins are represented by the port abbreviation, a period, and the pin number (e.g., P1.0).

1.3 Technical Support

1.3.1 Electronic Support Systems

Intel's site on the World Wide Web (http://www.intel.com/) provides up-to-date technical information and product support. This information is available 24 hours per day, 7 days per week, providing technical information whenever you need it.

1.3.1.1 Online Documents

Product documentation is provided online in a variety of web-friendly formats at:

http://developer.intel.com/design/litcentr/index.htm

1.3.1.2 Intel Product Forums

Intel provides technical expertise through electronic messaging. With publicly accessible forums, you have all of the benefits of email technical support, with the added benefit of the option of viewing previous messages written by other participants, and providing suggestions and tips that can help others.

Each of Intel's technical support forums is based on a single product or product family. Questions and replies are limited to the topic of the particular forum. Intel also provides several non-technical support related forums.

Complete information on Intel forums is available at:

http://support.intel.com/newsgroups/index.htm

1.3.2 Telephone Technical Support

In the U.S. and Canada, technical support representatives are available to answer your questions between 5 a.m. and 5 p.m. PST. You can also fax your questions to us. (Please include your voice telephone number and indicate whether you prefer a response by phone or by fax). Outside the U.S. and Canada, please contact your local distributor.

1-800-628-8686	U.S. and Canada
916-356-7599	U.S. and Canada
916-356-6100 (fax)	U.S. and Canada

1.4 Product Literature

You can order product literature from the following Intel literature centers.

1-800-548-4725	U.S. and Canada
708-296-9333	U.S. (from overseas)
44(0)1793-431155	Europe (U.K.)
44(0)1793-421333	Germany
44(0)1793-421777	France
81(0)120-47-88-32	Japan (fax only)

1.5 Related Documents

Table 1-1. Related Resources

Document Title	Order Number
Low-Power Embedded Pentium® Processor with MMX™ Technology datasheet	273184
Pentium® Processor for Embedded Applications Specification Update	273183
Embedded Pentium® Processor Family Developer's Manual	273204
Embedded Pentium® Processor with MMX™ Technology Flexible Motherboard Design Guidelines	273206
Voltage Guidelines for Pentium® Processors with MMX™ Technology	243186
Intel Architecture Software Developer's Manual, Volume 1: Basic Architecture	243190
Intel Architecture Software Developer's Manual, Volume 2: Instruction Set Reference	243191
Intel Architecture Software Developer's Manual, Volume 3: System Programming Guide	243192
Intel® 430TX PCIset: 82439TX System Controller (MTXC) datasheet	290559
Intel 430TX PCIset (MTXC) Specification Update	290615
Intel® 430TX PCIset System Controller (MTXC) Timing Specification	273134
82371AB (PIIX4) and 82371EB (PIIX4E) PCI-TO-ISA/IDE Xcelerator datasheet	290562
Intel 82371EB (PIIX4E) Specification Update	290635
Intel 82371AB PCI ISA IDE Xcelerator (PIIX4) Timing Specification	273135

Getting Started 2

This chapter identifies the evaluation platform kit's key components, features and specifications, and tells you how to set up the board for operation.

2.1 Overview

The evaluation platform consists of a baseboard and a processor assembly.

- The processor assembly contains a low-power Pentium® processor with MMX™ technology and the System Controller from the Intel® 430TX PCIset chipset.
- The baseboard contains the 82371EB PCI ISA IDE Xcelerator (PIIX4E) and other system board components and peripheral connectors.

Warning: The assembly is attached to the baseboard at the factory. Do *not* remove the processor assembly from the baseboard. Intel will not support the processor assembly or the baseboard if the assembly is removed by the customer for any reason.

2.1.1 Processor Assembly Features

The processor assembly contains:

- 166 MHz or 266 MHz low-power Pentium processor with MMX technology
- 512 Kbyte L2 cache
- Intel 430TX PCIset: 82439TX System Controller (MTXC) with 66 MHz front side bus
- Core voltage regulator
- It is populated with an ITP connector to interface to an ITP debugger

See the *Low-Power Embedded Pentium® Processor with MMX™ Technology* datasheet for more information on the processor. See the *Intel® 430TX PCIset: 82439TX System Controller (MTXC)* datasheet for more information on the system controller.

2.1.2 Baseboard Features

The evaluation platform baseboard has these features:

- ATX form factor
- Flash system BIOS ROM
  - — General Software system BIOS
  - — In-circuit BIOS upgradability
- 2 SDRAM DIMM connectors
- 32-Mbyte SDRAM DIMM included
  - — 4 Mbyte x64, 3.3 V, 66 MHz with a CAS latency of 2

- User-accessible on-board connectors include:
  - Two serial RS-232 ports; COM1, COM2
  - One EPP/ECP parallel port
  - PS/2 keyboard and PS/2 mouse (6-pin mini-DIN connectors)
  - Two USB ports
  - Two IDE bus connectors
  - One floppy connector
  - Three PCI expansion slots and two ISA expansion slots. There are no shared slots so all are usable.
  - One AGP connector (reserved for future use)
  - Standard ATX power supply connector
- Miscellaneous features include:
  - On board post-code debugger (Port 80)
  - Reset push button
  - Stand-off feet for table-top operation

2.2 Included Hardware

- Evaluation platform (baseboard and processor assembly combination)
- 3.2-Gbyte hard disk drive pre-loaded with the QNX Real Time Operating System*
- 32-Mbyte SDRAM DIMM
- Attached heat sink and fan
- PCI video graphics adapter using the CHIPS* 69000 HiQVideo* Accelerator
- Mounting hardware
- IDE cable for the hard disk drive

2.3 Software Key Features

The software in the kit was chosen to facilitate development of real-time applications based on the components used in the evaluation platform. The software tools included in your kit are described in this section.

Note: Software in the kit is provided free by the vendor and is only licensed for evaluation purposes. Customers using the tools that work with Microsoft products must have licensed those products. Any targets created by those tools should also have appropriate licenses.

2.3.1 Annasoft Systems

Annasoft Systems is extending support for the Microsoft Windows CE PC platform found in Windows CE 2.0 Embedded Toolkit for Visual C++ (ETK). With Windows CE PC, embedded developers can now develop Windows CE applications on an inexpensive and readily available PC

platform. Annasoft takes Windows CE one step closer to your solution with the creation of CE Launcher. The CE Launcher allows you to boot Windows CE from any PC disk without the help of MS-DOS. Now any Pentium or 486 processor-based embedded PC platform can run Windows CE.

Jump Start your Windows CE PC development with Annasoft's CE Launcher. Features include:

- Launch Windows CE without the need for MS-DOS
- Small 11K footprint
- Any Pentium or 486 embedded PC can run Windows CE
- Boot Windows CE from any type of disk media

2.3.2 General Software, Inc.

Embedded BIOS is a full-featured BIOS for x86-based handheld, embedded, and volume consumer electronics applications. This product offers a winning combination of superior OEM configurability and superior embedded features.

Embedded BIOS leads the industry with all the on-target embedded features that OEMs making embedded, handheld, mobile, and consumer electronics demand:

- CE Ready*, the Windows CE* launcher
- Integrated BIOS-aware debugger
- Resident Flash Disk disk emulator
- ROM disk and RAM disk emulators
- Manufacturing Mode for in-field diagnosis and software upgrades
- Power management that can operate in an APM or stand-alone environment
- PCI resource management
- Matrix keyboard support
- LCD panel drivers
- Console redirection over RS232 ports
- Flexibility to boot from many disk servers
- OEM-configurable setup screen system
- Embedded DOS*-ROM (adaptation kit and license)
- Total compatibility with industry standards

2.3.3 QNX Software Systems, Ltd.

QNX Real Time Operating System for Intel Architecture.

- Small memory footprint of the QNX operating system with microGUI
- QNX microGUI is a full featured graphical user interface (GUI) and windowing system
- Photon Application Builder
- QNX Development kit provides the basic utilities to build and program Intel Flash
- Watcom C/C++ Development Suite: is a full featured development suite
- Includes compiler, assembler and debugger with full support for the QNX microGUI function library

- Makes development of the QNX executables fast, easy and optimized

2.3.4 RadiSys Corporation

INtime* provides real-time control with industry standard Windows NT.

- Field-proven real-time technology to maximize the reliability of your products
- Win32 API extensions provide real-time capabilities in a Windows NT environment
- Robust, non-intrusive integration with Windows NT ensures continued future compatibility with Windows NT
- Fully featured, high-end real-time capabilities for even the most demanding applications
- Fully integrated with Microsoft Visual Developer Studio C/C++, including real-time Wizard extensions
- Patented architecture provides protected real-time execution
- Full memory protection for real-time kernel and real-time tasks
- Ensures survival of real-time threads in the event of total Windows failure

2.3.5 VenturCom, Inc.

2.3.5.1 Real-Time Extension* (RTX)

- Delivers real-time response for Windows NT applications
- Deterministic response times
- Fixed-priority scheduling with 128 priorities
- IPC with semaphores, mail slots, and shared memory objects
- Real-time process and thread management
- Memory locking, mapping and management functions
- High-speed clocks and timers
- Perform direct I/O register reads and writes
- Manage hardware interrupts

2.3.5.2 Component Integrator* (CI)

- Configuration management tools to efficiently build dedicated Windows NT systems
- Import custom applications and commercial-off-the-shelf components
- Build embedded Windows NT systems
- Utilize VenturCom's embedded and real-time extensions
- Analyze RAM and persistent storage requirements
- Validate system completeness
- Preconfigure operating system and applications

2.3.6 WindRiver Systems

Tornado* Evaluation Kit 1.0.1; Tornado Development Environment

- A superior development and deployment platform for the embedded developer
- Makes all tools available regardless of target resources or connection strategy
- Runs on UNIX workstation or PCs using Microsoft Windows 95 or Windows NT
- Offers published APIs for easy customization and third-party tool integration
- Provides central “control panel” and productivity-enhancing GUI
- Supports industry standards including ANSI-C, POSIX, and Tcl
- Includes the proven, high-performance VxWorks* operating system
- Scalable across all real-time implementations

2.4 Before You Begin

Before you set up and configure your evaluation board, you may want to gather some additional hardware and software.

VGA Monitor	You can use any standard VGA or multi-resolution monitor. The setup instructions in this chapter assume that you are using a standard VGA monitor.
Power Supply	You must use an ATX-type PC power supply.
Keyboard	You need a keyboard with a PS/2 style connector or adapter.
Mouse	Optional. You can use a mouse with a PS/2 style connector or adapter.
Floppy or CD-ROM Drive	You can connect up to four IDE drives and a floppy drive to the evaluation platform. Two devices (master and slave) can be attached to each IDE connector. You will need to provide the cables for these drives. You may have all these storage devices attached to the board at the same time.
Video Adapter	You can use the Chips and Technologies video adapter supplied with your kit, or you can use a different adapter. The evaluation board supports both PCI and ISA video cards. It is up to you to install the correct drivers for video adapters other than the one provided. The AGP slot located on the board is reserved for future use.
Other Devices and Adapters	The evaluation platform behaves much like a standard desktop computer motherboard. Most PC compatible peripherals can be attached and configured to work with the evaluation board. For example, you may want to install a sound card or network adapter.

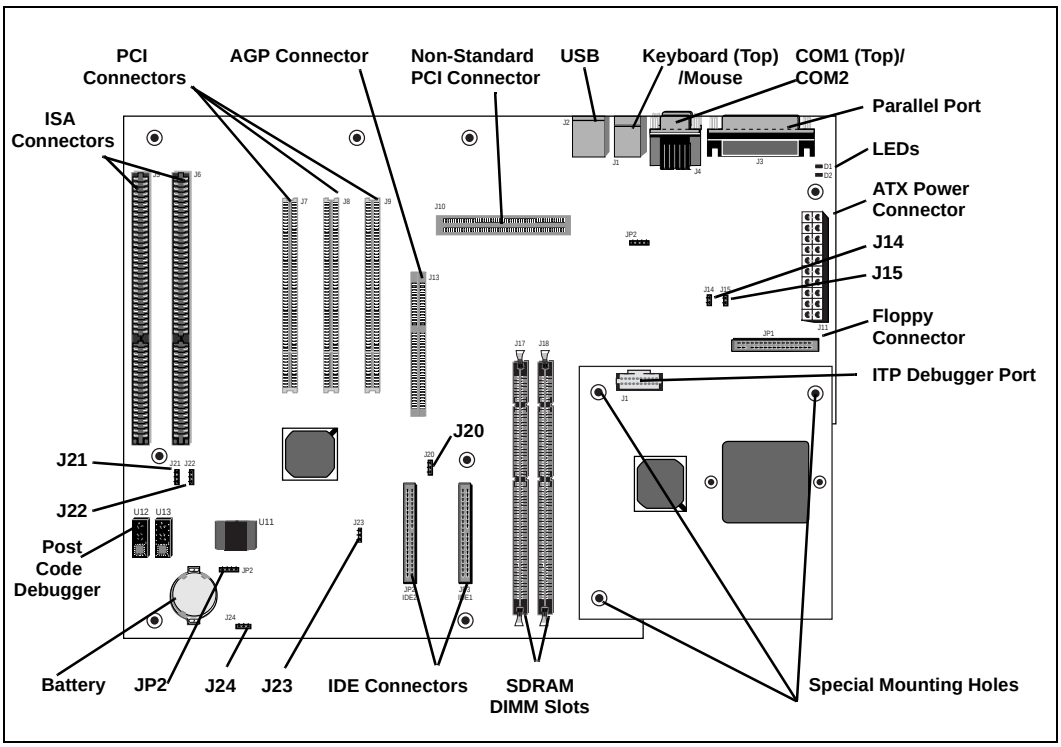
2.5 Setting up the Evaluation Platform

Once you have gathered the hardware described in the last section, follow the steps below to set up your evaluation platform. This manual assumes you are familiar with basic concepts involved with installing and configuring hardware for a personal computer system. Refer to Figure 2-1 for locations of connectors, jumpers, etc.

1. Make sure you are in a static-free environment before removing any components from their anti-static packaging. The evaluation board is susceptible to electro-static discharge damage; such damage may cause product failure or unpredictable operation.
2. Inspect the contents of your kit. Check for damage that may have occurred during shipment. Contact your sales representative if any items are missing or damaged.

Caution: Connecting the wrong cable or reversing the cable can damage the evaluation board and may damage the device being connected. Since the board is not in a protective chassis, use caution when connecting cables to this product.

Figure 2-1. Evaluation Platform Jumpers and Connectors



3. Make sure the board's jumpers are set to the following default locations.

- J14 - Not installed
- J15 - Installed
- J20 - Jumper pins 2-3
- J21 - Jumper pins 2-3
- J22 - Jumper pins 2-3
- J23 - Jumper pins 2-3
- J24 - Jumper pins 1-2

4. Mount the hardware:

   - Table-top operation: The evaluation platform is shipped with standoff “feet” for use in a table-top environment. These feet are installed on the evaluation platform to raise it off the table surface.Your kit contains two bags of mounting hardware. One bag contains eight standoff feet, eight mounting screws, and eight washers. Another bag has three *shorter* feet that must be attached slightly differently.

     — To mount the eight standard feet, insert a washer onto a screw, then push the screw through the top of the board. From below the board, thread one of the longer feet onto the screw.

     — To mount the three special feet, screw the three *shorter* feet onto the existing screws. See Figure 2-1 for the location of the three special holes.

Warning: Do not remove the nuts from these three holes! This will detach the processor assembly from the baseboard, and Intel will no longer support the evaluation platform.

   - The evaluation platform can also be mounted in a standard ATX-style chassis.

5. Connect desired storage devices to the evaluation platform:

   The evaluation platform supports Primary and Secondary IDE interfaces that can each host one or two devices (master/slave). When you are using multiple devices, such as a hard disk and a CD-ROM drive, make sure the hard disk drive has a jumper in the master position and the CD-ROM has a jumper in the slave position. When you are using a single IDE device with the evaluation board, be sure that the jumpers set correctly for single master operation. For jumper settings for other configurations, consult the drive’s documentation.

Note: The evaluation platform BIOS only supports hard drives of 16 Gbytes or less.

   - Installing the IDE hard disk drive included in your kit:

     — Connect the hard drive’s IDE connector to the JP4 connector on the evaluation board. Be sure to align Pin 1 of the cable connector with pin 1 of JP4.

     — Connect the other end to the hard disk drive.

Caution: Make sure the tracer on the ribbon cable is aligned with pin 1 on both the hard disk and the IDE connector header. Connecting the cable backwards can damage the evaluation platform or the hard disk.

     — Connect the hard drive to the power supply.

Note: The hard disk is already formatted and is pre-loaded with the QNX Real-Time Operating System for Intel Architecture.

     — You may have to make changes to the system BIOS to enable this hard disk. See Chapter 5, “BIOS Quick Reference” for more information.

   - Floppy drive: A floppy disk drive connected to the evaluation board is the most direct method for loading software.

     — Insert floppy cable into JP1 (be sure to orient Pin 1 correctly).

     — Connect the other end of the ribbon cable to the floppy drive.

     — Connect a power cable to the floppy drive.

     — You must make changes to the system BIOS to enable this floppy disk. See Chapter 5, “BIOS Quick Reference” for more information.

6. Make sure the SDRAM DIMM is installed in the socket labeled J18.
7. Connect a PS/2 mouse and keyboard (see Figure 2-1 for connector locations).

Note: J1 (on the baseboard) is a stacked PS/2 connector. The *bottom* connector is for the mouse and the *top* is for the keyboard.

8. Make sure the fan's power connector is plugged into Jumper J12.
9. Install the Chips and Technologies PCI video adapter into one of the available PCI slots. Connect the monitor cable to the VGA port on the card.
10. Connect the power supply:

    You'll need a standard ATX PC power supply. Make sure the power supply is unplugged (or turned off), then connect the power supply cable to the power header (J11).

Note: Some ATX power supplies do not have an on/off switch. In this case remove jumper J20 before plugging in the ATX power connector. J20 controls an internal power supply on/off switch. When you are ready to apply power, insert the jumper on pins 2-3. You may want to wire this header up to a toggle switch for convenience.

When the power is on you should see two power-indicator LEDs light up (located next to the ATX power connector in the upper right corner of the board, see Figure 2-1). Check to see that the fan on the processor is operating.

Follow the instructions in the next section for entering the BIOS setup screens and configuring the BIOS according to your needs (hard drive parameters, floppy drive, operating system, etc.).

2.6 Configuring the BIOS

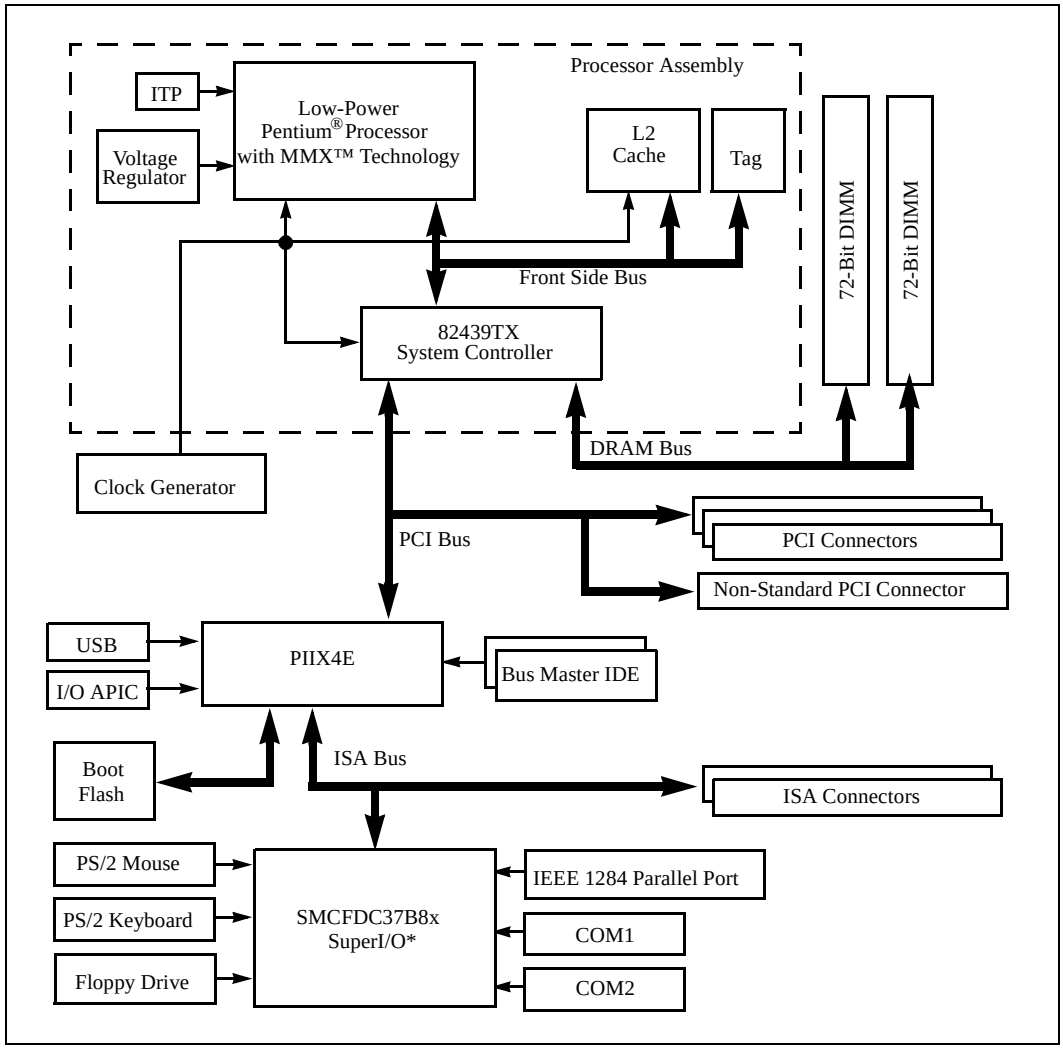
General Software's BIOS software is pre-loaded on the evaluation platform. You will have to make changes to the BIOS to enable hard disks, floppy disks and other supported features You can use the Setup program to modify BIOS settings and control the special features of the system. Setup options are configured through a menu-driven user interface. Chapter 5, "BIOS Quick Reference" contains a description of BIOS options.

BIOS updates may periodically be posted to Intel's Developers' web site at http://developer.intel.com/.

Theory Of Operation 3

3.1 Block Diagram

Figure 3-1. Evaluation Platform Block Diagram



3.2 Mechanical Design

The evaluation board conforms to the ATX form factor. For extra protection in a development environment users may want to install the evaluation board in an ATX chassis. The evaluation board has two ISA connectors, four PCI connectors and two DRAM DIMM connectors across the back. The I/O connectors are in the rear of the board in the defined ATX I/O window.

3.3 System Operation

The low-power Pentium® processor with MMX™ technology evaluation platform is a full-featured ATX form-factor system board and processor assembly that includes a 166 MHz or 266 MHz low-power Pentium processor with MMX technology. The evaluation platform also features 512 Kbytes of L2 cache, the Intel 82439 TX (MTXC) system controller, the Intel 82371EB PCI ISA IDE Xcelerator (PIIX4E), and other system and I/O peripherals.

3.3.1 82439TX System Controller

The 82439TX System Controller (MTXC) provides a completely integrated solution for the system controller and data path components in a Pentium processor system. The MTXC has a 64-bit host and DRAM bus interface, a 32-bit PCI bus interface, a second level cache interface and it integrates the PCI arbiter.

The MTXC interfaces with the Pentium processor host bus, a dedicated memory data bus, and the PCI bus. The MTXC bus interfaces are designed to interface with 2.5 V, 3.3 V and 5 V busses. The MTXC implements 2.5 V and 3.3 V drivers and 5 V tolerant receivers. The MTXC connects directly to the Pentium processor 3.3 V or 2.5 V host bus, directly to 5 V or 3.3 V DRAMs, and directly to the 5 V or 3.3 V PCI bus. The 430TX also interfaces directly to the 3.3 V or 5.0 V TAG RAM and 3.3 V Cache.

3.3.2 Processor

The low-power embedded Pentium processors with MMX technology for high performance embedded applications (166 and 266 MHz) are fully compatible with the existing Pentium processors with MMX technology (200 and 233 MHz) with the following differences: voltage supplies, power consumption, and performance.

The low-power embedded Pentium processor with MMX technology has several features which allow for high-performance embedded designs. These features include the following:

- 1.8 V core (HL-PBGA – 166), 2.0 V core (HL-PBGA – 266)
- 2.5 V I/O buffer V_{CC3} inputs to reduce power consumption
- SL Enhanced feature set

The processor used on the evaluation platform is a low-power embedded Pentium processor with MMX technology in a 352-ball High-Thermal Low-Profile–Plastic Ball Grid Array (HL-PBGA) package. The HL-PBGA package allows designers to use surface mount technology to create small form-factor designs.

3.3.3 L2 Cache

The second level cache is direct mapped and supports a 512-Kbyte SRAM configuration using pipeline burst SRAM or DRAM cache SRAM. The cache line read/write performance is 3-1-1-1 and the performance for back-to-back reads that are pipelined is 3-1-1-1-1-1-1-1.

3.3.4 ITP

The evaluation platform is populated with a 2.5 V ITP debugger port. The ITP port provides a path for debugger tools like emulators, in-target probes, and logic analyzers to gain access to the Pentium processor's registers and signals without affecting high speed operation. This allows the system to operate at full speed with the debugger attached.

3.3.5 82371EB PCI to ISA/IDE Xcelerator (PIIX4E)

The 82371EB is the PCI south bridge. The 82371EB connects to the PCI bus and requests control of the PCI bus via the PHOLD# signal and becomes the PCI master upon receipt of the PHOLDA# signal from the processor assembly. The PIIX4E contains the PCI and ISA interrupt controller, along with legacy functions such as a DMA controller, a bus master IDE interface, an ISA bus interface, and a boot ROM interface. A USB hub controller is also included.

3.3.6 DRAM

The evaluation platform provides two 168-pin DIMM module connectors. The DRAM interface is a 64-bit data path that supports Synchronous DRAM (SDRAM). The DRAM interface supports 4 Mbytes to 256 Mbytes of 4-Mbit, 16-Mbit and 64-Mbit DRAM and SRAM technology (both symmetrical and asymmetrical). Parity is not supported. One 32-Mbyte SDRAM DIMM is included in the kit.

3.3.7 Power

The evaluation board uses an industry standard ATX-style power supply with a 20-pin connector. A 230-watt (minimum) supply is recommended. Note that the ATX power connector is keyed to prevent incorrect insertion. See "ATX Power Connector" on page 4-3 for a detailed description of the power connector.

Make sure that the ATX power supply is *not* plugged into the wall when connecting or disconnecting it from the evaluation board.

3.3.8 Boot ROM

The system boot ROM installed at U11 is a 2-Mbit 28F002BC flash device. The system is set up for in-circuit reprogramming of the BIOS, but the flash device is also socketed. This device is addressable on the XD bus extension of the ISA bus.

3.3.9 RTC/NVRAM

The RTC and NVRAM are contained within the 82371EB PIIX4E device. CMOS NVRAM backup is provided by a 3-V lithium-ion battery.

3.3.10 Legacy I/O

Support for legacy I/O functions is provided by the Intel 82371EB PIIX4E and the SMC FDC37B8X SuperI/O* device.

3.3.11 IDE Support

The evaluation board supports both a primary and secondary IDE interface via two 40-pin IDE connectors. The connector labeled IDE1 is the primary interface. IDE2 is the secondary interface.

3.3.12 Floppy Disk Support

Floppy disk support is provided by the SMC FDC37B8X SuperI/O device. One 34-pin floppy connector is provided on the evaluation board.

3.3.13 Keyboard/Mouse

Keyboard and mouse support are provided by the SMC FDC37B8X SuperI/O device. The keyboard and mouse connectors (J1) are PS/2 style, 6-pin stacked miniature DIN connectors. The top connector is for the keyboard and the bottom connector is for the mouse.

3.3.14 USB

USB support is provided through the PIIX4E and can be used through connectors J2.

3.3.15 RS232 Ports

Two serial I/O ports provided by the SMC FDC37B78X SuperI/O device. Two 9-pin RS232 connectors are provided on a single stacked connector (J4).

3.3.16 IEEE 1284 Parallel Port

One 25-pin IEEE 1284 parallel port connector controlled by the SMC FDC37B78X SuperI/O device is provided (J3).

3.3.17 PCI Connectors

Three industry standard 32-bit, 5-V PCI connectors are provided on the evaluation platform. The connectors are designed to handle either a 5-V only card or a universal card. 3.3-V cards are not supported.

There is a fourth connector, J10, which is a custom PCI expansion connector. This connector is reserved for future devices that may be included with the kit at a later date. This connector is *not* compliant with any PCI industry standard and is not supported outside the scope of this evaluation board.

3.3.18 ISA Connectors

Two 16-bit ISA connectors are provided on the evaluation board.

3.3.19 AGP Connector

Connector J13 is reserved for AGP graphics cards. These cards are *not* supported with this version of the evaluation boards, since the Pentium processor and 82439TX Host System controller combination does not support AGP.

3.3.20 Post Code Debugger

The evaluation board has an on-board Post Code Debugger. Data from any program that does an I/O write to 0080H is latched and displayed on the two LEDs (U12 and U13). During BIOS startup, codes are posted to these LEDs to indicate what the BIOS is doing. Application programs can post their own data to these LEDs by writing to I/O address 0080H.

3.3.21 Clock Generation

There are three devices on the baseboard which generate and distribute the clocks used by the entire system. These are the CY2280 clock synthesizer, CY2318NZ clock buffer and the CY23009 zero delay buffer. Not all of these devices are used on this version of the evaluation platform.

The CY2280 generates the clocks for the processor, System Controller, cache, PCI, USB and ISA bus. The processor clock runs at 66 MHz. The PCI clocks run at 33 MHz. This device is capable of spread spectrum clocking. If spread spectrum clocking is enabled, a 0.5% down spread will be introduced in the processor and PCI clocks.

The CY2309 Zero Delay Buffer is used to buffer the clock signals sent to the SDRAM DIMMS. The SDRAM interface operates at 66 MHz.

The CY2318NZ clock buffer is not used by the evaluation platform.

3.3.22 Interrupt Map

Table 3-1. Interrupts

IRQ	System Resources
NMI	I/O Channel Check
0	Reserved, Interval Timer
1	Reserved, Keyboard buffer full
2	Reserved, Cascade interrupt from slave PIC
3	Serial Port 2
4	Serial Port 1
5	Parallel Port (PNP0 option)
6	Floppy
7	Parallel Port 1
8	Real Time Clock
9	IRQ2 Redirect
10	Reserved. Not supported.

Table 3-1. Interrupts

IRQ	System Resources
11	Reserved. Not supported.
12	Onboard Mouse Port if present, else user available
13	Reserved, Math coprocessor
14	Primary IDE if present, else user available
15	Reserved. Not supported.

3.3.23 Memory Map

Table 3-2. Memory Map

Address Range (Hex)	Size	Description
100000-8000000	127.25M	Extended Memory
E0000-FFFFF	128K	BIOS
C8000-DFFFF		Available expansion BIOS area (Flash disk memory window)
A0000-C7FFF		Off-board video memory and BIOS
9FC00-9FFFF	1K	Extended BIOS Data (movable by QEMM, 386MAX)
80000-9FBFF	127K	Extended conventional
00000-7FFFF	512K	Conventional

Hardware Reference 4

This section provides reference information on the system design. Included in this section is connector pinout information, jumper settings, and other system design information.

- Processor Assembly
- In-Circuit BIOS Update
- Post Code Debugger
- ITP Debugger Port
- ISA and PCI Expansion Slots
- PCI Device Mapping
- Connector Pinouts
- Jumpers

4.1 Processor Assembly

The processor assembly contains all of the host bus devices such as the low power Pentium processor with MMX technology, the 82439TX System Controller (MTXC), L2 cache, and tag RAM. The processor assembly also includes a voltage regulator and an ITP debugger connector. The assembly connects to the baseboard via a 400-pin connector.

Warning: The assembly is attached to the baseboard at the factory. Do *not* remove the processor assembly from the baseboard. Intel will not support the processor assembly or the baseboard if the assembly is removed by the customer for any reason.

4.2 In-Circuit BIOS Update

The BIOS can be upgraded in-circuit. BIOS updates may periodically be posted to Intel's Developers' site at http://www.intel.com/design/.

To reprogram the BIOS:

1. Download the new BIOS upgrade file from Intel's Developers' web site.
2. Extract the BIOS upgrade zip file onto a bootable floppy.
3. Insert the floppy disk into the floppy drive attached to the evaluation board.
4. Reboot the evaluation board so that it reboots from the floppy.
5. Follow the on-screen instructions.

4.3 Post Code Debugger

The evaluation board has an on-board Post Code Debugger. Data from any code that does an I/O write to 80H is latched on the two led displays (U12/U13). During BIOS startup, code is posted to these LEDs to indicate what the BIOS is doing. Application code can post its own data to these LEDs by doing an I/O write to address 80H. The 22V10 PLD code used to implement this function is included in Appendix A, “PLD Code Listing.”

4.4 ITP Debugger Port

The evaluation platform is populated with a 2.5 V ITP debugger port. The ITP port provides a path for debugger tools like emulators, in-target probes, and logic analyzers to gain access to the Pentium processor’s registers and signals without affecting high speed operation. This allows the system to operate at full speed with the debugger attached.

4.5 ISA and PCI Expansion Slots

The evaluation platform has three PCI expansion slots and two ISA slots.

4.6 PCI Device Mapping

On the evaluation platform the PCI devices are mapped to PCI device numbers by connecting an address line to the IDSEL signal of each PCI device. Table 4-1 shows the mapping of PCI devices.

Table 4-1. PCI Device Mapping

Device	Address Line	PCI Device Number
PIIX4E	AD18	7
PCI Slot 0 (J7)	AD28	17
PCI Slot 1 (J8)	AD29	18
PCI Slot 2 (J9)	AD30	19
PCI Connector 3 (J10)	AD31	20

4.7 Connector Pinouts

4.7.1 ATX Power Connector

Table 4-2 shows the signals assigned to the ATX style power connector.

Table 4-2. Primary Power Connector (J11)

Pin	Name	Function
1	3.3 V	3.3 V
2	3.3 V	3.3 V
3	GND	Ground
4	+5V	+5 V VCC
5	GND	Ground
6	+5V	+5 V VCC
7	GND	Ground
8	PWRGD	Power Good
9	5VSB	Standby 5 V
10	+12 V	+12 V
11	3.3 V	3.3 V
12	–12 V	–12 V
13	GND	Ground
14	PS_ON#	Soft-off control
15	GND	Ground
16	GND	Ground
17	GND	Ground
18	–5 V	–5 Volts
19	+5 V	+5 V VCC
20	+5 V	+5 V VCC

4.7.2 ITP Debugger Connector

Table 4-3. ITP Connector Pin Assignment (J1 on the Processor Module)

Pin	Signal	Pin	Signal
1	INIT	11	PRDY
2	DBRESET	12	TDI
3	RESET	13	TDO
4	GND	14	TMS
5	N/C	15	GND
6	3.3V	16	TCLK
7	R/S#	17	GND
8	GND	18	TRST#
9	N/C	19	N/C
10	GND	20	N/C

4.7.3 Stacked USB

P0 is the bottom connector. P1 is on top.

Table 4-4. USB Connector Pinout (J2)

Pin	P0 Signals	P1 Signals
1	VCC0	VCC1
2	D0-	D1-
3	D0+	D1+
4	GND0	GND1

4.7.4 Mouse and Keyboard Connectors

The keyboard port is on top. The mouse port is on the bottom.

Table 4-5. Keyboard and Mouse Connector Pinouts (J1 on the Baseboard)

Pin	Signal Name
1	Data
2	No Connect
3	Ground
4	+5 V (fused)
5	Clock
6	No Connect

4.7.5 Parallel Port

Table 4-6. DB25 Parallel Port Connector Pinout (J3)

Pin	Signal Name	Pin	Signal Name
1	Strobe#	14	Auto Feed#
2	Data Bit 0	15	Fault#
3	Data Bit 1	16	INIT#
4	Data Bit 2	17	SLCT IN#
5	Data Bit 3	18	Ground
6	Data Bit 4	19	Ground
7	Data Bit 5	20	Ground
8	Data Bit 6	21	Ground
9	Data Bit 7	22	Ground
10	ACK#	23	Ground
11	Busy	24	Ground
12	Paper end	25	Ground
13	SLCT		

4.7.6 Serial Ports

COM1 is the top connector. COM2 is the bottom connector.

Table 4-7. Serial Port Connector Pinout (J4)

Pin	Signal Name
1	DCD
2	Serial In (SIN)
3	Serial Out (SOUT)
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

4.7.7 IDE Connector

Table 4-8. PCI IDE1 (JP3) and IDE2 (JP4) Connector

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Host Data 7	4	Host Data 8
5	Host Data 6	6	Host Data 9
7	Host Data 5	8	Host Data 10
9	Host Data 4	10	Host Data 11
11	Host Data 3	12	Host Data 12
13	Host Data 2	14	Host Data 13
15	Host Data 1	16	Host Data 14
17	Host Data 0	18	Host Data 15
19	Ground	20	Key
21	DRQ3	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	BALE
29	DACK3#	30	Ground
31	IRQ14	32	IOCS16#
33	Addr 1	34	Ground
35	Addr 0	36	Addr 2
37	Chip Select 0#	38	Chip Select 1#
39	Activity	40	Ground

4.7.8 Floppy Drive Connector

Table 4-9. Diskette Drive Header Connector (JP1)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	FDHDIN
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	Index
9	Ground	10	Motor Enable A#
11	Ground	12	Drive Select B#
13	Ground	14	Drive Select A#
15	Ground	16	Motor Enable B#
17	Ground	18	DIR#
19	Ground	20	STEP#
21	Ground	22	Write Data#
23	Ground	24	Write Gate#
25	Ground	26	Track 00#
27	Ground	28	Write Protect#
29	Ground	30	Read Data#
31	Ground	32	Side 1 Select#
33	Ground	34	Diskette Change#

4.7.9 PCI Slot Connector

Table 4-10. PCI Slots J7, J8, J9)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	VCC	B1	- 12V	A32	AD16	B32	AD17
A2	+ 12V	B2	GND	A33	3.3V	B33	CBE2#
A3	VCC	B3	GND	A34	FRAME#	B34	GND
A4	VCC	B4	No Connect	A35	GND	B35	IRDY#
A5	VCC	B5	VCC	A36	TRDY#	B36	3.3 V
A6	PIRQ1#	B6	VCC	A37	GND	B37	DEVSEL#
A7	PIRQ3#	B7	PIRQ2#	A38	STOP#	B38	GND
A8	VCC	B8	PIRQ0	A39	3.3 V	B39	LOCK#
A9	No Connect	B9	PRSNT1B#	A40	SDONE	B40	PERR#
A10	VCC	B10	No Connect	A41	SBO#	B41	3.3 V
A11	No Connect	B11	PRSNT2B#	A42	GND	B42	SERR#
A12	GND	B12	GND	A43	PAR	B43	3.3V
A13	GND	B13	GND	A44	AD15	B44	CBE1#
A14	No Connect	B14	No Connect	A45	3.3V	B45	AD14
A15	RST#	B15	GND	A46	AD13	B46	GND
A16	VCC	B16	PCLK3	A47	AD11	B47	AD12
A17	GNT1#	B17	GND	A48	GND	B48	AD10
A18	GND	B18	REQ#	A49	AD9	B49	GND
A19	Reserved	B19	VCC	A50	KEY	B50	KEY
A20	AD30	B20	AD31	A51	KEY	B51	KEY
A21	3.3V	B21	AD29	A52	CBEO#	B52	AD8
A22	AD28	B22	GND	A53	3.3 V	B53	AD7
A23	AD26	B23	AD27	A54	AD6	B54	3.3 V
A24	GND	B24	AD25	A55	AD4	B55	AD5
A25	AD24	B25	3.3 V	A56	GND	B56	AD3
A26	IDSEL	B26	CBE3#	A57	AD2	B57	GND
A27	3.3V	B27	AD23	A58	AD0	B58	AD1
A28	AD22	B28	GND	A59	VCC	B59	VCC
A29	AD20	B29	AD21	A60	REQ64#	B60	ACK64#
A30	GND	B30	AD19	A61	VCC	B61	VCC
A31	AD18	B31	3.3 V	A62	VCC	B62	VCC

4.7.10 ISA Slot Connector

Table 4-11. ISA Slots (J5, J6)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	IOCHK#	B1	GND	A26	SA5	B26	DACK2#
A2	SD7	B2	RSTSLOT	A27	SA4	B27	TC
A3	SD6	B3	VCC	A28	SA3	B28	BALE
A4	SD5	B4	IRQB9	A29	SA2	B29	VCC
A5	SD4	B5	–5V	A30	SA1	B30	OSC
A6	SD3	B6	DREQ2	A31	SA0	B31	GND
A7	SD2	B7	–12V	C1	SBHE#	D1	MEMCS16#
A8	SD1	B8	ZEROWS#	C2	LA23	D2	IOCS16#
A9	SD0	B9	+12V	C3	LA22	D3	IRQB10
A10	IOCHRDY	B10	GND	C4	LA21	D4	IRQB11
A11	AEN	B11	SMEMW#	C5	LA20	D5	IRQB11
A12	SA19	B12	SMEMR#	C6	LA19	D6	IRQ15
A13	SA18	B13	IOW#	C7	LA18	D7	IRQ14
A14	SA17	B14	IOR#	C8	LA17	D8	DACK0
A15	SA16	B15	DACK3#	C9	MEMR#	D9	DREQ0
A16	SA15	B16	DREQ3	C10	MEMW#	D10	DACK5
A17	SA14	B17	DACK1#	C11	SD8	D11	DREQ5
A18	SA13	B18	DREQ1	C12	SD9	D12	DACK6#
A19	SA12	B19	REFRESH#	C13	SD10	D13	DREQ6
A20	SA11	B20	SYSCLK	C14	SD11	D14	DACK7#
A21	SA10	B21	IRQA7	C15	SD12	D15	DREQ7#
A22	SA9	B22	IRQA6	C16	SD13	D16	VCC
A23	SA8	B23	IRQA5	C17	SD14	D17	MASTER#
A24	SA7	B24	IRQA4	C18	SD15	D18	GND
A25	SA6	B25	IRQA3				

4.8 Jumpers

Table 4-12 shows default Jumper settings.

Table 4-12. Default Jumper Settings

Jumper	Function	Settings
J14	Enable Spread Spectrum Clocking	In – Enable Spread Spectrum Out – Disable Spread Spectrum (Default)
J15	Clock Frequency Selection	In – 66 MHz Processor Clock (Default) Out – Reserved
J20	On/Off	1-2 Reserved 2-3 On (Default) No Jumper Installed – Off
J21	Flash BIOS VPP Select	1-2 12 V 2-3 5 V (Default)
J22	Flash BIOS boot block control	1-2 12 V 2 –3 5 V (Default)
J23	SMI# Source	1-2 SMI# controlled by IOAPIC 2-3 SMI# controlled by PIIX4E (Default)
J24	CMOS RAM Clear	1-2 Normal Operation (Default) 2-3 Clear CMOS RAM

4.8.1 Clock Frequency Selection (J15)

This jumper controls the frequency of the processor clock. When the jumper is in 66 MHz operation is supported. This is the only setting supported by this evaluation kit.

Caution: Leave this jumper installed. When the jumper is out, 100 MHz processor clocks will be generated. This position is not supported and may cause damage to the processor.

4.8.2 Enable Spread Spectrum Clocking (J14)

This jumper is used to enable or disable spread spectrum clocking on the clock synthesizer. When this jumper is in, a 0.5% down spread will be introduced into the PCI and CPU clocks. The default setting is no jumper installed, which disables spread spectrum clocking.

4.8.3 SMI# Source Control (J23)

This jumper selects the source of the SMI# interrupt to the processor. Only the 2-3 position which selects the PIIX4E is supported. The 1-2 position is reserved for future use.

4.8.4 CMOS RAM Clear (J24)

This jumper controls power to the battery backed-up CMOS RAM. This RAM is used to store information about the system configuration that is required by the BIOS. The 1-2 position is for normal operation. The 2-3 position allows for the RAM to be cleared.

To clear the RAM perform the following steps:

1. Remove power from the evaluation platform by removing jumper J20
2. Move J24 to the 2-3 position for a few seconds.
3. Install J24 in the 1-2 position.
4. Reboot the system and enter the BIOS setup screen to configure the system.

4.8.5 Flash BIOS VPP Select (J21)

This jumper controls the voltage presented to the flash BIOS VPP pin. The 2-3 position supplies 5 V and is the default for normal operation. This position inhibits programming or erasing the flash BIOS.

The 1-2 position supplies 12 V and should only be used if directed to do so by a utility that is used to reprogram the BIOS.

4.8.6 Flash BIOS Boot Block Control (J22)

This jumper controls the Boot Block protection of the Flash BIOS. When this jumper is in the 2-3 position, the boot block is locked and cannot be programmed. This is the default position of this jumper.

The 1-2 position unlocks the boot block so that it can be erased and reprogrammed. This position should only be used under the direction of a utility that is designed to reprogram the boot block of the flash device.

4.8.7 On/Off (J20)

This jumper is used to control the state of the ATX power supply. When this jumper is removed, the power supply will be turned off. Placing the jumper in the 2-3 position will turn the power supply on.

The 1-2 position is reserved and should not be used.

4.8.8 Push Button Switches

There are two push button switches on the evaluation board labeled S1 and S2. S1 is non-functional and reserved for future use. S2 is the reset button. Pressing S2 will force a complete hardware reset of the system.

BIOS Quick Reference 5

The Low-Power Pentium® processor with MMX™ Technology Evaluation Platform is licensed with a single copy of Embedded BIOS and Embedded DOS software from General Software, Inc.[1] This software is provided for demonstration purposes only and must be licensed directly from General Software, Inc. for integration with new designs. General Software may be reached at (800) 850-5755, on the web at http://www.gensw.com, or via email at sales@gensw.com.

5.1 BIOS and Pre-Boot Features

The system's pre-boot environment is managed with an adaptation of Embedded BIOS from General Software. The pre-boot environment includes POST, Setup Screen System, Manufacturing Mode, Console Redirection, Windows CE Loader (CE Ready), and Integrated BIOS Debugger. A REFLASH tool is also available to update the BIOS image with new builds of Embedded BIOS that may be obtained from General Software.

Before using the system, please read the following to properly configure CMOS settings, and learn how to use the embedded features of the pre-boot firmware, Embedded BIOS.

The last two sections of this chapter provide the BIOS POST Codes and Beep codes.

5.2 Power-On Self-Test (POST)

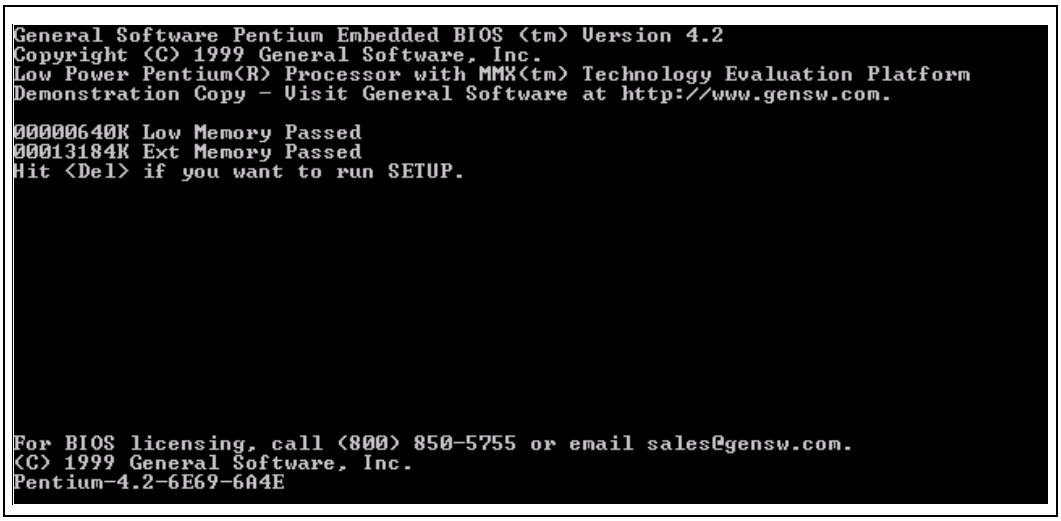
When the system is powered on, Embedded BIOS tests and initializes the hardware and programs the chipset and other peripheral components. During this time, POST progress codes are written by the system BIOS to I/O port 80H, allowing the user to monitor the progress with a special monitor. "Embedded BIOS POST Codes" on page 5-12 lists the POST codes and their meanings.

During early POST, no video is available to display error messages should a critical error be encountered; therefore, POST uses beeps on the speaker to indicate the failure of a critical system component during this time. Consult "Embedded BIOS Beep Codes" on page 5-15 for a list of Beep codes used by the system's BIOS.

POST displays its progress on the system video device, which may be the video screen if a VGA card is used, or on a terminal emulation program's screen if output is redirected over a serial port.

1. General Software™, the GS Logo, Embedded BIOS™, BIOStart™, CE-Ready™, and Embedded DOS™ are trademarks or registered trademarks of General Software, Inc.

Figure 5-1. BIOS POST Pre-Boot Environment



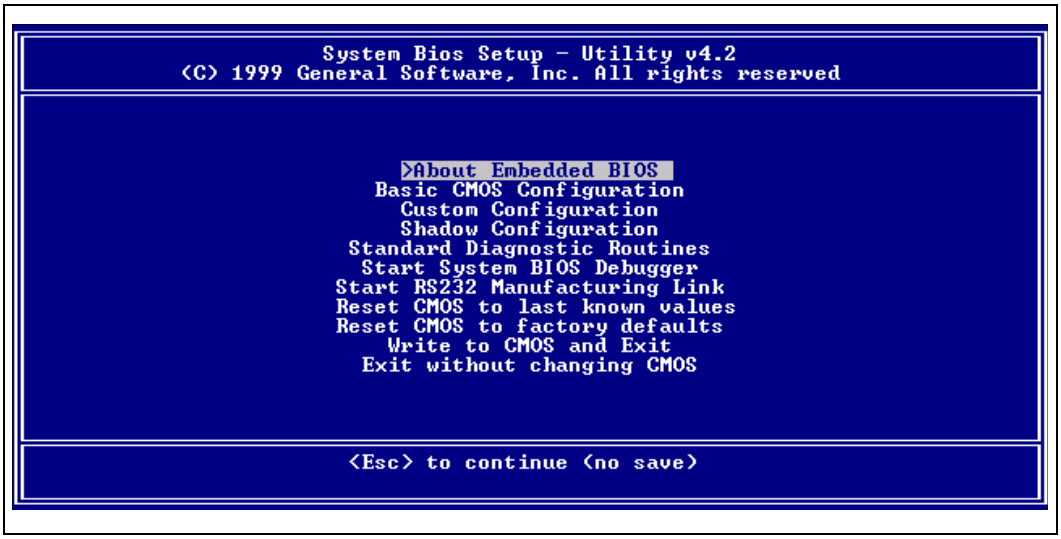
When the system is powered on for the first time, you'll need to configure the system through the Setup Screen System (described later) before peripherals, such as disk drives, are recognized by the BIOS. The information is written to battery-backed CMOS RAM on the board's Real Time Clock. Should the board's battery fail, this information will be lost and the board will need to be reconfigured.

OEMs can modify the look-and-feel of POST with the Embedded BIOS adaptation kit. While the demonstration BIOS looks and feels like a desktop PC, it is possible to eliminate messages, sounds, delays, to make the POST effectively invisible.

5.3 Setup Screen System

The system is configured from within the Setup Screen System, which is a series of menus that can be invoked from POST by pressing the <DEL> key if the main keyboard is being used, or by pressing ^C if the console is being redirected to a terminal program.

Figure 5-2. Embedded BIOS Setup Screen Menu

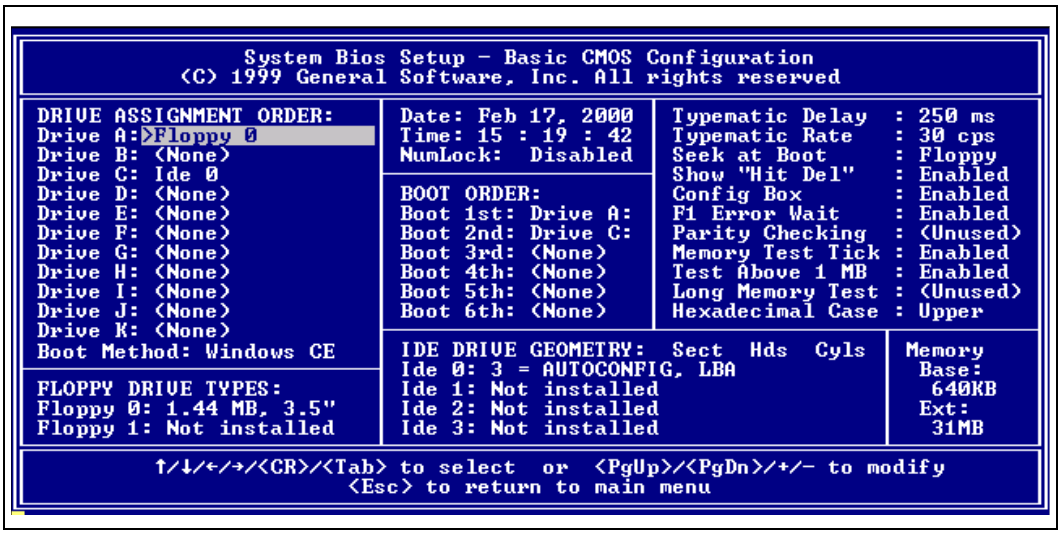


Once in the Setup Screen System (Figure 5-2), the user can navigate with the UP and DOWN arrow keys from the main console, or use the ^E and ^X keys from the remote terminal program to accomplish the same thing. TAB and ENTER are used to advance to the next field, and '+' and '-' keys cycle through values, such as those in the Basic Setup Screen, or the Diagnostics Setup Screen.

5.3.1 Basic CMOS Configuration Screen

The system's drive types, boot activities, and POST optimizations are configured from the Basic Setup Screen (Figure 5-3). In order to use disk drives with your system, you must select appropriate assignments of drive types in the left-hand column. Then, if you are using true floppy and IDE drives (not memory disks that emulate these drives), you need to configure the drive types themselves in the Floppy Drive Types and IDE Drive Geometry sections. Finally, you'll need to configure the boot sequence in the middle of the screen. Once these selections have been made, your system is ready to use.

Figure 5-3. Embedded BIOS Basic Setup Screen



5.3.2 Configuring Drive Assignments

Embedded BIOS allows the user to map a different file system to each drive letter. The BIOS allows file systems for each floppy (Floppy0 and Floppy1), each IDE drive (Ide0, Ide1, Ide2, and Ide3), and memory disks when configured (Flash0, ROM0, RAM0, etc.) Figure 5-3 shows how the first floppy drive (Floppy0) is assigned to drive A: in the system, and then how the first IDE drive (Ide0) is assigned to drive C: in the system.

To switch two floppy disks around or two hard disks around, just map Floppy0 to B: and Floppy1 to A:, and for hard disks map Ide0 to D: and Ide1 to C:.

Caution: Take care to not skip drive A: when making floppy disk assignments, as well as drive C: when making hard disk assignments. The first floppy should be A:, and the first hard drive should be C:. Also, do not assign the same file system to more than one drive letter. Thus, Floppy0 should not be used for both A: and B:. The BIOS permits this to allow embedded devices to alias drives, but desktop operating systems may not be able to maintain cache coherency with such a mapping in place.

A special field in this section entitled “Boot Method: (Windows CE/Boot Sector)” is used to configure the CE Ready feature of the BIOS. For normal booting (DOS, Windows NT, etc.), select “Boot Sector” or “Unused”.

5.3.2.1 Configuring Floppy Drive Types

If true floppy drive file systems (and not their emulators, such as ROM, RAM, or flash disks) are mapped to drive letters, then the floppy drives themselves must be configured in this section. Floppy0 refers to the first floppy disk drive on the drive ribbon cable (normally drive A:), and Floppy1 refers to the second drive (drive B:).

5.3.3 Configuring IDE Drive Types

If true IDE disk file systems (and not their emulators, such as ROM, RAM, or flash disks) are mapped to drive letters, then the IDE drives themselves must be configured in this section. The following table shows the drive assignments for Ide0-Ide3:

Table 5-1. IDE0-IDE3 Drive Assignments

File System Name	Controller	Master/Slave
Ide0	Primary (1f0h)	Master
Ide1	Primary (1f0h)	Slave
Ide2	Secondary (170h)	Master
Ide3	Secondary (170h)	Slave

To use the primary master IDE drive in your system (the typical case), just configure Ide0 in this section, and map Ide0 to drive C: in the Configuring Drive Assignments section.

The IDE Drive Types section lets you select the type for each of the four IDE drives: None, User, Physical, LBA, or CHS.

User This type allows the user to select the maximum cylinders, heads, and sectors per track associated with the IDE drive. This method is now rarely used since LBA is now in common use.

Physical This type instructs the BIOS to query the drive's geometry from the controller on each POST. No translation on the drive's geometry is performed, so this type is limited to drives of 512 Mbytes or less. Commonly, this is used with embedded ATA PC Cards.

LBA This type instructs the BIOS to query the drive's geometry from the controller on each POST, but then translate the geometry according to the industry-standard LBA convention. This supports up to 16-Gbyte drives. *Use this method for all new drives.*

CHS This type instructs the BIOS to query the drive's geometry from the controller on each POST, but then translate the geometry according to the Phoenix CHS convention. Using this type on a drive previously formatted with LBA or Physical geometry might show data as being missing or corrupted.

5.4 Configuring Boot Actions

Embedded BIOS supports up to six different user-defined steps in the boot sequence. When the entire system has been initialized, POST executes these steps in order until an operating system successfully loads. In addition, other pre-boot features can be run before, after, or between operating system load attempts. The following actions can be used:

Drive A: - K: Boot operating system from specified drive. If “Loader” is set to “BootRecord” or “Unused”, then the standard boot record will be invoked, causing DOS, Windows95/98, Windows NT, or other industry-standard operating systems to load. If “Boot Method” is set to “Windows CE”, then the boot drive’s boot record will not be used, and instead the BIOS will attempt to load and execute the Windows CE Kernel file, NK.BIN, from the root directory of each boot device.

Debugger Launch the Integrated BIOS Debugger. To return to the boot process from the debugger environment, type “G” at the debugger prompt and press ENTER.

MFGMODE Initiate Manufacturing Mode, allowing the system to be configured remotely via an RS232 connect to a host computer.

WindowsCE Execute a ROM-resident copy of Windows CE, if available. This feature is not applicable unless properly configured by the OEM in the BIOS adaptation.

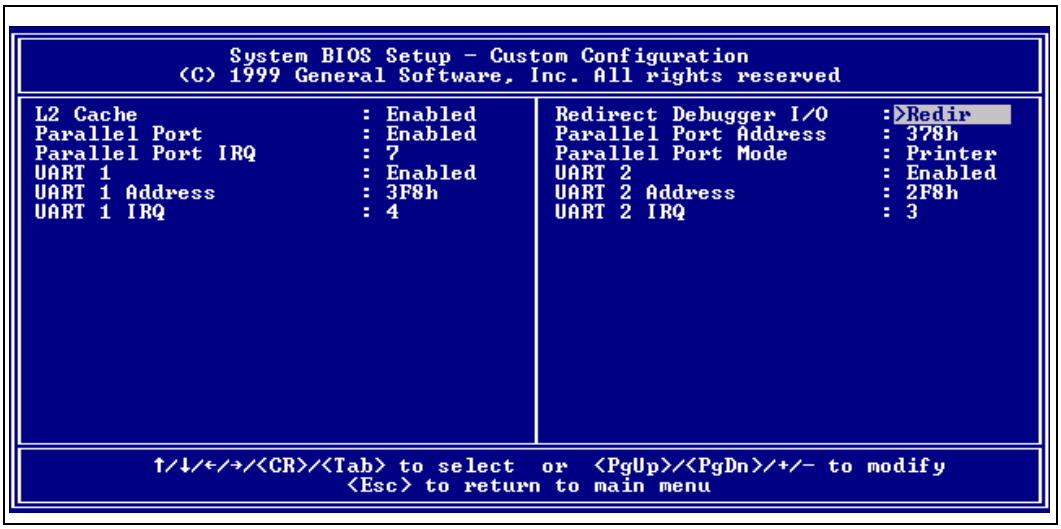
DOS in ROM Execute a ROM-resident copy of DOS, if available. This feature is not applicable unless an XIP copy of DOS, such as Embedded DOS-ROM, has been stored in the BIOS boot ROM. Copies of Embedded DOS-ROM may be obtained from General Software.

None No action; POST proceeds to the next activity in the sequence.

5.5 Custom Configuration Setup Screen

The system’s hardware-specific features are configured with the Custom Setup Screen (Figure 5-4). All features are straightforward except for the Redirect Debugger I/O option, which is an extra embedded feature that allows the user to select whether the Integrated BIOS Debugger should use standard keyboard and video or RS232 console redirection for interaction with the user. If no video is available, the debugger is always redirected.

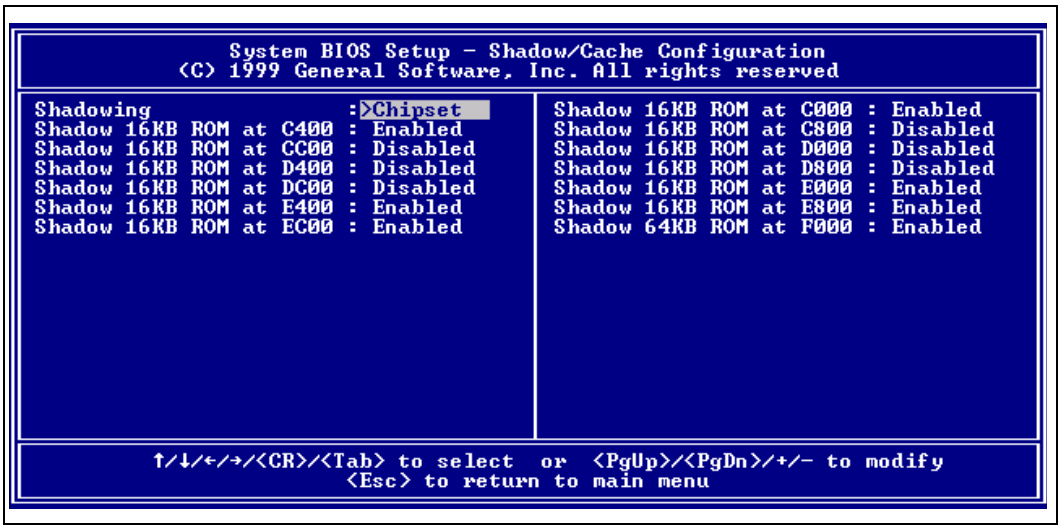
Figure 5-4. Embedded BIOS Custom Setup Screen



5.6 Shadow Configuration Setup Screen

The system's Shadow Configuration Setup Screen (Figure 5-5) allows the selective enabling and disabling of shadowing in 16 Kbyte sections, except for the top 64 Kbytes of the BIOS ROM, which is shadowed as a unit. Normally, shadowing should be enabled at C000/C400 (to enhance VGA ROM BIOS performance), and then E000-F000 should be shadowed to maximize system ROM BIOS performance.

Figure 5-5. Embedded BIOS Shadow Setup Screen



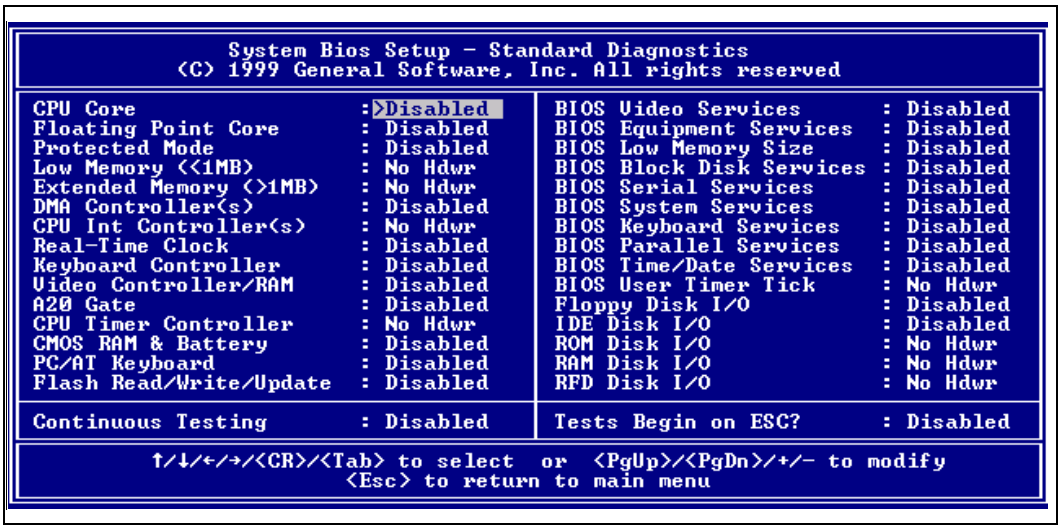
5.7 Standard Diagnostics Routines Setup Screen

Embedded systems may require automated burn-in testing in the development cycle. This facility is provided directly in the system's system BIOS through the Standard Diagnostics Routines Setup Screen (Figure 5-6). To use the system, selectively enable or disable features to be tested, and then enable the "Tests Begin on ESC?" option to cause the system test suite to be invoked. To repeat the system test battery continuously, you should also enable the "Continuous Testing" option. When continuous testing is started, the system will continue until an error is encountered.

Caution: The disk I/O diagnostics perform write operations on those drives; therefore, only spare drives should be used which do not contain data that could be harmed by the test.

Caution: The keyboard test may fail when in fact the hardware is operating within reasonable limits. This is because although the device may produce occasional errors, the BIOS retries operations when failures occur during normal operation of the system.

Figure 5-6. Standard Diagnostic Routines Setup Screen



5.8 Start System BIOS Debugger Setup Screen

The Embedded BIOS Integrated Debugger may be invoked from the Setup Screen main menu, as well as a boot activity. Once invoked, the debugger will display the debugger prompt:

EB42DBG:

and await debugger commands. To resume back to the Setup Screen main menu, type the following command, which instructs the debugger to "go":

EB42DBG: **G** <ENTER>

5.9 Start RS232 Manufacturing Link Setup Screen

The Embedded BIOS Manufacturing Mode may be invoked from the Setup Screen main menu, as well as a boot activity. Once invoked, Manufacturing Mode takes over the system and freezes the console of the system (Figure 5-7). The host can resume operation of the system and give control back to the system Setup Screen system with special control software.

Figure 5-7. Start RS232 Manufacturing Link Setup Screen

5.10 Manufacturing Mode

The system's BIOS provides a special mode, called Manufacturing Mode, that allows the target to be controlled by a host computer such as a laptop or desktop PC. Running special software supplied by General Software, the host can access the target's drives and manage the file systems on the target, reprogram flash memories, and test target hardware.

A full discussion of the uses of Manufacturing Mode is beyond the scope of this chapter. Complete documentation and host-side software is available directly from General Software. For more information, visit the General Software web site at http://www.gensw.com.

5.10.1 Console Redirection

The system can operate either with a standard PC/AT or PS/2 keyboard and VGA video monitor, or with a special emulation of a console over an RS232 cable connected to a host computer running a terminal program. To see an example session with HYPERTERMINAL, see the debugger section's screen display (Figure 5-9).

To use the Console Redirection feature, simply remove the video display card from the system so that no video ROM is available for the BIOS to detect. In the absence of any video support, the BIOS automatically switches its keyboard and screen functions to serial I/O over COM1 on the board. The hardware connection to the host computer requires a null modem cable.

The software on the target can be any terminal emulation program that supports ANSI terminal mode, using 9600 baud, no parity, and one stop bit (Note: This can be modified by the OEM during BIOS adaptation.) The program must be set to not use flow control, or the console may seem to stall or not accept input.

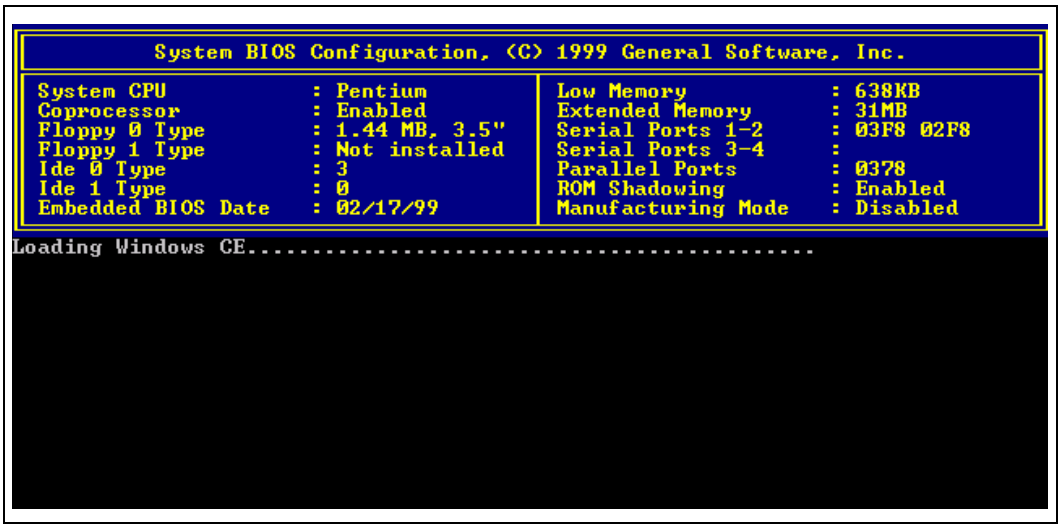
Caution: HYPERTERMINAL's default setting is to use flow control, which will render the console inoperative. To change this, create a new session, change the flow control setting to "none", save the session, and exit HYPERTERMINAL. Then reinvoke HYPERTERMINAL with the session and it will operate with the new flow control setting.

5.10.2 CE-Ready Windows CE Loader

Your system's BIOS is "CE-Ready" and can directly boot Windows CE* without loading an intermediate operating system such as DOS and LOADCEPC. Instead, the NK.BIN file can be placed on a disk drive or drive emulator, and then the BIOS can be configured through the Basic CMOS Configuration Setup Screen to boot the NK.BIN file from the boot drives instead of the boot records on those drives.

To configure your system to boot Windows CE natively from a disk drive, set the "Boot Method" field to "Windows CE" in the Basic CMOS Configuration Setup Screen. Then, place a copy of NK.BIN suitable for execution by LOADCEPC in the root directory of your normal boot drive, such as drive C:. Then, reboot the system. The configuration box should be displayed (Figure 5-8), and immediately following should be the message "Loading Windows CE…" followed by a series of dots, indicating that the loading process is continuing. Once fully loaded, Windows CE takes over the system and runs using the standard PC keyboard, screen, and PS/2 mouse.

Figure 5-8. CE-Ready Boot Feature

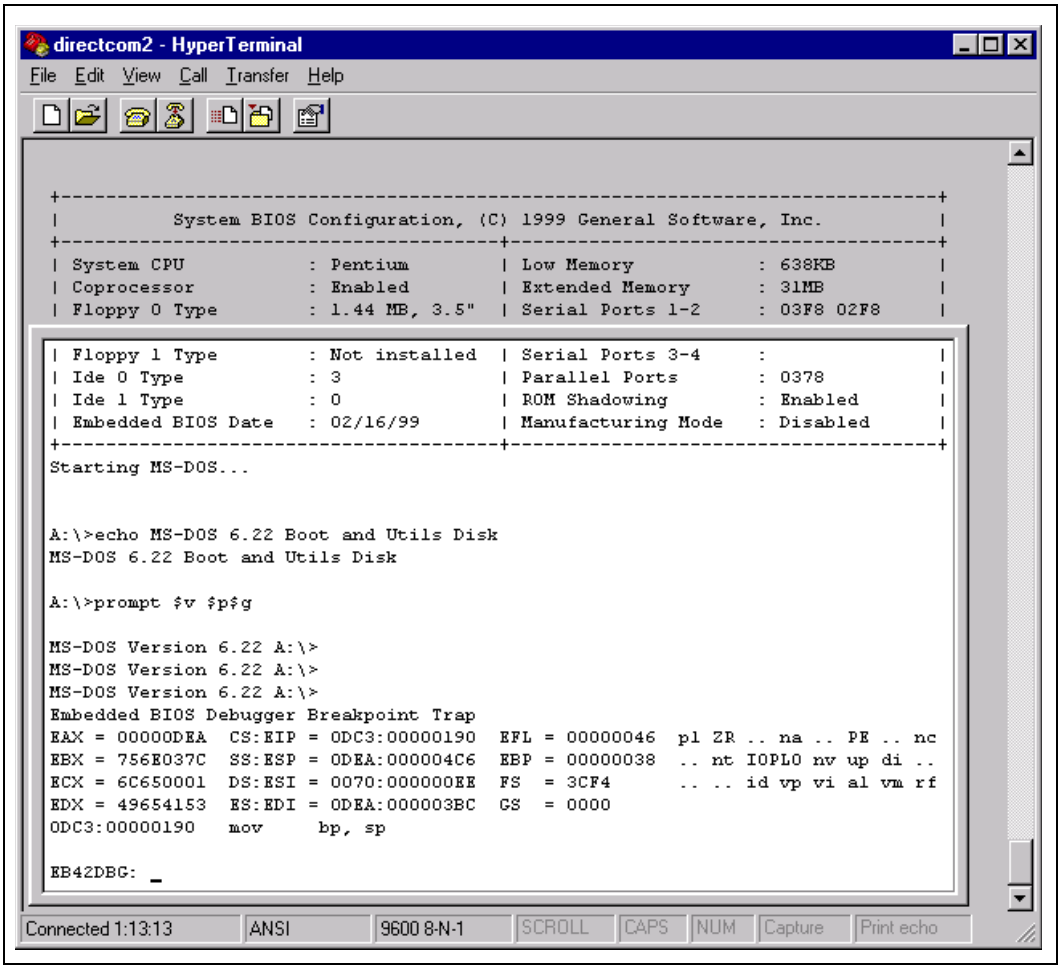


5.10.3 Integrated BIOS Debugger

The system's BIOS contains a built-in debugger that can be a valuable tool to aid the board bring-up process on new designs similar to the evaluation platform. It supports a DOS SYMDEB-style command line interface, and can be used on the main console's keyboard and screen, or over a redirected connection to a terminal program (see "Console Redirection" on page 5-9).

To activate the debugger at any time from the main console, press the left shift and the control keys together. A display similar to the one in the HYPERTERMINAL session below (Figure 5-9) will appear, containing the title, “Embedded BIOS Debugger Breakpoint Trap” and a snapshot of the processor general registers.

Figure 5-9. Integrated BIOS Debugger Running Over a Remote Terminal



To leave the debugger and resume the interrupted activity (whether POST, BIOS, DOS, Windows, or an application program), enter the “G” command (short for “go”) and press ENTER. If you were at a DOS prompt when you entered the debugger, then DOS will still be waiting for its command, and will not prompt again until you press ENTER again.

The debugger can also be entered from the Setup Screen System, and as a boot activity (see “Basic CMOS Configuration Screen” on page 5-3), as a last ditch effort during board bring-up and development if no bootable device is available.

If your version of DOS, an application, or any OEM-supplied BIOS extensions have debugging code (i.e., “INT 3” instructions) remaining, then these will invoke the debugger automatically, although this is not an error. To continue, use the “G” command. When Embedded BIOS is adapted by the OEM, the debugger can be removed from the final production BIOS, and superfluous debugging code in the application will not cause the debugger to be invoked.

A complete discussion of the debugger is beyond the scope of this chapter; however, complete documentation is available from General Software via the web at http://www.gensw.com.

5.11 Embedded BIOS POST Codes

Embedded BIOS writes progress codes, also known as POST codes, to I/O port 80H during POST, in order to provide information to OEM developers about system faults. These POST codes may be monitored on the on-board Post Code Debugger located at U12 and U13. They are not displayed on the screen. For more information about POST codes, contact General Software.

Mnemonic Code	Code	System Progress Report
POST_STATUS_START	00h	Start POST (BIOS is executing).
POST_STATUS_CPUTEST	01h	Start CPU register test.
POST_STATUS_DELAY	02h	Start power-on delay.
POST_STATUS_DELAYDONE	03h	Power-on delay finished.
POST_STATUS_KBDBATRDY	04h	Keyboard BAT finished.
POST_STATUS_DISABSHADOW	05h	Disable shadowing & cache.
POST_STATUS_CALCCKSUM	06h	Compute ROM CRC, wait for KBC.
POST_STATUS_CKSUMGOOD	07h	CRC okay, KBC ready.
POST_STATUS_BATVRFY	08h	Verifying BAT command to KB.
POST_STATUS_KBDCMD	09h	Start KBC command.
POST_STATUS_KBDDATA	0ah	Start KBC data.
POST_STATUS_BLKUNBLK	0bh	Start pin 23,24 blocking & unblocking.
POST_STATUS_KBDNOP	0ch	Start KBC NOP command.
POST_STATUS_SHUTTEST	0dh	Test CMOS RAM shutdown register.
POST_STATUS_CMOSDIAG	0eh	Check CMOS checksum.
POST_STATUS_CMOSINIT	0fh	Initialize CMOS contents.
POST_STATUS_CMOSSTATUS	10h	Initialize CMOS status for date/time.
POST_STATUS_DISABDMAINT	11h	Disable DMA, PICs.
POST_STATUS_DISABPORTB	12h	Disable Port B, video display.
POST_STATUS_BOARD	13h	Initialize board, start memory bank detection.
POST_STATUS_TESTTIMER	14h	Start timer tests.
POST_STATUS_TESTTIMER2	15h	Test 8254 T2, for speaker, port B.
POST_STATUS_TESTTIMER1	16h	Test 8254 T1, for refresh.
POST_STATUS_TESTTIMER0	17h	Test 8254 T0, for 18.2Hz.
POST_STATUS_MEMREFRESH	18h	Start memory refresh.
POST_STATUS_TESTREFRESH	19h	Test memory refresh.
POST_STATUS_TEST15US	1ah	Test 15usec refresh ON/OFF time.
POST_STATUS_TEST64KB	1bh	Test base 64KB memory.
POST_STATUS_TESTDATA	1ch	Test data lines.
POST_STATUS_TESTADDR	20h	Test address lines.
POST_STATUS_TESTPARITY	21h	Test parity (toggling).
POST_STATUS_TESTMEMRDWR	22h	Test Base 64KB memory.
POST_STATUS_SYSINIT	23h	Prepare system for IVT initialization.
POST_STATUS_INITVECTORS	24h	Initialize vector table.
POST_STATUS_8042TURBO	25h	Read 8042 for turbo switch setting.
POST_STATUS_POSTTURBO	26h	Initialize turbo data.
POST_STATUS_POSTVECTORS	27h	Modification of IVT.
POST_STATUS_MONOMODE	28h	Video in monochrome mode verified.
POST_STATUS_COLORMODE	29h	Video in color mode verified.
POST_STATUS_TOGGLEPARITY	2ah	Toggle parity before video ROM test.
POST_STATUS_INITBEFOREVIDEO	2bh	Initialize before video ROM check.

POST_STATUS_VIDEOROM	2ch	Passing control to video ROM.
POST_STATUS_POSTVIDEO	2dh	Control returned from video ROM.
POST_STATUS_CHECKEGAVGA	2eh	Check for EGA/VGA adapter.
POST_STATUS_TESTVIDEOMEMORY	2fh	No EGA/VGA found, test video memory.
POST_STATUS_RETRACE	30h	Scan for video retrace signal.
POST_STATUS_ALTDISPLAY	31h	Primary retrace failed.
POST_STATUS_ALTRETRACE	32h	Alternate found.
POST_STATUS_VRFYSWADAPTER	33h	Verify video switches.
POST_STATUS_SETDISPMODE	34h	Establish display mode.
POST_STATUS_CHECKSEG40A	35h	Initialize ROM BIOS data area.
POST_STATUS_SETCURSOR	36h	Set cursor for power-on msg.
POST_STATUS_PWRONDISPLAY	37h	Display power-on message.
POST_STATUS_SAVECURSOR	38h	Save cursor position.
POST_STATUS_BIOSIDENT	39h	Display BIOS identification string.
POST_STATUS_HITDEL	3ah	Display "Hit <DEL> to ..." message.
POST_STATUS_VIRTUAL	40h	Prepare protected mode test.
POST_STATUS_DESCR	41h	Prepare descriptor tables.
POST_STATUS_ENTERVM	42h	Enter virtual mode for memory test.
POST_STATUS_ENABINT	43h	Enable interrupts for diagnostics mode.
POST_STATUS_CHECKWRAP1	44h	Initialize data for memory wrap test.
POST_STATUS_CHECKWRAP2	45h	Test for wrap, find total memory size.
POST_STATUS_HIGHPATTERNS	46h	Write extended memory test patterns.
POST_STATUS_LOWPATTERNS	47h	Write conventional memory test patterns.
POST_STATUS_FINDLOWMEM	48h	Find low memory size from patterns.
POST_STATUS_FINDHIMEM	49h	Find high memory size from patterns.
POST_STATUS_CHECKSEG40B	4ah	Verify ROM BIOS data area again.
POST_STATUS_CHECKDEL	4bh	Check for <DEL> pressed.
POST_STATUS_CLREXTMEM	4ch	Clear extended memory for soft reset.
POST_STATUS_SAVEMEMSIZE	4dh	Save memory size.
POST_STATUS_COLD64TEST	4eh	Cold boot: Display 1st 64KB memtest.
POST_STATUS_COLDLOWTEST	4fh	Cold boot: Test all of low memory.
POST_STATUS_ADJUSTLOW	50h	Adjust memory size for EBDA usage.
POST_STATUS_COLDHITEST	51h	Cold boot: Test high memory.
POST_STATUS_REALMODETEST	52h	Prepare for shutdown to real mode.
POST_STATUS_ENTERREAL	53h	Return to real mode.
POST_STATUS_SHUTDOWN	54h	Shutdown successful.
POST_STATUS_DISABA20	55h	Disable A20 line.
POST_STATUS_CHECKSEG40C	56h	Check ROM BIOS data area again.
POST_STATUS_CHECKSEG40D	57h	Check ROM BIOS data area again.
POST_STATUS_CLRHITDEL	58h	Clear "Hit <DEL>" message.
POST_STATUS_TESTDMAPAGE	59h	Test DMA page register file.
POST_STATUS_VRFYDISPMEM	60h	Verify from display memory.
POST_STATUS_TESTDMA0BASE	61h	Test DMA0 base register.
POST_STATUS_TESTDMA1BASE	62h	Test DMA1 base register.
POST_STATUS_CHECKSEG40E	63h	Checking ROM BIOS data area again.
POST_STATUS_CHECKSEG40F	64h	Checking ROM BIOS data area again.
POST_STATUS_PROGDMA	65h	Program DMA controllers.
POST_STATUS_INITINTCTRL	66h	Initialize PICs.
POST_STATUS_STARTKBDTEST	67h	Start keyboard test.
POST_STATUS_KBDRESET	80h	Issue KB reset command.
POST_STATUS_CHECKSTUCKKEYS	81h	Check for stuck keys.
POST_STATUS_INITCIRCBUFFER	82h	Initialize circular buffer.
POST_STATUS_CHECKLOCKEDKEYS	83h	Check for locked keys.
POST_STATUS_MEMSIZEMISMATCH	84h	Check for memory size mismatch.
POST_STATUS_PASSWORD	85h	Check for password or bypass setup.

```
POST_STATUS_BEFORESETUP      86h   Password accepted.
POST_STATUS_CALLSETUP        87h   Entering setup system.
POST_STATUS_POSTSETUP        88h   Setup system exited.
POST_STATUS_DISPPWRON        89h   Display power-on screen message.
POST_STATUS_DISPWAIT         8ah   Display "Wait..." message.
POST_STATUS_ENABSHADOW       8bh   Shadow system & video BIOS.
POST_STATUS_STDCMOSSETUP     8ch   Load standard setup values from CMOS.
POST_STATUS_MOUSE            8dh   Test and initialize mouse.
POST_STATUS_FLOPPY           8eh   Test floppy disks.
POST_STATUS_CONFIGFLOPPY     8fh   Configure floppy drives.
POST_STATUS_IDE              90h   Test hard disks.
POST_STATUS_CONFIGIDE        91h   Configure IDE drives.
POST_STATUS_CHECKSEG40G      92h   Checking ROM BIOS data area.
POST_STATUS_CHECKSEG40H      93h   Checking ROM BIOS data area.
POST_STATUS_SETMEMSIZE       94h   Set base & extended memory sizes.
POST_STATUS_SIZEADJUST       95h   Adjust low memory size for EBDA.
POST_STATUS_INITC8000        96h   Initialize before calling C800h ROM.
POST_STATUS_CALLC8000        97h   Call ROM BIOS extension at C800h.
POST_STATUS_POSTC8000        98h   ROM C800h extension returned.
POST_STATUS_TIMERPRNBASE     99h   Configure timer/printer data.
POST_STATUS_SERIALBASE       9ah   Configure serial port base addresses.
POST_STATUS_INITBEFORENPX    9bh   Prepare to initialize coprocessor.
POST_STATUS_INITNPX          9ch   Initialize numeric coprocessor.
POST_STATUS_POSTNPX          9dh   Numeric coprocessor initialized.
POST_STATUS_CHECKLOCKS       9eh   Check KB settings.
POST_STATUS_ISSUEKBDID       9fh   Issue keyboard ID command.
POST_STATUS_RESETID          0a0h  KB ID flag reset.
POST_STATUS_TESTCACHE        0a1h  Test cache memory.
POST_STATUS_DISPSOFTERR      0a2h  Display soft errors.
POST_STATUS_TYPEMATIC        0a3h  Set keyboard typematic rate.
POST_STATUS_MEMWAIT          0a4h  Program memory wait states.
POST_STATUS_CLRSCR           0a5h  Clear screen.
POST_STATUS_ENABPTYNMI       0a6h  Enable parity and NMIs.
POST_STATUS_INITE000         0a7h  Initialize before calling ROM at E000h.
POST_STATUS_CALLE000         0a8h  Call ROM BIOS extension at E000h.
POST_STATUS_POSTE000         0a9h  ROM extension returned.
POST_STATUS_DISPCONFIG       0b0h  Display system configuration box.
POST_STATUS_INT19BOOT        00h   Call INT 19h bootstrap loader.
POST_STATUS_LOWMEMEXH        0b1h  Test low memory exhaustively.
POST_STATUS_EXTMEMEXH        0b2h  Test extended memory exhaustively.
POST_STATUS_PCIENUM          0b3h  Enumerate PCI busses.
```

5.12 Embedded BIOS Beep Codes

Embedded BIOS tests much of the system hardware early in POST before messages can be displayed on the screen. When system failures are encountered at these early stages, POST uses beep codes (a sequence of tones on the speaker) to identify the source of the error.

The following is a comprehensive list of POST beep codes for the system BIOS. BIOS extensions, such as VGA ROMs and SCSI adapter ROMs, may use their own beep codes, including short/long sequences, or possibly beep codes that sound like the ones below. When diagnosing a system failure, remove these adapters if possible before making a final determination of the actual POST test that failed.

Mnemonic Code	Beep Count	Description of Problem
POST_BEEP_REFRESH	1	Memory refresh is not working.
POST_BEEP_PARITY	2	Parity error found in 1st 64KB of memory.
POST_BEEP_BASE64KB	3	Memory test of 1st 64KB failed.
POST_BEEP_TIMER	4	T1 timer test failed.
POST_BEEP_CPU	5	CPU test failed.
POST_BEEP_GATEA20	6	Gate A20 test failed.
POST_BEEP_DMA	7	DMA page/base register test failed.
POST_BEEP_VIDEO	8	Video controller test failed.
POST_BEEP_KEYBOARD	9	Keyboard test failed.
POST_BEEP_SHUTDOWN	10	CMOS shutdown register test failed.
POST_BEEP_CACHE	11	External cache test failed.
POST_BEEP_BOARD	12	General board initialization failed.
POST_BEEP_LOWMEM	13	Exhaustive low memory test failed.
POST_BEEP_EXTMEM	14	Exhaustive extended memory test failed.
POST_BEEP_CMOS	15	CMOS restart byte test failed.
POST_BEEP_ADDRESS_LINE	16	Address line test failed.
POST_BEEP_DATA_LINE	17	Data line test failed.
POST_BEEP_INTERRUPT	18	Interrupt controller test failed.
POST_BEEP_PASSWORD	1	Incorrect password used to access SETUP.

PLD Code Listing A

The code listing below is for the 22V10 PLD.

```
TITLE       22V10 PORT 80 ADDRESS DECODER / FLASH DECODE
PATTERN     1
REVISION    B
AUTHOR      CHRIS BANYAI
COMPANY     INTEL CORPORATION
DATE        10/1/97

OPTIONS
    SECURITY = OFF


;  ( part was 22V10FN before conversion )
CHIP  P80B iPLD22V10N

PIN         19    IOWR_BAR
PIN          3    AEN
PIN      [6:7]    SA[0:1]
PIN     [9:13]    SA[2:6]
PIN         16    SA7
PIN      [5:4]    SA[8:9]
PIN    [26:23]    SA[19:16]
PIN    [21:20]    SA[15:14]
PIN          2    SEL

PIN         18   /CS_BAR
PIN         17   /CS_DOC
PIN         27    OX

EQUATIONS
CS_BAR = /IOWR_BAR * /AEN * /SA0 * /SA1 * /SA2 * /SA3 * /SA4 * /SA5 * /SA6
              * SA7 * /SA8 * /SA9
CS_BAR.TRST = VCC

CS_DOC = /SEL * /AEN * SA19 * SA18 * /SA17 * /SA16 * SA15 * /SA14
       + SEL * /AEN * SA19 * SA18 * /SA17 * SA16 * /SA15 * /SA14
CS_DOC.TRST = VCC

OX = /IOWR_BAR
OX.TRST = VCC

SIMULATION

    SETF /AEN /SA0 /SA1 /SA2 /SA3 /SA4 /SA5 /SA6 /SA7 /SA8 /SA9 IOWR_BAR
    SETF SA7 IOWR_BAR
    SETF /IOWR_BAR
    SETF IOWR_BAR
```

```
SETF AEN /IOWR_BAR
SETF /AEN
SETF IOWR_BAR
SETF SA0 /IOWR_BAR
SETF /SA0 /IOWR_BAR
SETF IOWR_BAR
SETF /SA0 /SA1 /SA2 /SA3 /SA4 /SA5 /SA6 /SA7 /SA8 /SA9
SETF /SA19 /SA18 /SA17 /SA16 /SA15 /SA14
SETF /SEL
SETF SA19 SA18 /SA17 /SA16 SA15 /SA14
SETF /SEL
SETF /AEN
SETF /SA19
SETF SA19
SETF /SA18
SETF SA18
SETF SA17
SETF /SA17
SETF SA16
SETF /SA16
SETF /SA15
SETF SA15
SETF SA14
SETF /SA14
SETF /SEL
SETF SA19 SA18 /SA17 SA16 /SA15 /SA14
SETF /SEL
SETF /AEN
SETF SEL
SETF /SA19
SETF SA19
SETF /SA18
SETF SA18
SETF SA17
SETF /SA17
SETF /SA16
SETF SA16
SETF SA15
SETF /SA15
SETF SA14
SETF /SA14
SETF /SEL
```

Bill of Materials B

Table B-1 is the bill of materials for the baseboard. Table B-2 is the bill of materials for the processor assembly.

Table B-1. Baseboard Bill of Materials (Sheet 1 of 4)

Qty	Reference	Description	Manufacturer	Manufacturer P/N
240	J14,J15	Conn,Jumper2,1X2 25-mil sq/100-mil space,HDR2	3M	929647-09-02
570	J20-24	Conn,Jumper3,1X3 25-mil sq/100-mil space,HDR3	3M	929647-09-03
130	JP2	Conn,Speaker,1X4 25-mil sq/100-mil space,HDR4	3M	929647-09-04
130	J10	Conn,FLASH,2X70 C19 Recept	AMP	1-316077-0
130	J12	Conn,Fan	AMP	173981-3
130	J25	Conn,2x70 Plug /Flash Daughtercard	AMP	6-353185-1
130	XU9	PLCC, Socket 28	AMP	822271-1
130	J19	Conn,CPU,400 Pin Array (BGA),BGA40X10-400R	Berg	74219-002
130	U6	IC,Clock Generator,CK100,SSOP300-48(PIN)	Cypress	CY2280PVC-11S
130	U26	IC,Clock Buffer,Zero Delay 3.3V,16PIN,150MIL,TSSOP,PSSOP 16	Cypress	CY2309ZC-1H
130	U16	IC,Clock Buffer,18 Output low skew,SSOP300-48(PIN)	Cypress	CY2318ANZPVC-1
130	Y2	Crystal,32.768KHz,XTAL/MC-405	Epson	MC-405
240	J17,J18	Conn,SDRAM DIMM,168 Pin Recept	FOXCONN	AT08403-K8
130	J4	Conn, Serial Stack,DB9MX2	FOXCONN	DM10156-73
130	J3	Conn, DB25,DB25FM1	FOXCONN	DT11323-R5T
350	J7,J8,J9	Conn,PCI Edge Recept,145154-120	FOXCONN	EH06001-PC-W
240	J5,J6	Conn,ISA Edge Recept.,isa-98	FOXCONN	EQ04901-S6
130	JP1	Conn,Floppy,17X2 Header	FOXCONN	HL07173-P4
240	JP3,JP4	Conn, IDE,20X2 Header	FOXCONN	HL07206-D2
130	J11	Conn,Power,5566DP-20/ATX	FOXCONN	HM20100-P2
130	J1	Conn,PS2 Keyboard / Mouse Connector	FOXCONN	MH11067-D2
130	J13	Conn,AGP Edge Recept., 120 pins,AGP-124	FOXCONN	PC1243K-10
130	J2	2 USB Stack Connectors	FOXCONN	UB1112C-D3

Table B-1. Baseboard Bill of Materials (Sheet 2 of 4)

130	U11	BIOS FLASH Memory,TSOP12X20/40S	INTEL	28F002BC
130	U8	VLSI,PIIX4,PCI to IDE &ISA Bridge,324 mBGA,BGA20x20-324	Intel	FW82371EB
460	U17-20	MEMORY,FLASH, StrataFlash,BGA8x9-56	Intel	G28F640J5-150
130	U14	IC,Interrupt Controller, 82093AA,QFP16x22-64	INTEL	S82093AA
680	C99,C100,C132,C133,C209,C214	Chip Capacitor,10pF, 50V,CC0603	Kemet	C0603C100J5GAC
9260	C: 22,42-43,48-49,54,59-65,70-71,73,75-76,85-87,90-92,96-97, 102,106-108,111-112,114,116-118, 126-127,129-131, 136,137,139-140, 142-144,146-147, 151,157,159-162, 174-176,181-183, 187-200,205-206,208,218-219,226-229	Chip Capacitor,0.1uF, 16V,CC0603	Kemet	C0603C104K4RAC
2550	C27-C41,C44-C47,C50-C53	Chip Capacitor,470pF, 50V,CC0603	Kemet	C0603C471K5RAC
1670	C3-5,C8,C55-57, C94,C119-121, C134,C138,C145, C153	Cap,Tant,10uF,15V,C Case,6032	Kemet	T491C106K016AS
1120	C93,C103-105, C128,C135,C152, C154-156	Cap,Tant,47uF, 20V,D Case,7343	Kemet	T491D476M020AS
1010	C2,C6,C58,C72, C84,C88,C89,C95, C109	Cap,Tant,100uF, 10V,D Case,7343	Kemet	T495D107M010AS
5630	C1,C7,C23,C66-C68,C74,C77-C82, C101,C113,C115, C141,C158,C163-173,C177-180, C184-186,C201-202,C204,C207, C211-213,C216-217,C220-C225	Chip Capacitor,0.01uF 50V,CC0603	Kemet	C0603C103J5RAC
130	U9	IC,PLD,PLCC28,Socket28	LATTICE	GAL22V10B-7LJ
130	U23	IC,Linear Voltage Regulator,SOT-223	Linear Tech.	LT1117-3.3cst
130	U5	IC,Linear Voltage Regulator,SOT-223	Linear Tech.	LT1117CST
130	XU11	40TSOP BIOS Socket,TSOP12X20/40S	Meritec	980020-40-01
240	XU12,XU13	TIL311 SOCKET,DIP14	MILLMAX	110-99-314-41-001
130	U25	IC,Logic,74ACT05,SO14	Motorola	MC74ACT05DR
1010	FB1-FB9	Ferrite Bead,SM1806,Z-Bead	Murata	BLM41A800S
130	U22	IC,Logic,74ALS00,SOIC14	National	DM74ALS00M
130	U7	IC,Tranciever,8-Bit Bidirectional Buffer,SOIC20,SO20W	National	DM74ALS245AWM
460	C69,C83,C98,C110	Cap,Electrolitic,220uF, 25v,6.3mmx11.2mm,PCAPR200-300	Panasonic	ECE-A1EU221
2550	R33,R35,R37,R48,R52,R98-R100, R106,R108-R116,R118-R122	Chip Resistor,0 Ohm Shunt,5%,CR0805	Panasonic	ERJ6GEY0R00V

Table B-1. Baseboard Bill of Materials (Sheet 3 of 4)

1230	R6,R25,R42,R45,R49,R60-R63,R101,R102	Chip Resistor,1K,5%,CR0805	Panasonic	ERJ6GEYJ102V
2000	R2,R4,R5,R11,R40,R41,R43,R53-R56,R59,R97,R105,R117,R123-124,R127	Chip Resistor,10K,5%,CR0805	Panasonic	ERJ6GEYJ103V
680	R1,R3,R88,R89.R90,R91	Chip Resistor,15K,5%,CR0805	Panasonic	ERJ6GEYJ153V
130	R9	Chip Resistor,22,5%,CR0805	Panasonic	ERJ6GEYJ220V
790	R10,R12,R13,R14,R39,R58,R70	Chip Resistor,220,5%,CR0805	Panasonic	ERJ6GEYJ221V
460	R92-R95	Chip Resistor,27,5%,CR0805	Panasonic	ERJ6GEYJ270V
460	R20,R44,R57,R71	Chip Resistor,2.7K,5%,CR0805	Panasonic	ERJ6GEYJ272V
1890	R17-R19,R21-R24,R26-R32,R34,R36,R38	Chip Resistor,33,5%,CR0805	Panasonic	ERJ6GEYJ330V
240	R103,R104	Chip Resistor,470,5%,CR0805	Panasonic	ERJ6GEYJ471V
1120	R7,R64-R69, R125,R126,R128	Chip Resistor,4.7k,5%,CR0805	Panasonic	ERJ6GEYJ472V
2000	R72-R87,R96,R107	Chip Resistor,8.2K,5%,CR0805	Panasonic	ERJ6GEYJ822V
240	S1,S2	Switch-Push Button,PBSW/ PNASNC2	Panasonic	EVQ-PHP03T
1670	RP2,RP3,RP41-RP47,RP54-RP56, RP58,RP60,RP61	Res,Array,SMT,33,5%,EXB-V	Panasonic	EXB33V330JV
350	RP10,RP18,RP23	Res,Array,SMT,1K,5%,EXB-V	Panasonic	EXB38V102JV
2990	RP8-9,RP11,RP13-17,RP19-RP22, RP24,RP26-33, RP35-36, RP39, RP51-52,RP59	Res,Array,SMT,10K,5%,EXB-V	Panasonic	EXB38V103JV
350	RP1,RP4,RP48	Res,Array,SMT,22,5%,EXB-V	Panasonic	EXB38V220JV
790	RP25,RP37,RP38,RP40,RP49, RP50,RP53	Res,Array,SMT,2.7K,5%,EXB-V	Panasonic	EXB38V272JV
130	RP57	Res,Array,SMT,47,5%,EXB-V	Panasonic	EXB38V470JV
350	RP5,RP6,RP7	Res,Array,SMT,4.7K,5%,EXB-V	Panasonic	EXB38V472JV
240	RP12,RP34	Res,Array,SMT,5.6k,5%,EXB-V	Panasonic	
130	U24	IC,Logic,Inverter, Schmitt Trigger,SOIC14	Philips	74HCT14D
130	U10	IC,Logic,10 Bit Bus Switch,QSOP,SO24W	Quality Semi	QS3384SO
130	Y1	Crystal,14.318MHz,XTAL,FOX-HC495D	Raltron	AS-14.31818-20
350	F1-F3	Fuse,Drawing,SM250	RayChem	SMD250-2
130	XBT1	Battery Holder Socket	Renata	HU-2032-1
130	BT1	Battery	Reneta	CR2032
350	D1,D2,D5	Diode,LED,SOT23-A	Siemens	LGS260-DO
130	U1	VLSI,Super I/O,QFP128	SMSC	FDC37B78X
460	C122-C125	Chip Capacitor,47pF,CC0603	TDK	C1608C0G1H470JT$
1780	C9-C21,C24-C26	Chip Capacitor,220pF,CC0603	TDK	C1608X7R1H221KT009A

Table B-1. Baseboard Bill of Materials (Sheet 4 of 4)

130	U15	IC,Logic,3 state buffer,SOP-14	TI	74LVC125A
130	U21	IC,Logic,SOP-14	TI	74LVC14A
240	U3,U4	IC,RS232 Transceiver, SOIC20,SO20W	TI	GD75232DW
130	U27	IC,Logic,PCI to CardBus Controller,SQFP20x20-144	TI	PCI1210PGE
130	U2	IC,Logic,Open Drain Buffer,SOP-14	TI	SN7407D
240	U12,U13	7 Segment LED display,DIP14	TI	TIL311
460	D3-D4,D6-D7	Schottky Diode,SOT23-E	ZETEX	BAT54
570	R8,R15,R16,R46,R47	Chip Resistor,124,1%,CR0805		
105		SDRAM DIMMS		

Table B-2. Processor Assembly Bill of Materials (Sheet 1 of 2)

Qty	Reference	Description	Manufacturer	Manufacturer P/N
130	J1	ITP	AMP	104068-1
570	C13,C21,C81-83	100uF	AVX	TPSD107M010R0065
240	C35,C107	150uF 10V 20%	AVX	TPSD157M010R0100
790	C12,C36-37,C48,C50,C108-109	220uF	AVX	TPSD227M006R0100
130	U8	BGA,40x10-400	Berg	74221-001
240	D3-4	CMDSH-3	Central Semi	CMDSH-3
130	R26	0.02	Dale Elect	WSL-2010R020F
130	R10	0.075	Dale Elect	WSL-2010R075F
570	R7,R37-39,R41	22	Digikey	Y4220CT-ND
350	R34,R36,R42	4.7K	Digikey	Y4472CT-ND
130	R9	8.2K	Digikey	Y4822CT-ND
240	U3,U7	PBSRAM,64Kx32,QFP14x21-100	Etron	EM542323TQ-11
130	U2	SOJ28/300	IDT	71V256SB15Y
130	U4	BGA 20x20-324	Intel	82439TX
130	U5	BGA 26X26-352W/HS	Intel	GC80503CSM66266 SL389
2770	C8,C16,C22,C62,C67-68,C70,C77-C78,C80,C85-86,C90,C93-97,C99,C101-106	0.01uF,5%,50V	Kemet	C0603C103J5RAC
5630	C3-5,C7,C9-11,C14-15,C18,C23-27,C29,C32,C40,C45-46,C51-61,C63-66,C69,C71-76,C79,C84,C87-89,C91-92,C98,C100	0.1uF 16V 10%	Kemet	C0603C104K4RAC
570	C30-31,C39,C42,C44	1000pF 50V 10%	Kemet	C0805C102J5RAC
130	C17	1uF 20% 10V	Kemet	T491A105M010AS
0	C38	10uF,10%,16v	Kemet	T491C106K016AS

Table B-2. Processor Assembly Bill of Materials (Sheet 2 of 2)

460	C1,C2,C16,C19	22uF 20% 16V	Kemet	T491C226M016AS
130	C20	33uF 20% 16V	Kemet	T491D336M016AS
130	u1	SSOP28	Linear Tech.	LTC1438CG-ADJ
240	D2,D5	MBRS140T3	Motorola	MBRS140T3
130	R23	30K 0.1%	Panasonic	ERA-6YEBxxx
130	R12	39K 0.1%	Panasonic	ERA-6YEBxxx
350	R11,R20,R24	43K 0.1%	Panasonic	ERA-6YEBxxx
130	R19	47K 0.1%	Panasonic	ERA-6YEBxxx
350	R2-3,R17,R45	0 1/10W	Panasonic	ERJ6GEY0R00V
570	R13-15,R21-22	10 1/10W 5%	Panasonic	ERJ6GEYJ100V
460	R1,R4,R8,R43	1K,1/10W,5%	Panasonic	ERJ6GEYJ102V
350	R18,R25,R35	10K 1/10W 5%	Panasonic	ERJ6GEYJ103V
130	R33	2K 1/10W 5%	Panasonic	ERJ6GEYJ202V
130	R5	22K 1/10W 5%	Panasonic	ERJ6GEYJ223V
240	R27-R28	270 1/10W 5%	Panasonic	ERJ6GEYJ271V
240	R16,R30	3.3K 1/10W 5%	Panasonic	ERJ6GEYJ332V
240	R6,R40,R44	4.7K,1/10W,5%	Panasonic	ERJ6GEYJ472V
130	D1	BAT54C	Philips	BAT54C
130	L1	33uH/1.68A	Sumida	CDH115
130	L2	15uH/4.50A	Sumida	CDRH127
350	C33,C47,C49	220pF 50V 10%	TDK	C1608X7R1H221KT009A
350	C28,C41,C43	100pF 50V 5%	TDK Corp	C2012COG1H101JT009A
130	U1	SN74LVC04A-DB	TI	SN74LVC04A-DB
440	X3-6	MNT_HOLE,MTG125/300V		PCB FEATURE
3960	TP1-36	Test Point,TSTPAD/030		PCB FEATURE
240	Q1-2	SO8		Si4412DY
240	Q3-Q4	S08		Si9426DY
130	C34	68pF 5% 16V		

Note: The following devices are not to be populated: R6,R29,R31,R32,R2, C38

Schematics C

The most current schematics, including "flat" schematics (without the 400-pin connector), are located on Intel's Developer Web site at: http://www.intel.com/design/intarch/schems/.

Schematics are provided for the following items:

Baseboard

- Block Diagram
- Mini PCI Connector
- CPU Connector
- DIMM0
- DIMM1
- DIMM2
- Clocks
- ISA/PCI Pullups
- PCI Slots 0 & 1
- PCI Slot 2
- AGP Connector
- PIIX4 Part 1
- PIIX4 Part 2
- IDE Connectors
- Super I/O
- USB Connectors
- ISA Connectors
- COMx, DB25, Floppy
- BIOS/ Port 80
- ATX Power Connector
- Unused Gates

Processor Assembly

- Low-Power Pentium Processor with MMX Technology
- 82439TX System Controller
- Cache and Tags
- ITP / Strapping Options
- Regulators
- Connector
- CPU Decoupling

Evaluation Platform
System Electronics Board

Revision D

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History

Changes made to Revision D.

1. Added Signals PWROK(A24) +12V(A33) MB12#_R(B33) to J19A.
2. Moved J20
3. Added C229 to -PCIRST

Changes made to Revision C.

1. Tied VBAT (pin 65) to 3.3V on Super I/O.

Changes made to Revision B.

1. Swapped AD23 and AD19 on 400 pin connector.
2. Separated CSEL on IDE0 and IDE1
3. Swapped pins 1 and 3 (V5 with TP) on CPU-Fan connector.
4. Tied VBAT (pin 65) to 5.0V on Super I/O.
5. Changed RP48 to 4.7K. (Pullups for mouse and keyboard.)
6. Inverted POWERON# signal (SUSC#) from PIIX4 to control soft-on feature.
7. Changed Bulk decoupling on +12 and -12 to 2x220uF from 2x400uF.
8. Changed Bulk decoupling cap C154 from 10uF to 47uF to reduce BOM line items.

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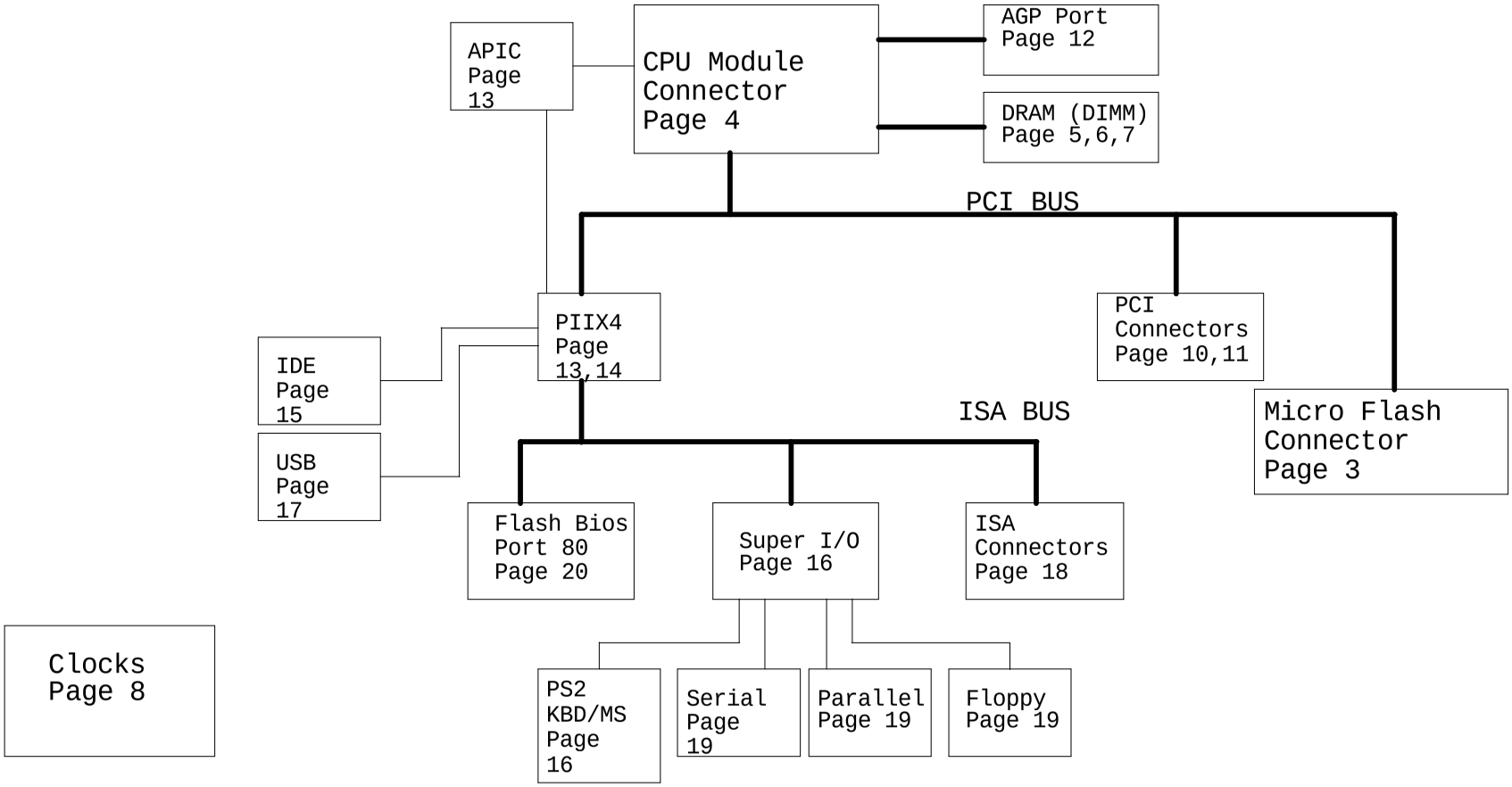
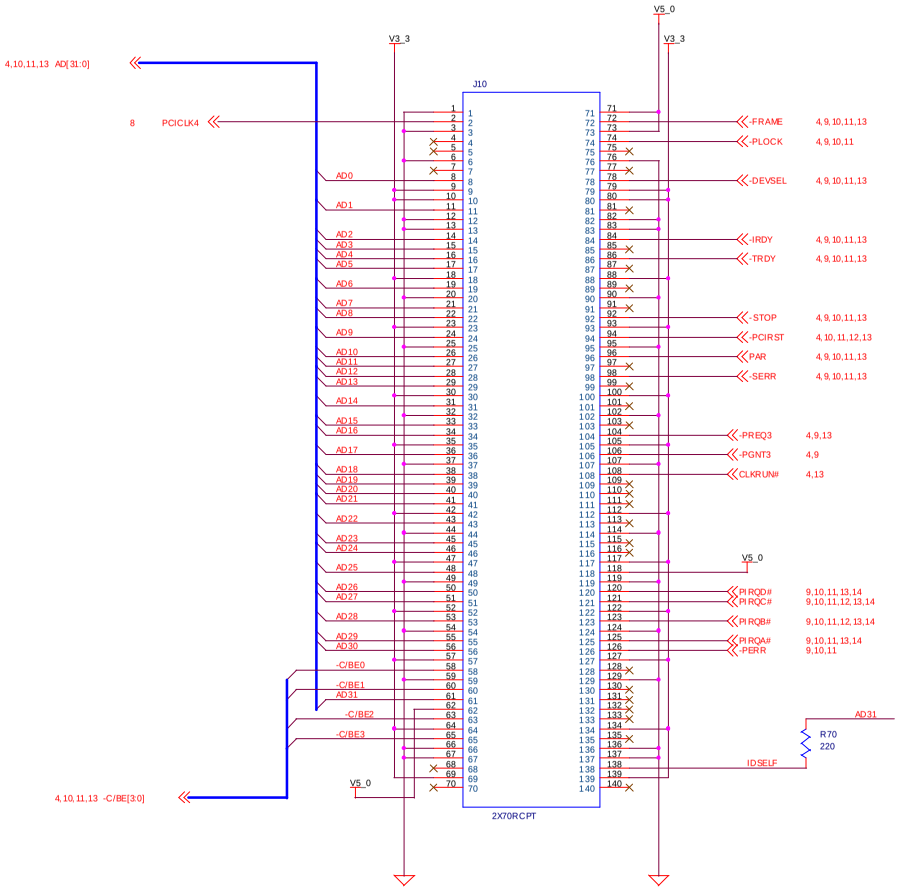
Title: Changes		
Size: C	Document Number:	Rev: D
Date: Thursday, February 25, 1999	Sheet 1 of 22	



Title: Shakopee		
Size: C	Document Number: {Doc}	Rev: D
Date: Thursday, February 25, 1999	Sheet 2 of 22	



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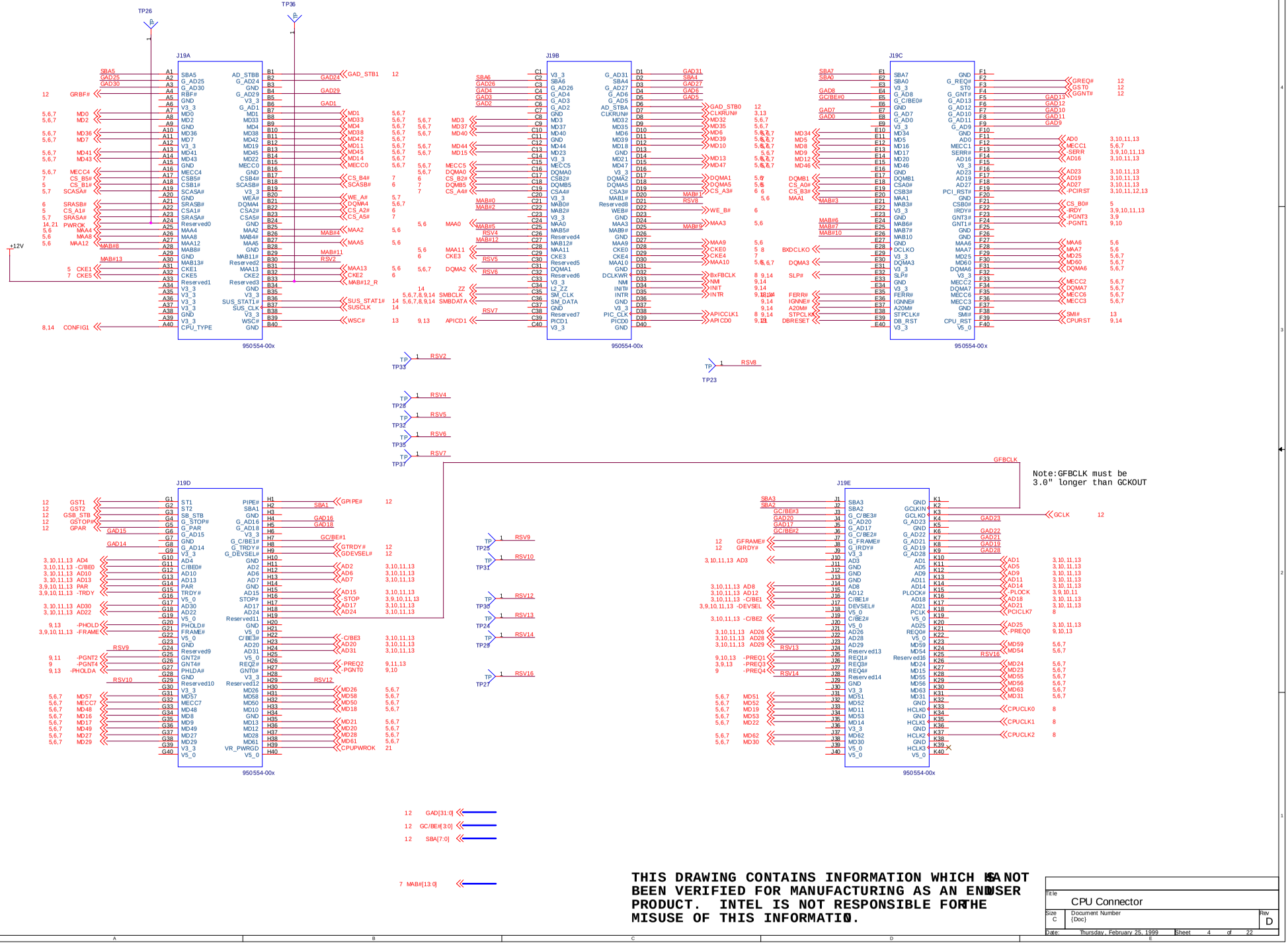
Title: Mini PCI Connector

Size	Document Number	Rev
C	{Doc}	D

Date: Thursday, February 25, 1999 Sheet 3 of 22


TP26
TP36
J19A
J19B
J19C
J19D
J19E
950554-00x
+12V
TP33
TP28
TP32
TP35
TP37
TP23
TP25
TP31
TP30
TP24
TP29
TP27
RSV2
RSV4
RSV5
RSV6
RSV7
RSV8
RSV9
RSV10
RSV12
RSV13
RSV14
RSV16
GFBCLK
Note:GFBCLK must be 3.0" longer than GCKOUT
12 GAD[31:0]
12 GC/BE#[3:0]
12 SBA[7:0]
7 MAB#[13:0]
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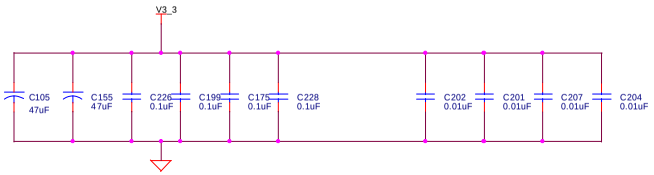
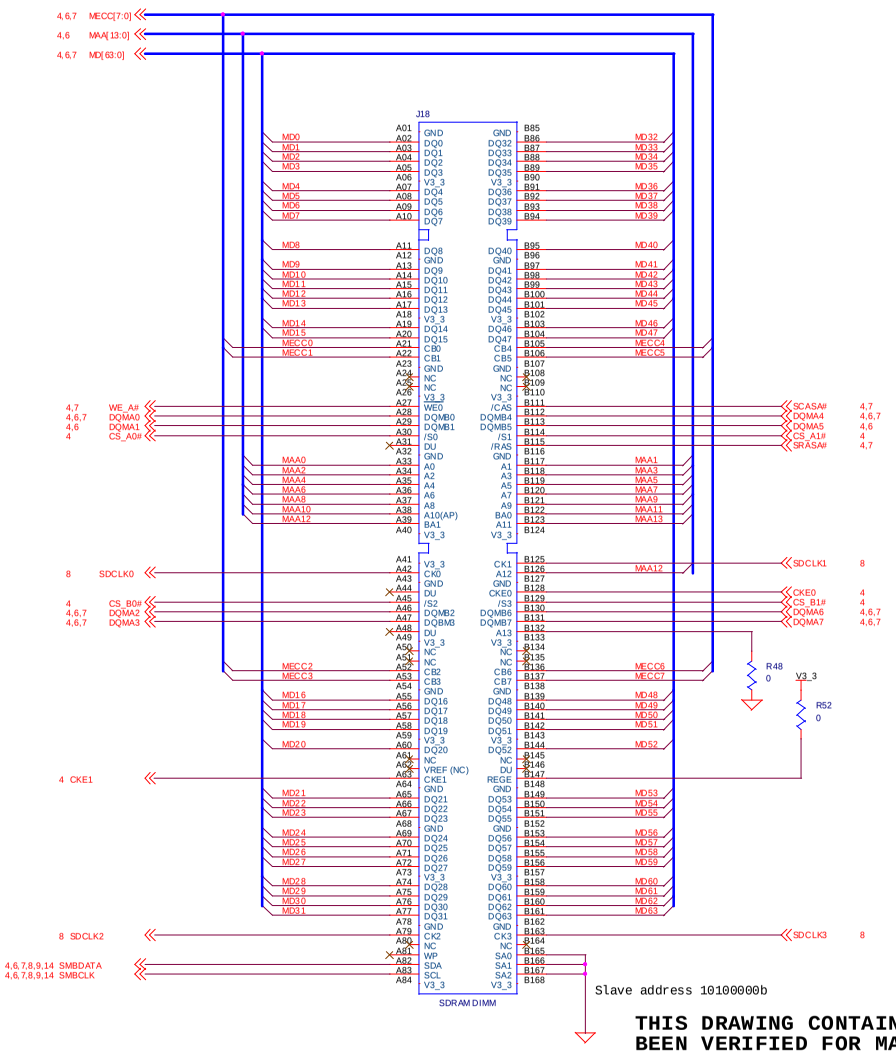
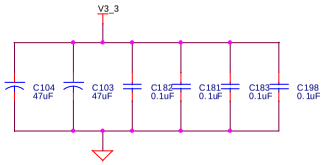
Title
CPU Connector
Size C
Document Number {Doc}
Rev D
Date: Thursday, February 25, 1999
Sheet 4 of 22



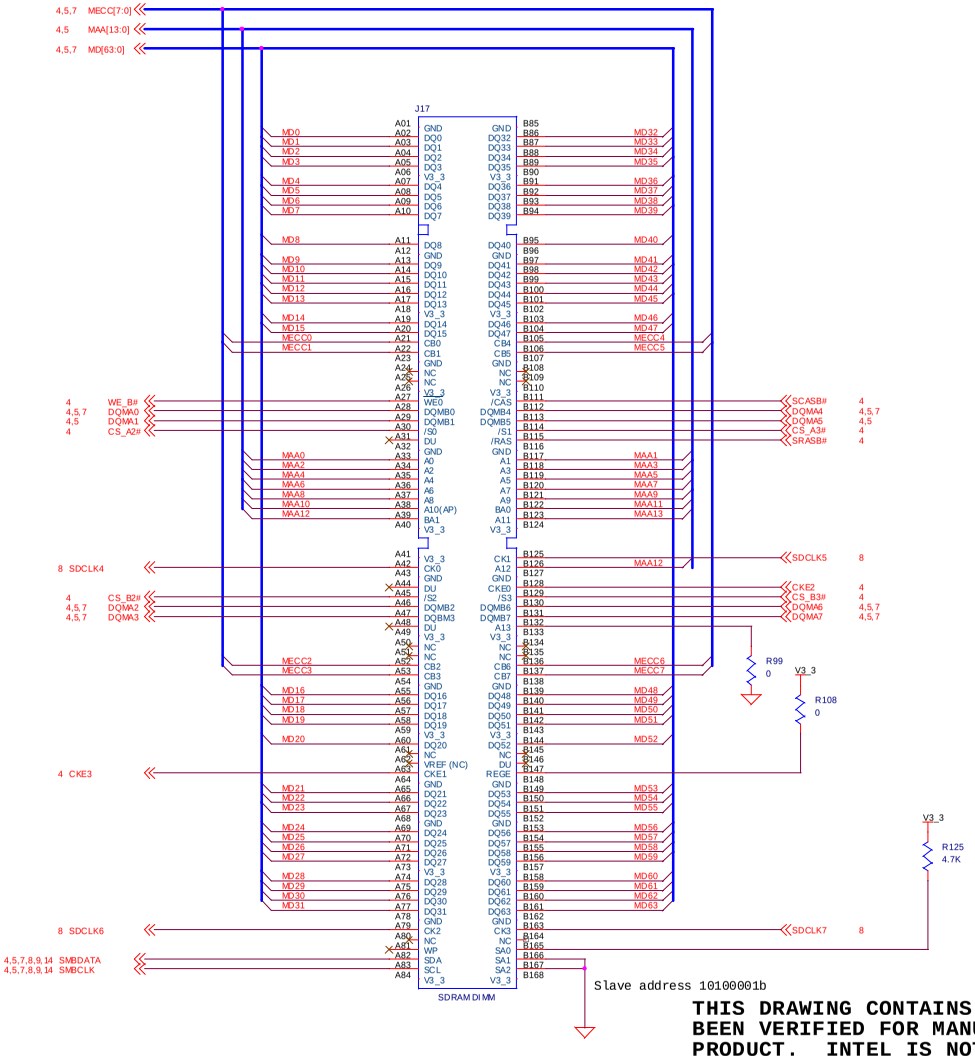
Socket 0



Title: DIMM0		
Size: C	Document Number: {Doc}	Rev: D
Date: Thursday, February 25, 1999	Sheet 5 of 22	



Socket 1



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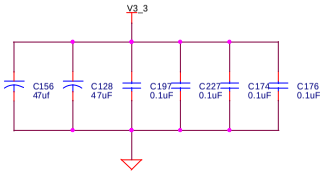
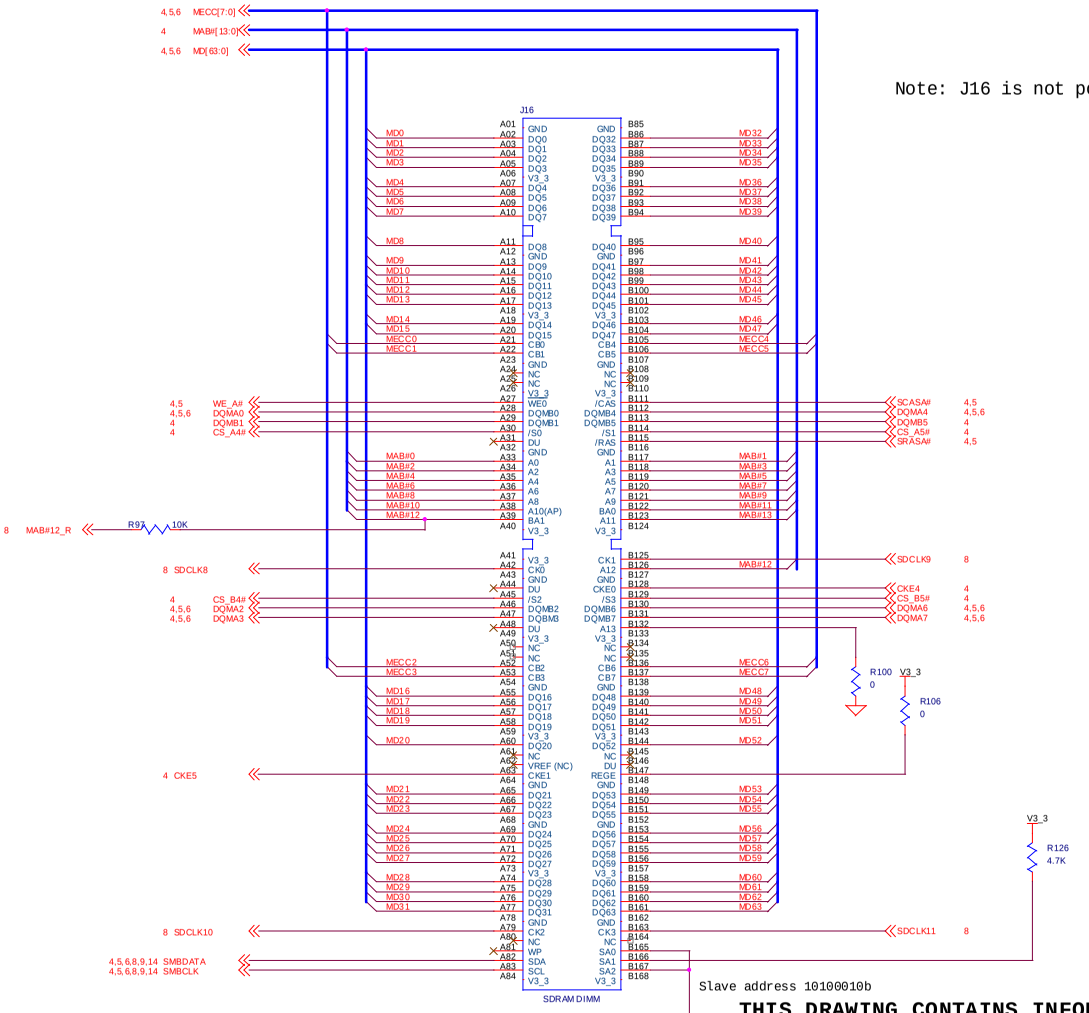
Size: C	Document Number: {Doc}	Rev: D
Date: Thursday, February 25, 1999	Sheet 6 of 22	

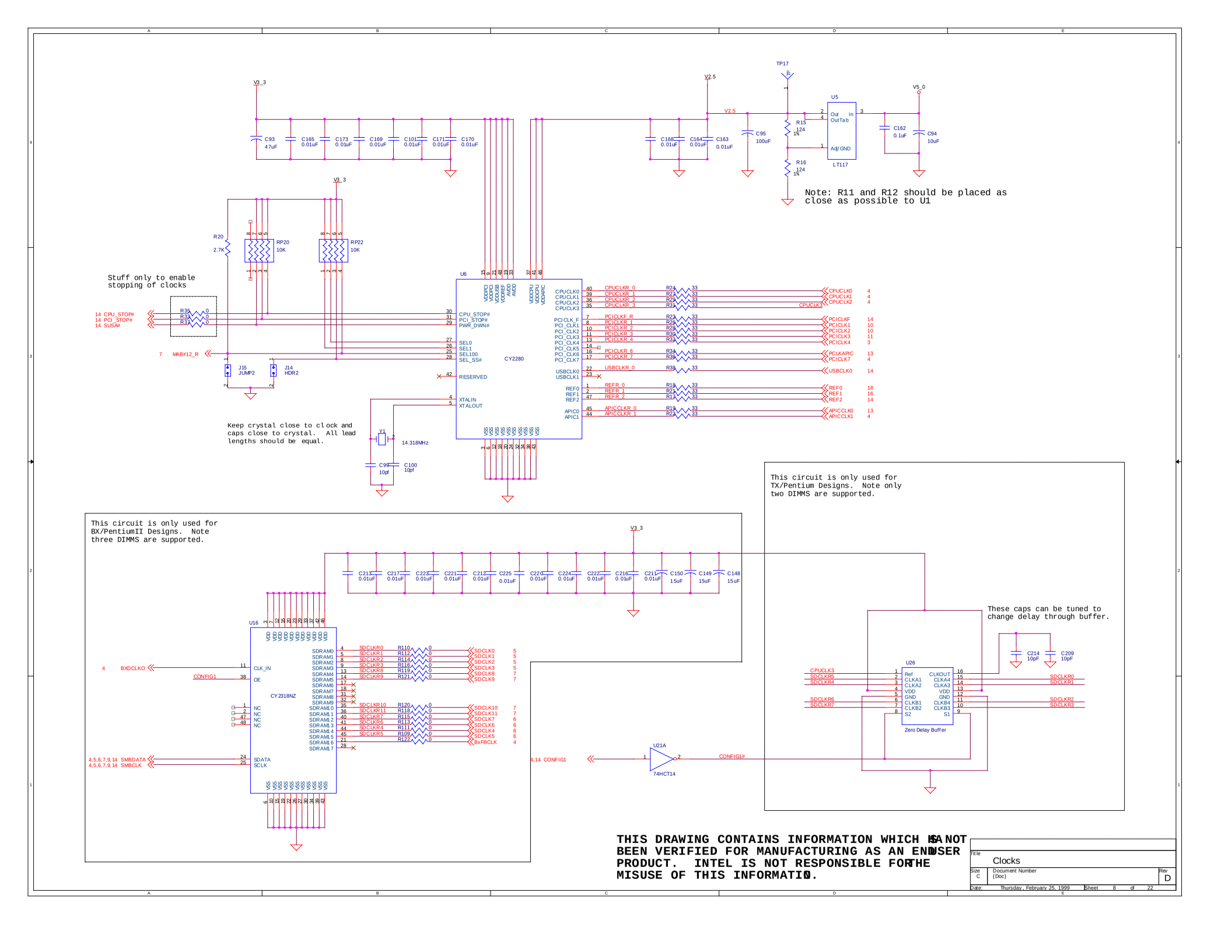


Socket 2

Note: J16 is not popula ted



Title	DIMM2	
Size C	Document Number {Doc}	Rev D
Date: Thursday, February 25, 1999	Sheet 7 of 22	


Note: R11 and R12 should be placed as close as possible to U1
Stuff only to enable stopping of clocks
Keep crystal close to clock and caps close to crystal. All lead lengths should be equal.
This circuit is only used for BX/PentiumII Designs. Note three DIMMS are supported.
This circuit is only used for TX/Pentium Designs. Note only two DIMMS are supported.
These caps can be tuned to change delay through buffer.
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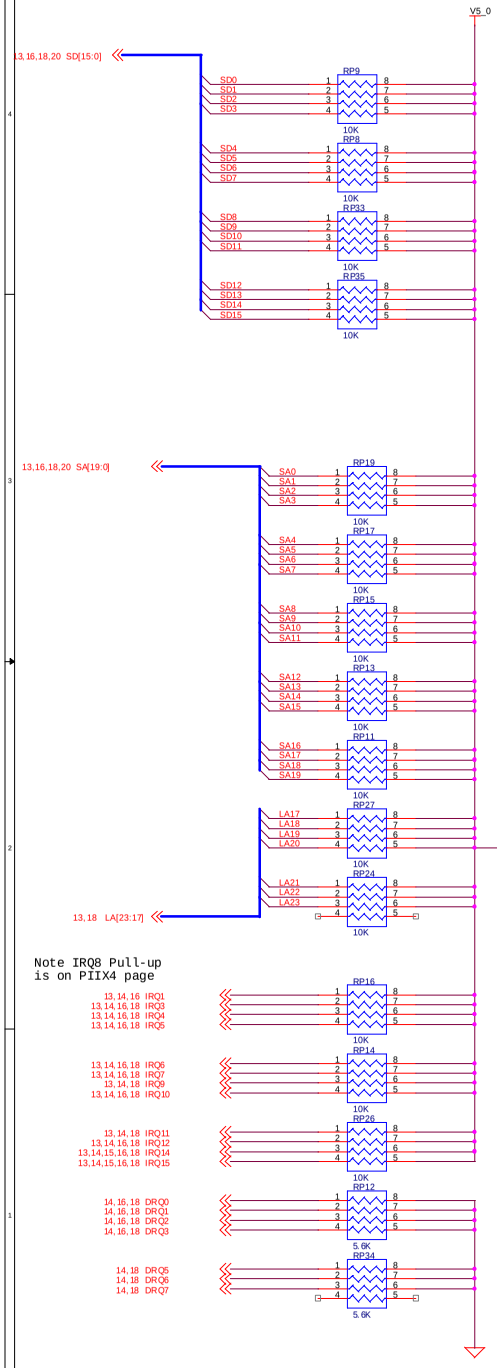
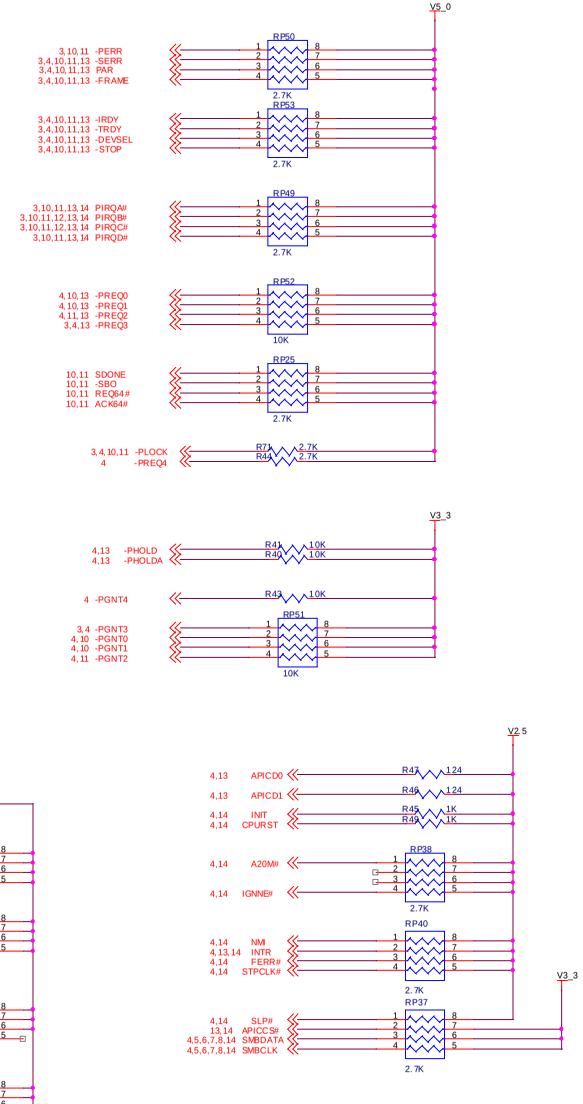
Title
Clocks
Size C
Document Number {Doc}
Rev D
Date: Thursday, February 25, 1999
Sheet 8 of 22

ISA Pullups



PCI Pullups



Title	ISA/PCI Pullups	
Size C	Document Number {Doc}	Rev D
Date: Thursday, February 25, 1999	Sheet 9 of 22	

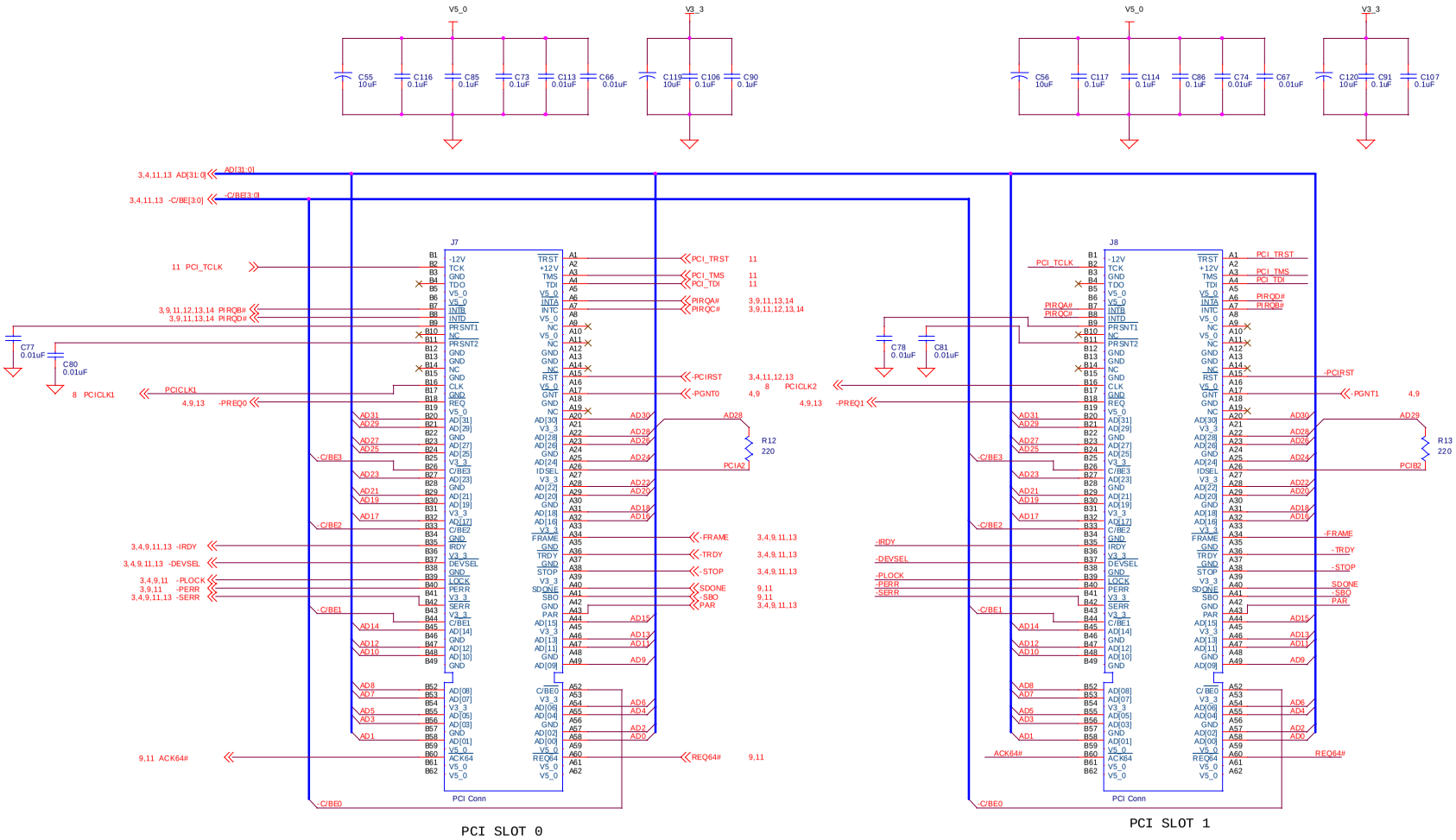
J7/J8 V5_0:
A5, A8, A10, A16, A59, A61, A62 | A1, A3, A4
B5, B6, B19, B22, B59, B61, B62

J7/J8 V3_3:
A21, A27, A33, A39 A45, A53
B25, B31, B36, B41, B43, B54

J7/J8 NC:
A9, A11, A1 4, A19
B10, B14

J7/J8 GND:
A12, A13, A18, A24, A30, A35, A37, A42, A48, A56
B3, B12, B13, B15, B17, B28, B34, B38, B46, B49,
B57

J7/J8 +12V: A2
-12V: B1



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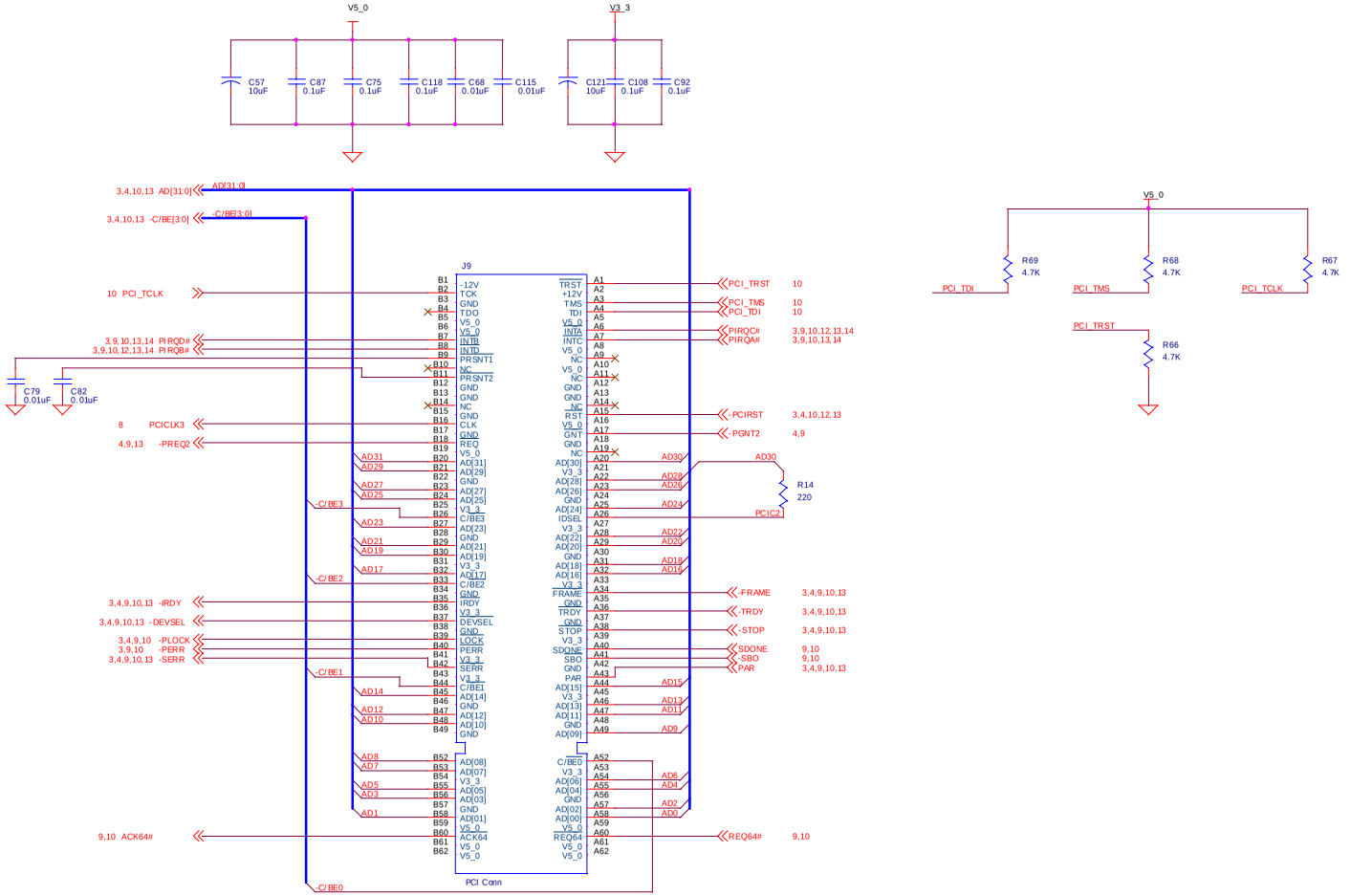
Title: PCI Slots 0 & 1		
Size: C	Document Number: {Doc}	Rev: D
Date: Thursday, February 25, 1999	Sheet 10 of 22	



PCI SLOT 2

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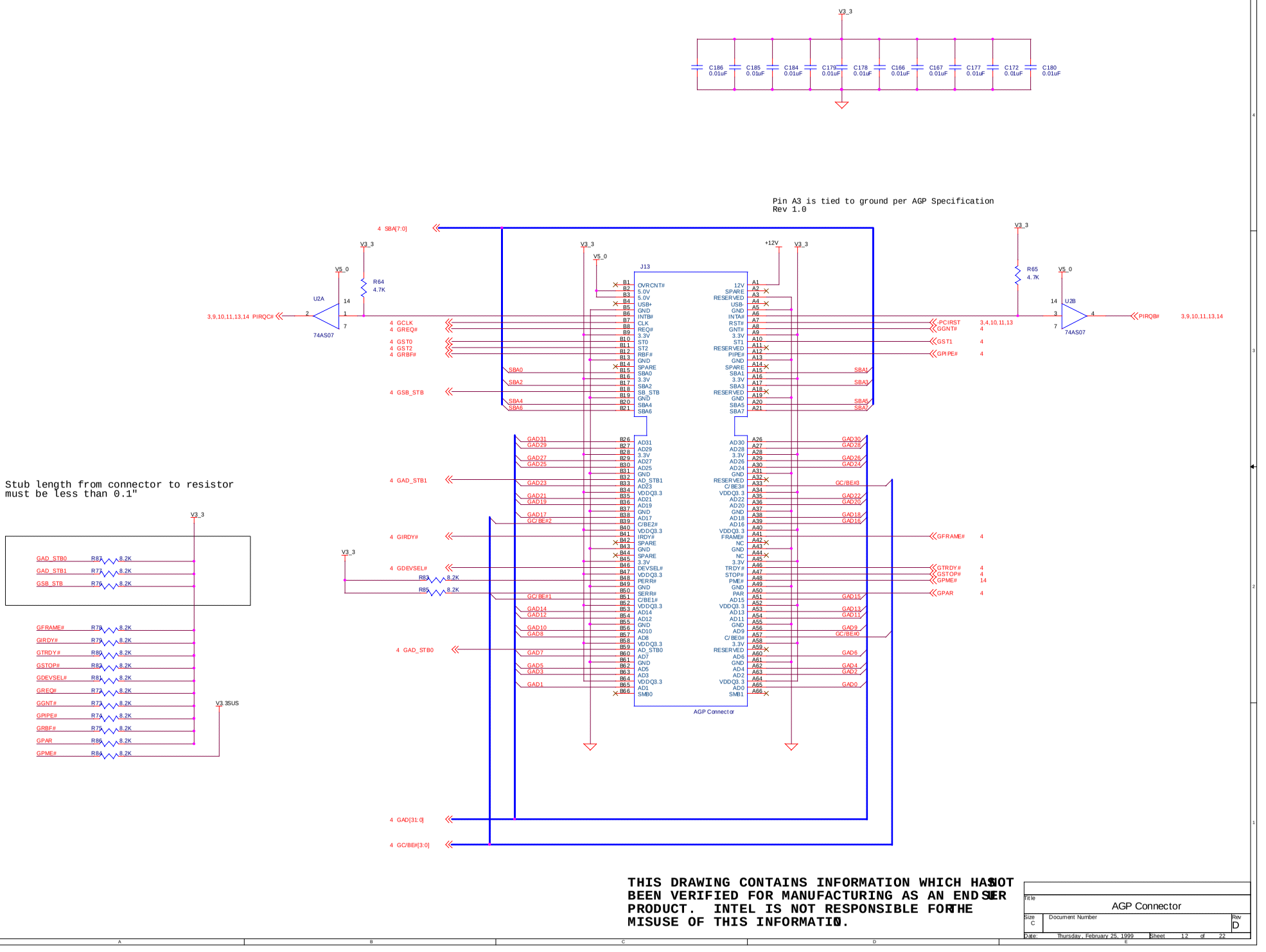
Title	PCI Slot 2
Size C	Document Number {Doc}
Rev	D
Date: Thursday, February 25, 1999	Sheet 11 of 22



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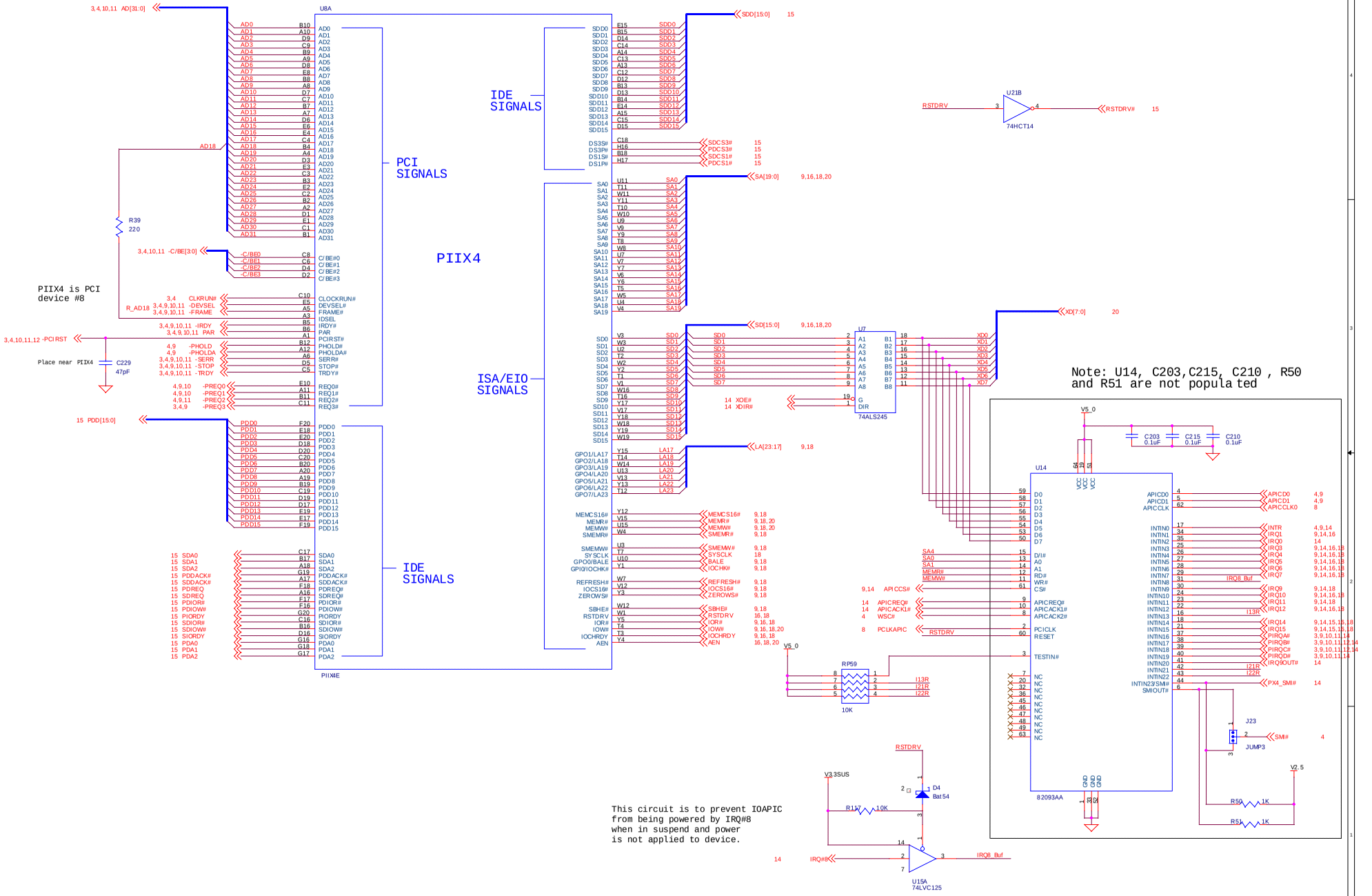
Title	AGP Connector	
Size C	Document Number	Rev D
Date: Thursday, February 25, 1999	Sheet 12 of 22	


U8A
PIIX4
PCI SIGNALS
IDE SIGNALS
ISA/EIO SIGNALS
IDE SIGNALS
PIIX4 is PCI device #8
Place near PIIX4
C229 47pF
R39 220
74HCT14
74ALS245
74LVC125
82093AA
RP59 10K
JUMP3
Note: U14, C203,C215, C210 , R50 and R51 are not populated
This circuit is to prevent IOAPIC from being powered by IRQ#8 when in suspend and power is not applied to device.
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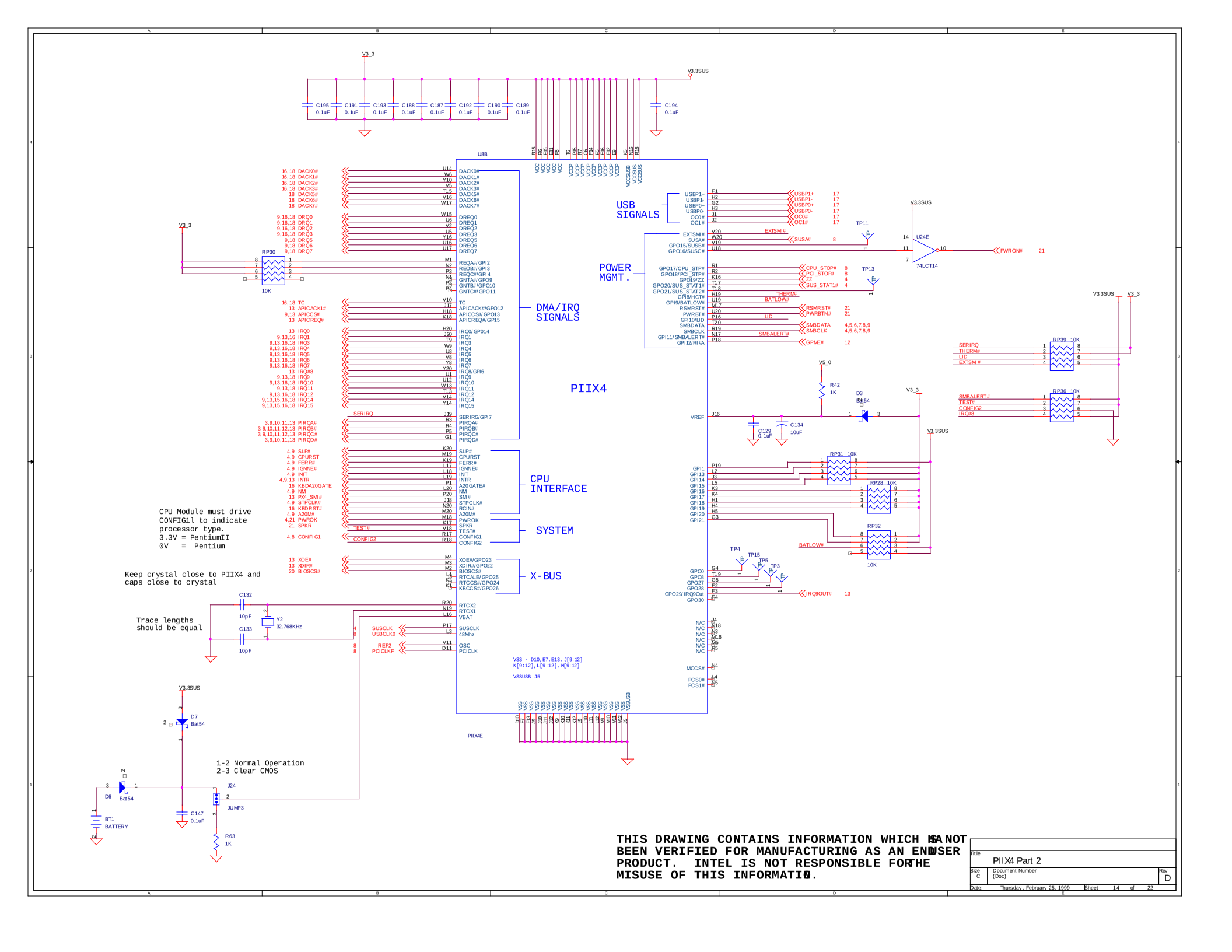
Title
PIIX4 Part 1
Size C
Document Number {Doc}
Rev D
Date: Thursday, February 25, 1999
Sheet 13 of 22


U8B
PIIX4
USB SIGNALS
POWER MGMT.
DMA/IRQ SIGNALS
CPU INTERFACE
SYSTEM
X-BUS
CPU Module must drive CONFIG1 to indicate processor type.
3.3V = PentiumII
0V = Pentium
Keep crystal close to PIIX4 and caps close to crystal
Trace lengths should be equal
1-2 Normal Operation
2-3 Clear CMOS
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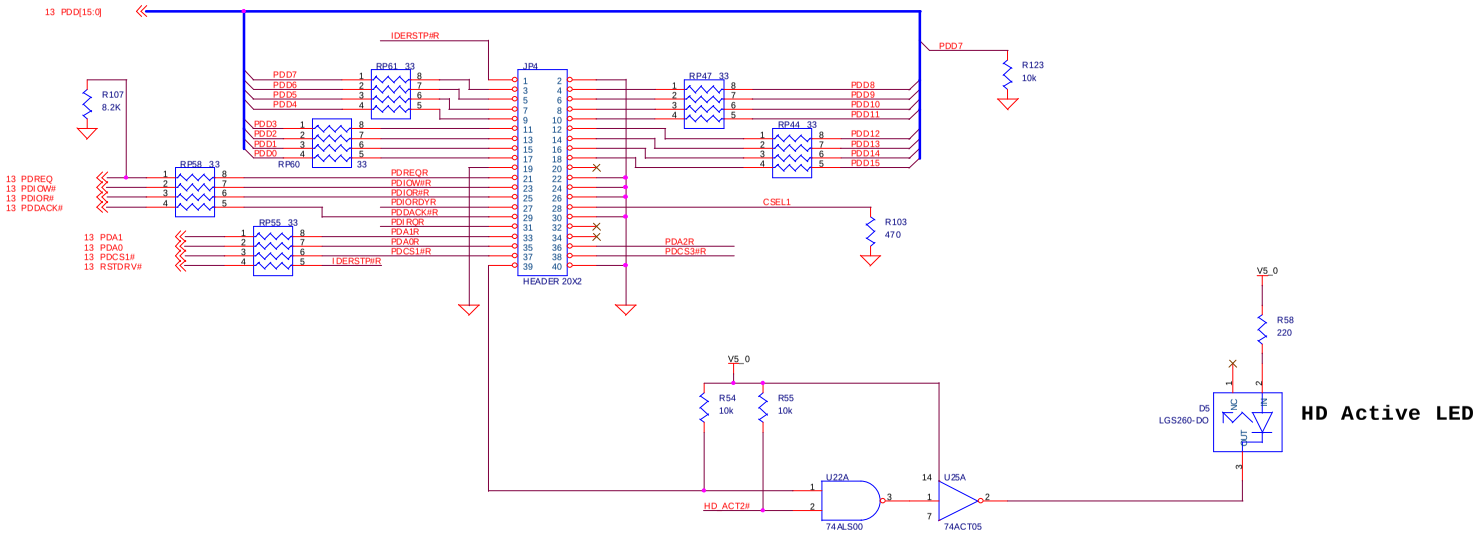
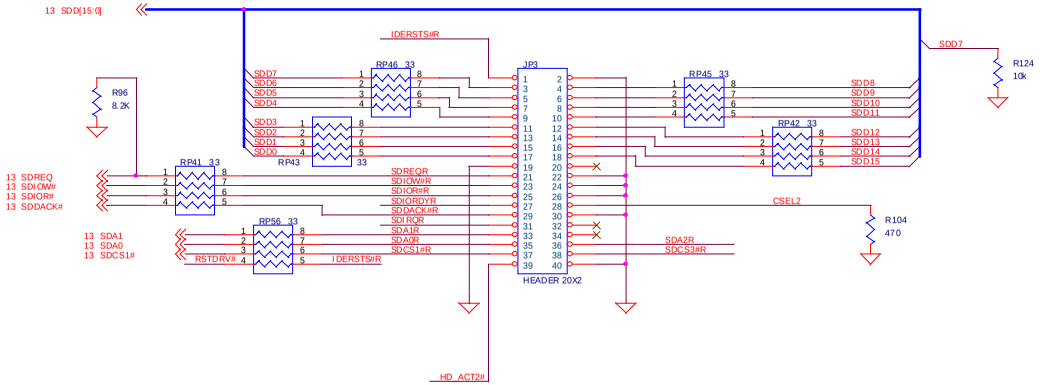
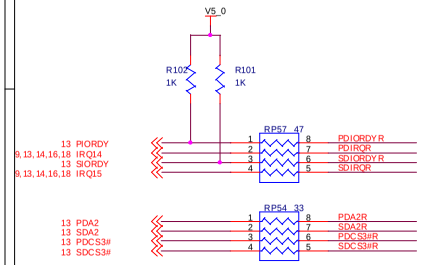
PIIX4 Part 2
Document Number {Doc}
Rev D
Thursday, February 25, 1999
Sheet 14 of 22

Primary IDE Connector



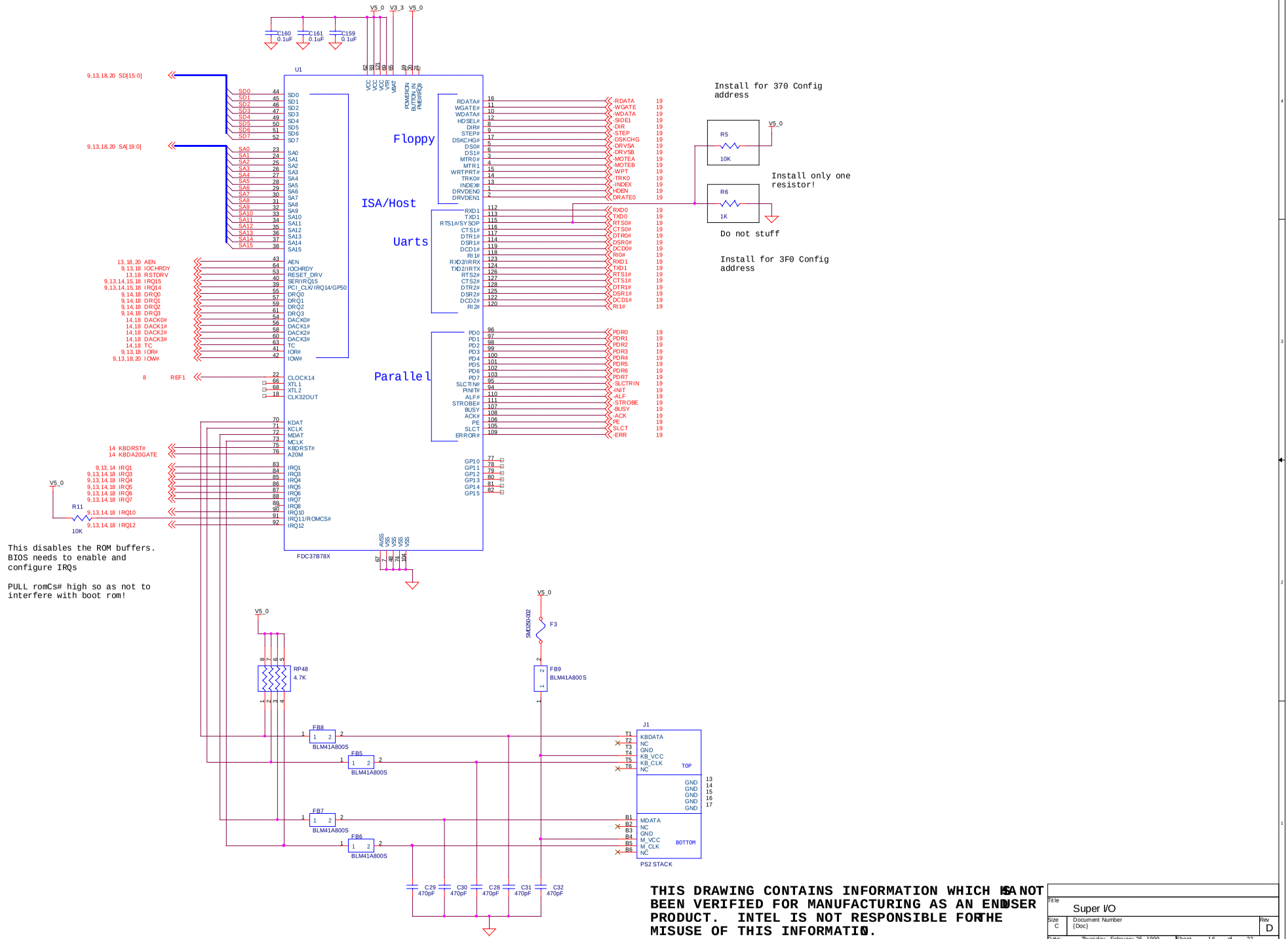
Secondary IDE Connector





THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.

Title: IDE Connectors		
Size: C	Document Number: {Doc}	Rev: D
Date: Thursday, February 25, 1999	Sheet 15 of 22	



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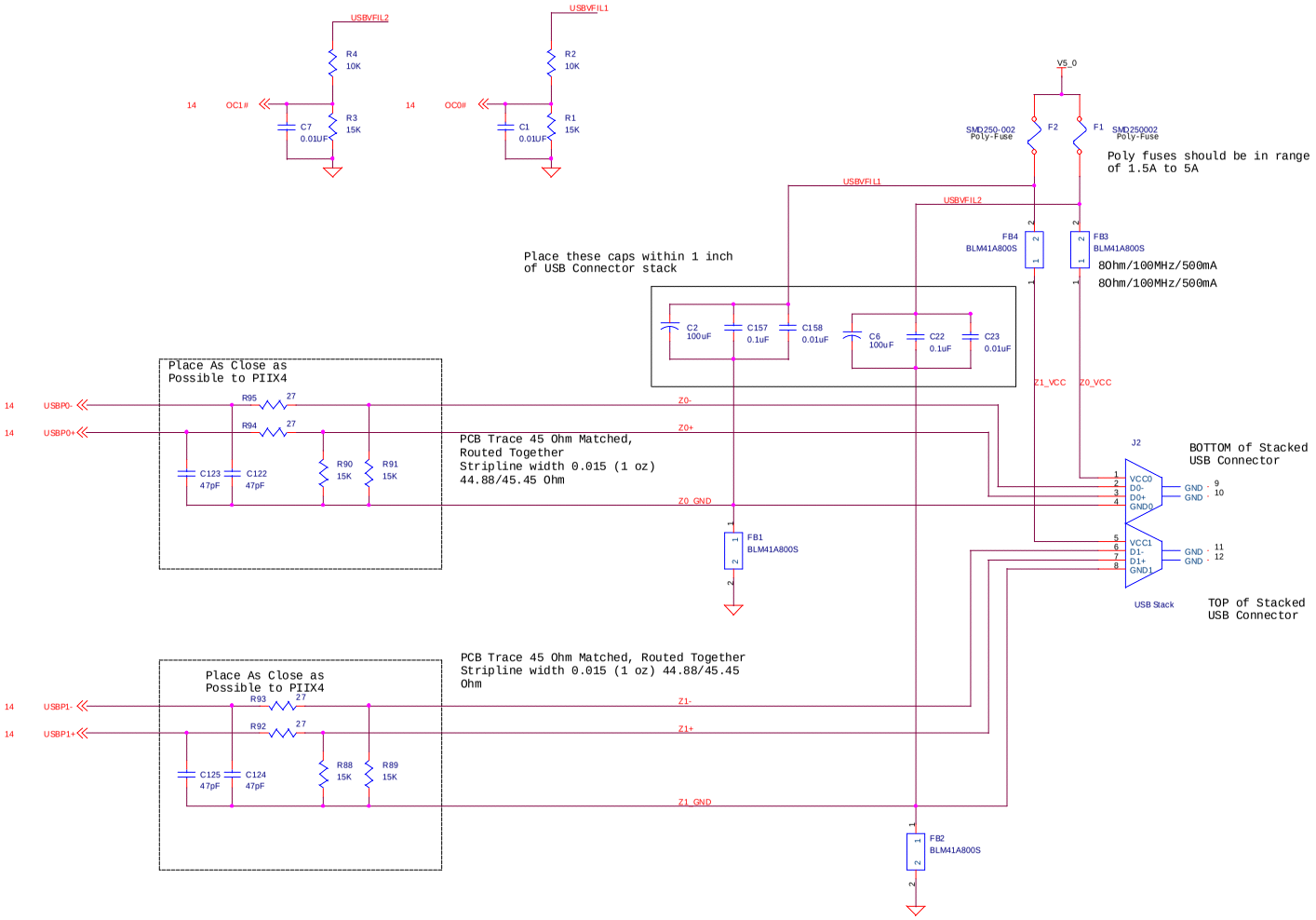
Title	Super I/O
Size	C
Document Number	{Doc}
Rev	D
Date:	Thursday, February 25, 1999
Sheet	16 of 22



NOTE 1: USB differential traces route together (Z0- & Z0+) and (Z1- & Z1+).
Must be 45 Ohm Matched
Stripline width 0.015 (for 1 oz)->44.88/45.45 Ohm.

NOTE 2: Protect differential traces w/ guard traces or
double space to any other signal.

NOTE 3: Place ferrites at connector.

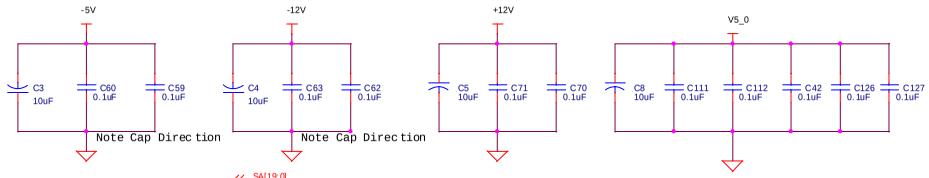
NOTE 4: Poly-fuse min 1.5A
max 5A.

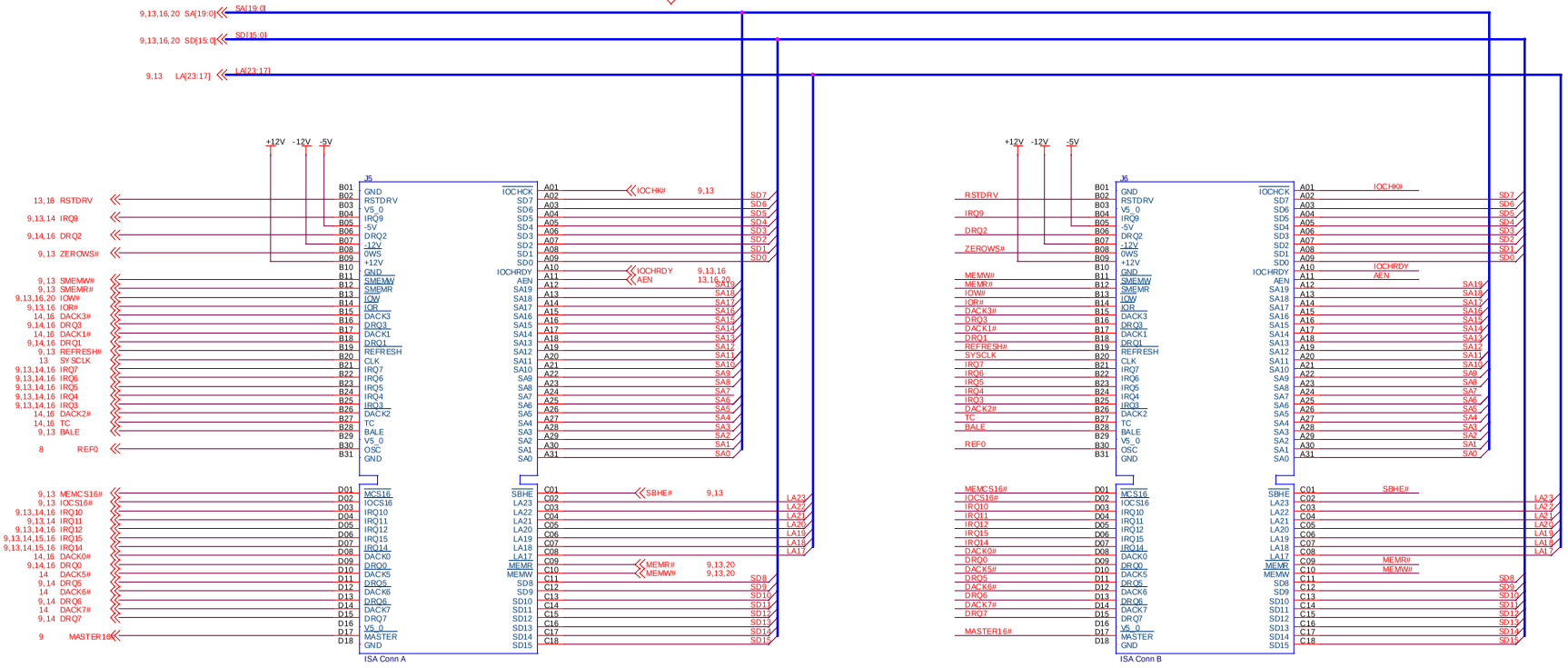
Title: USB Connectors

Size: C | Document Number: {Doc} | Rev: D

Date: Thursday, February 25, 1999 | Sheet 17 of 22

ISA Slots





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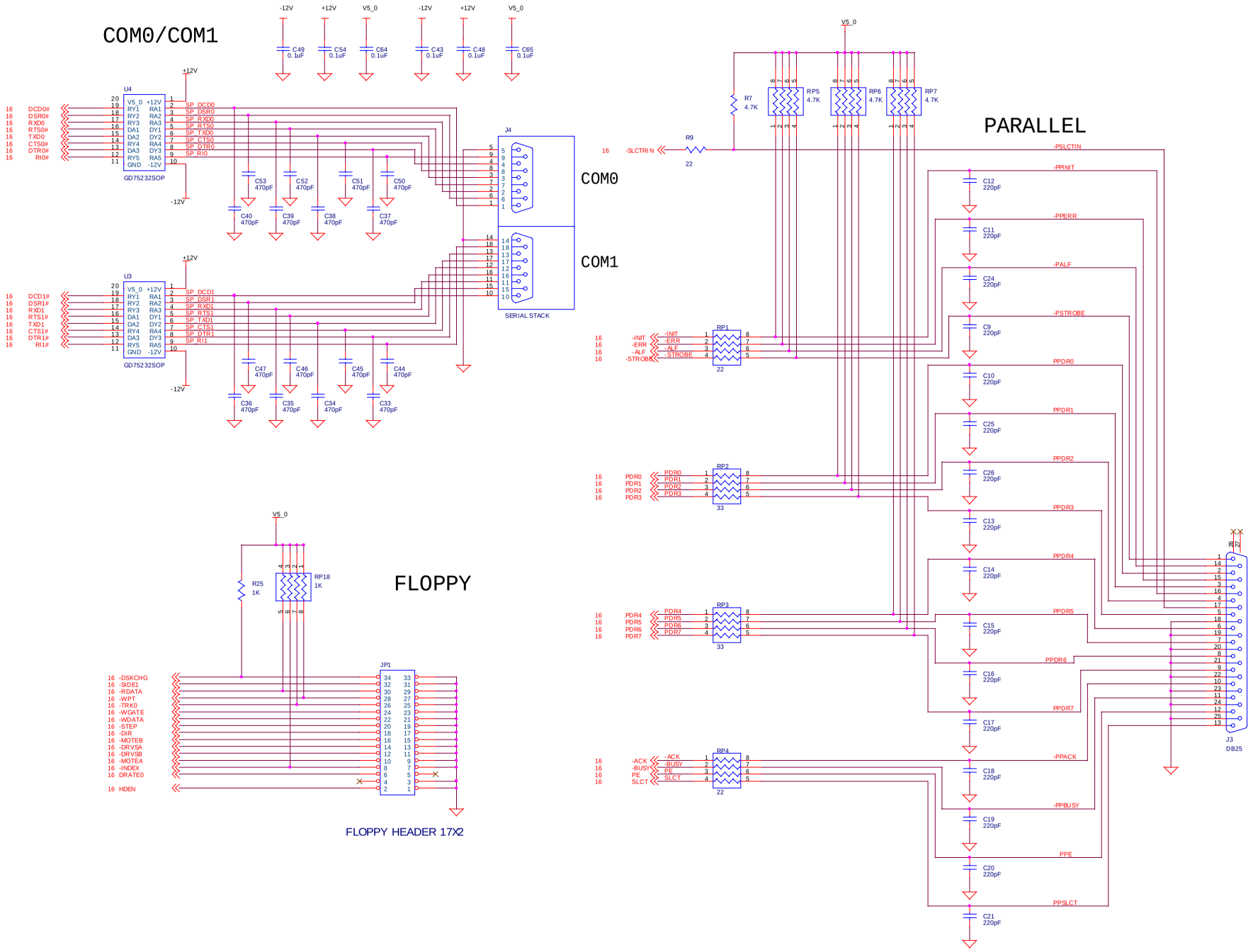
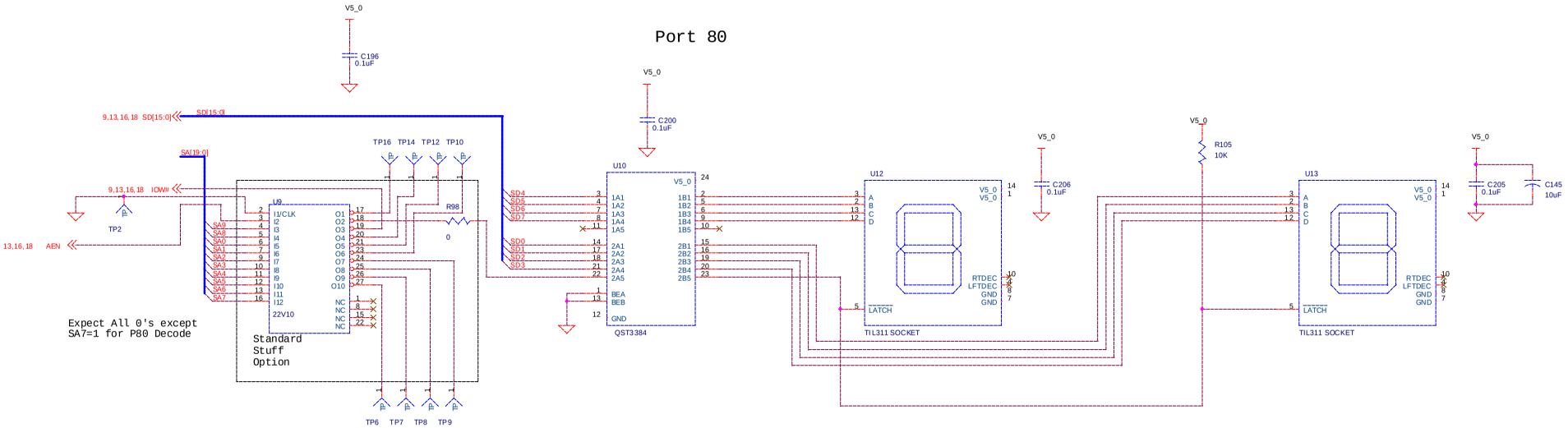
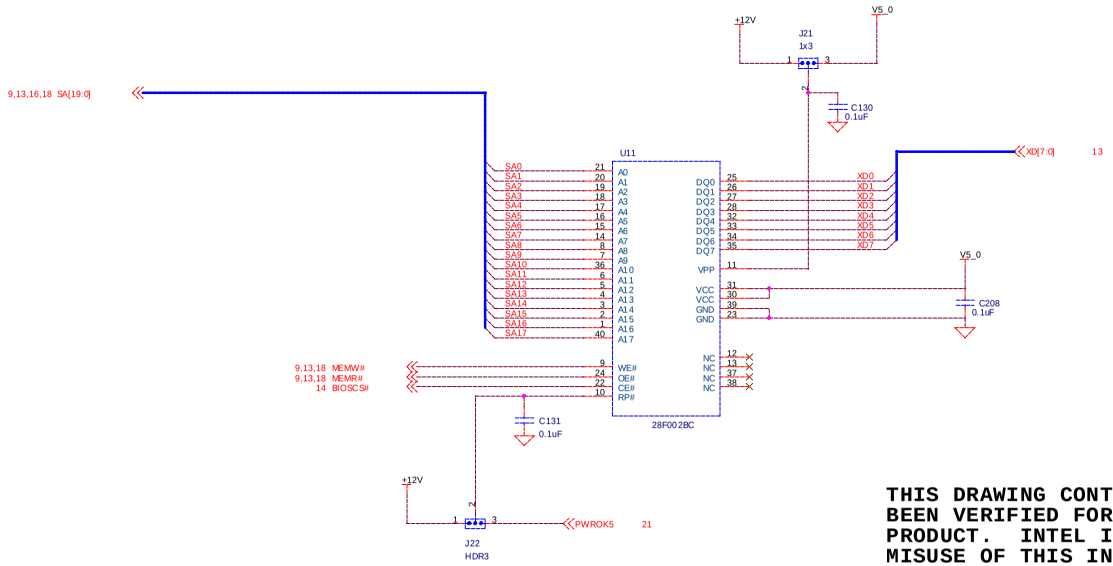
Title: ISA Connectors		
Size: C	Document Number: {Doc}	Rev: D
Date: Thursday, February 25, 1999	Sheet 18 of 22	


COM0/COM1
-12V
+12V
V5_0
C49 0.1uF
C54 0.1uF
C64 0.1uF
C43 0.1uF
C48 0.1uF
C65 0.1uF
U4
GD75232SOP
DCD0#
DSR0#
RXD0
RTS0#
TXD0
CTS0#
DTR0#
RI0#
SP_DCD0
SP_DSR0
SP_RXD0
SP_RTS0
SP_TXD0
SP_CTS0
SP_DTR0
SP_RI0
C53 470pF
C52 470pF
C51 470pF
C50 470pF
C40 470pF
C39 470pF
C38 470pF
C37 470pF
J4
SERIAL STACK
COM0
COM1
U3
GD75232SOP
DCD1#
DSR1#
RXD1
RTS1#
TXD1
CTS1#
DTR1#
RI1#
SP_DCD1
SP_DSR1
SP_RXD1
SP_RTS1
SP_TXD1
SP_CTS1
SP_DTR1
SP_RI1
C47 470pF
C46 470pF
C45 470pF
C44 470pF
C36 470pF
C35 470pF
C34 470pF
C33 470pF
FLOPPY
R25 1K
RP18 1K
JP1
-DSKCHG
-SIDE1
-RDATA
-WPT
-TRK0
-WGATE
-WDATA
-STEP
-DIR
-MOTEB
-DRVSA
-DRVSB
-MOTEA
-INDEX
DRATE0
HDEN
FLOPPY HEADER 17X2
PARALLEL
R7 4.7K
RP5 4.7K
RP6 4.7K
RP7 4.7K
R9 22
-SLCTRIN
-INIT
-ERR
-ALF
-STROBE
RP1
PDR0
PDR1
PDR2
PDR3
RP2
PDR4
PDR5
PDR6
PDR7
RP3
-ACK
-BUSY
PE
SLCT
RP4
-PSLCTIN
-PPINIT
-PPERR
-PALF
-PSTROBE
PPDR0
PPDR1
PPDR2
PPDR3
PPDR4
PPDR5
PPDR6
PPDR7
-PPACK
-PPBUSY
PPE
PPSLCT
C12 220pF
C11 220pF
C24 220pF
C9 220pF
C10 220pF
C25 220pF
C26 220pF
C13 220pF
C14 220pF
C15 220pF
C16 220pF
C17 220pF
C18 220pF
C19 220pF
C20 220pF
C21 220pF
J3
DB25
THIS DRAWING CONTAINS INFORMATION WHICH HAS NOT BEEN VERIFIED FOR MANUFACTURING AS AN END USER PRODUCT. INTEL IS NOT RESPONSIBLE FOR THE MISUSE OF THIS INFORMATION.
Title
COMx, DB25, Floppy
Size C
Document Number {Doc}
Rev D
Date: Thursday, February 25, 1999
Sheet 19 of 22

Port 80





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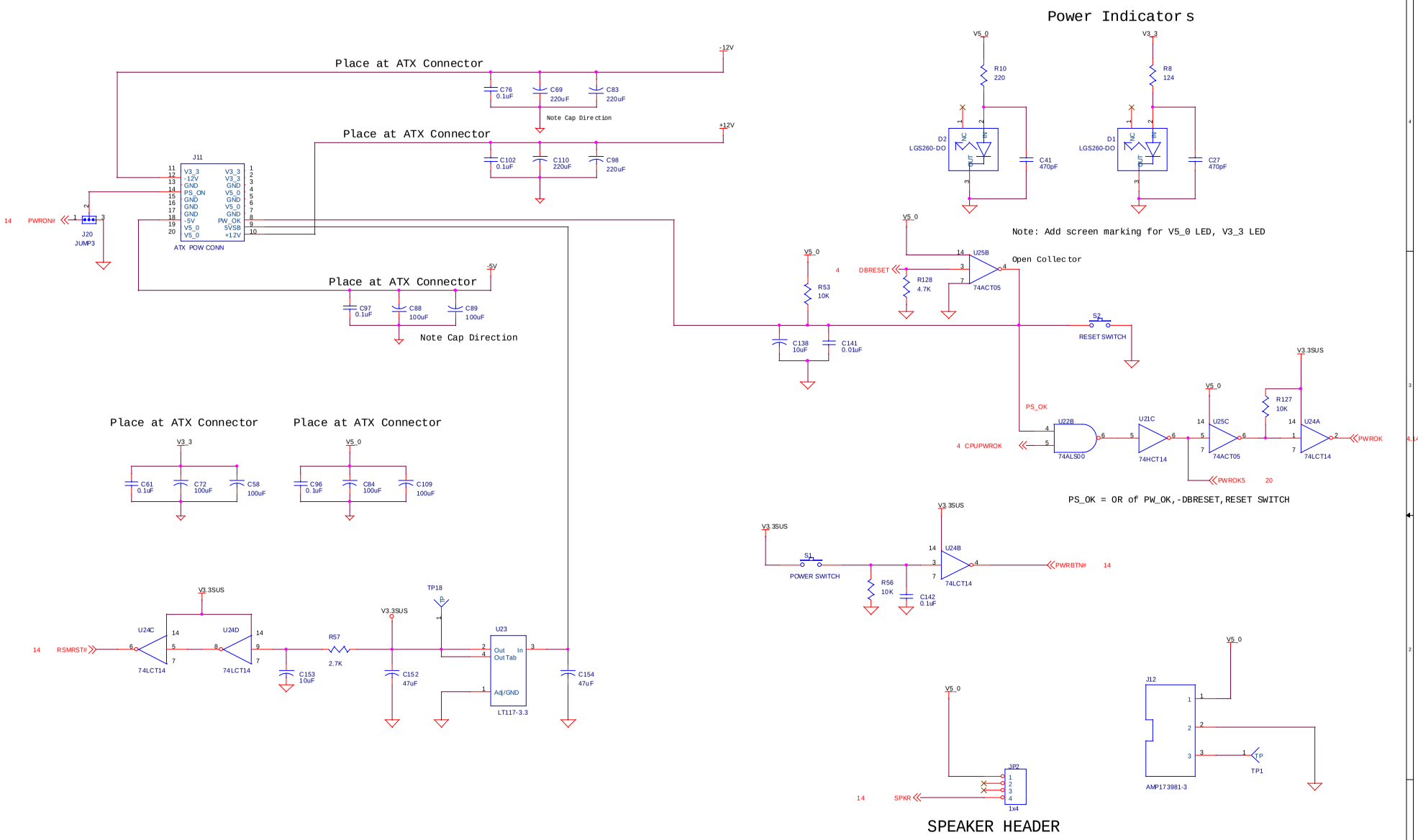
Title: BIOS/ Port 80		
Size: C	Document Number: {Doc}	Rev: D
Date: Thursday, February 25, 1999	Sheet 20 of 22	



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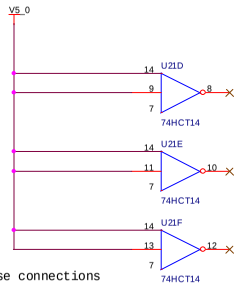
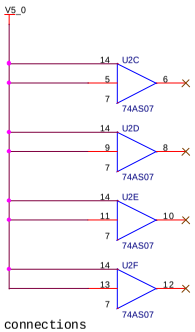
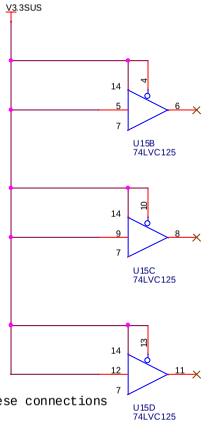
Title	AXT Power Connector	
Size C	Document Number {Doc}	Rev D
Date: Thursday, February 25, 1999	Sheet 21 of 22	



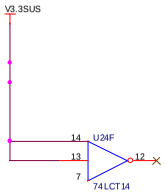
Make these connections
Cutable



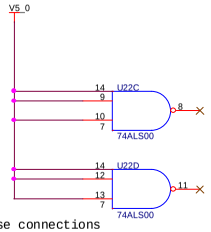
Make these connections
Cutable



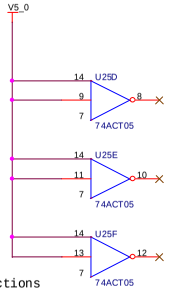
Make these connections
Cutable



Make these connections
Cutable



Make these connections
Cutable



Make these connections
Cutable

Title: Unused Gates		
Size: C	Document Number: {Doc}	Rev: D
Date: Thursday, February 25, 1999	Sheet 22 of 22	

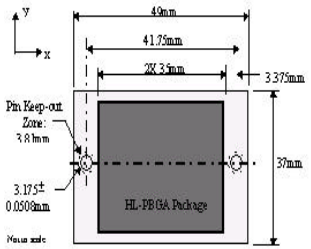
REVISION HISTORY:

1. ITP Vsense reference changed from 3.3V to 2.5V (R1 page 7)
2. Power good timing cap (C38) net change so cap is between gnd and VR_PWRGD (page 6).
3. Byte 1 and Byte 2 of DRAM bus swapped in layout to minimize line length. Bytes 5/6 also swapped.
4. To support the byte-swapping in item 3. Byte enables were also swapped. Done in schematics between the r-packs R7, R37 and U5 (TX). Notice DQM1 goes through R37 and connects to V20 of U4 (normally DQM2). Notice DQM2 goes through R7 and connects to W20 of U4 (normally DQM1). DQM5/6 are swapped similarly.
5. Silkscreen updated to Rev B.
6. Most netlisters do not like the global V(CPU) . The netlist was run and the node V(CPU) was changed to VCPU by hand.
7. Board stack-up is 65 Ohm nominal, 8 layer, 1oz planes
8. Fixed Reference designators in notes -RMK 2/17/99

Title: Revision History		
Size: C	Document Number: XXXX-XXX	Rev: B.0
Date: Thursday, February 25, 1999	Sheet 1 of 8	

Low Power Pentium(r) Processor with MMX(tm) Technology

1. See drawing for keep out mounting holes. Make 50mm x 50mm height restricted box around this. No parts in keepout. Parts <=5mm between keepout and restricted boundary.
2. Make sure BE0#-BE7#, CACHE#, and LOCK# have at least one accessable via.
3. Place test points as close to U2 as possible. Can be a via pad.



BUS FRACTION BIT SETTING BF[2:0]

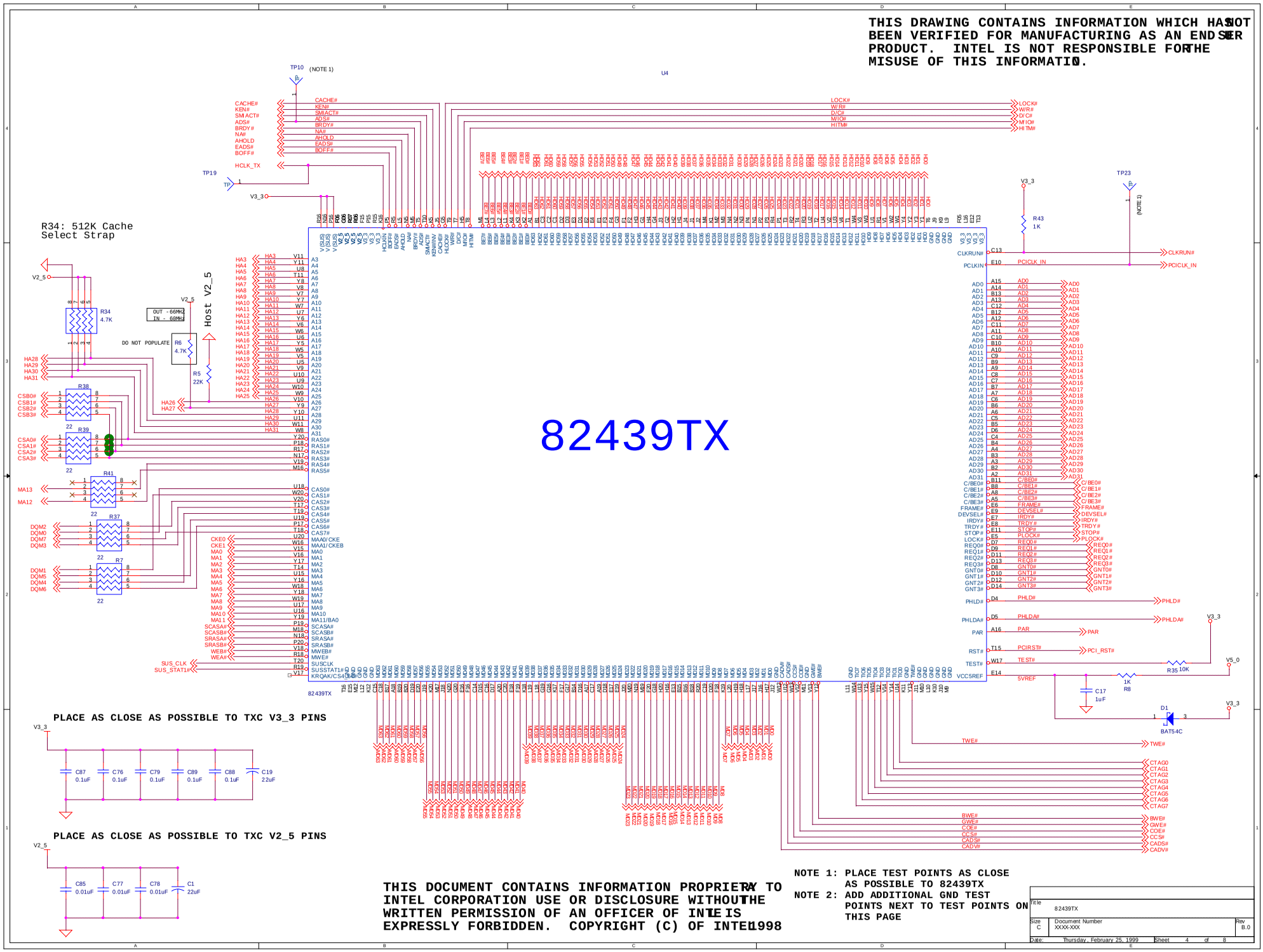
SETTING BF2	BF1	BF0	BUS FRACTION	
0	0	0	2/5	66/166
0	0	1	1/3	66/200
0	1	1	2/7	66/233
1	0	0	1/4	*66/266

All other combinations are reserved.

NOTE 1: PLACE TEST POINTS AS CLOSE AS POSSIBLE TO TilaSLM

NOTE 2: ADD ADDITIONAL GND TEST POINTS NEXT TO TEST POINTS ON THIS PAGE

Title	CPU
Size C	Document Number XXXX-XXX
Rev	B.0
Date:	Thursday, February 25, 1999
Sheet	2 of 8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82439TX
R34: 512K Cache Select Strap
Host V2_5
PLACE AS CLOSE AS POSSIBLE TO TXC V3_3 PINS
PLACE AS CLOSE AS POSSIBLE TO TXC V2_5 PINS
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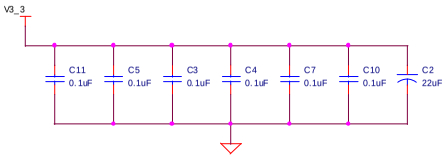
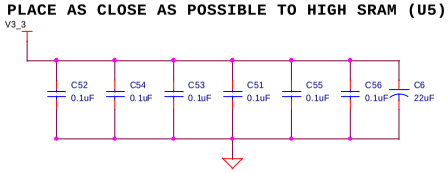
NOTE 1: PLACE TEST POINTS AS CLOSE AS POSSIBLE TO 82439TX
NOTE 2: ADD ADDITIONAL GND TEST POINTS NEXT TO TEST POINTS ON THIS PAGE
Title 82439TX
Size C
Document Number XXXX-XXX
Rev B.0
Date: Thursday, February 25, 1999
Sheet 4 of 8

PLACE AS CLOSE AS POSSIBLE TO LOW SRAM (U4)

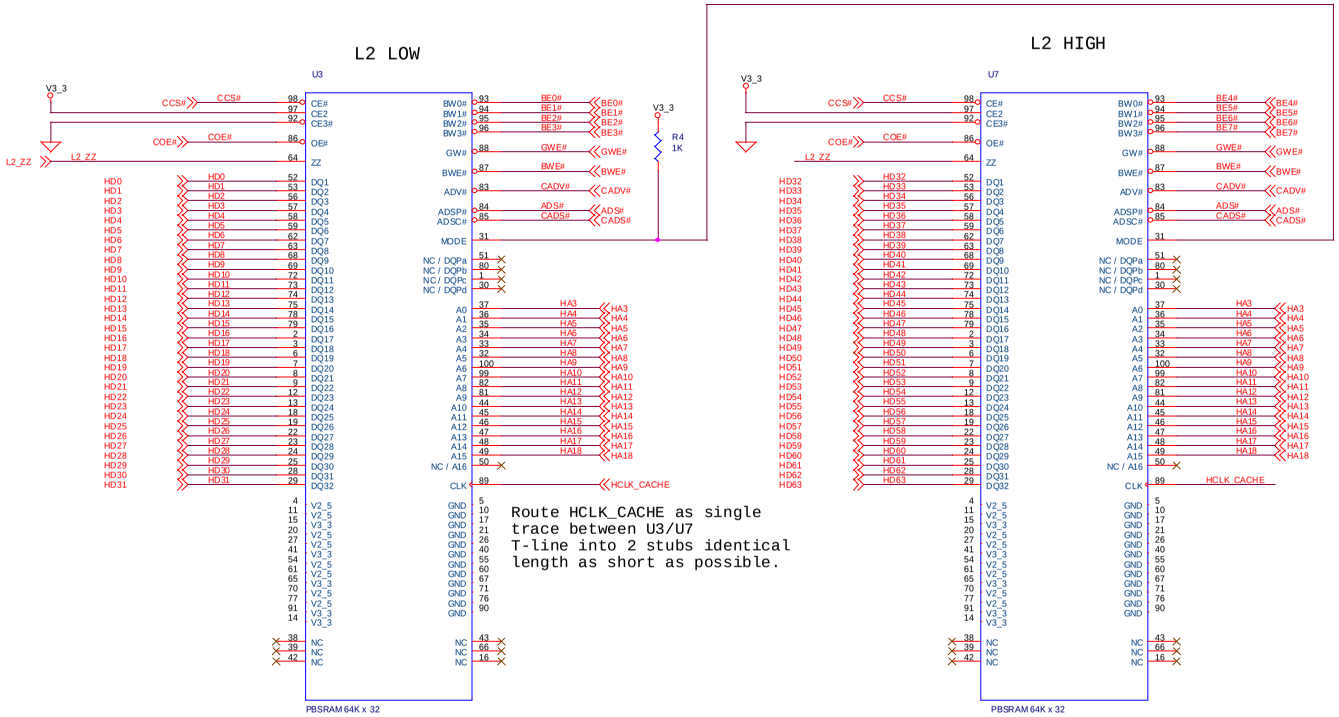


PLACE AS CLOSE AS POSSIBLE TO HIGH SRAM (U5)



L2 LOW

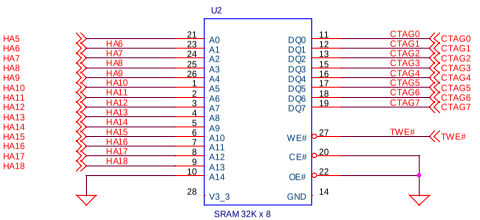
L2 HIGH



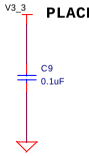
Route HCLK_CACHE as single trace between U3/U7
T-line into 2 stubs identical length as short as possible.

BSRAM V3_3 : 4,11,15,20,27,41,54,61,65,70,77,91
BSRAM GND : 5,10,17,21,26,40,55,60,65,67,71,76,90

TAGS

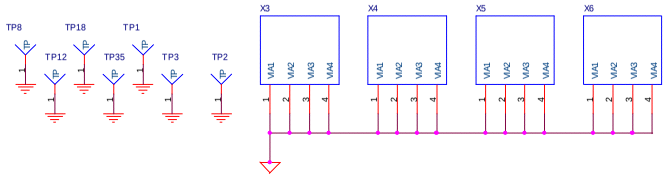


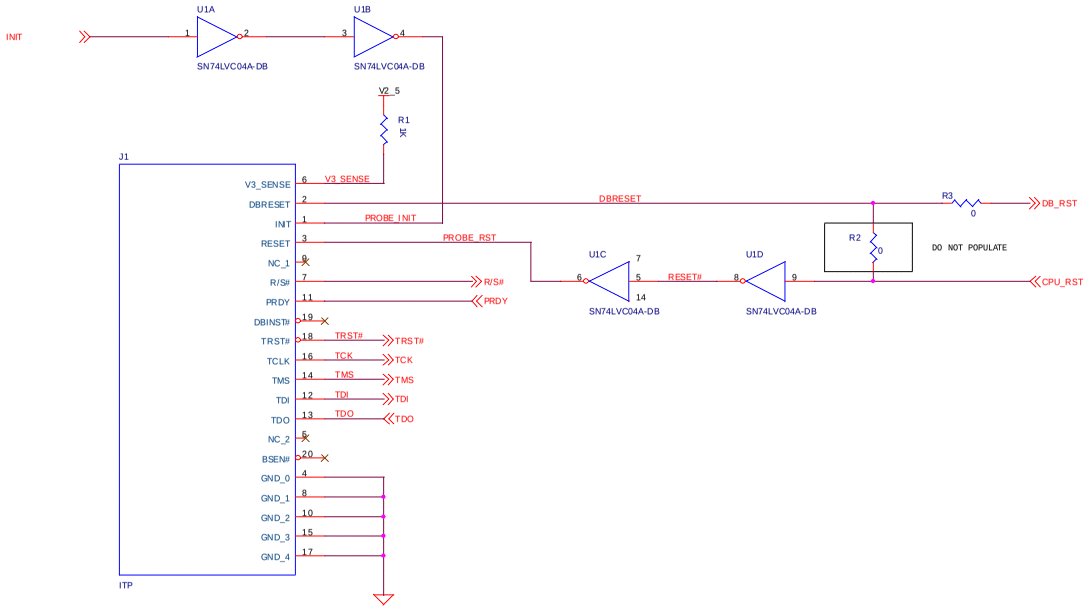
PLACE AS CLOSE AS POSSIBLE TO SRAM TAG

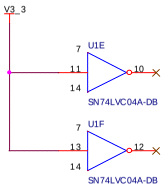


TAG V3_3: 28
TAG GND: 10,14, 20, 22

Title	Cache and Tags	
Size C	Document Number XXXX-XXX	Rev B.0
Date: Thursday, February 25, 1999	Sheet 5 of 8	

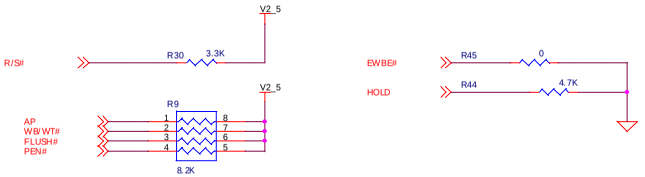




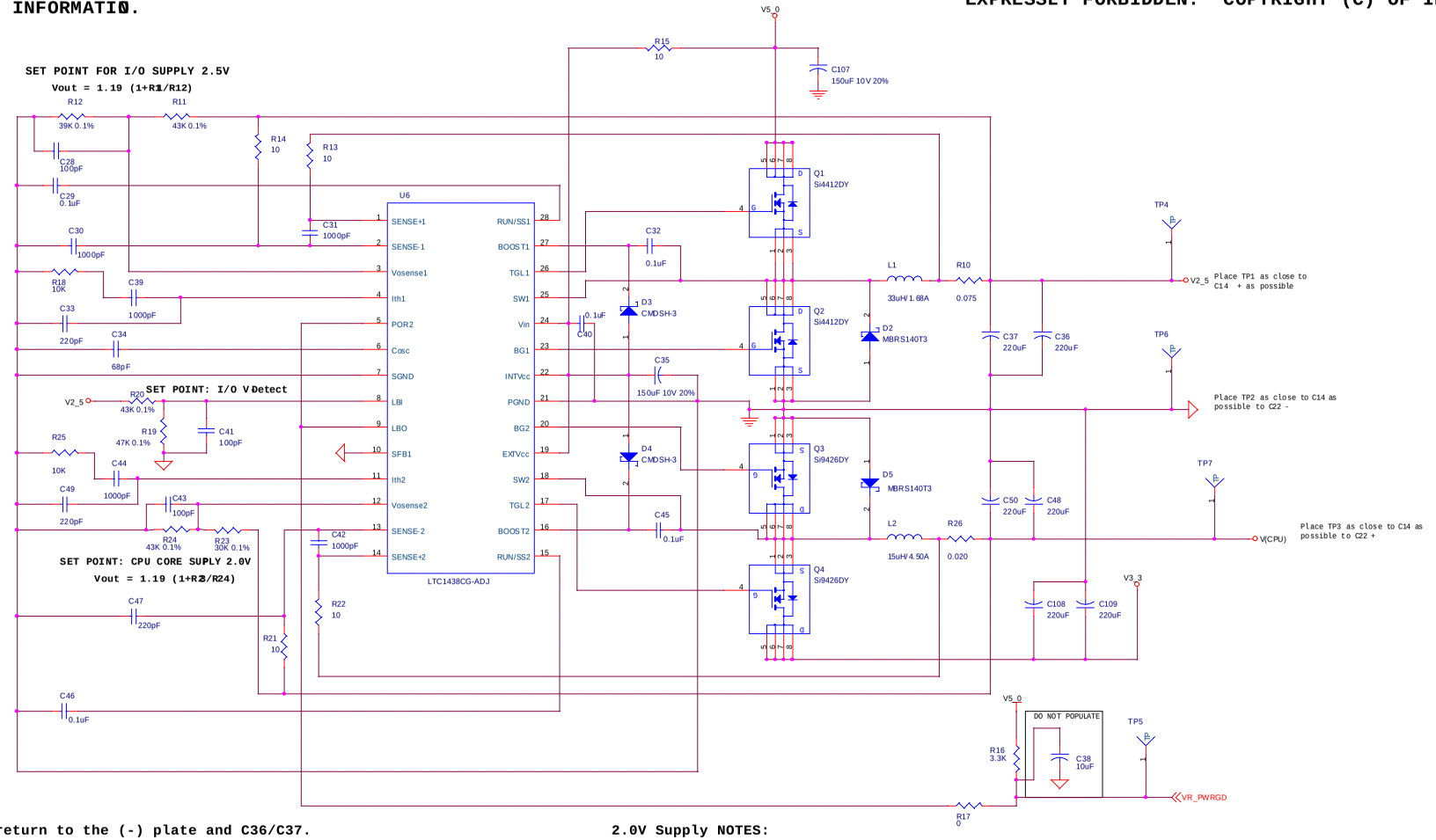


UNUSED

Processor PULLUP / PULLDOWN CONNECTIONS



Title	ITP / Strapping Options	
Size C	Document Number XXXX-XXX	Rev B.0
Date: Thursday, February 25, 1999	Sheet 7 of 8	



2.5V Supply NOTES:

1. SGND(2_5) must return to the (-) plate and C36/C37.
2. Make the power ground connects to the source of the bottom N-channel MOSFET Q2 2.5V, anode of the Schottky diode D2 2.5V, and (-) plates of C36, C37 as short lead lengths as possible.
3. The resistive divider R11/R12 must be connected between the (+) plates of C36/C37
4. Keep the following U6 trace pair routed together with minimum PC trace spacing: SENSE1+ (pin 1) and SENSE1- (pin 2)
5. Keep the (+) plate of C107 as close to the drain of the upper MOSFET (Q1) as possible. (These caps provide the AC current to the MOSFETs.)
6. Keep the switching node away from sensitive small signal nodes. Keep this node as remote as reasonably possible from U6.

2.0V Supply NOTES:

1. SGND(2_0) must return to the (-) plate and C48/C50.
2. Make the power ground connects to the source of the bottom N-channel MOSFET Q3 2.0V, anode of the Schottky diode D4 2.0V, and (-) plates of C48, C50 as short lead lengths as possible.
3. The resistive divider R23/R24 must be connected between the (+) plates of C48/C50
4. Keep the following U6 trace pair routed together with minimum PC trace spacing SENSE2+ (pin 14) and SENSE2- (pin 13)
5. Keep the (+) plates of C108/C109 as close to the drain of the upper MOSFET (Q4) as possible. (These caps provide the AC current to the MOSFETs.)
6. Keep the switching node away from sensitive small signal nodes. Keep this node as remote as reasonably possible from U6.

GENERAL NOTE:

Keep all components on this page as close as possible to U6. Components shown to the left of the symbol should be layed out to the left of the chip (these are the small signal components/ small signal side of the chip). Connect ground of these components at a single point. Done in layout as a gap in a ground plane slot that divides the chip left/right.

Title: Regulators		
Size: C	Document Number: {Doc}	Rev: B.0
Date: Thursday, February 25, 1999	Sheet 6 of 8	

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THE FOLLOWING V5_0 PINS ARE NO-CONNECTS ON THE CHASKA MODULE: G16, J18, G19, K19, J20, H21, G22, K22, H25. ONLY J39, J40, H40, G40, K40, F40 ARE USED TO SUPPLY THE 1.25A V5_0->V2_5 REGULATOR.

NOTE: PLACE ADDITIONAL GND TESTPONTS NEAR CONNECTOR TEST POINTS

Title: Connector		
Size: C	Document Number: XXXX-XXX	Rev: B.0
Date: Thursday, February 25, 1999	Sheet 8 of 8	

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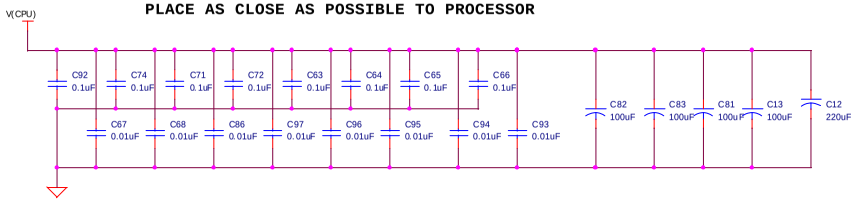
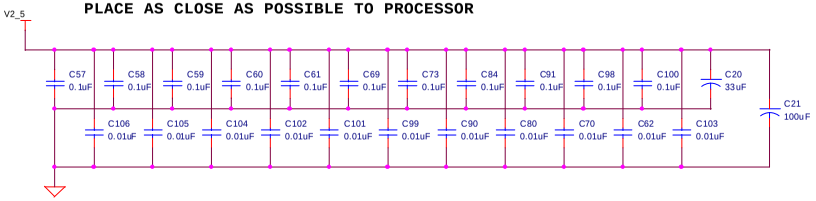
PLACE AS CLOSE AS POSSIBLE TO PROCESSOR

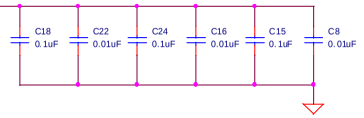


PLACE AS CLOSE AS POSSIBLE TO PROCESSOR

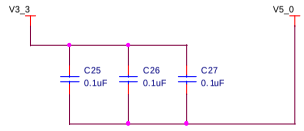


V3_3

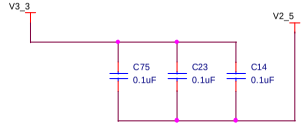
PLACE AT 400PIN CONNECTOR ACROSS 3.3V to GND PLANE.



PLACE ACROSS 3.3v TO 5.0v signal crossing.



PLACE ACROSS 3.3v TO 2.5v signal crossing.



Title: CPU Decoupling		
Size: C	Document Number: XXXX-XXX	Rev: B.0
Date: Thursday, February 25, 1999	Sheet 3 of 8	

Index