I/O Buffer Models 20

This chapter describes the 3.3 V I/O buffer models of the embedded Pentium® processor.

The first order I/O buffer model is a simplified representation of the complex input and output buffers used in the Pentium processor family. Figure 20-1 and Figure 20-2 show the structure of the input buffer model and Figure 20-3 shows the output buffer model. Table 20-1 and Table 20-2 show the parameters used to specify these models.

Although simplified, these buffer models will accurately model flight time and signal quality. For these parameters, there is very little added accuracy in a complete transistor model.

The following two models represent the input buffer models. The first model, Figure 20-1, represents all of the input buffers of the Pentium processor except for a special group of input buffers. The second model, Figure 20-2, represents these special buffers. These buffers are: AHOLD, EADS#, KEN#, WB/WT#, INV, NA#, EWBE#, BOFF#, CLK, and PICCLK.

The embedded Pentium processor supports 5 V tolerant buffers on the CLK and PICCLK pins. It is important to note that all inputs of the embedded Pentium processor with MMX™ technology are 3.3 V tolerant only. The CLK and PICCLK pins are not 5 V tolerant on the embedded Pentium processor with MMX technology.

Figure 20-1. Input Buffer Model, Except Special Group

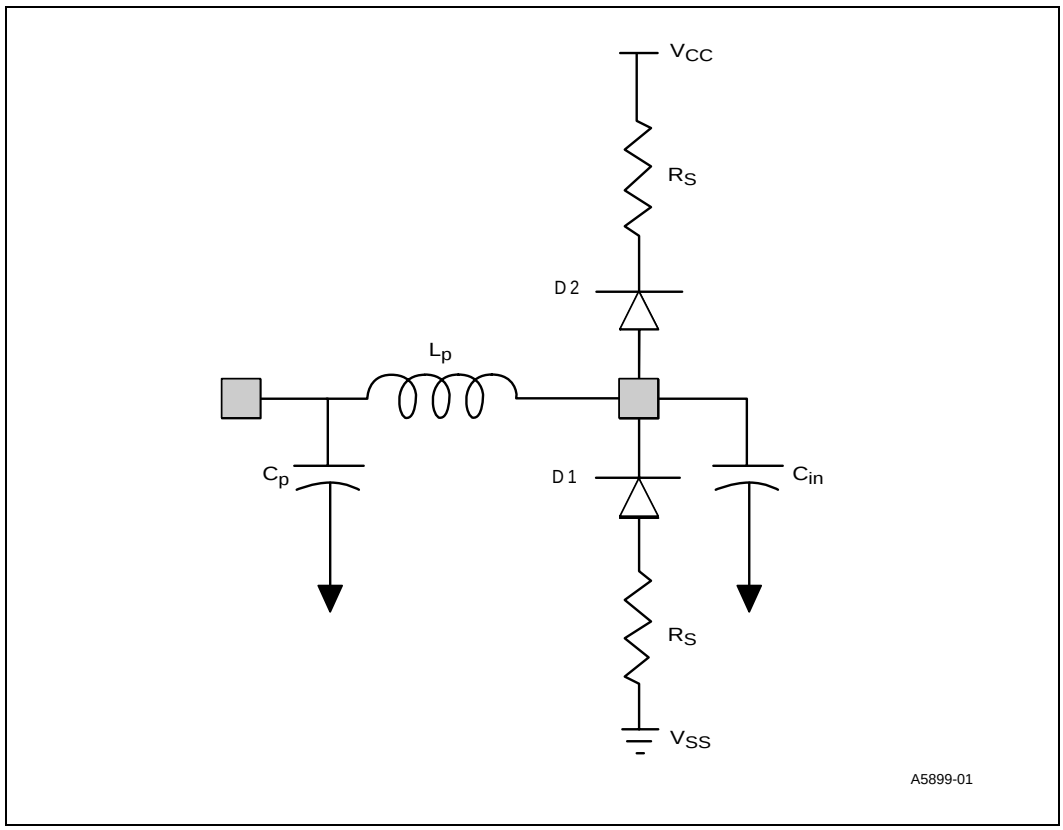


Figure 20-2. Input Buffer Model for Special Group

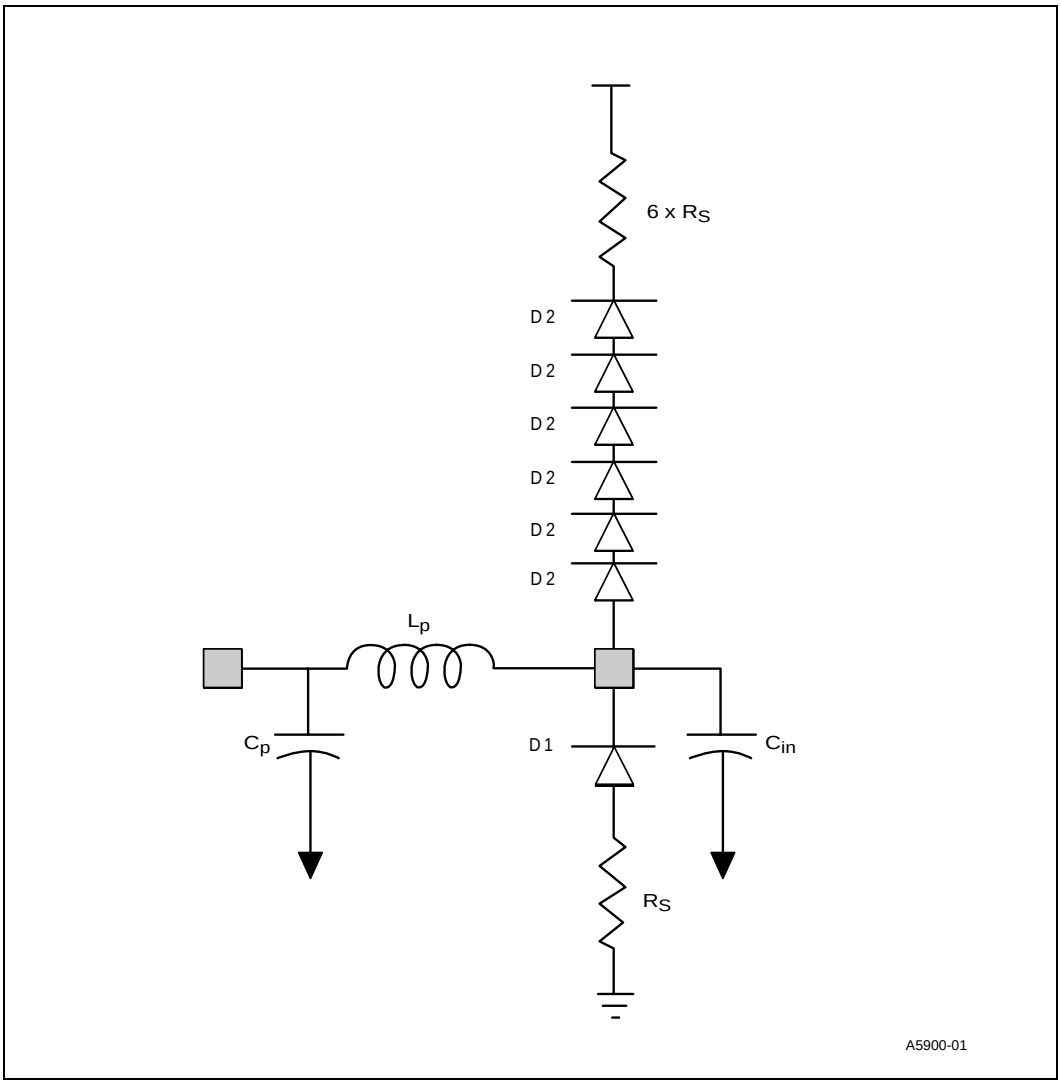


Table 20-1. Parameters Used in the Specification of the First Order Input Buffer Mode

Parameter	Description
C_{in}	Minimum and Maximum value of the capacitance of the input buffer model.
L_p	Minimum and Maximum value of the package inductance.
C_p	Minimum and Maximum value of the package capacitance.
R_s	Diode Series Resistance
D1, D2	Ideal Diodes

Figure 20-3 shows the structure of the output buffer model. This model is used for all of the output buffers of the Pentium processor.

Figure 20-3. First Order Output Buffer Model

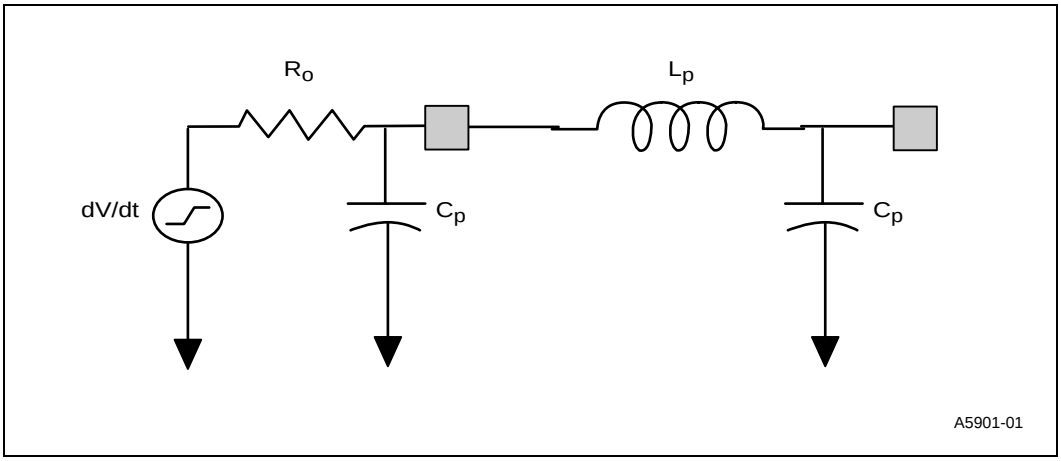


Table 20-2. Parameters Used in the Specification of the First Order Output Buffer Mode

Parameter	Description
dV/dt	Minimum and maximum value of the rate of change of the open circuit voltage source used in the output buffer model.
R_o	Minimum and maximum value of the output impedance of the output buffer model.
C_o	Minimum and Maximum value of the capacitance of the output buffer model.
L_p	Minimum and Maximum value of the package inductance.
C_p	Minimum and Maximum value of the package capacitance.

In addition to the input and output buffer parameters, input protection diode models are provided for added accuracy. These diodes have been optimized to provide ESD protection and provide some level of clamping. Although the diodes are not required for simulation, it may be more difficult to meet specifications without them.

Note however, that some signal quality specifications require that the diodes be removed from the input model. The series resistors (Rs) are a part of the diode model. Remove these when removing the diodes from the input model.

20.1 Buffer Model Parameters

This section gives the parameters for each Pentium processor input, output, and bidirectional signals, and the settings for the configurable buffers.

In dual processor mode, a few signals change from output signals to I/O signals. These signals are: ADS#, M/IO#, D/C#, W/R#, LOCK#, CACHE#, SCYC, HLDA, HIT#, and HITM#. When simulating these signals use the correct operation of the buffer while in DP mode.

Some pins on the processor have selectable buffer sizes to allow for faster switching of the buffer in heavily loaded environments. The buffer selection is done through the setting of configuration pins at power on RESET. Once selected, these cannot be changed without a power on RESET. The

BUSCHK# and BRDYC# pins are used to select the different buffer size. All configurable pins get set to the selected buffer size. There is no selection for specific signal groups to get specific buffers. Keep in mind that the largest buffer size is not always the best selection especially in a lightly loaded environment. AC timing and signal quality simulations should be done to ensure that the buffers used meet required timing and signal quality specifications for the components that will be used in the specific board design.

The pins with selectable buffer sizes use the configurable output buffer EB2. Table 20-3 shows the drive level required at falling edge of RESET, to select the buffer strength. Once selected, the buffer size cannot be changed without a power on RESET. The buffer sizes selected should be the appropriate size required, otherwise AC timings might not be met, or too much overshoot and ringback may occur. There are no other selection choices, all the configurable buffers get set to the same size at the same time.

Table 20-3 shows the proper settings on BRDYC# and BUSCHK# for proper buffer size selection.

Table 20-3. Buffer Selection Chart

Environment	BRDYC#	BUSCHK#	Buffer Selection
Typical Stand Alone Component	1	X	EB2
Loaded Component	0	1	EB2A
Heavily Loaded Component	0	0	EB2B

NOTE: X is a “don’t care” (0 or 1). Please refer to Table 20-4 for the groupings of the buffers

Table 20-4. Signal to Buffer Type

Signals	Type	Driver Buffer Type	Receiver Buffer Type
CLK	I		ER0
A20M#, AHOLD, BF1–BF0, BOFF#, BRDY#, BRDYC#, BUSCHK#, EADS#, EWBE#, FLUSH#, FRCMC#[2], HOLD, IGNNE#, INIT, INTR, INV, KEN#, NA#, NMI, PEN#, PICCLK, R/S#, RESET, SMI#, STPCLK#, TCK, TDI, TMS, TRST#, WB/WT#	I		ER1
ADSC#, APCHK#, BE7#–BE5#, BP3–BP2, BREQ, FERR#, IERR#, PCD, PCHK#, PM0/BP0, PM1/BP1, PRDY, PWT, SMIACT#, TDO, D/P#	O	ED1	
A31–A21, AP, BE4#–BE0#, CACHE#, D/C#, D63–D0, DP7–DP0, HLDA, LOCK#, M/IO#, PBGNT#, PBREQ#, PHIT#, PHITM#, SCYC	I/O	EB1	EB1
A20–A3, ADS#, HITM#, W/R#	I/O	EB2/A/B	EB2
HIT#	I/O	EB3	EB3
PICD0, PICD1	I/O	EB4	EB4

NOTES:
1. VCC2DET# has no buffer model – it is simply a short to V_{SS} on the embedded Pentium® processor with MMX™ technology . This pin is an INC on the embedded Pentium processor.
2. FRCMC# is defined only for the embedded Pentium processor.

The input, output and bidirectional buffers values are listed in Table 20-5. Table 20-5 contains listings for all three types; do not get them confused during simulation. When a bidirectional pin is operating as an input, just use the C_{in}, C_p and L_p values, if it is operating as a driver use all the data parameters.

Table 20-5. Input, Output and Bidirectional Buffer Model Parameters

Buffer Type	Transition	dV/dt (V/nsec)		Ro (Ohms)		Cp (pF)		Lp (nH)		Co/Cin (pF)	
		min	max	min	max	min	max	min	max	min	max
ER0	Rising					3.0	5.0	4.0	7.2	0.8	1.2
(input)	Falling					3.0	5.0	4.0	7.2	0.8	1.2
ER1	Rising					1.1	6.1	4.7	15.3	0.8	1.2
(input)	Falling					1.1	6.1	4.7	15.3	0.8	1.2
ED1	Rising	3/3.0	3.7/0.9	21.6	53.1	1.1	8.2	4.0	17.7	2.0	2.6
(output)	Falling	3/2.8	3.7/0.8	17.5	50.7	1.1	8.2	4.0	17.7	2.0	2.6
EB1	Rising	3/3.0	3.7/0.9	21.6	53.1	1.3	8.7	4.0	18.7	2.0	2.6
(bidir)	Falling	3/2.8	3.7/0.8	17.5	50.7	1.3	8.7	4.0	18.7	2.0	2.6
EB2	Rising	3/3.0	3.7/0.9	21.6	53.1	1.3	8.3	4.4	16.7	9.1	9.7
(bidir)	Falling	3/2.8	3.7/0.8	17.5	50.7	1.3	8.3	4.4	16.7	9.1	9.7
EB2A	Rising	3/2.4	3.7/0.9	10.1	22.4	1.3	8.3	4.4	16.7	9.1	9.7
(bidir)	Falling	3/2.4	3.7/0.9	9.0	21.2	1.3	8.3	4.4	16.7	9.1	9.7
EB2B	Rising	3/1.8	3.7/0.7	5.5	12.9	1.3	8.3	4.4	16.7	9.1	9.7
(bidir)	Falling	3/1.8	3.7/0.7	4.6	12.3	1.3	8.3	4.4	16.7	9.1	9.7
EB3	Rising	3/3.0	3.7/0.9	21.6	53.1	1.9	7.5	9.9	14.3	3.3	3.9
(bidir)	Falling	3/2.8	3.7/0.8	17.5	50.7	1.9	7.5	9.9	14.3	3.3	3.9
EB4	Rising	3/3.0	3.7/0.9	100K†	100K†	2.0	6.9	5.8	14.6	5.0	7.0
(bidir)	Falling	3/2.8	3.7/0.8	17.5	50.7	2.0	6.9	5.8	14.6	5.0	7.0

† The buffer is an open drain. For simulation purposes it should be modeled by a very large internal resistor with an additional external pull-up.

Table 20-6. Input Buffer Model Parameters: D (Diodes)

Symbol	Parameter	D1	D2
IS	Saturation Current	1.4e–14 A	2.78e–16 A
N	Emission Coefficient	1.19	1.00
RS	Series Resistance	6.5 ohms	6.5 ohms
TT	Transit Time	3 ns	6 ns
VJ	PN Potential	0.983 V	0.967 V
CJ0	Zero Bias PN Capacitance	0.281 pF	0.365 pF
M	PN Grading Coefficient	0.385	0.376

20.2 Signal Quality Specifications

Signals driven by the system into the Pentium processor must meet signal quality specifications to guarantee that the components read data properly and to ensure that incoming signals do not affect the reliability of the component. There are two signal quality parameters: Ringback and Settling Time. For more information, see “CLK/PICCLK Signal Quality Specification for the Pentium® Processor with MMX™ Technology” on page 20-374.

20.2.1 Ringback

Excessive ringback can contribute to long-term reliability degradation of the Pentium processor, and can cause false signal detection. Ringback is simulated at the input pin of a component using the input buffer model. Ringback can be simulated with or without the diodes that are in the input buffer model.

Ringback is the absolute value of the maximum voltage at the receiving pin below V_{CC} (or above V_{SS}) relative to V_{CC} (or V_{SS}) level after the signal has reached its maximum voltage level. The input diodes are assumed present.

- Maximum Ringtrack on Inputs = 0.8 V (with diodes)

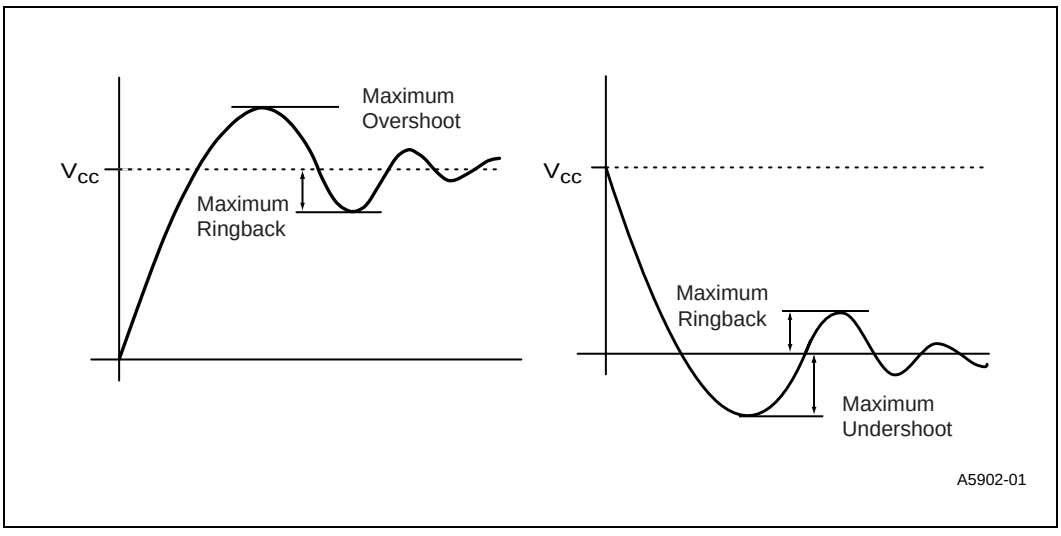
If simulated without the input diodes, follow the Maximum Overshoot/Undershoot specification. By meeting the overshoot/undershoot specification, the signal is guaranteed not to ringback excessively.

If simulated with the diodes present in the input model, follow the maximum ringback specification.

Overshoot (Undershoot) is the absolute value of the maximum voltage above V_{CC} (below V_{SS}). The guideline assumes the absence of diodes on the input.

- Maximum Overshoot/Undershoot on 3.3 V Pentium processor Inputs (including CLK and PICCLK) = 1.4 V above V_{CC3} (without diodes)

Figure 20-4. Overshoot/Undershoot and Ringback Guidelines



20.2.2 Settling Time

The settling time is defined as the time a signal requires at the receiver to settle within 10% of V_{CC} or V_{SS}. Settling time is the maximum time allowed for a signal to reach within 10% of its final value.

Most available simulation tools are unable to simulate settling time so that it accurately reflects silicon measurements. On a physical board, second-order effects and other effects serve to dampen the signal at the receiver. Because of all these concerns, settling time is a recommendation or a tool for layout tuning and not a specification.

Settling time is simulated at the slow corner, to make sure that there is no impact on the flight times of the signals if the waveform has not settled. Settling time may be simulated with the diodes included or excluded from the input buffer model. If diodes are included, settling time recommendation will be easier to meet.

Although simulated settling time has not shown good correlation with physical, measured settling time, settling time simulations can still be used as a tool to tune layouts.

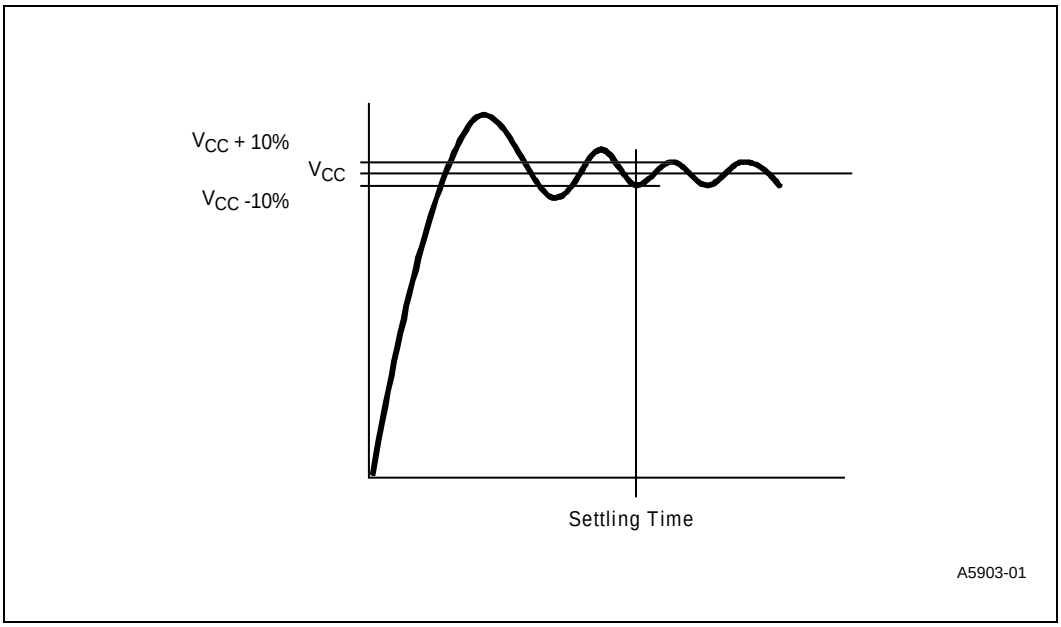
Use the following procedure to verify board simulation and tuning with concerns for settling time.

1. Simulate settling time at the slow corner for a particular signal.
2. If settling time violations occur, simulate signal trace with DC diodes in place at the receiver pin. The DC diode behaves almost identically to the actual (non-linear) diode on the part as long as excessive overshoot does not occur.
3. If settling time violations still occur, simulate flight times for five consecutive cycles for that particular signal.
4. If flight time values are consistent over the five simulations, settling time should not be a concern. If however, flight times are not consistent over the five simulations, tuning of the layout is required.

Note that, for signals that are allocated two cycles for flight time, the recommended settling time is doubled.

Maximum Settling Time to within 10% of V_{CC} is: 12.5 ns @66 MHz.

Figure 20-5. Settling Time



20.2.3 CLK/PICCLK Signal Quality Specification for the Pentium® Processor with MMX™ Technology

The maximum overshoot, maximum undershoot, overshoot threshold duration, undershoot threshold duration, and maximum ringback specifications for CLK/PICCLK are described below:

Maximum Overshoot And Maximum Undershoot Specification: The maximum overshoot of the CLK/PICCLK signals should not exceed V_{CC3}, nominal +0.9 V. The maximum undershoot of the CLK/PICCLK signals must not drop below –0.9 V.

Overshoot Threshold Duration Specification: The overshoot threshold duration is defined as the sum of all time during which the CLK/PICCLK signal is above V_{CC3}, nominal +0.5 V within a single clock period. The overshoot threshold duration must not exceed 20% of the period.

Undershoot Threshold Duration Specification: The undershoot threshold duration is defined as the sum of all time during which the CLK/PICCLK signal is below –0.5 V within a single clock period. The undershoot threshold duration must not exceed 20% of the period.

Maximum Ringback Specification: The maximum ringback of CLK/PICCLK associated with their high states (overshoot) must not drop below V_{CC3} –0.8 V as shown in Figure 20-7. Similarly, the maximum ringback of CLK/PICCLK associated with their low states (undershoot) must not exceed 0.8 V as shown in Figure 20-9.

Refer to Table 20-7 and Table 20-8 for a summary of the clock overshoot and undershoot specifications for the embedded Pentium processor with MMX technology.

Table 20-7. Overshoot Specification Summary

Specification Name	Value	Units	Notes
Threshold Level	V_{CC3}, nominal +0.5	V	(1) (2)
Maximum Overshoot Level	V_{CC3}, nominal +0.9	V	(1) (2)
Maximum Threshold Duration	20% of clock period above threshold voltage	ns	(2)
Maximum Ringback	V_{CC3}, nominal –0.8	V	(1) (2)

NOTES:
1. V_{CC3}, nominal refers to the voltage measured at the bottom side of the V_{CC3} pins.
2. See Figure 20-6 and Figure 20-7.

Table 20-8. Undershoot Specification Summary

Specification Name	Value	Units	Notes
Threshold Level	–0.5	V	(1)
Minimum Undershoot Level	–0.9	V	(1)
Maximum Threshold Duration	20% of clock period below threshold voltage	ns	(1)
Maximum Ringback	0.8	V	(1)

NOTE:
1. See Figure 20-8 and Figure 20-9.

20.2.3.1 Clock Signal Measurement Methodology

The waveform of the clock signals should be measured at the bottom side of the processor pins using an oscilloscope with a 3 dB bandwidth of at least 20 MHz (100 ms/s digital sampling rate). There should be a short isolation ground lead attached to a processor pin on the bottom side of the board. A 1 MOhm probe with loading of less than 1 pF (e.g., Tektronics 6243 or Tektronics 6245) is recommended. The measurement should be taken at the CLK (AK18) and PICCLK (H34) pins and their nearest V_{SS} pins (AM18 and H36, respectively).

Maximum Overshoot, Maximum Undershoot And Maximum Ringback Specifications: The display should show continuous sampling (e.g., infinite persistence) of the waveform at 500 mV/div and 5 ns/div (for CLK) or 20 ns/div (for PICCLK) for a recommended duration of approximately five seconds. Adjust the vertical position to measure the maximum overshoot and associated ringback with the largest possible granularity. Similarly, readjust the vertical position to measure the maximum undershoot and associated ringback. There is no allowance for crossing the maximum overshoot, maximum undershoot or maximum ringback specifications.

Overshoot Threshold Duration Specification: A snapshot of the clock signal should be taken at 500 mV/div and 500 ps/div (for CLK) or 2 ns/div (for PICCLK). Adjust the vertical position and horizontal offset position to view the threshold duration. The overshoot threshold duration is defined as the sum of all time during which the clock signal is above V_{CC3}, nominal +0.5 V within a single clock period. The overshoot threshold duration must not exceed 20% of the period.

Undershoot Threshold Duration Specification: A snapshot of the clock signal should be taken at 500 mV/div and 500 ps/div (for CLK) or 2 ns/div (for PICCLK). Adjust the vertical position and horizontal offset position to view the threshold duration. The undershoot threshold duration is defined as the sum of all time during which the clock signal is below –0.5 V within a single clock period. The undershoot threshold duration must not exceed 20% of the period.

These overshoot and undershoot specifications are illustrated in Figures 20-6 to 20-9.

Figure 20-6. Maximum Overshoot Level, Overshoot Threshold Level, and Overshoot Threshold Duration

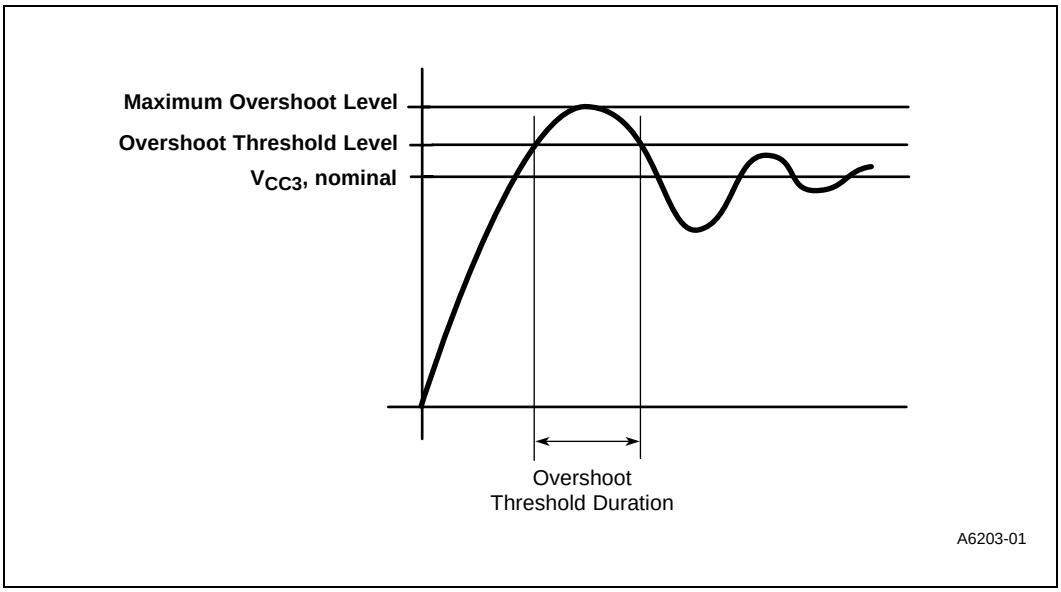


Figure 20-7. Maximum Ringback Associated with the Signal High State

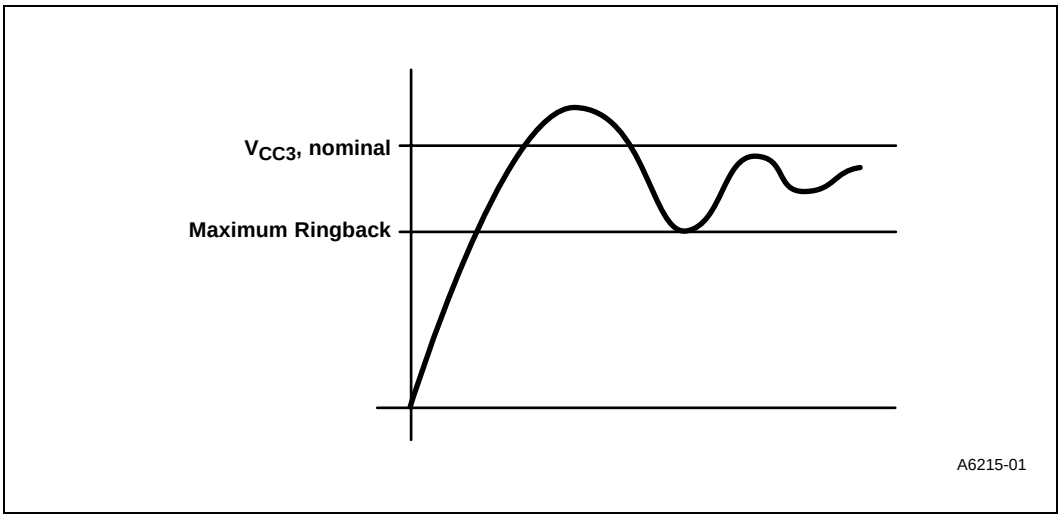


Figure 20-8. Maximum Undershoot Level, Undershoot Threshold Level, and Undershoot Threshold Duration

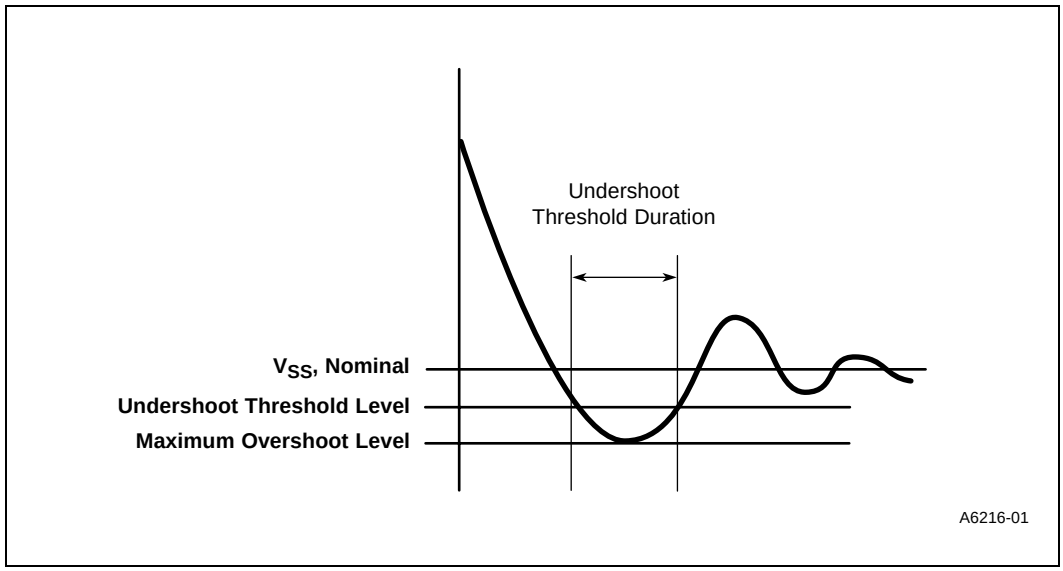


Figure 20-9. Maximum Ringback Associated with the Signal Low State