4.0 Embedded Pentium® Processor With Voltage Reduction Technology Packaging Information

4.1 Differences from the Pentium Processor

To better streamline the processor for embedded applications, the following features have been eliminated from the embedded Pentium processor with voltage reduction technology: Upgrade, Dual Processing (DP), APIC and Master/Checker functional redundancy. Table 22 lists the corresponding pins that exist on the SPGA 3.3-V Pentium processor but have been removed from the embedded Pentium processor with voltage reduction technology.

Table 22. Signals Removed from the Pentium® Processor with Voltage Reduction Technology

| Signal	Function
ADSC#	**Additional Address Status.** This signal is mainly used for large or standalone L2 cache memory subsystem support required for high-performance desktop or server models.
BRDYC#	**Additional Burst Ready.** This signal is mainly used for large or standalone L2 cache memory subsystem support required for high-performance desktop or server models.
CPUTYP	**CPU Type.** This signal is used for dual processing systems.
D/P#	**Dual/Primary processor identification.** This signal is only used for an upgrade processor.
FRCMC#	**Functional Redundancy Checking.** This signal is only used for error detection via processor redundancy, and requires two Pentium processors (master/checker).
PBGNT#	**Private Bus Grant.** This signal is only used for dual processing systems.
PBREQ#	**Private Bus Request.** This signal is used only for dual processing systems.
PHIT#	**Private Hit.** This signal is only used for dual processing systems.
PHITM#	**Private Modified Hit.** This signal is only used for dual processing systems.
PICCLK	**APIC Clock.** This signal is the APIC interrupt controller serial data bus clock.
PICD0 [DPEN#]	**APIC's Programmable Interrupt Controller Data line 0.** PICD0 shares a pin with DPEN# (Dual Processing Enable).
PICD1 [APICEN]	**APIC's Programmable Interrupt Controller Data line 1.** PICD1 shares a pin with APICEN (APIC Enable (on RESET)).

4.2 Pinout

The embedded Pentium processor with voltage reduction technology package has a pin array that is mechanically identical to the SPGA version of the 3.3-V Pentium processor, but some pins need to be connected differently. Table 22 lists the SPGA embedded Pentium processor with voltage reduction technology pins that are different from the SPGA 3.3-V Pentium processor.

The signals listed in Table 22 are now No Connect pins on the embedded Pentium processor with voltage reduction technology. Leave these pins unconnected. Table 25 includes the list of NC pins. Connection of these pins may result in component failure or incompatibility with processor steppings.

Note: The V_{CC2} pins are 3.1 V for the SPGA embedded Pentium processor with voltage reduction technology.

Figure 14 is the pin side SPGA pinout diagram. For a brief functional description of the pins, refer to Table 26. Additional Input and Output pin information is provided in Table 27, Table 28, and Table 29.

Figure 14. SPGA Pentium® Processor with Voltage Reduction Technology Pinout (Top Side View)

Figure 15. SPGA Pentium® Processor with Voltage Reduction Technology Pinout (Pin Side View)

A6056-01
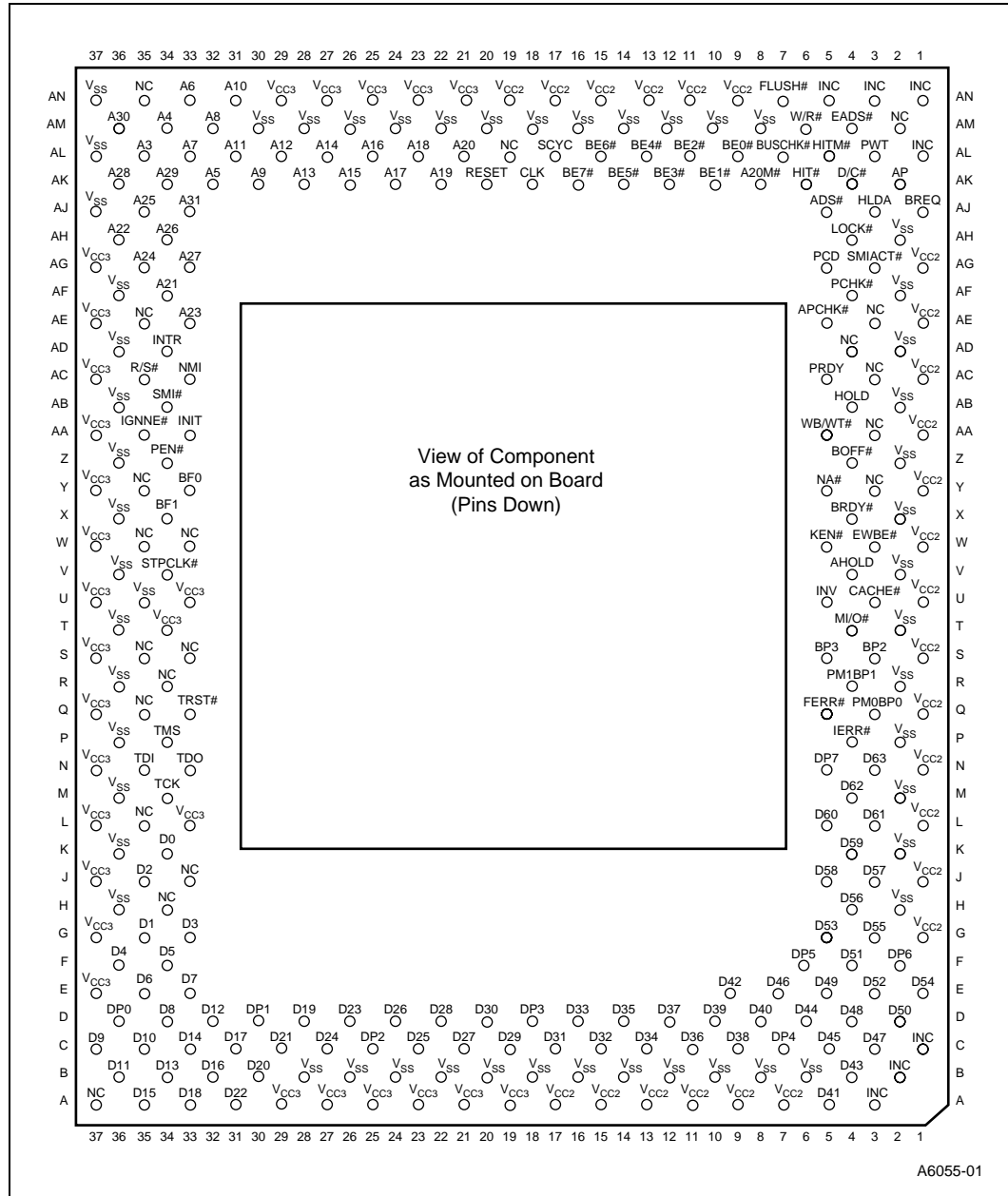
4.2.1 Pin Cross Reference

Table 23. Pin Cross-Reference by Pin Name — Address and Data Pins

Pin	Location	Pin	Location	Pin	Location	Pin	Location	Pin	Location
Address									
A3	AL35	A9	AK30	A15	AK26	A21	AF34	A27	AG33
A4	AM34	A10	AN31	A16	AL25	A22	AH36	A28	AK36
A5	AK32	A11	AL31	A17	AK24	A23	AE33	A29	AK34
A6	AN33	A12	AL29	A18	AL23	A24	AG35	A30	AM36
A7	AL33	A13	AK28	A19	AK22	A25	AJ35	A31	AJ33
A8	AM32	A14	AL27	A20	AL21	A26	AH34		
Data									
D0	K34	D13	B34	D26	D24	D39	D10	D52	E03
D1	G35	D14	C33	D27	C21	D40	D08	D53	G05
D2	J35	D15	A35	D28	D22	D41	A05	D54	E01
D3	G33	D16	B32	D29	C19	D42	E09	D55	G03
D4	F36	D17	C31	D30	D20	D43	B04	D56	H04
D5	F34	D18	A33	D31	C17	D44	D06	D57	J03
D6	E35	D19	D28	D32	C15	D45	C05	D58	J05
D7	E33	D20	B30	D33	D16	D46	E07	D59	K04
D8	D34	D21	C29	D34	C13	D47	C03	D60	L05
D9	C37	D22	A31	D35	D14	D48	D04	D61	L03
D10	C35	D23	D26	D36	C11	D49	E05	D62	M04
D11	B36	D24	C27	D37	D12	D50	D02	D63	N03
D12	D32	D25	C23	D38	C09	D51	F04		

Table 24. Pin Cross-Reference by Pin Name — Control Pins

Pin	Location	Pin	Location	Pin	Location	Pin	Location
A20M#	AK08	NC	Y03	FLUSH#	AN07	PEN#	Z34
ADS#	AJ05	BREQ	AJ01	HIT#	AK06	PM0/BP0	Q03
NC	AM02	BUSCHK#	AL07	HITM#	AL05	PM1/BP1	R04
AHOLD	V04	CACHE#	U03	HLDA	AJ03	PRDY	AC05
AP	AK02	NC	Q35	HOLD	AB04	PWT	AL03
APCHK#	AE05	D/C#	AK04	IERR#	P04	R/S#	AC35
BE0#	AL09	NC	AE35	IGNNE#	AA35	RESET	AK20
BE1#	AK10	DP0	D36	INIT	AA33	SCYC	AL17
BE2#	AL11	DP1	D30	INTR/LINT0	AD34	SMI#	AB34
BE3#	AK12	DP2	C25	INV	U05	SMIACT#	AG03
BE4#	AL13	DP3	D18	KEN#	W05	TCK	M34
BE5#	AK14	DP4	C07	LOCK#	AH04	TDI	N35
BE6#	AL15	DP5	F06	M/IO#	T04	TDO	N33
BE7#	AK16	DP6	F02	NA#	Y05	TMS	P34
BOFF#	Z04	DP7	N05	NMI/LINT1	AC33	TRST#	Q33
BP2	S03	EADS#	AM04	PCD	AG05	W/R#	AM06
BP3	S05	EWBE#	W03	PCHK#	AF04	WB/WT#	AA05
BRDY#	X04	FERR#	Q05				
Clock Control							
CLK	AK18	BF0	Y33	BF1	Y35	STPCLK#	V34

Table 25. No Connect, Power and Ground Pins

V_{CC2}[1]				
A07	A17	Q01	AA01	AN19
A09	G01	S01	AC01	AN15
A11	J01	U01	AE01	AG01
A13	L01	W01	AN11	AN09
A15	N01	Y01	AN13	AN17
V_{CC3}				
A19	AA37	AN25	L33	U33
A21	AC37	AN27	L37	U37
A23	AE37	AN29	N37	W37
A25	AG37	E37	Q37	Y37
A27	AN21	G37	S37	
A29	AN23	J37	T34	
No Connect (NC)[2]				
A37	AE03	AN35	Q35	W33
AA03	AE35	H34	R34	W35
AC03	AL19	J33	S33	Y03
AD04	AM02	L35	S35	

NOTE:
1. These V_{CC2} pins are 3.3-V V_{CC} pins for the SPGA 3.3-V Pentium® processor. For the SPGA embedded Pentium processor with voltage reduction technology, these pins are 3.1-V V_{CC2} supplies for the SPGA core.
2. These NC pins should be left unconnected. Connection of these pins may result in component failure or incompatibility with processor steppings.

4.2.2   Design Notes

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC3}. Unused active high inputs should be connected to GND (V_{SS}).

No Connect (NC) pins must remain unconnected. Connection of NC pins may result in component failure or incompatibility with processor steppings.

4.2.3   Pin Quick Reference

This section gives a brief functional description of each pin. For a detailed description, see the "Hardware Interface" chapter in the *Embedded Pentium® Processor Family Developer's Manual* (order number 273204). Note that all input pins must meet their AC/DC specifications to guarantee proper functional behavior.

The # symbol at the end of a signal name indicates that the active or asserted state occurs when the signal is at a low voltage. When a # symbol is not present after the signal name, the signal is active, or asserted at the high voltage level.

Table 26. Pin Quick Reference

Symbol	Type	Function
A20M#	I	When the **address bit 20 mask** pin is asserted, the Pentium® processor emulates the address wraparound at 1 Mbyte that occurs on the 8086. When A20M# is asserted, the processor masks physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode.
A31–A3	I/O	As outputs, the **address** lines of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31–A5.
ADS#	O	The **address status** indicates that a new valid bus cycle is currently being driven by the processor.
AHOLD	I	In response to the assertion of **address hold**, the processor will stop driving the address lines (A31-A3), and AP in the next clock. The rest of the bus will remain active so data can be returned or driven for previously issued bus cycles.
AP	I/O	**Address parity** is driven by the processor with even parity information on all processor generated cycles in the same clock in which the address is driven. Even parity must be driven back to the processor during inquire cycles on this pin in the same clock as EADS# to ensure that the correct parity check status is indicated.
APCHK#	O	The **address parity check** status pin is asserted two clocks after EADS# is sampled active if the processor has detected a parity error on the address bus during inquire cycles. APCHK# will remain active for one clock each time a parity error is detected.
BE7#–BE5# BE4#–BE0#	O I/O	The **byte enable** pins are used to determine which bytes must be written to external memory, or which bytes were requested by the processor for the current cycle. The byte enables are driven in the same clock as the address lines (A31–A3).
BF1–BF0	I	**Bus Frequency** determines the bus-to-core ratio. The bus frequency pins are sampled at RESET, and cannot be changed until another non-warm (1 ms) assertion of RESET. Additionally, BF must not change values while RESET is active. For proper operation of the embedded Pentium processor with voltage reduction technology, the BF1 pin should be strapped high, and the BF0 pin should be strapped low. This sets the bus-to-core ratio at 1/2. Other combinations are reserved.
BOFF#	I	The **backoff** input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the processor will float all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time the processor restarts the aborted bus cycle(s) in their entirety.
BP3–BP2 PM1/BP1– PM0/BP0	O	The **breakpoint** pins (BP3–BP0) correspond to the debug registers, DR3–DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the **performance monitoring** pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
BRDY#	I	The **burst ready** input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the processor data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states.
BREQ	O	The **bus request** output indicates to the external system that the processor has internally generated a bus request. This signal is always driven whether or not the processor is driving its bus.

Table 26. Pin Quick Reference

Symbol	Type	Function
BUSCHK#	I	The **bus check** input allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the processor will latch the address and control signals in the machine check registers. If, in addition, the MCE bit in CR4 is set, the processor will vector to the machine check exception.
CACHE#	O	For processor-initiated cycles, the **cache** pin indicates internal cacheability of the cycle (if a read), and indicates a burst writeback cycle (if a write). If this pin is driven inactive during a read cycle, the processor does not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).
CLK	I	The **clock** input provides the fundamental timing for the processor. Its frequency is the operating frequency of the processor's external bus and requires TTL levels. All external timing parameters except TDI, TDO, TMS, and TRST# are specified with respect to the rising edge of CLK. It is recommended that CLK begin 150 ms after V_{CC} reaches its proper operating level. This recommendation is only to assure the long term reliability of the device.
D/C#	O	The **data/code** output is one of the primary bus cycle definition pins. It is driven valid in the same clock in which the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.
D63–D0	I/O	These are the 64 **data lines** for the processor. Lines D7–D0 define the least significant byte of the data bus; lines D63–D56 define the most significant byte of the data bus. When the processor is driving the data lines, they are driven during the T2, T12 or T2P clocks for that cycle. During reads, the processor samples the data bus when BRDY# is returned.
DP7–DP0	I/O	These are the **data parity** pins for the processor. There is one for each byte of the data bus. They are driven by the processor with even parity information on writes in the same clock as write data. Even parity information must be driven back to the embedded Pentium processor with voltage reduction technology on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the processor. DP7 applies to D63–D56; DP0 applies to D7–D0.
EADS#	I	This signal indicates that a valid **external address** has been driven onto the processor address pins to be used for an inquire cycle.
EWBE#	I	The **external write buffer empty** input, when inactive (high), indicates that a write cycle is pending in the external system. When the processor generates a write and EWBE# is sampled inactive, the processor will hold off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# being active.
FERR#	O	The **floating-point error** pin is driven active when an unmasked floating-point error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using DOS-type floating-point error reporting.
FLUSH#	I	When asserted, the **cache flush** input forces the processor to write back all modified lines in the data cache and invalidate its internal caches. A Flush Acknowledge special cycle is generated by the processor indicating completion of the writeback and invalidation. If FLUSH# is sampled low when RESET transitions from high to low, three-state test mode is entered.
HIT#	O	The **hit** indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either the data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. If the inquire cycle misses the cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.

Table 26. Pin Quick Reference

Symbol	Type	Function
HITM#	O	The **hit to a modified line** output is driven to reflect the outcome of an inquire cycle. It is asserted after an inquire cycle that results in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.
HLDA	O	The **bus hold acknowledge** pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the processor has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA is driven inactive and the processor resumes driving the bus. If the processor has a bus cycle pending, it will be driven in the same clock in which HLDA is deasserted.
HOLD	I	In response to the **bus hold request**, the processor will float most of its output and input/output pins and assert HLDA after completing all outstanding bus cycles. The processor will maintain its bus in this state until HOLD is deasserted. HOLD is not recognized during LOCK cycles. The processor will recognize HOLD during reset.
IERR#	O	The **internal error** pin is used to indicate internal parity errors. If a parity error occurs on a read from an internal array, the processor will assert the IERR# pin for one clock and then shutdown.
IGNNE#	I	The **ignore numeric error** input has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0 and the IGNNE# pin is asserted, the processor ignores any pending unmasked numeric exception and continues executing floating-point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the processor will execute the instruction in spite of the pending exception. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the processor will stop execution and wait for an external interrupt.
INIT	I	The processor **initialization** input pin forces the processor to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, write buffers, and floating-point registers retain the values they had prior to INIT. INIT may NOT be used in lieu of RESET after power up. If INIT is sampled high when RESET transitions from high to low, the processor will perform built-in self test prior to the start of program execution.
INTR	I	An active **maskable interrupt** input indicates that an external interrupt has been generated. If the IF bit in the EFLAGS register is set, the processor will generate two locked interrupt acknowledge bus cycles and vector to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to ensure that the interrupt is recognized.
INV	I	The **invalidation** input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock in which EADS# is sampled active.
KEN#	I	The **cache enable** pin is used to determine whether the current cycle is cacheable or not and is consequently used to determine cycle length. When the processor generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle will be transformed into a burst line fill cycle.
LOCK#	O	The **bus lock** pin indicates that the current bus cycle is locked. The processor does not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be deasserted for at least one clock between back-to-back locked cycles.

Table 26. Pin Quick Reference

Symbol	Type	Function
M/IO#	O	The **memory/input-output** is one of the primary bus cycle definition pins. It is driven valid in the same clock in which the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.
NA#	I	An active **next address** input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The processor will issue ADS# for a pending cycle two clocks after NA# is asserted. The processor supports up to two outstanding bus cycles.
NMI	I	The **non-maskable interrupt** request signal indicates that an external non-maskable interrupt has been generated.
PCD	O	The **page cache disable** pin reflects the state of the PCD bit in CR3, Page Directory Entry or Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page-by-page basis.
PCHK#	O	The **parity check** output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned.
PEN#	I	The **parity enable** input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. If this pin is sampled active in the clock, a data parity error is detected. The processor will latch the address and control signals of the cycle with the parity error in the machine check registers. If, in addition, the machine check enable bit in CR4 is set to "1", the processor will vector to the machine check exception before the beginning of the next instruction.
PM1/BP1–PM0/BP0	O	These pins function as part of the performance monitoring feature. The **breakpoint 1–0** pins are multiplexed with the **performance monitoring 1-0** pins. The PB1 and PB0 bits in the Debug Mode Control Register determine whether the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The **probe ready** output pin indicates that the processor has stopped normal execution in response to the R/S# pin going active or Probe Mode being entered.
PWT	O	The **page writethrough** pin reflects the state of the PWT bit in CR3, the page directory entry, or the page table entry. The PWT pin is used to provide an external writeback indication on a page-by-page basis.
R/S#	I	The **run/stop** input is an asynchronous, edge-sensitive interrupt used to stop the normal execution of the processor and place it into an idle state. A high to low transition on the R/S# pin will interrupt the processor and cause it to stop execution at the next instruction boundary.
RESET	I	**RESET** forces the processor to begin execution at a known state. All the processor internal caches will be invalidated upon the RESET. Modified lines in the data cache are not written back. FLUSH# and INIT are sampled when RESET transitions from high to low to determine if three-state test mode will be entered or if BIST will be run.
SCYC	O	The **split cycle** output is asserted during misaligned LOCKed transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles that are not locked.
SMI#	I	The **system management interrupt** causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.
SMIACT#	O	An active **system management interrupt active** output indicates that the processor is operating in System Management Mode.

Table 26. Pin Quick Reference

Symbol	Type	Function
STPCLK#	I	Assertion of the **stop clock** input signifies a request to stop the internal clock of the embedded Pentium processor with voltage reduction technology thereby causing the core to consume less power. When the processor recognizes STPCLK#, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, and generate a Stop Grant Acknowledge cycle. When STPCLK# is asserted, the processor will still respond to external snoop requests.
TCK	I	The **testability clock** input provides the clocking function for the processor boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the processor during boundary scan.
TDI	I	The **test data input** is a serial input for the test logic. TAP instructions and data are shifted into the processor on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.
TDO	O	The **test data output** is a serial output of the test logic. TAP instructions and data are shifted out of the processor on the TDO pin on TCK's falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the **test mode select** input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the **test reset** input allows the TAP controller to be asynchronously initialized.
VCC2	I	These pins are the **3.1 V power inputs** to the embedded Pentium processor with voltage reduction technology.
VCC3	I	These pins are the **3.3 V power inputs** to the embedded Pentium processor with voltage reduction technology.
VSS	I	These pins are the **ground inputs** to the embedded Pentium processor with voltage reduction technology.
W/R#	O	**Write/read** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The **writeback/writethrough** input allows a data cache line to be defined as writeback or writethrough on a line-by-line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

4.2.4 Pin Reference Tables

Table 27. Output Pins

Name	Active Level	When Floated
ADS#	Low	Bus Hold, BOFF#
APCHK#	Low	
BE7#–BE5#	Low	Bus Hold, BOFF#
BREQ	High	
CACHE#	Low	Bus Hold, BOFF#
FERR#	Low	
HIT#	Low	
HITM#	Low	
HLDA	High	
IERR#	Low	
LOCK#	Low	Bus Hold, BOFF#
M/IO#, D/C#, W/R#	n/a	Bus Hold, BOFF#
PCHK#	Low	
BP3–BP2, PM1/BP1, PM0/BP0	High	
PRDY	High	
PWT, PCD	High	Bus Hold, BOFF#
SCYC	High	Bus Hold, BOFF#
SMIACT#	Low	
TDO	n/a	All states except Shift-DR and Shift-IR

NOTE: All output and input/output pins are floated during three-state test mode (except TDO).

Table 28. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal resistor	Qualified
A20M#	Low	Asynchronous		
AHOLD	High	Synchronous		
BF	High	Synchronous/RESET	Pullup	
BOFF#	Low	Synchronous		
BRDY#	Low	Synchronous	Pullup	Bus State T2, T12, T2P
BUSCHK#	Low	Synchronous	Pullup	BRDY#
CLK	n/a			
EADS#	Low	Synchronous		
EWBE#	Low	Synchronous		BRDY#
FLUSH#	Low	Asynchronous		
HOLD	High	Synchronous		
IGNNE#	Low	Asynchronous		
INIT	High	Asynchronous		
INTR	High	Asynchronous		
INV	High	Synchronous		EADS#
KEN#	Low	Synchronous		First BRDY#/NA#
NA#	Low	Synchronous		Bus State T2,TD,T2P
NMI	High	Asynchronous		
PEN#	Low	Synchronous		BRDY#
R/S#	n/a	Asynchronous	Pullup	
RESET	High	Asynchronous		
SMI#	Low	Asynchronous	Pullup	
STPCLK#	Low	Asynchronous	Pullup	
TCK	n/a		Pullup	
TDI	n/a	Synchronous/TCK	Pullup	TCK
TMS	n/a	Synchronous/TCK	Pullup	TCK
TRST#	Low	Asynchronous	Pullup	
WB/WT#	n/a	Synchronous		First BRDY#/NA#

Table 29. Input/Output Pins

Name	Active Level	When Floated[1]	Qualified (when an input)	Internal Resistor
A31–A3	n/a	Address Hold, Bus Hold, BOFF#	EADS#	
AP	n/a	Address Hold, Bus Hold, BOFF#	EADS#	
BE4#–BE0#	Low	Bus Hold, BOFF#	RESET	Pulldown[2]
D63–D0	n/a	Bus Hold, BOFF#	BRDY#	
DP7–DP0	n/a	Bus Hold, BOFF#	BRDY#	

NOTES:
1. All output and input/output pins are floated during three-state test mode (except TDO).
2. BE3#–BE0# have pulldowns during RESET only.

4.2.5   Pin Grouping According to Function

Table 30 organizes the pins with respect to their function.

Table 30. Pin Functional Grouping

Function	Pins
Clock	CLK
Initialization	RESET, INIT, BF
Address Bus	A31–A3, BE7#–BE0#
Address Mask	A20M#
Data Bus	D63–D0
Address Parity	AP, APCHK#
Data Parity	DP7–DP0, PCHK#, PEN#
Internal Parity Error	IERR#
System Error	BUSCHK#
Bus Cycle Definition	M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK#
Bus Control	ADS#, BRDY#, NA#
Page Cacheability	PCD, PWT
Cache Control	KEN#, WB/WT#
Cache Snooping/Consistency	AHOLD, EADS#, HIT#, HITM#, INV
Cache Flush	FLUSH#
Write Ordering	EWBE#
Bus Arbitration	BOFF#, BREQ, HOLD, HLDA
Interrupts	INTR, NMI
Floating-Point Error Reporting	FERR#, IGNNE#
System Management Mode	SMI#, SMIACT#
TAP Port	TCK, TMS, TDI, TDO, TRST#
Breakpoint/Performance Monitoring	PM0/BP0, PM1/BP1, BP3–BP2
Clock Control	STPCLK#
Probe Mode	R/S#, PRDY

4.3 Mechanical Specifications

The embedded Pentium processor with voltage reduction technology is offered in an SPGA package without a heat spreader. The package is mechanically equivalent to the package used on the 3.3-V Pentium processor C2 stepping except that the SPGA embedded Pentium processor with voltage reduction technology will use a metal lid instead of a ceramic lid, and has the dimensions shown in Figure 16.

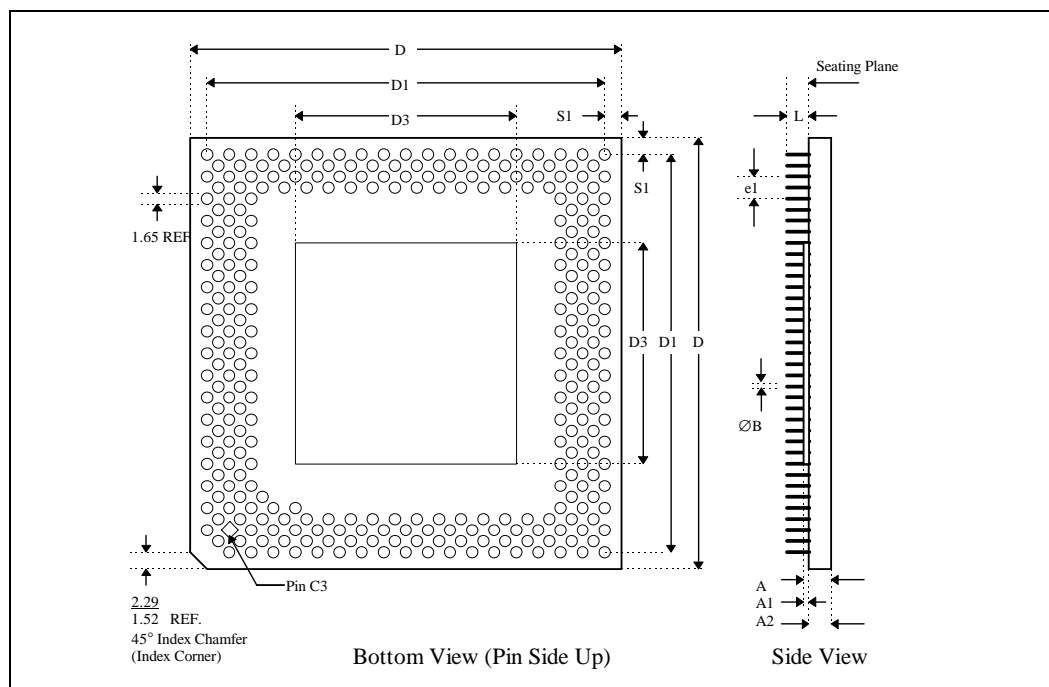**Figure 16. 296-Pin Staggered Pin Grid Array Package (SPGA)**

Table 31. 296-Pin Staggered Pin Grid Array Package Dimensions Key

Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.27	3.83	Metal Lid	0.129	0.151	Metal Lid
A1	0.66	0.86	Metal Lid	0.026	0.034	Metal Lid
A2	2.62	2.97		0.103	0.117	
B	0.43	0.51		0.017	0.020	
D	49.28	49.78		1.940	1.960	
D1	45.59	45.85		1.795	1.805	
D3	24.00	24.25	Includes Fillet	0.945	0.955	Includes Fillet
e1	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	1.130	
N	296		Total Pins	296		Total Pins
S1	1.52	2.54		0.060	0.100	

4.4 Thermal Specifications

The SPGA embedded Pentium processor with voltage reduction technology is specified for proper operation when the case temperature, T_{CASE} (T_C), is within the specified range of 0° C to 85° C.

The power dissipation specification in Table 32 is provided for designing thermal solutions for operation at a sustained maximum level. This is the worst-case power the device would dissipate in a system for a sustained period of time. This number is provided to assist in the design of a thermal solution for the device.

Table 32. Power Dissipation Requirements for Thermal Solution Design

| Parameter	Typical[1]	Max[2]	Unit	Notes
Active Power Dissipation	3.0–4.0	7.9	Watts	
Stop Grant and Auto Halt Powerdown Power Dissipation		1.3	Watts	Note 3
Stop Clock Power Dissipation	0.02	0.05	Watts	Note 4

NOTES:
1. This is the typical power dissipation in a system. This value was the average value measured in a system using a typical device at V_{CC2} = 3.1 V and V_{CC3} = 3.3 V running typical applications. This value is highly dependent upon the specific system configuration.
2. Systems must be designed to thermally dissipate the maximum Active Power Dissipation. It is determined using a worst-case instruction mix with V_{CC2} = 3.1 V and V_{CC3} = 3.3 V. The use of nominal V_{CC} in this measurement takes into account the thermal time constant of the package.
3. Stop Grant/Auto Halt Powerdown Power Dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction.
4. Stop Clock Power Dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input.

4.4.1 Measuring Thermal Values

To verify that the proper case temperature (T_C) is maintained for the embedded Pentium processor with voltage reduction technology, it should be measured at the center of the package top surface (encapsulant). To minimize any measurement errors, the following techniques are recommended:

- Use 36 gauge or finer diameter K, T, or J type thermocouples. Intel's laboratory testing was done using a thermocouple made by Omega (part number: 5TC-TTK-36-36).

- Attach the thermocouple bead or junction to the center of the package top surface using highly thermally conductive cements. Intel's laboratory testing was done by using Omega Bond (part number: OB-100).

- Attach the thermocouple at a 90° angle as shown in Figure 17.

Figure 17. Technique for Measuring Case Temperature (T_C)
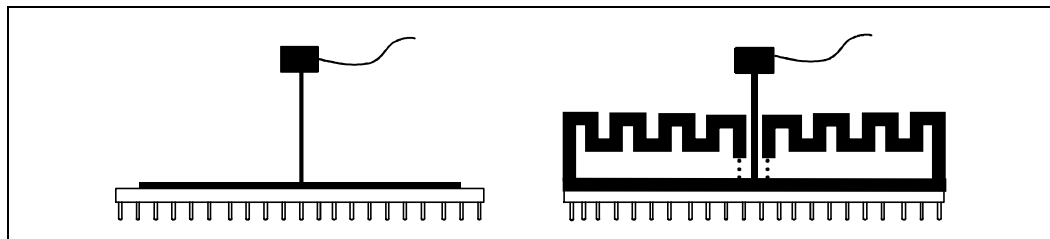
4.4.2 Thermal Equations

For the embedded Pentium processor with voltage reduction technology, an ambient temperature, T_A (air temperature around the processor), is not specified directly. The only requirement is that the case temperature (T_C) is met. To calculate T_A values, use the following equations:

$$T_A = T_C - (P * \theta_{CA})$$

$$\theta_{CA} = \theta_{JA} - \theta_{JC}$$

where,

T_A and T_C =	ambient and case temperature (°C)
θ_{CA} =	case-to-ambient thermal resistance (°C/W)
θ_{JA} =	junction-to-ambient thermal resistance (°C/W)
θ_{JC} =	junction-to-case thermal resistance (°C/W)
P =	maximum power consumption in Watts (see Table 32)

Table 33 lists the θ_{CA} values for the Pentium processor with passive heatsinks.

Thermal data collection parameters:

• Heatsinks are omnidirectional pin aluminum alloy

• Features were based on standard extrusion practices for a given height

• Pin size ranged from 50 to 129 mils

• Pin spacing ranged from 93 to 175 mils

• Base thickness ranged from 79 to 200 mils

• Heatsink attach was 0.005" of thermal grease

• Using an attach thickness of 0.002" improves performance by approximately 0.3 °C/W

**Table 33. Thermal Resistances for Embedded Pentium® Processors
with Voltage Reduction Technology**

Heatsink Height in Inches	θ_{JC} (°C/Watt)	θ_{CA}(°C/Watt) vs. Laminar Airflow (Linear ft/min)					
		0	100	200	400	600	800
0.25	1.25	9.4	8.3	6.9	4.7	3.9	3.3
0.35	1.25	9.1	7.8	6.3	4.3	3.6	3.1
0.45	1.25	8.7	7.3	5.6	3.9	3.2	2.8
0.55	1.25	8.4	6.8	5.0	3.5	2.9	2.6
0.65	1.25	8.0	6.3	4.6	3.3	2.7	2.4
0.80	1.25	7.3	5.6	4.2	2.9	2.5	2.3
1.00	1.25	6.6	4.9	3.9	2.9	2.4	2.1
1.20	1.25	6.2	4.6	3.6	2.7	2.3	2.1
1.40	1.25	5.7	4.2	3.3	2.5	2.2	2.0
Without Heatsink	1.7	14.5	13.8	12.6	10.5	8.6	7.5