8.0 Pentium Processor® with MMX™ Technology Packaging Information

8.1 Pinout

Figure 31. Pentium® Processor with MMX™ Technology PPGA Package Pinout - Top Side View

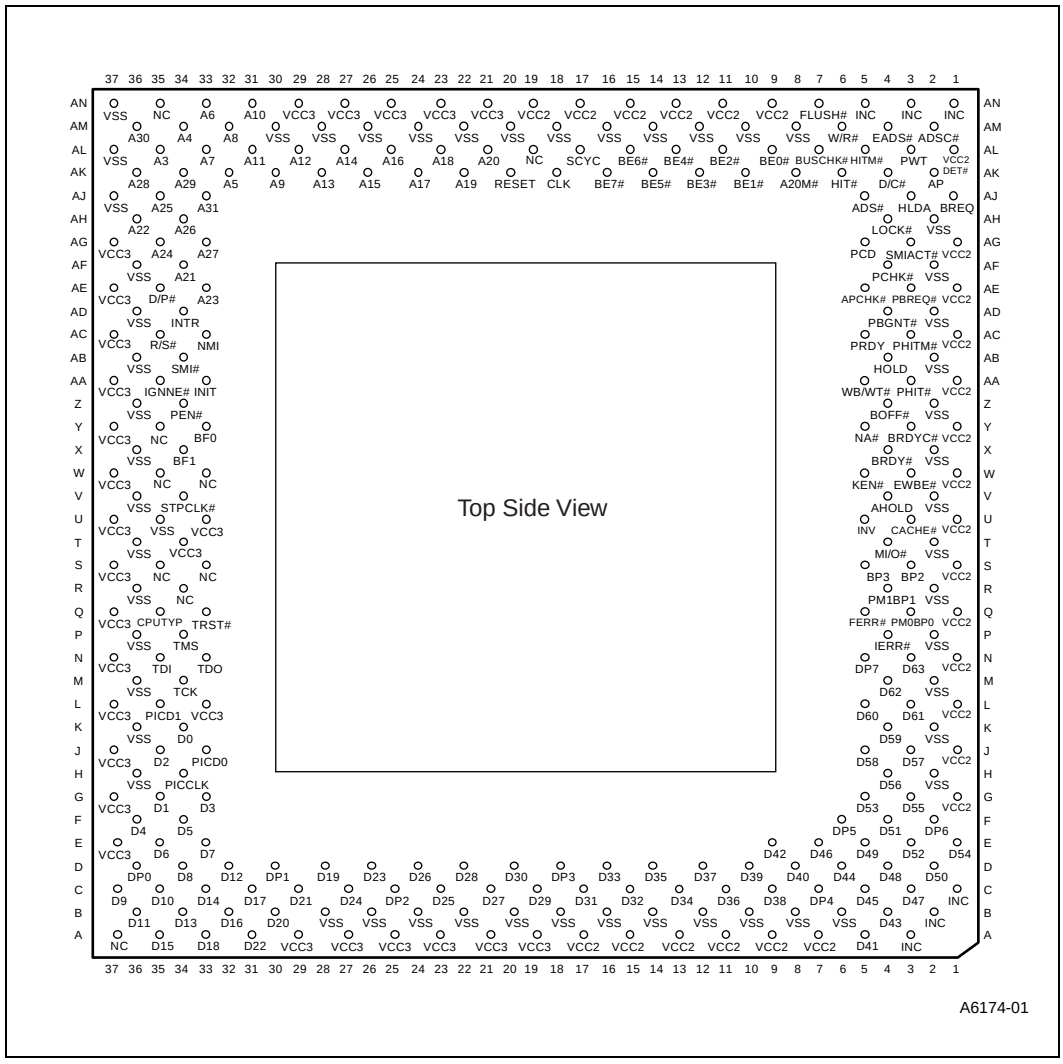
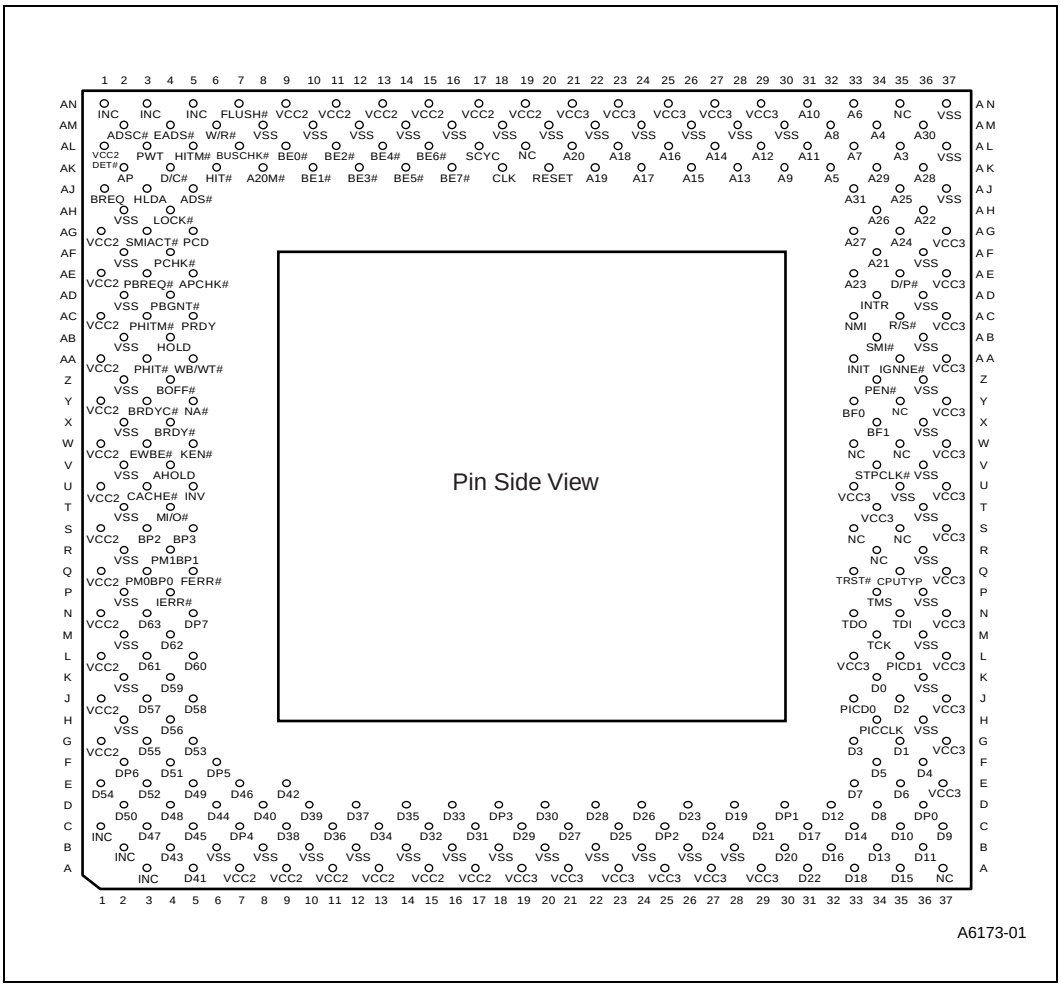


Figure 32. Pentium® Processor with MMX™ Technology PPGA Package Pinout - Bottom Side View



8.1.1 Pin Cross Reference

Table 46. Pin Cross-Reference by Pin Name — Address and Data Pins

Pin	Location	Pin	Location	Pin	Location	Pin	Location	Pin	Location
Address									
A3	AL35	A9	AK30	A15	AK26	A21	AF34	A27	AG33
A4	AM34	A10	AN31	A16	AL25	A22	AH36	A28	AK36
A5	AK32	A11	AL31	A17	AK24	A23	AE33	A29	AK34
A6	AN33	A12	AL29	A18	AL23	A24	AG35	A30	AM36
A7	AL33	A13	AK28	A19	AK22	A25	AJ35	A31	AJ33
A8	AM32	A14	AL27	A20	AL21	A26	AH34		
Data									
D0	K34	D13	B34	D26	D24	D39	D10	D52	E03
D1	G35	D14	C33	D27	C21	D40	D08	D53	G05
D2	J35	D15	A35	D28	D22	D41	A05	D54	E01
D3	G33	D16	B32	D29	C19	D42	E09	D55	G03
D4	F36	D17	C31	D30	D20	D43	B04	D56	H04
D5	F34	D18	A33	D31	C17	D44	D06	D57	J03
D6	E35	D19	D28	D32	C15	D45	C05	D58	J05
D7	E33	D20	B30	D33	D16	D46	E07	D59	K04
D8	D34	D21	C29	D34	C13	D47	C03	D60	L05
D9	C37	D22	A31	D35	D14	D48	D04	D61	L03
D10	C35	D23	D26	D36	C11	D49	E05	D62	M04
D11	B36	D24	C27	D37	D12	D50	D02	D63	N03
D12	D32	D25	C23	D38	C09	D51	F04		

Table 47. Pin Cross-Reference by Pin Name — Control Pins

Pin	Location	Pin	Location	Pin	Location	Pin	Location
Control							
A20M#	AK08	BREQ	AJ01	HIT#	AK06	PRDY	AC05
ADS#	AJ05	BUSCHK#	AL07	HITM#	AL05	PWT	AL03
ADSC#	AM02	CACHE#	U03	HLDA	AJ03	R/S#	AC35
AHOLD	V04	CPUTYP	Q35	HOLD	AB04	RESET	AK20
AP	AK02	D/C#	AK04	IERR#	P04	SCYC	AL17
APCHK#	AE05	D/P#	AE35	IGNNE#	AA35	SMI#	AB34
BE0#	AL09	DP0	D36	INIT	AA33	SMIACT#	AG03
BE1#	AK10	DP1	D30	INTR/LINT 0	AD34	TCK	M34
BE2#	AL11	DP2	C25	INV	U05	TDI	N35
BE3#	AK12	DP3	D18	KEN#	W05	TDO	N33
BE4#	AL13	DP4	C07	LOCK#	AH04	TMS	P34
BE5#	AK14	DP5	F06	M/IO#	T04	TRST#	Q33
BE6#	AL15	DP6	F02	NA#	Y05	VCC2DET#	AL01
BE7#	AK16	DP7	N05	NMI/LINT1	AC33	W/R#	AM06
BOFF#	Z04	EADS#	AM04	PCD	AG05	WB/WT#	AA05
BP2	S03	EWBE#	W03	PCHK#	AF04		
BP3	S05	FERR#	Q05	PEN#	Z34		
BRDY#	X04	FLUSH#	AN07	PM0/BP0	Q03		
BRDYC#	Y03	FRCMC#[1]	Y35	PM1/BP1	R04		
APIC							
PICCLK	H34[2]	PICD0/[DPEN#]	J33	PICD1/[APICEN]	L35		
Clock Control							
CLK	AK18[2]	[BF0]	Y33	[BF1]	X34	STPCLK#	V34
Dual Processor Private Interface							
PBGNT#	AD04	PBREQ#	AE03	PHIT#	AA03	PHITM#	AC03

NOTES:
1. The FRCMC# pin is not defined for the Pentium® processor with MMX™ technology. This pin should be left as a “NC” or tied to V_{CC3} via an external pull-up resistor on the Pentium processor with MMX technology.
2. PICCLK and CLK are 3.3 V-tolerant-only on the Pentium processor with MMX technology. Please refer to the *Embedded Pentium® Processor Family Developer's Manual* (order number 273204) for the CLK and PICCLK signal quality specification.

Table 48. Pin Cross-Reference by Pin Name — Power, Ground and No Connect Pins

V_{CC2}									
A17	A11	G01	N01	U01	AA01	AE01	AN09	AN13	AN17
A15	A09	J01	Q01	W01	AC01	AG01	AN11	AN15	AN19
A13	A07	L01	S01	Y01					
V_{CC3}									
A19	A25	E37	L37	Q37	U33	Y37	AE37	AN27	AN21
A21	A27	G37	L33	S37	U37	AA37	AG37	AN25	
A23	A29	J37	N37	T34	W37	AC37	AN29	AN23	
V_{SS}									
B06	B18	H02	P02	T36	X36	AD02	AJ37	AM14	AM24
B08	B20	H36	P36	U35	Z02	AD36	AL37	AM16	AM26
B10	B22	K02	R02	V02	Z36	AF02	AM08	AM18	AM28
B12	B24	K36	R36	V36	AB02	AF36	AM10	AM20	AM30
B14	B26	M02	T02	X02	AB36	AH02	AM12	AM22	AN37
B16	B28	M36							
NC									
A37	R34	S33	S35	W33	W35	AL19	AN35	Y35	
INC									
A03	B02	C01	AN01	AN03	AN05				

8.1.2 Design Notes

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC3}. Unused active high inputs should be connected to GND.

Note: No Connect (NC) pins *must* remain unconnected. Connection of NC or INC pins may result in component failure or incompatibility with future processor steppings.

8.1.3 Pin Quick Reference

This section gives a brief functional description of each of the pins. For a detailed description, see the Hardware Interface chapter in the *Embedded Pentium® Processor Family Developer's Manual* (order number 273204).

Note: All input pins must meet their AC/DC specifications to guarantee proper functional behavior.

The # symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage. When a # symbol is not present after the signal name, the signal is active, or asserted at the high voltage level. Square brackets around a signal name indicate that the signal is defined only at RESET.

The following pins become I/O pins when two Pentium processors with MMX technology are operating in a dual processing environment:

ADS#, CACHE#, HIT#, HITM#, HLDA#, LOCK#, M/IO#, D/C#, W/R#, SCYC, BE4#

Table 49. Quick Pin Reference (Sheet 1 of 7)

Symbol	Type	Name and Function
A20M#	I	When the **address bit 20 mask** pin is asserted, the processor emulates the address wraparound at 1 Mbyte which occurs on the 8086 by masking physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode. A20M# is internally masked by the processor when configured as a Dual processor.
A31–A3	I/O	As outputs, the **address** lines of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31–A5.
ADS#	O	The **address strobe** indicates that a new valid bus cycle is currently being driven by the processor.
ADSC#	O	The **address strobe (copy)** is functionally identical to ADS#.
AHOLD	I	In response to the assertion of **address hold**, the Pentium® processor with MMX™ technology stops driving the address lines (A31–A3) and AP in the next clock. The rest of the bus remains active so data can be returned or driven for previously issued bus cycles.
AP	I/O	**Address parity** is driven by the processor with even parity information on all processor generated cycles in the same clock that the address is driven. Even parity must be driven back to the processor during inquire cycles on this pin in the same clock as EADS# to ensure that correct parity check status is indicated by the processor.
APCHK#	O	The **address parity check** status pin is asserted two clocks after EADS# is sampled active when the processor has detected a parity error on the address bus during inquire cycles. APCHK# remains active for one clock each time a parity error is detected (including during dual processing private snooping).
[APICEN] PICD1	I	**Advanced Programmable Interrupt Controller Enable** enables or disables the on-chip APIC interrupt controller. When sampled high at the falling edge of RESET, the APIC is enabled. APICEN shares a pin with the PICD1 signal.
BE7#–BE4# BE3#–BE0#	O I/O	The **byte enable** pins are used to determine which bytes must be written to external memory or which bytes were requested by the processor for the current cycle. The byte enables are driven in the same clock as the address lines (A31–A3). Additionally, the lower 4-byte enables (BE3#–BE0#) are used on the Pentium processor with MMX technology as APIC ID inputs and are sampled at RESET. In dual processing mode, BE4# is used as an input during Flush cycles.
BF1–BF0	I	The **bus frequency** pins determine the bus-to-core frequency ratio. BF1–BF0 are sampled at RESET, and cannot be changed until another non-warm (1 ms) assertion of RESET. Additionally, BF1–BF0 must not change values while RESET is active. See Table 50 for Bus Frequency Selections.
BOFF#	I	The **backoff** input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the processor floats all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time the processor restarts the aborted bus cycle(s) in their entirety.
BP3–BP2 PM1–PM0/ BP1–BP0	O	The **breakpoint** pins (BP3–BP0) correspond to the debug registers, DR3–DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the **performance monitoring** pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.

Table 49. Quick Pin Reference (Sheet 2 of 7)

Symbol	Type	Name and Function
BRDY#	I	The **burst ready** input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the processor data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states.
BRDYC#	I	The **burst ready (copy)** is functionally identical to BRDY#.
BREQ	O	The **bus request** output indicates to the external system that the processor has internally generated a bus request. This signal is always driven whether or not the processor is driving its bus.
BUSCHK#	I	The **bus check** input allows the system to signal an unsuccessful completion of a bus cycle. If this pin is sampled active, the processor latches the address and control signals in the machine check registers. When the MCE bit in CR4 is set and the BUSCHK# pin is active, the processor vectors to the machine check exception. To assure that BUSCHK# is always recognized, STPCLK# must be deasserted any time BUSCHK# is asserted by the system, before the system allows another external bus cycle. When BUSCHK# is asserted by the system for a snoop cycle while STPCLK# remains asserted, usually (if MCE=1) the processor vectors to the exception after STPCLK# is deasserted. But if another snoop to the same line occurs during STPCLK# assertion, the processor can lose the BUSCHK# request.
CACHE#	O	For processor-initiated cycles, the **cache** pin indicates internal cacheability of the cycle (if a read), and indicates a burst write back cycle (when a write). When this pin is driven inactive during a read cycle, the processor does not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).
CLK	I	The **clock** input provides the fundamental timing for the processor. Its frequency is the operating frequency of the processor external bus, and requires TTL levels. All external timing parameters except TDI, TDO, TMS, TRST#, and PICD0–PICD1 are specified with respect to the rising edge of CLK. This pin is 3.3-V-tolerant-only on the Pentium processor with MMX technology. Please refer to the *Embedded Pentium® Processor Family Developer's Manual* (order number 273204) for the CLK and PICCLK signal quality specification. It is recommended that CLK begin toggling within 150 ms after V_{CC} reaches its proper operating level. This recommendation is to ensure long-term reliability of the device.
CPUTYP	I	**CPU type** distinguishes the Primary processor from the Dual processor. In a single processor environment, or when the processor is acting as the Primary processor in a dual processing system, CPUTYP should be strapped to V_{SS}. The Dual processor should have CPUTYP strapped to V_{CC3}.
D/C#	O	The **data/code** output is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.
D/P#	O	The **dual/primary** processor indication. The Primary processor drives this pin low when it is driving the bus, otherwise it drives this pin high. D/P# is always driven. D/P# can be sampled for the current cycle with ADS# (like a status pin). This pin is defined only on the Primary processor. Dual processing is supported in a system only if both processors are operating at identical core and bus frequencies. Within these restrictions, two processors of different steppings may operate together in a system.
D63–D0	I/O	These are the 64 **data lines** for the processor. Lines D7–D0 define the least significant byte of the data bus; lines D63–D56 define the most significant byte of the data bus. When the processor is driving the data lines, they are driven during the T2, T12, or T2P clocks for that cycle. During reads, the processor samples the data bus when BRDY# is returned.

Table 49. Quick Pin Reference (Sheet 3 of 7)

Symbol	Type	Name and Function
DP7–DP0	I/O	These are the **data parity** pins for the processor. There is one for each byte of the data bus. They are driven by the processor with even parity information on writes in the same clock as write data. Even parity information must be driven back to the processor on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the processor. DP7 applies to D63–D56, DP0 applies to D7–D0.
[DPEN#] PICD0	I/O	**Dual processing enable** is an output of the Dual processor and an input of the Primary processor. The Dual processor drives DPEN# low to the Primary processor at RESET to indicate that the Primary processor should enable dual processor mode. DPEN# may be sampled by the system at the falling edge of RESET to determine if the dual-processor socket is occupied. DPEN# is multiplexed with PICD0.
EADS#	I	This signal indicates that a valid **external address** has been driven onto the processor address pins to be used for an inquire cycle.
EWBE#	I	The **external write buffer empty** input, when inactive (high), indicates that a write cycle is pending in the external system. When the processor generates a write, and EWBE# is sampled inactive, the processor holds off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, which is indicated by EWBE# being active.
FERR#	O	The **floating-point error** pin is driven active when an unmasked **floating-point** error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using DOS-type **floating-point** error reporting. FERR# is never driven active by the Dual processor.
FLUSH#	I	When asserted, the **cache flush** input forces the processor to write back all modified lines in the data cache and invalidate its internal caches. A Flush Acknowledge special cycle will be generated by the processor to indicate the completion of the write back and invalidation. When FLUSH# is sampled low when RESET transitions from high to low, three-state test mode is entered. When two Pentium processors with MMX technology are operating in dual processing mode and FLUSH# is asserted, the Dual processor performs a flush first (without a flush acknowledge cycle), then the Primary processor performs a flush followed by a flush acknowledge cycle. When the FLUSH# signal is asserted in dual processing mode, it must be deasserted at least one clock prior to BRDY# of the FLUSH Acknowledge cycle to avoid DP arbitration problems.
HIT#	O	The **hit** indication is driven to reflect the outcome of an inquire cycle. When an inquire cycle hits a valid line in the processor data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. When the inquire cycle misses the processor cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.
HITM#	O	The **hit to a modified line** output is driven to reflect the outcome of an inquire cycle. It is asserted after inquire cycles which resulted in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.
HLDA	O	The **bus hold acknowledge** pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the processor has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA will be driven inactive and the Pentium processor with MMX technology will resume driving the bus. If the processor has a bus cycle pending, it will be driven one clock cycle after HLDA is deasserted.

Table 49. Quick Pin Reference (Sheet 4 of 7)

Symbol	Type	Name and Function
HOLD	I	In response to the **bus hold request**, the processor floats most of its output and input/output pins and asserts HLDA after completing all outstanding bus cycles. The processor maintains its bus in this state until HOLD is deasserted. HOLD is not recognized during LOCK cycles. The processor recognizes HOLD during reset.
IERR#	O	The **internal error** pin is used to indicate internal parity errors. When a parity error occurs on a read from an internal array, the processor asserts the IERR# pin for one clock and then shuts down.
IGNNE#	I	This is the **ignore numeric error** input. This pin has no effect when the NE bit in CR0 is set to 1. When the CR0.NE bit is 0, and the IGNNE# pin is asserted, the processor ignores any pending unmasked numeric exception and continues executing floating-point instructions for the entire duration that this pin is asserted. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one of FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the processor executes the instruction in spite of the pending exception. When the CR0.NE bit is 0, IGNNE# is not asserted, a pending unmasked numeric exception exists (SW.ES = 1), and the floating-point instruction is one other than FINIT, FCLEX, FSTENV, FSAVE, FSTSW, FSTCW, FENI, FDISI, or FSETPM, the processor stops execution and waits for an external interrupt. IGNNE# is internally masked when the processor is configured as a Dual processor.
INIT	I	The processor **initialization** input pin forces the processor to begin execution in a known state. The processor state after INIT is the same as the state after RESET except that the internal caches, write buffers, and floating-point registers retain the values they had prior to INIT. INIT may *not* be used instead of RESET after power-up. When INIT is sampled high when RESET transitions from high to low, the processor performs a built-in self test prior to the start of program execution.
INTR/LINT0	I	An active **maskable interrupt** input indicates that an external interrupt has been generated. When the IF bit in the EFLAGS register is set, the processor generates two locked interrupt acknowledge bus cycles and vectors to an interrupt handler after the current instruction execution is completed. INTR must remain active until the first interrupt acknowledge cycle is generated to ensure that the interrupt is recognized. When the local APIC is enabled, this pin becomes LINT0.
INV	I	The **invalidation** input determines the final cache line state (S or I) in case of an inquire cycle hit. It is sampled together with the address for the inquire cycle in the clock EADS# is sampled active.
KEN#	I	The **cache enable** pin is used to determine whether the current cycle is cacheable or not and is consequently used to determine cycle length. When the processor generates a cycle that can be cached (CACHE# asserted) and KEN# is active, the cycle is transformed into a burst line fill cycle.
LINT0/INTR	I	When the APIC is enabled, this pin is **local interrupt 0**. When the APIC is disabled, this pin is INTR.
LINT1/NMI	I	When the APIC is enabled, this pin is **local interrupt 1**. When the APIC is disabled, this pin is NMI.
LOCK#	O	The **bus lock** pin indicates that the current bus cycle is locked. The Pentium processor with MMX technology does not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be deasserted for at least one clock between back-to-back locked cycles.

Table 49. Quick Pin Reference (Sheet 5 of 7)

Symbol	Type	Name and Function
M/IO#	O	The **memory/input-output** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.
NA#	I	An active **next address** input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The processor issues ADS# for a pending cycle two clocks after NA# is asserted. The processor supports up to two outstanding bus cycles.
NMI/LINT1	I	The **non-maskable interrupt** request signal indicates that an external non-maskable interrupt has been generated. When the local APIC is enabled, this pin becomes LINT1.
PBGNT#	I/O	**Private bus grant** is the grant line that is used when two Pentium processors with MMX technology are configured in dual processing mode, in order to perform private bus arbitration. PBGNT# should be left unconnected if only one Pentium processor with MMX technology exists in a system.
PBREQ#	I/O	**Private bus request** is the request line that is used when two Pentium processors with MMX technology are configured in dual processing mode, in order to perform private bus arbitration. PBREQ# should be left unconnected when only one processor exists in a system.
PCD	O	The **page cache disable** pin reflects the state of the PCD bit in CR3, the Page Directory Entry, or the Page Table Entry. PCD provides an external cacheability indication on a page by page basis.
PCHK#	O	The **parity check** output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned. When two Pentium processors with MMX technology are operating in dual processing mode, PCHK# may be driven two or three clocks after BRDY# is returned.
PEN#	I	The **parity enable** input (along with CR4.MCE) determines whether a machine check exception will be taken as a result of a data parity error on a read cycle. When this pin is sampled active in the clock a data parity error is detected, the processor latches the address and control signals of the cycle with the parity error in the machine check registers. When PEN# is sampled active and the machine check enable bit in CR4 is set to “1”, the processor vectors to the machine check exception before the beginning of the next instruction.
PHIT#	I/O	**Private hit** is a hit indication used when two Pentium processors with MMX technology are configured in dual processing mode, in order to maintain local cache coherency. PHIT# should be left unconnected when only one processor exists in a system.
PHITM#	I/O	**Private modified hit** is a hit on a modified cache line indication used when two Pentium processors with MMX technology are configured in dual processing mode, in order to maintain local cache coherency. PHITM# should be left unconnected if only one processor exists in a system.
PICCLK	I	The APIC interrupt controller serial data bus clock is driven into the **programmable interrupt controller clock** input of the processor. This pin is 3.3-V-tolerant-only on the Pentium processor with MMX technology. Please refer to the *Embedded Pentium® Processor Family Developer’s Manual* (order number 273204) for the CLK and PICCLK signal quality specification.
PICD0/[DPEN#]– PICD1/[APICEN]	I/O	**Programmable interrupt controller data lines 0–1** of the Pentium processor with MMX technology comprise the data portion of the APIC 3-wire bus. They are open-drain outputs that require external pull-up resistors. These signals are multiplexed with DPEN# and APICEN respectively.

Table 49. Quick Pin Reference (Sheet 6 of 7)

Symbol	Type	Name and Function
PM1/BP1–PM0/BP0	O	These pins function as part of the performance monitoring feature. The breakpoint 1–0 pins are multiplexed with the **performance monitoring 1–0** pins. The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The **probe ready** output pin is provided for use with the Intel debug port. Please refer to the *Embedded Pentium® Processor Family Developer's Manual* (order number 273204) for more details.
PWT	O	The **page write through** pin reflects the state of the PWT bit in CR3, the page directory entry, or the page table entry. The PWT pin is used to provide an external write back indication on a page-by-page basis.
R/S#	I	The **run/stop** input is provided for use with the Intel debug port. Please refer to the *Embedded Pentium® Processor Family Developer's Manual* (order number 273204) for more details.
RESET	I	**RESET** forces the processor to begin execution at a known state. All the processor internal caches will be invalidated upon the RESET. Modified lines in the data cache are not written back. FLUSH# and INIT are sampled when RESET transitions from high to low to determine if three-state test mode or checker mode will be entered, or if Built-In Self-Test (BIST) will be run.
SCYC	O	The **split cycle** output is asserted during misaligned LOCKed transfers to indicate that more than two cycles will be locked together. This signal is defined for locked cycles only. It is undefined for cycles which are not locked.
SMI#	I	The **system management interrupt** causes a system management interrupt request to be latched internally. When the latched SMI# is recognized on an instruction boundary, the processor enters System Management Mode.
SMIACT#	O	An active **system management interrupt active** output indicates that the processor is operating in System Management Mode.
STPCLK#	I	Assertion of the **stop clock** input signifies a request to stop the internal clock of the processor, thereby causing the core to consume less power. When the processor recognizes STPCLK#, the processor stops execution on the next instruction boundary, unless superseded by a higher priority interrupt, and generates a stop grant acknowledge cycle. When STPCLK# is asserted, the processor still responds to interprocessor and external snoop requests.
TCK	I	The **testability clock** input provides the clocking function for the processor boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the processor during boundary scan.
TDI	I	The **test data input** is a serial input for the test logic. TAP instructions and data are shifted into the processor on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.
TDO	O	The **test data output** is a serial output of the test logic. TAP instructions and data are shifted out of the processor on the TDO pin on TCK's falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the **test mode select** input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the **test reset** input allows the TAP controller to be asynchronously initialized.
VCC2	I	The Pentium processor with MMX technology has 25 2.8 V **power** inputs.
VCC3	I	The Pentium processor with MMX technology has 28 3.3 V **power** inputs.
VCC2DET#	O	**V_{CC2} detect** is used in flexible motherboard implementations to configure the voltage output set-point appropriately for the V_{CC2} inputs of the processor.

Table 49. Quick Pin Reference (Sheet 7 of 7)

Symbol	Type	Name and Function
VSS	I	The Pentium processor with MMX technology has 53 **ground** inputs.
W/R#	O	**Write/read** is one of the primary bus cycle definition pins. It is driven valid in the same clock as the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The **write back/write through** input allows a data cache line to be defined as write back or write through on a line-by-line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

Core and bus frequencies can be set according to Table 50. Each Pentium processor with MMX technology is specified to operate within a single bus-to-core ratio and a specific minimum-to-maximum bus-frequency range (corresponding to a minimum-to-maximum core-frequency range). Operation in other bus-to-core ratios or outside the specified operating frequency range is not supported or advocated. For example, the 166 MHz Pentium processor with MMX technology does not operate beyond the 66 MHz bus frequency and only supports the 2/5 bus-to-core ratio; it does not support the 1/3, 1/2, or 2/3 bus-to-core ratios.

Table 50. Bus Frequency Selections

BF1	BF0	Bus/Core Ratio	Max Bus/Core Frequency (MHz)	Min Bus/Core Frequency (MHz)
0	1	1/3	66/200	33/100
0	0	2/5	N/A(2)	N/A(2)
1	0	1/2(1,2)	N/A(2)	N/A(2)
1	1	2/7	66/233	33/117

NOTES:
1. This is the default bus to core ratio for the Pentium® processor with MMX™ technology. If the BF pins are left floating, the processor will be configured for the 1/2 bus to core frequency ratio.
2. Currently, there are no embedded products that support these bus fractions.

8.1.4 Pin Reference Tables

Table 51. Output Pins

Name	Active Level	When Floated
ADS# (1)	Low	Bus Hold, BOFF#
ADSC#	Low	Bus Hold, BOFF#
APCHK#	Low	
BE7#–BE4#	Low	Bus Hold, BOFF#
BREQ	High	
CACHE#(1)	Low	Bus Hold, BOFF#
D/P#(2)	N/A	
FERR# (2)	Low	
HIT# (1)	Low	
HITM# (1, 3)	Low	
HLDA (1)	High	
IERR#	Low	
LOCK# (1)	Low	Bus Hold, BOFF#
M/IO#(1), D/C#(1), W/R#(1)	N/A	Bus Hold, BOFF#
PCHK#	Low	
BP3–BP2, PM1/BP1, PM0/BP0	High	
PRDY	High	
PWT, PCD	High	Bus Hold, BOFF#
SCYC(1)	High	Bus Hold, BOFF#
SMIACT#	Low	
TDO	N/A	All states except Shift-DR and Shift-IR
VCC2DET#	Low	

NOTES:

All output and input/output pins are floated during three-state test mode (except IERR#).

1. These are I/O signals when two Pentium® processors with MMX™ technology are operating in dual processing mode.
2. These signals are undefined when the processor is configured as a Dual processor.
3. M# pin has an internal pull-up resistor.

Table 52. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal Resistor	Qualified
A20M#†	Low	Asynchronous		
AHOLD	High	Synchronous		
APICEN	High	Synchronous/RESET	Pull-up	
BF0	N/A	Synchronous/RESET	Pull-down	
BF1	N/A	Synchronous/RESET	Pull-up	
BOFF#	Low	Synchronous		
BRDY#	Low	Synchronous	Pull-up	Bus State T2, T12, T2P
BRDYC#	Low	Synchronous	Pull-up	Bus State T2, T12, T2P
BUSCHK#	Low	Synchronous	Pull-up	BRDY#
CLK	N/A			
CPUTYP	High	Synchronous/RESET	Pull-down	
EADS#	Low	Synchronous		
EWBE#	Low	Synchronous		BRDY#
FLUSH#	Low	Asynchronous		
HOLD	High	Synchronous		
IGNNE#†	Low	Asynchronous		
INIT	High	Asynchronous		
INTR	High	Asynchronous		
INV	High	Synchronous		EADS#
LINT1–LINT0	High	Asynchronous		APICEN at RESET
KEN#	Low	Synchronous		First BRDY#/NA#
NA#	Low	Synchronous		Bus State T2, TD, T2P
NMI	High	Asynchronous		
PEN#	Low	Synchronous		BRDY#
PICCLK	High	Asynchronous	Pull-up	
R/S#	N/A	Asynchronous	Pull-up	
RESET	High	Asynchronous		
SMI#	Low	Asynchronous	Pull-up	
STPCLK#	Low	Asynchronous	Pull-up	
TCK	N/A		Pull-up	
TDI	N/A	Synchronous/TCK	Pull-up	TCK
TMS	N/A	Synchronous/TCK	Pull-up	TCK
TRST#	Low	Asynchronous	Pull-up	
WB/WT#	N/A	Synchronous		First BRDY#/NA#

† Undefined when the processor is configured as a Dual processor.

Table 53. Input/Output Pins

Name[1]	Active Level	When Floated	Qualified (when an input)	Internal Resistor
A31–A3	N/A	Address Hold, Bus Hold, BOFF#	EADS#	
AP	N/A	Address Hold, Bus Hold, BOFF#	EADS#	
BE3#–BE0#	Low	Address Hold, Bus Hold, BOFF#	RESET	Pull-down[2]
D63–D0	N/A	Bus Hold, BOFF#	BRDY#	
DP7–DP0	N/A	Bus Hold, BOFF#	BRDY#	
DPEN#	low		RESET	Pull-up
PICD0	N/A			Pull-up
PICD1	N/A			Pull-down

NOTES:
1. All output and input/output pins are floated during three-state test mode (except TDO, IERR# and TDO).
2. BE3#–BE0# have Pull-downs during RESET only.

Table 54. Inter-processor Input/Output Pins

Name	Active Level	Internal Resistor
PHIT#	Low	Pull-up
PHITM#	Low	Pull-up
PBGNT#	Low	Pull-up
PBREQ#	Low	Pull-up

NOTE: For proper inter-processor operation, the system cannot load these signals.

8.1.5 Pin Grouping According to Function

Table 55 organizes the pins with respect to their function.

Table 55. Pin Functional Grouping

Function	Pins
Clock	CLK
Initialization	RESET, INIT, BF1–BF0
Address Bus	A31–A3, BE7#–BE0#
Address Mask	A20M#
Data Bus	D63–D0
Address Parity	AP, APCHK#
APIC Support	PICCLK, PICD1–PICD0
Data Parity	DP7–DP0, PCHK#, PEN#
Internal Parity Error	IERR#
System Error	BUSCHK#
Bus Cycle Definition	M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK#
Bus Control	ADS#, ADSC#, BRDY#, BRDYC#, NA#
Page Cacheability	PCD, PWT
Cache Control	KEN#, WB/WT#
Cache Snooping/Consistency	AHOLD, EADS#, HIT#, HITM#, INV
Cache Flush	FLUSH#
Write Ordering	EWBE#
Bus Arbitration	BOFF#, BREQ, HOLD, HLDA
Dual Processing Private Bus Control	PBGNT#, PBREQ#, PHIT#, PHITM#
Interrupts	INTR, NMI
Floating-Point Error Reporting	FERR#, IGNNE#
System Management Mode	SMI#, SMIACT#
TAP Port	TCK, TMS, TDI, TDO, TRST#
Breakpoint/Performance Monitoring	PM0/BP0, PM1/BP1, BP3–BP2
Power Management	STPCLK#
Miscellaneous Dual Processing	CPUTYP, D/P#
Debugging	R/S#, PRDY
Voltage Detection	VCC2DET#

8.2 Mechanical Specifications

Package summary information is provided in Table 56. The mechanical specifications for the Pentium processor with MMX technology are provided in Table 57 and Figure 33.

Table 56. PPGA Package Information

Package Type	Total Pins	Pin Array	Package Size
Plastic Staggered Pin Grid Array (PPGA)	296	37 x 37	1.95" x 1.95" 4.95 cm x 4.95 cm

Figure 33. PPGA Package Dimensions

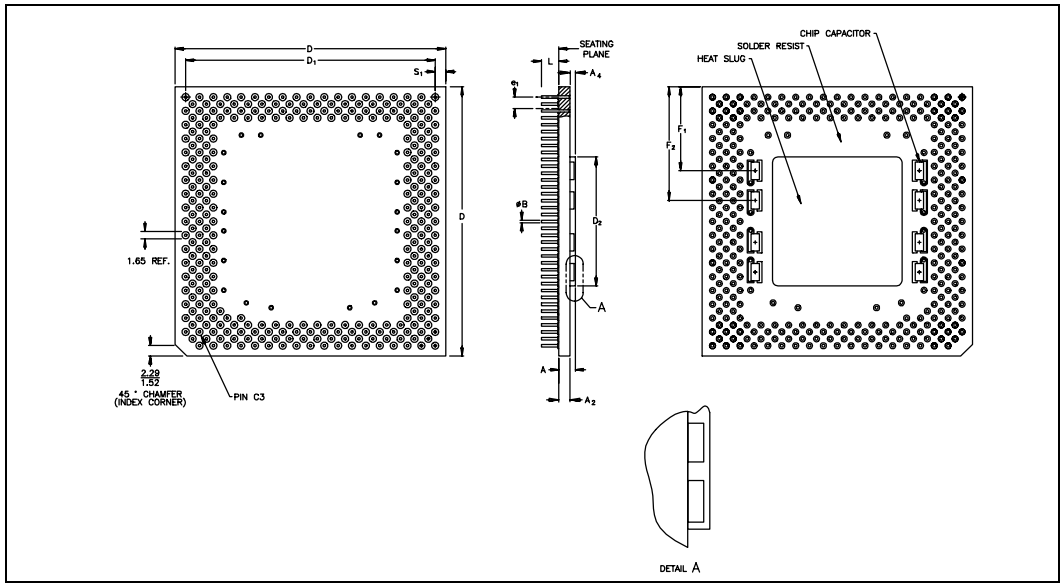


Table 57. PPGA Package Dimensions

Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.72	3.33		0.107	0.131	
A_1	1.83	2.23		0.072	0.088	
A_2	1.00			0.039		
B	0.40	0.51		0.016	0.020	
D	49.43	49.63		1.946	1.954	
D_1	45.59	45.85		1.795	1.805	
D_2	23.44	23.95		0.923	0.943	
e_1	2.29	2.79		0.090	0.110	
F_1	17.56			0.692		
F_2	23.04			0.907		
L	3.05	3.30		0.120	0.130	
N	296		Lead Count	296		Lead Count
S_1	1.52	2.54		0.060	0.100	

8.3 Thermal Specifications

The Pentium processor with MMX technology is specified for proper operation when case temperature, T_{CASE}, (T_C) is within the range of 0° C to 70° C.

The power dissipation specification in Table 58 is provided for designing thermal solutions for operation at a sustained maximum level. This is the worst-case power the device would dissipate in a system for a sustained period of time. This number is provided to assist in the design of a thermal solution for the device.

Table 58. Power Dissipation Requirements for Thermal Design

Measured at V_{CC2}=2.8 V and V_{CC3}=3.3 V

Parameter	Typical (1)	Max (2)	Unit	Notes
Active Power	7.9(3) 7.3(3)	17.0(4) 15.7(4)	Watts Watts	233 MHz 200 MHz
Stop Grant/Auto Halt Powerdown Power		2.61 2.41	Watts Watts	233 MHz, Note 5 200 MHz, Note 5
Stop Clock Power	0.03	< 0.3	Watts	All frequencies, Note 6

NOTES:
1. This is the typical power dissipation in a system. This value is expected to be the average value that will be measured in a system using a typical device at V_{CC2} = 2.8 V running typical applications. This value is highly dependent upon the specific system configuration. Typical power specifications are not tested.
2. Systems must be designed to thermally dissipate the maximum active power dissipation. It is determined using worst case instruction mix with V_{CC2} = 2.8 V and V_{CC3} = 3.3 V and also takes into account the thermal time constants of the package.
3. Active Power (typ) is the average power measured in a system using a typical device running typical applications under normal operating conditions at nominal V_{CC} and room temperature.
4. Active Power (max) is the maximum power dissipation under normal operating conditions at nominal V_{CC2}, worst-case temperature, while executing the worst case power instruction mix. Active power (max) is equivalent to Thermal Design Power (max).
5. Stop Grant/Auto Halt Power Down Power Dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction.
6. Stop Clock Power Dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input.

8.4 Measuring Thermal Values

To verify that the proper T_C is maintained, it should be measured at the center of the package top surface (opposite of the pins). The measurement is made in the same way with or without a heatsink attached. When a heatsink is attached, a hole (smaller than 0.150” diameter) should be drilled through the heatsink to allow probing the center of the package. See Figure 34 for an illustration of how to measure T_C.

To minimize the measurement errors, use the following approach:

- Use 36-gauge or finer diameter K, T, or J type thermocouples. The laboratory testing was done using a thermocouple made by Omega (part number 5TC-TTK-36-36).
- Attach the thermocouple bead or junction to the center of the package top surface using high thermal conductivity cements. The laboratory testing was done by using Omega Bond* (part number OB-100).
- Attach the thermocouple at a 90-degree angle as shown in Figure 34.

- The hole size should be smaller than 0.150” in diameter.
- Make sure there is no contact between thermocouple cement and heatsink base. The contact will affect the thermocouple reading.

8.4.1 Thermal Equations

For the Pentium processor with MMX technology, an ambient temperature, T_A (air temperature around the processor), is not specified directly. The only restriction is that T_C is met. To calculate T_A values, use the following equations:

$T_A = T_C – (P * \theta_{CA})$

$\theta_{CA} = \theta_{JA} - \theta_{JC}$

Where:

T_A and T_C =Ambient and case temperature (°C)

θ_{CA} = Case-to-ambient thermal resistance (ºC/Watt)

θ_{JA} = Junction-to-ambient thermal resistance (ºC/Watt)

θ_{JC} = Junction-to-case thermal resistance (ºC/Watt)

P = Maximum power consumption (Watt)

Table 59 lists the θ_{JC} and θ_{CA} values for the Pentium processor with MMX technology and a passive heatsink. θ_{JC} is thermal resistance from die to package case. θ_{JC} values shown in these tables are typical values. The actual θ_{JC} values depend on actual thermal conductivity and process of die attach. θ_{CA} is thermal resistance from package case to the ambient. θ_{CA} values shown in these tables are typical values. The actual θ_{CA} values depend on the heatsink design, the interface between the heatsink and the package, the air flow in the system, and thermal interactions between the processor and the surrounding components through the printed-circuit board and the ambient air. Figure 35 is a graph of the data from Table 59.

Thermal data collection parameters:

- Heatsinks are omni-directional pin aluminum alloy
- Features were based on standard extrusion practices for a given height
- Pin size ranged from 50 to 129 mils
- Pin spacing ranged from 93 to 175 mils
- Base thickness ranged from 79 to 200 mils
- Heatsink attach was 0.005” of thermal grease
- Attach thickness of 0.002" will improve performance approximately 0.3º C/Watt

Figure 34. Technique for Measuring T_C on PPGA Packages

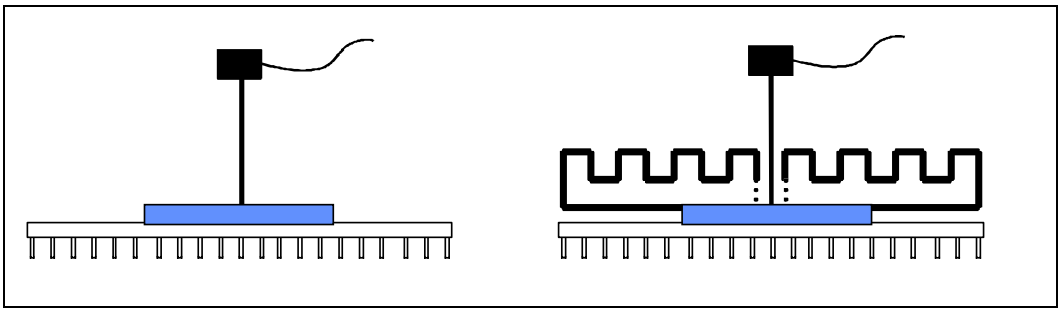


Table 59. Thermal Resistance for PPGA Packages

Heat Sink Height (inches)	θ_{JC} (°C/Watt)	θ_{CA} (°C/Watt) vs. Laminar Airflow (linear ft/min)					
		0	100	200	400	600	800
0.25	0.4	8.9	7.8	6.4	4.3	3.4	2.8
0.35	0.4	8.6	7.3	5.8	3.8	3.1	2.6
0.45	0.4	8.2	6.8	5.1	3.4	2.7	2.3
0.55	0.4	7.9	6.3	4.5	3.0	2.4	2.1
0.65	0.4	7.5	5.8	4.1	2.8	2.2	1.9
0.80	0.4	6.8	5.1	3.7	2.6	2.0	1.8
1.00	0.4	6.1	4.5	3.4	2.4	1.9	1.6
1.20	0.4	5.7	4.1	3.1	2.2	1.8	1.6
1.40	0.4	5.2	3.7	2.8	2.0	1.7	1.5
None	1.2	12.9	12.2	11.2	7.7	6.3	5.4

Figure 35. Thermal Resistance vs. Heatsink Height, PPGA Packages