1.0 Embedded Pentium® Processor Packaging Information

1.1 Pentium® Processor Pinout

Figure 1. Pentium® Processor SPGA Package Pinout (Top Side View)

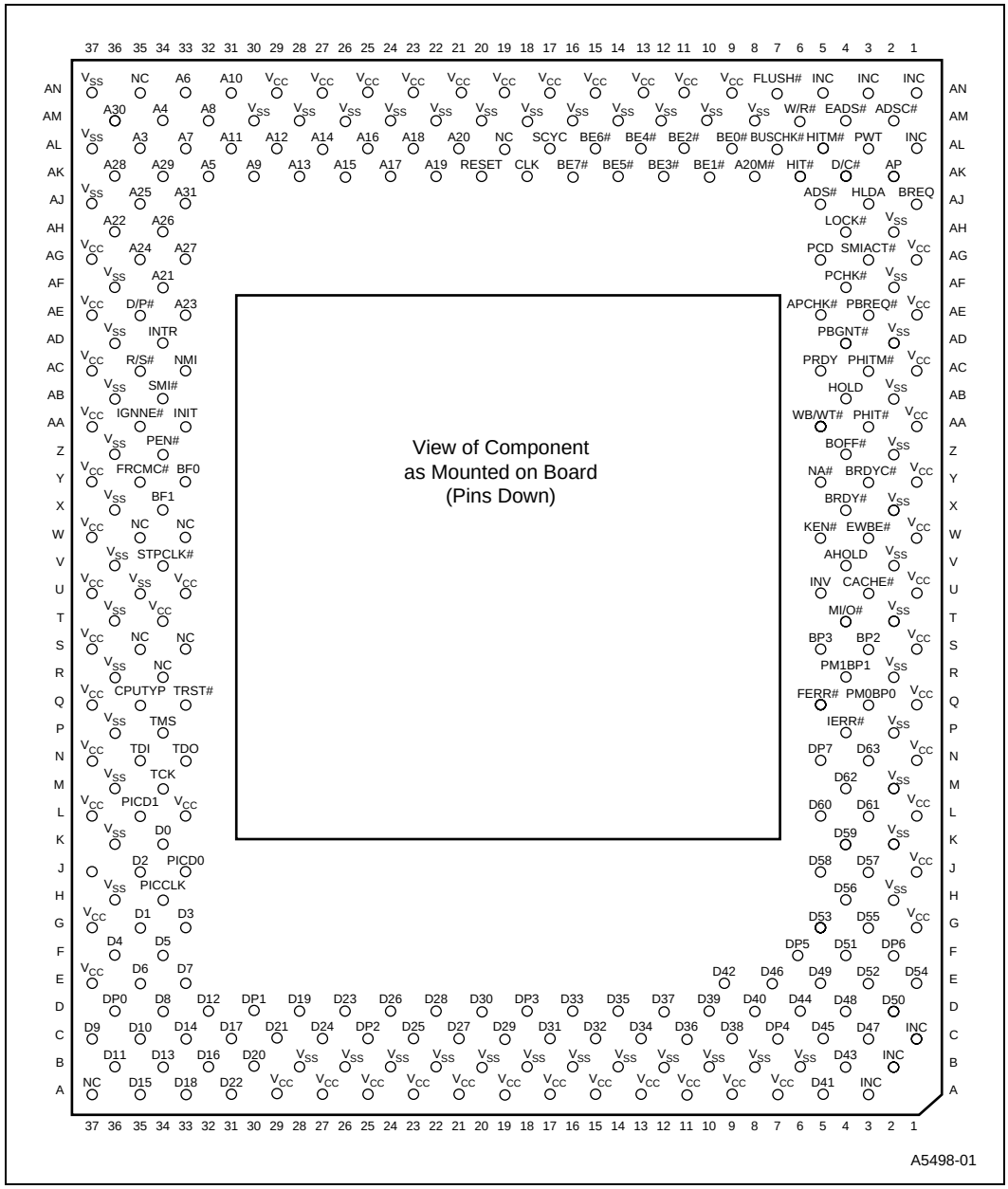
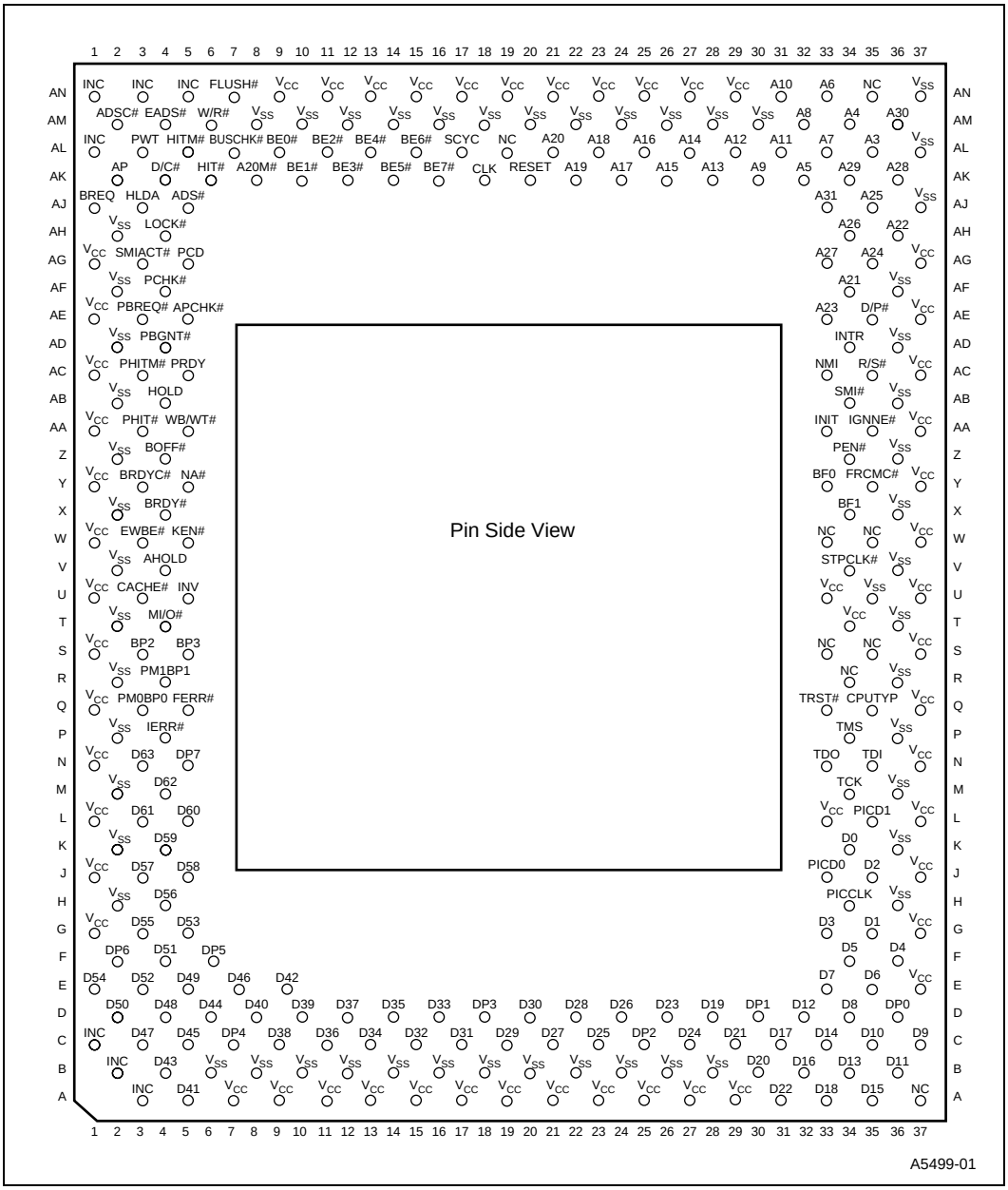


Figure 2. Pentium® Processor SPGA Package Pinout (Pin Side View)



1.1.1 Pin Cross Reference

Table 1. Pin Cross-Reference by Pin Name — Address and Data Pins

Pin	Location	Pin	Location	Pin	Location	Pin	Location	Pin	Location
Address									
A3	AL35	A9	AK30	A15	AK26	A21	AF34	A27	AG33
A4	AM34	A10	AN31	A16	AL25	A22	AH36	A28	AK36
A5	AK32	A11	AL31	A17	AK24	A23	AE33	A29	AK34
A6	AN33	A12	AL29	A18	AL23	A24	AG35	A30	AM36
A7	AL33	A13	AK28	A19	AK22	A25	AJ35	A31	AJ33
A8	AM32	A14	AL27	A20	AL21	A26	AH34		
Data									
D0	K34	D13	B34	D26	D24	D39	D10	D52	E03
D1	G35	D14	C33	D27	C21	D40	D08	D53	G05
D2	J35	D15	A35	D28	D22	D41	A05	D54	E01
D3	G33	D16	B32	D29	C19	D42	E09	D55	G03
D4	F36	D17	C31	D30	D20	D43	B04	D56	H04
D5	F34	D18	A33	D31	C17	D44	D06	D57	J03
D6	E35	D19	D28	D32	C15	D45	C05	D58	J05
D7	E33	D20	B30	D33	D16	D46	E07	D59	K04
D8	D34	D21	C29	D34	C13	D47	C03	D60	L05
D9	C37	D22	A31	D35	D14	D48	D04	D61	L03
D10	C35	D23	D26	D36	C11	D49	E05	D62	M04
D11	B36	D24	C27	D37	D12	D50	D02	D63	N03
D12	D32	D25	C23	D38	C09	D51	F04		

Table 2. Pin Cross-Reference by Pin Name — Control Pins

Pin	Location	Pin	Location	Pin	Location	Pin	Location
A20M#	AK08	BRDYC#	Y03	FLUSH#	AN07	PEN#	Z34
ADS#	AJ05	BREQ	AJ01	FRCMC#	Y35	PM0/BP0	Q03
ADSC#	AM02	BUSCHK#	AL07	HIT#	AK06	PM1/BP1	R04
AHOLD	V04	CACHE#	U03	HITM#	AL05	PRDY	AC05
AP	AK02	CPUTYP	Q35	HLDA	AJ03	PWT	AL03
APCHK#	AE05	D/C#	AK04	HOLD	AB04	R/S#	AC35
BE0#	AL09	D/P#	AE35	IERR#	P04	RESET	AK20
BE1#	AK10	DP0	D36	IGNNE#	AA35	SCYC	AL17
BE2#	AL11	DP1	D30	INIT	AA33	SMI#	AB34
BE3#	AK12	DP2	C25	INTR/ LINT0	AD34	SMIACT#	AG03
BE4#	AL13	DP3	D18	INV	U05	TCK	M34
BE5#	AK14	DP4	C07	KEN#	W05	TDI	N35
BE6#	AL15	DP5	F06	LOCK#	AH04	TDO	N33
BE7#	AK16	DP6	F02	M/IO#	T04	TMS	P34
BOFF#	Z04	DP7	N05	NA#	Y05	TRST#	Q33
BP2	S03	EADS#	AM04	NMI/LINT1	AC33	W/R#	AM06
BP3	S05	EWBE#	W03	PCD	AG05	WB/WT#	AA05
BRDY#	X04	FERR#	Q05	PCHK#	AF04		
APIC							
PICCLK	H34	PICD0/ [DPEN#]	J33	PICD1/ [APICEN]	L35		
Clock Control							
CLK	AK18	BF0	Y33	BF1	X34	STPCLK#	V34
Dual Processor Private Interface							
PBGNT#	AD04	PBREQ#	AE03	PHIT#	AA03	PHITM#	AC03

Table 3. Pin Cross-Reference by Pin Name — Power, Ground and No Connect Pins

V_{CC}								
A07	A19	E37	L33	S01	W01	AC01	AN09	AN21
A09	A21	G01	L37	S37	W37	AC37	AN11	AN23
A11	A23	G37	N01	T34	Y01	AE01	AN13	AN25
A13	A25	J01	N37	U01	Y37	AE37	AN15	AN27
A15	A27	J37	Q01	U33	AA01	AG01	AN17	AN29
A17	A29	L01	Q37	U37	AA37	AG37	AN19	
V_{SS}								
B06	B18	H02	P02	U35	Z36	AF36	AM12	AM24
B08	B20	H36	P36	V02	AB02	AH02	AM14	AM26
B10	B22	K02	R02	V36	AB36	AJ37	AM16	AM28
B12	B24	K36	R36	X02	AD02	AL37	AM18	AM30
B14	B26	M02	T02	X36	AD36	AM08	AM20	AN37
B16	B28	M36	T36	Z02	AF02	AM10	AM22	
NC/INC†								
A03	B02	R34	S35	W35	AL19	AN03	AN35	
A37	C01	S33	W33	AL01	AN01	AN05		

† These pins should be left unconnected. Connection of these pins may result in component failure or incompatibility with processor steppings.

1.1.2 Design Notes

For reliable operation, always connect unused inputs to an appropriate signal level. Unused active low inputs should be connected to V_{CC}. Unused active high inputs should be connected to GND. No Connect (NC) pins must remain unconnected. Connection of NC pins may result in component failure or incompatibility with processor steppings.

1.1.3 Pin Quick Reference

This section gives a brief functional description of each of the pins. For a detailed description, see the *Pentium® Processor Family Developer's Manual* (order number 273204).

Note: All input pins must meet their AC/DC specifications to guarantee proper functional behavior.

The # symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage. When a # symbol is not present after the signal name, the signal is active, or asserted at the high voltage level. Square brackets around a signal name indicate that the signal is defined only at RESET.

The following pins become I/O pins when two Pentium processors are operating in a dual processing environment:

- ADS#, CACHE#, HIT#, HITM#, HLDA#, LOCK#, M/IO#, D/C#, W/R#, SCYC

Table 4. Pin Quick Reference

Symbol	Type†	Name and Function
A20M#	I	When the **address bit 20 mask** pin is asserted, the processor emulates the address wraparound at 1 Mbyte that occurs on the 8086 by masking physical address bit 20 (A20) before performing a lookup to the internal caches or driving a memory cycle on the bus. The effect of A20M# is undefined in protected mode. A20M# must be asserted only when the processor is in real mode. A20M# is internally masked by the processor when configured as a Dual processor.
A31–A3	I/O	As outputs, the **address lines** of the processor along with the byte enables define the physical area of memory or I/O accessed. The external system drives the inquire address to the processor on A31–A5.
ADS#	O	The **address strobe** indicates that a new valid bus cycle is currently being driven by the processor.
ADSC#	O	The **additional address strobe** signal is functionally identical to ADS#. This signal can be used to relieve tight board timings by easing the load on the ADS# signal.
AHOLD	I	In response to the assertion of **address hold**, the processor stops driving the address lines (A31–A3), and AP in the next clock. The rest of the bus remains active so data can be returned or driven for previously issued bus cycles.
AP	I/O	**Address parity** is driven by the processor with even parity information on all processor generated cycles in the same clock in which the address is driven. Even parity must be driven back to the processor during inquire cycles on this pin in the same clock as EADS# to ensure that the correct parity check status is indicated by the processor.
APCHK#	O	The **address parity check** status pin is asserted two clocks after EADS# is sampled active if the processor has detected a parity error on the address bus during inquire cycles. APCHK# remains active for one clock each time a parity error is detected (including during dual processing private snooping).
[APICEN] PICD1	I	**Advanced programmable interrupt controller enable** enables or disables the on–chip APIC interrupt controller. If sampled high at the falling edge of RESET, the APIC is enabled. APICEN shares a pin with the PICD1 signal.
BE7#–BE5# BE4#–BE0#	O I/O	The **byte enable** pins determine which bytes must be written to external memory, or which bytes were requested by the CPU for the current cycle. The byte enables are driven in the same clock as the address lines (A31–A3). The lower four byte enable pins (BE3#–BE0#) are used as APIC ID inputs and are sampled at RESET. In dual processing mode, BE4# is used as an input during Flush cycles.
BF1–BF0	I	**Bus frequency** determines the bus-to-core frequency ratio. BF1–BF0 are sampled at RESET, and cannot be changed until another non-warm (1 ms) assertion of RESET. Additionally, BF1–BF0 must not change values while RESET is active. See Table 5 for bus frequency selections.
BOFF#	I	The **backoff** input is used to abort all outstanding bus cycles that have not yet completed. In response to BOFF#, the processor floats all pins normally floated during bus hold in the next clock. The processor remains in bus hold until BOFF# is negated, at which time the processor restarts the aborted bus cycle(s) in their entirety.
BP3–BP2 PM1/BP1– PM0/BP0	O	The **breakpoint** pins (BP3–BP0) correspond to the debug registers, DR3–DR0. These pins externally indicate a breakpoint match when the debug registers are programmed to test for breakpoint matches. BP1 and BP0 are multiplexed with the **performance monitoring** pins (PM1 and PM0). The PB1 and PB0 bits in the Debug Mode Control Register determine if the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.

† The pins are classified as Input or Output based on their function in Master Mode. See the *Pentium® Processor Family Developer's Manual* (order number 273204) for more information.

Table 4. Pin Quick Reference

Symbol	Type†	Name and Function
BRDY#	I	The **burst ready** input indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted the processor data in response to a write request. This signal is sampled in the T2, T12 and T2P bus states.
BRDYC#	I	The **additional burst ready** signal has the same functionality as BRDY#. This signal can be used to relieve tight board timings by easing the load on the Burst Ready signal.
BREQ	O	The **bus request** output indicates to the external system that the processor has internally generated a bus request. This signal is always driven whether or not the processor is driving its bus.
BUSCHK#	I	The **bus check** input allows the system to signal an unsuccessful completion of a bus cycle. When this pin is sampled active, the processor latches the address and control signals in the machine check registers. When BUSCHK# is asserted and the MCE bit in CR4 is set, the processor vectors to the machine check exception. To ensure that BUSCHK# is always recognized, STPCLK# must be deasserted any time BUSCHK# is asserted by the system, before the system allows another external bus cycle. When BUSCHK# is asserted by the system for a snoop cycle while STPCLK# remains asserted, normally (when MCE=1) the processor vectors to the exception after STPCLK# is deasserted. When another snoop to the same line occurs during STPCLK# assertion, the processor can lose the BUSCHK# request.
CACHE#	O	For processor-initiated cycles, the **cacheability** pin indicates internal cacheability of the cycle (if a read), and indicates a burst write back cycle (if a write). When this pin is driven inactive during a read cycle, the processor does not cache the returned data, regardless of the state of the KEN# pin. This pin is also used to determine the cycle length (number of transfers in the cycle).
CLK	I	The **clock** input provides the fundamental timing for the processor. Its frequency is the operating frequency of the processor's external bus, and requires TTL levels. All external timing parameters except TDI, TDO, TMS, TRST#, and PICD1–PICD0 are specified with respect to the rising edge of CLK. It is recommended that CLK begin toggling within 150 ms after V_{CC} reaches its proper operating level. This recommendation is to ensure long-term reliability of the device.
CPUTYP	I	**CPU type** distinguishes the Primary processor from the Dual processor. In a single processor environment, or when the processor is acting as the Primary processor in a dual processing system, CPUTYP should be strapped to V_{SS}. The Dual processor should have CPUTYP strapped to V_{CC}.
D/C#	O	The **data/code** output is one of the primary bus cycle definition pins. It is driven valid in the same clock in which the ADS# signal is asserted. D/C# distinguishes between data and code or special cycles.
D/P#	O	The **dual/primary** processor indication. The Primary processor drives this pin low when it is driving the bus, otherwise it drives this pin high. D/P# is always driven. D/P# can be sampled for the current cycle with ADS# (like a status pin). This pin is defined only on the Primary processor. Dual processing is supported in a system only if both processors are operating at identical core and bus frequencies. Within these restrictions, two processors of different steppings may operate together in a system.
D63–D0	I/O	These are the 64 **data lines** for the processor. Lines D7–D0 define the least significant byte of the data bus; lines D63–D56 define the most significant byte of the data bus. When the CPU is driving the data lines, they are driven during the T2, T12, or T2P clocks for that cycle. During reads, the CPU samples the data bus when BRDY# is returned.

† The pins are classified as Input or Output based on their function in Master Mode. See the *Pentium® Processor Family Developer's Manual* (order number 273204) for more information.

Table 4. Pin Quick Reference

Symbol	Type†	Name and Function
DP7–DP0	I/O	These are the **data parity** pins for the processor. There is one for each byte of the data bus. They are driven by the Pentium processor with even parity information on writes in the same clock as write data. Even parity information must be driven back to the processor on these pins in the same clock as the data to ensure that the correct parity check status is indicated by the Pentium processor. DP7 applies to D63–D56, DP0 applies to D7–D0.
[DPEN#] PICD0	I/O	**Dual processing enable** is an output of the Dual processor and an input of the Primary processor. The Dual processor drives DPEN# low to the Primary processor at RESET to indicate that the Primary processor should enable dual processor mode. DPEN# may be sampled by the system at the falling edge of RESET to determine if the dual-processor socket is occupied. DPEN# shares a pin with PICD0.
EADS#	I	The **external address strobe** signal indicates that a valid external address has been driven onto the processor address pins to be used for an inquire cycle.
EWBE#	I	The **external write buffer empty** input, when inactive (high), indicates that a write cycle is pending in the external system. When the processor generates a write, and EWBE# is sampled inactive, the processor holds off all subsequent writes to all E- or M-state lines in the data cache until all write cycles have completed, as indicated by EWBE# being active.
FERR#	O	The **floating-point error** pin is driven active when an unmasked floating-point error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using DOS-type floating-point error reporting. FERR# is never driven active by the Dual processor.
FLUSH#	I	When asserted, the **cache flush** input forces the processor to write back all modified lines in the data cache and invalidate its internal caches. A Flush Acknowledge special cycle is generated by the processor to indicate completion of the write back and invalidation. When FLUSH# is sampled low when RESET transitions from high to low, three-state test mode is entered. If two Pentium processors are operating in dual processing mode and FLUSH# is asserted, the Dual processor performs a flush first (without a flush acknowledge cycle), then the Primary processor performs a flush followed by a flush acknowledge cycle. When the FLUSH# signal is asserted in dual processing mode, it must be deasserted at least one clock prior to BRDY# of the FLUSH Acknowledge cycle to avoid DP arbitration problems.
FRCMC#	I	The **functional redundancy checking master/checker** mode input is used to determine whether the processor is configured in master mode or checker mode. When configured as a master, the processor drives its output pins as required by the bus protocol. When configured as a checker, the processor three-states all outputs (except IERR# and TDO) and samples the output pins. The configuration as a master/checker is set after RESET and may not be changed other than by a subsequent RESET.
HIT#	O	The **inquire cycle hit/miss** indication is driven to reflect the outcome of an inquire cycle. If an inquire cycle hits a valid line in either the processor data or instruction cache, this pin is asserted two clocks after EADS# is sampled asserted. If the inquire cycle misses the processor cache, this pin is negated two clocks after EADS#. This pin changes its value only as a result of an inquire cycle and retains its value between the cycles.
HITM#	O	The **inquire cycle hit/miss to a modified line** output is driven to reflect the outcome of an inquire cycle. It is asserted after an inquire cycle that results in a hit to a modified line in the data cache. It is used to inhibit another bus master from accessing the data until the line is completely written back.

† The pins are classified as Input or Output based on their function in Master Mode. See the *Pentium® Processor Family Developer's Manual* (order number 273204) for more information.

Table 4. Pin Quick Reference

Symbol	Type†	Name and Function
HLDA	O	The **bus hold acknowledge** pin goes active in response to a hold request driven to the processor on the HOLD pin. It indicates that the processor has floated most of the output pins and relinquished the bus to another local bus master. When leaving bus hold, HLDA is driven inactive and the processor resumes driving the bus. When the processor has a bus cycle pending, it is driven in the same clock in which HLDA is deasserted.
HOLD	I	In response to the **bus hold request**, the processor floats most of its output and input/output pins and asserts HLDA after completing all outstanding bus cycles. The processor maintains its bus in this state until HOLD is deasserted. HOLD is not recognized during LOCK cycles. The processor recognizes HOLD during reset.
IERR#	O	The **internal error** pin is used to indicate two types of errors, internal parity errors and functional redundancy errors. When a parity error occurs on a read from an internal array, the processor asserts the IERR# pin for one clock and then shuts down. When the processor is configured as a checker and a mismatch occurs between the value sampled on the pins and the corresponding value computed internally, the processor asserts IERR# two clocks after the mismatched value is returned.
LOCK#	O	The **bus lock** pin indicates that the current bus cycle is locked. The processor does not allow a bus hold when LOCK# is asserted (but AHOLD and BOFF# are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the BRDY# is returned for the last locked bus cycle. LOCK# is guaranteed to be deasserted for at least one clock between back-to-back locked cycles.
M/IO#	O	The **memory/input-output** is one of the primary bus cycle definition pins. It is driven valid in the same clock in which the ADS# signal is asserted. M/IO# distinguishes between memory and I/O cycles.
NA#	I	An active **next address** input indicates that the external memory system is ready to accept a new bus cycle although all data transfers for the current cycle have not yet completed. The processor issues ADS# for a pending cycle two clocks after NA# is asserted. The processor supports up to two outstanding bus cycles.
NMI/LINT1	I	The **non-maskable interrupt** request signal indicates that an external non-maskable interrupt has been generated. When the local APIC is enabled, this pin becomes LINT1.
PBGNT#	I/O	When two Pentium processors are configured in dual processing mode, **Private bus grant** is the grant line that is used to perform private bus arbitration. PBGNT# should be left unconnected if only one Pentium processor exists in a system.
PBREQ#	I/O	When two Pentium processors are configured in dual processing mode, **Private bus request** is the request line that is used to perform private bus arbitration. PBREQ# should be left unconnected if only one Pentium processor exists in a system.
PCD	O	The **page cacheability disable** pin reflects the state of the PCD bit in CR3, the Page Directory Entry, or the Page Table Entry. The purpose of PCD is to provide an external cacheability indication on a page-by-page basis.
PCHK#	O	The **data parity check** output indicates the result of a parity check on a data read. It is driven with parity status two clocks after BRDY# is returned. PCHK# remains low one clock for each clock in which a parity error was detected. Parity is checked only for the bytes on which valid data is returned. When two Pentium processors are operating in dual processing mode, PCHK# may be driven two or three clocks after BRDY# is returned.
PEN#	I	The **parity enable** input (along with CR4.MCE) determines whether a machine check exception is taken as a result of a data parity error on a read cycle. When this pin is sampled active in the clock during which a data parity error is detected, the processor latches the address and control signals of the cycle with the parity error in the machine check registers. When PEN# is active and the machine check enable bit in CR4 is set to “1”, the processor vectors to the machine check exception before the beginning of the next instruction.

† The pins are classified as Input or Output based on their function in Master Mode. See the *Pentium® Processor Family Developer’s Manual* (order number 273204) for more information.

Table 4. Pin Quick Reference

Symbol	Type†	Name and Function
PHIT#	I/O	**Private inquire cycle hit/miss** is a hit indication used to maintain local cache coherency when two Pentium processors are configured in dual processing mode. PHIT# should be left unconnected if only one Pentium processor exists in a system.
PHITM#	I/O	**Private inquire cycle hit/miss to a modified line** is a hit indication used to maintain local cache coherency when two Pentium processors are configured in dual processing mode. PHITM# should be left unconnected if only one Pentium processor exists in a system.
PICCLK	I	The APIC interrupt controller serial data bus clock is driven into the **processor interrupt controller clock** input of the processor.
PICD1/[DPEN#]–PICD0/[APICEN]	I/O	**Processor interrupt controller data lines 0–1** of the processor comprise the data portion of the APIC 3-wire bus. They are open-drain outputs that require external pull-up resistors. These signals share pins with DPEN# and APICEN respectively.
PM1/BP1–PM0/BP0	O	These pins function as part of the performance monitoring feature. The breakpoint 1–0 pins are multiplexed with the **performance monitoring 1–0** pins. The PB1 and PB0 bits in the Debug Mode Control Register determine whether the pins are configured as breakpoint or performance monitoring pins. The pins come out of RESET configured for performance monitoring.
PRDY	O	The **probe ready** output pin indicates that the processor has stopped normal execution in response to the R/S# pin going active, or Probe Mode being entered.
SMIACT#	O	An active **system management interrupt active** output indicates that the processor is operating in System Management Mode.
STPCLK#	I	Assertion of the **stop clock** input signifies a request to stop the internal clock of the processor, which causes the core to consume less power. When the processor recognizes STPCLK#, the processor stops execution on the next instruction boundary, unless superseded by a higher priority interrupt, and generates a stop grant acknowledge cycle. When STPCLK# is asserted, the processor still responds to interprocessor and external snoop requests.
TCK	I	The **testability clock input** provides the clocking function for the Pentium processor boundary scan in accordance with the IEEE Boundary Scan interface (Standard 1149.1). It is used to clock state information and data into and out of the processor during boundary scan.
TDI	I	The **test data input** is a serial input for the test logic. TAP instructions and data are shifted into the processor on the TDI pin on the rising edge of TCK when the TAP controller is in an appropriate state.
TDO	O	The **test data output** is a serial output of the test logic. TAP instructions and data are shifted out of the processor on the TDO pin on TCK's falling edge when the TAP controller is in an appropriate state.
TMS	I	The value of the **test mode select** input signal sampled at the rising edge of TCK controls the sequence of TAP controller state changes.
TRST#	I	When asserted, the **test reset** input allows the TAP controller to be asynchronously initialized.
V_{CC}	I	The Pentium processor has 53 3.3 V **power** inputs.
V_{SS}	I	The Pentium processor has 53 **ground** inputs.
W/R#	O	**Write/read** is one of the primary bus cycle definition pins. It is driven valid in the same clock in which the ADS# signal is asserted. W/R# distinguishes between write and read cycles.
WB/WT#	I	The **write back/write through** input allows a data cache line to be defined as write back or write through on a line-by-line basis. As a result, it determines whether a cache line is initially in the S or E state in the data cache.

† The pins are classified as Input or Output based on their function in Master Mode. See the *Pentium® Processor Family Developer's Manual* (order number 273204) for more information.

Table 5. Bus Frequency Selections

Pentium® Processor Core Frequency (max)	External Bus Frequency (max)	Bus/Core Ratio	BF1	BF0
166 MHz	66 MHz	2/5	0	0
133 MHz	66 MHz	1/2	1	0
100 MHz	66 MHz	2/3	1	1

1.1.4 Pin Reference Tables

Table 6. Output Pins

Name	Active Level[1]	When Floated
ADS#[2]	Low	Bus Hold, BOFF#
ADSC#	Low	Bus Hold, BOFF#
APCHK#	Low	
BE7#–BE5#	Low	Bus Hold, BOFF#
BREQ	High	
CACHE#[2]	Low	Bus Hold, BOFF#
D/P#[3]	n/a	
FERR#[3]	Low	
HIT#[2]	Low	
HITM#[2]	Low	
HLDA[2]	High	
IERR#	Low	
LOCK#[2]	Low	Bus Hold, BOFF#
M/IO#[2], D/C#[2], W/R#[2]	n/a	Bus Hold, BOFF#
PCHK#	Low	
BP3–BP2, PM1/BP1, PM0/BP0	High	
PRDY	High	
PWT, PCD	High	Bus Hold, BOFF#
SCYC[2]	High	Bus Hold, BOFF#
SMIACT#	Low	
TDO	n/a	All states except Shift-DR and Shift-IR

NOTES:
1. All output and input/output pins are floated during three-state test mode and checker mode (except IERR#).
2. These are I/O signals when two Pentium processors are operating in dual processing mode.
3. These signals are undefined when the processor is configured as a dual processor.

Table 7. Input Pins

Name	Active Level	Synchronous/ Asynchronous	Internal Resistor	Qualified
A20M#†	Low	Asynchronous		
AHOLD	High	Synchronous		
BF1–BF0	High	Synchronous/RESET	Pullup	
BOFF#	Low	Synchronous		
BRDY#	Low	Synchronous		Bus State T2, T12, T2P
BRDYC#	Low	Synchronous	Pullup	Bus State T2, T12, T2P
BUSCHK#	Low	Synchronous	Pullup	BRDY#
CLK	n/a			
CPUTYP	High	Synchronous/RESET		
EADS#	Low	Synchronous		
EWBE#	Low	Synchronous		BRDY#
FLUSH#	Low	Asynchronous		
FRCMC#	Low	Asynchronous		
HOLD	High	Synchronous		
IGNNE#†	Low	Asynchronous		
INIT	High	Asynchronous		
INTR	High	Asynchronous		
INV	High	Synchronous		EADS#
KEN#	Low	Synchronous		First BRDY#/NA#
NA#	Low	Synchronous		Bus State T2,TD,T2P
NMI	High	Asynchronous		
PEN#	Low	Synchronous		BRDY#
PICCLK	High	Asynchronous	Pullup	
R/S#	n/a	Asynchronous	Pullup	
RESET	High	Asynchronous		
SMI#	Low	Asynchronous	Pullup	
STPCLK#	Low	Asynchronous	Pullup	
TCK	n/a		Pullup	
TDI	n/a	Synchronous/TCK	Pullup	TCK
TMS	n/a	Synchronous/TCK	Pullup	TCK
TRST#	Low	Asynchronous	Pullup	
WB/WT#	n/a	Synchronous		First BRDY#/NA#

† Undefined when the processor is configured as a dual processor.

Table 8. Input/Output Pins

Name	Active Level	When Floated[1]	Qualified (when an input)	Internal Resistor
A31–A3	n/a	Address Hold, Bus Hold, BOFF#	EADS#	
AP	n/a	Address Hold, Bus Hold, BOFF#	EADS#	
BE4#–BE0#	Low	Address Hold, Bus Hold, BOFF#	RESET	Pulldown[2]
D63–D0	n/a	Bus Hold, BOFF#	BRDY#	
DP7–DP0	n/a	Bus Hold, BOFF#	BRDY#	
PICD0[DPEN#]				Pullup
PICD1[APICEN]				Pulldown

NOTES:
1. All output and input/output pins are floated during three-state test mode (except TDO) and checker mode (except IERR# and TDO).
2. BE3#–BE0# have pulldowns during RESET only.

Table 9. Inter-processor Input/Output Pins

Name†	Active Level	Internal Resistor
PHIT#	Low	Pullup
PHITM#	Low	Pullup
PBGNT#	Low	Pullup
PBREQ#	Low	Pullup

† For proper interprocessor operation, the system cannot load these signals.

1.1.5 Pin Grouping According to Function

Table 10. Pin Functional Grouping

Function	Pins
Clock	CLK
Initialization	RESET, INIT, BF1–BF0
Address Bus	A31–A3, BE7#–BE0#
Address Mask	A20M#
Data Bus	D63–D0
Address Parity	AP, APCHK#
APIC Support	PICCLK, PICD1–PICD0
Data Parity	DP7–DP0, PCHK#, PEN#
Internal Parity Error	IERR#
System Error	BUSCHK#
Bus Cycle Definition	M/IO#, D/C#, W/R#, CACHE#, SCYC, LOCK#
Bus Control	ADS#, ADSC#, BRDY#, BRDYC#, NA#
Page Cacheability	PCD, PWT
Cache Control	KEN#, WB/WT#
Cache Snooping/Consistency	AHOLD, EADS#, HIT#, HITM#, INV
Cache Flush	FLUSH#
Write Ordering	EWBE#
Bus Arbitration	BOFF#, BREQ, HOLD, HLDA
Dual Processing Private Bus Control	PBGNT#, PBREQ#, PHIT#, PHITM#
Interrupts	INTR, NMI
Floating-point Error Reporting	FERR#, IGNNE#
System Management Mode	SMI#, SMIACT#
Functional Redundancy Checking	FRCMC# (IERR#)
TAP Port	TCK, TMS, TDI, TDO, TRST#
Breakpoint/Performance Monitoring	PM0/BP0, PM1/BP1, BP3–BP2
Power Management	STPCLK#
Miscellaneous Dual Processing	CPUTYP, D/P#
Probe Mode	R/S#, PRDY

1.2 Mechanical Specifications

The embedded Pentium processor is packaged in a 296-pin ceramic staggered pin grid array (SPGA) package. The pins are arranged in a 37 x 37 matrix and the package dimensions are 1.95" x 1.95" (Table 11). Figure 3 and Table 12 show the package dimensions.

Table 11. Package Information Summary for Pentium® Processor

Package Type		Total Pins	Pin Array	Package Size
Ceramic Staggered Pin Grid Array	SPGA	296	37 x 37	1.95" x 1.95" 4.95 cm x 4.95 cm

Figure 3. SPGA Package Dimensions

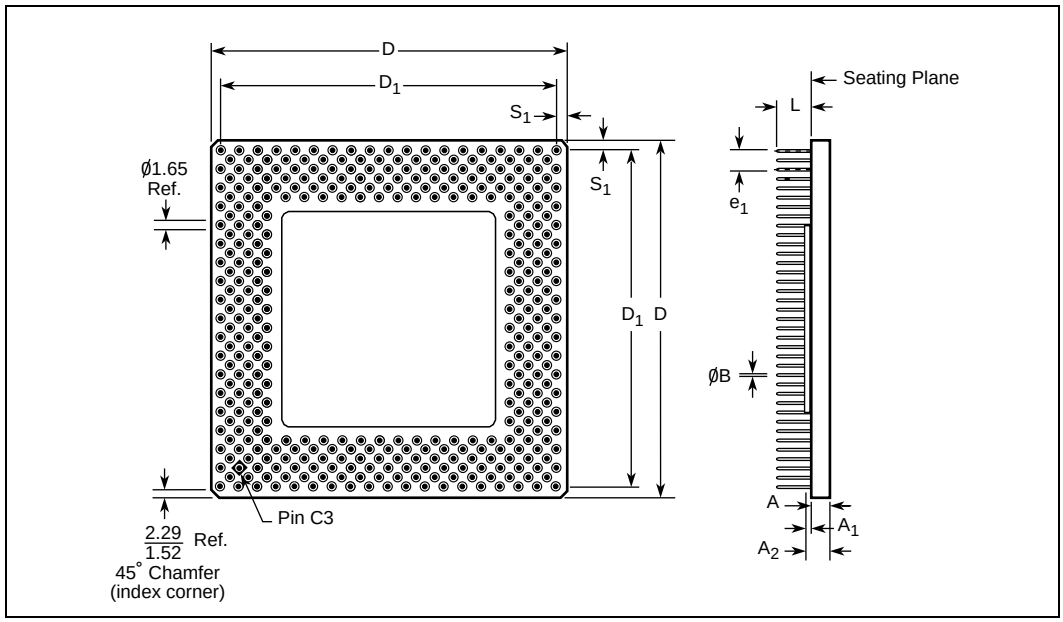


Table 12. SPGA Package Dimensions Key

Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.62	2.97		0.103	0.117	
A_1	0.69	0.84	Metal Lid	0.027	0.033	Metal Lid
A_2	3.31	3.81	Metal Lid	0.130	0.150	Metal Lid
B	0.43	0.51		0.017	0.020	
D	49.28	49.78		1.940	1.960	
D_1	45.59	45.85		1.795	1.805	
e_1	2.29	2.79		0.090	0.110	
L	3.05	3.30		0.120	0.130	
N	296		Lead Count	296		Lead Count
S_1	1.52	2.54		0.060	0.100	

1.3 Thermal Specifications

The Pentium processor is specified for proper operation when case temperature, T_{CASE} (T_C), is within the specified range of 0° C to 70° C.

The power dissipation specification in Table 13 is provided for designing thermal solutions for operation at a sustained maximum level. This is the worst-case power the device would dissipate in a system. This number is used for design of a thermal solution for the device.

Table 13. Power Dissipation Requirements for Thermal Solution Design

Parameter	Typical[1]	Max	Unit	Notes
Active Power Dissipation	5.4 4.3 3.9	14.5[2] 11.2[3] 10.1[3]	Watts	166 MHz 133 MHz 100 MHz
Stop Grant and Auto Halt Powerdown Power Dissipation		2.1 1.7 1.55	Watts	166 MHz, Note 4 133 MHz, Note 4 100 MHz, Note 4
Stop Clock Power Dissipation	0.02	<0.3	Watts	Note 5

NOTES:
1. This is the typical power dissipation in a system. This value was the average value measured in a system using a typical device at nominal V_{CC} (3.3 V for 100 and 133 MHz processors and 3.5 V for 166 MHz processors) running typical applications. This value is highly dependent upon the specific system configuration.
2. Systems must be designed to thermally dissipate the maximum active power of the device. It is determined using a worst-case instruction mix with V_{CC}=3.5 V, and also takes into account the thermal time constants of the package.
3. Systems must be designed to thermally dissipate the maximum active power of the device. It is determined using a worst case instruction mix with V_{CC} = 3.3 V and also takes into account the thermal time constants of the package.
4. Stop Grant/Auto Halt Powerdown power dissipation is determined by asserting the STPCLK# pin or executing the HALT instruction.
5. Stop Clock power dissipation is determined by asserting the STPCLK# pin and then removing the external CLK input.

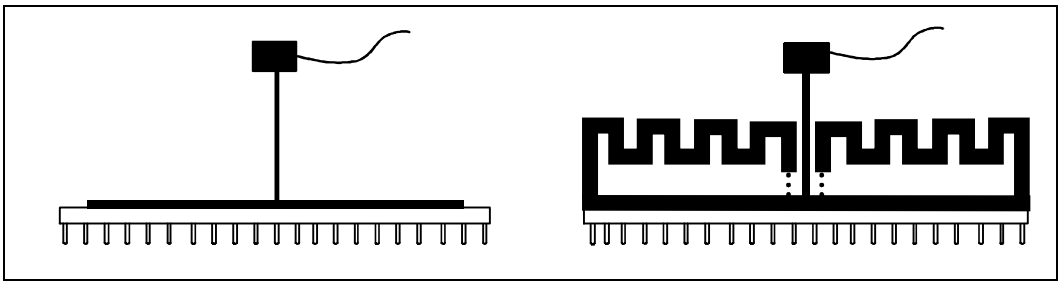
1.3.1 Measuring Thermal Values

To verify that the proper T_C (case temperature) is maintained, it should be measured at the center of the package top surface (opposite of the pins). The measurement is made in the same way with or without a heatsink attached. When a heatsink is attached, a hole (0.150" diameter or smaller) should be drilled through the heatsink to allow a probe to touch the center of the package. See Figure 4 for an illustration of how to measure T_C.

To minimize the measurement errors, use the following approach:

- Use 36-gauge or finer diameter K, T, or J type thermocouples.
- Attach the thermocouple bead or junction to the center of the package top surface using high thermal conductivity cements.
- Attach the thermocouple at a 90-degree angle as shown in Figure 4.
- The hole size should be 0.150" or less in diameter.

Figure 4. Technique for Measuring Case Temperature (T_C)



1.3.2 Thermal Equations And Data

For the Pentium processor, an ambient temperature, T_A (air temperature around the processor), is not specified directly. The only restriction is that the case temperature (T_C) is met. To calculate T_A values, use the following equations:

$T_A = T_C - (P * \theta_{CA})$

$\theta_{CA} = \theta_{JA} - \theta_{JC}$

where:

T_A and T_C =	ambient and case temperature (°C)
θ_{CA} =	case-to-ambient thermal resistance (°C/W)
θ_{JA} =	junction-to-ambient thermal resistance (°C/W)
θ_{JC} =	junction-to-case thermal resistance (°C/W)
P =	maximum power consumption in Watts (see Table 13)

Table 14 lists the θ_{CA} values for the Pentium processor with passive heatsinks.

Thermal data collection parameters:

- Heatsinks are omnidirectional pin aluminum alloy
- Features were based on standard extrusion practices for a given height
- Pin size ranged from 50 to 129 mils
- Pin spacing ranged from 93 to 175 mils
- Base thickness ranged from 79 to 200 mils
- Heatsink attach was 0.005" of thermal grease
- Using an attach thickness of 0.002” improves performance by approximately 0.3 °C/W

Table 14. Thermal Resistances for Embedded Pentium® Processors

Heatsink Height in Inches	θ_{JC} (°C/Watt)	θ_{CA}(°C/Watt) vs. Laminar Airflow (Linear ft/min)					
		0	100	200	400	600	800
0.25	1.25	9.4	8.3	6.9	4.7	3.9	3.3
0.35	1.25	9.1	7.8	6.3	4.3	3.6	3.1
0.45	1.25	8.7	7.3	5.6	3.9	3.2	2.8
0.55	1.25	8.4	6.8	5.0	3.5	2.9	2.6
0.65	1.25	8.0	6.3	4.6	3.3	2.7	2.4
0.80	1.25	7.3	5.6	4.2	2.9	2.5	2.3
1.00	1.25	6.6	4.9	3.9	2.9	2.4	2.1
1.20	1.25	6.2	4.6	3.6	2.7	2.3	2.1
1.40	1.25	5.7	4.2	3.3	2.5	2.2	2.0
Without Heatsink	1.7	14.5	13.8	12.6	10.5	8.6	7.5