Embedded Processor Module Evaluation Platform

Developer's Manual

April 1998

Order Number: 273122-004

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About This Manual 1

This manual tells you how to set up and use the Embedded Processor Module Evaluation Platform.

1.1 Content Overview

Chapter 1, “About This Manual” - This chapter contains a description of conventions used in this manual. The last few sections tell you how to obtain literature and contact customer support.

Chapter 2, “Getting Started” - Provides complete instructions on how to configure the board by setting jumpers, providing power, connecting peripherals, and configuring the BIOS.

Chapter 3, “Theory Of Operation” - This chapter provides information on the system design.

Chapter 4, “Hardware Reference” - This chapter provides a description of jumper settings and functions, and pinout information for each connector.

Chapter 5, “BIOS Quick Reference” - This chapter describes how to configure the BIOS for your system configuration. A summary of all BIOS menu options is provided.

Appendix A, “PLD Code Listing” - This appendix includes a sample code listing for the Post Code Debugger and the M-Systems DiskOnChip* chip select.

Appendix B, “Bill of Materials” - This appendix contains the bill of materials for the development platform.

Appendix C, “Schematics” - This appendix contains schematics for selected connectors and subsystems for the development platform.

1.2 Text Conventions

The following notations are used throughout this manual.

#	The pound symbol (#) appended to a signal name indicates that the signal is active low.
Variables	Variables are shown in italics. Variables must be replaced with correct values.
New Terms	New terms are shown in italics. See the Glossary for a brief definition of commonly used terms.
Instructions	Instruction mnemonics are shown in uppercase. When you are programming, instructions are not case-sensitive. You may use either upper- or lowercase.

Numbers Hexadecimal numbers are represented by a string of hexadecimal digits followed by the character *H*. A zero prefix is added to numbers that begin with *A* through *F*. (For example, *FF* is shown as *0FFH*.) Decimal and binary numbers are represented by their customary notations. (That is, 255 is a decimal number and 1111 1111 is a binary number. In some cases, the letter *B* is added for clarity.)

Units of Measure The following abbreviations are used to represent units of measure:

A	amps, amperes
Gbyte	gigabytes
Kbyte	kilobytes
KΩ	kilo-ohms
mA	milliamps, milliamperes
Mbyte	megabytes
MHz	megahertz
ms	milliseconds
mW	milliwatts
ns	nanoseconds
pF	picofarads
W	watts
V	volts
µA	microamps, microamperes
µF	microfarads
µs	microseconds
µW	microwatts

Signal Names Signal names are shown in uppercase. When several signals share a common name, an individual signal is represented by the signal name followed by a number, while the group is represented by the signal name followed by a variable (*n*). For example, the lower chip-select signals are named CS0#, CS1#, CS2#, and so on; they are collectively called CS*n*#. A pound symbol (#) appended to a signal name identifies an active-low signal. Port pins are represented by the port abbreviation, a period, and the pin number (e.g., P1.0).

1.3 Related Documents

Document Name	Order Number
Intel Embedded Processor Module datasheet	273105
Intel Embedded Processor Module Design Guide	273120
Intel Embedded Processor Module (EMBMOD133) Thermal Design Guide	273143
Pentium® Processor with Voltage Reduction Technology at 75/100/120/133/150 MHz datasheet	242557
Pentium® Processor Family Developer's Manual	241428
Intel Architecture Software Developer's Manual (Vols. 1 and 2)	243190 and 243191
Intel 430HX PCIset 82439HX System Controller (TXC) datasheet	290551
Intel 430HX PCIset 82439HX System Controller (TXC) Timing Specification	272945
Intel 430HX PCIset Design Guide	297467

1.4 Electronic Support Systems

Intel's FaxBack* service provides up-to-date technical information. Intel also offers a variety of information on the World Wide Web. These systems are available 24 hours a day, 7 days a week, providing technical information whenever you need it.

1.4.1 FaxBack Service

FaxBack is an on-demand publishing system that sends documents to your fax machine. You can get product announcements, change notifications, product literature, device characteristics, design recommendations, and quality and reliability information from FaxBack 24 hours a day, 7 days a week.

1-800-525-3019 (US or Canada)
+44-1793-496646 (Europe)
+65-256-5350 (Singapore)
+852-2-844-4448 (Hong Kong)
+886-2-514-0815 (Taiwan)
+822-767-2594 (Korea)
+61-2-975-3922 (Australia)
1-503-264-6835 (Worldwide)

Think of the FaxBack service as a library of technical documents that you can access with your phone. Just dial the telephone number and respond to the system prompts. After you select a document, the system sends a copy to your fax machine.

1.4.2 World Wide Web

Intel offers a variety of information through the World Wide Web (http://developer.intel.com/).

1.4.3 Technical Support

In the U.S. and Canada, technical support representatives are available to answer your questions between 5 a.m. and 5 p.m. PST. You can also fax your questions to us. (Please include your voice telephone number and indicate whether you prefer a response by phone or by fax). Outside the U.S. and Canada, please contact your local distributor.

1-800-628-8686	U.S. and Canada
916-356-7599	U.S. and Canada
916-356-6100 (fax)	U.S. and Canada

1.5 Product Literature

Copies of Intel documents may be obtained by calling 1-800-548-4725, or you can download them from Intel's website at http://developer.intel.com.

Getting Started 2

This chapter identifies the Embedded Processor Module Evaluation Platform Kit's key components, features and specifications, and tells you how to set up the board for operation.

2.1 Overview

The evaluation board supports Embedded Processor Modules based on the Intel 430HX PCIset chipset. When you use an Embedded Processor Module the high-speed elements of your design are already done. This reduces your product's time-to-market, and ensures a more reliable design.

The evaluation board has these features:

- ATX Form Factor
- Embedded Processor Module:
  - — The Embedded Processor Module included in the kit is populated with an ITP debug port. (Note that the ITP port on the *production* version of the module is *not* populated.)
- Flash System BIOS ROM:
  - — PhoenixPICO* System BIOS
  - — PhoenixPICO BIOS setup utility
  - — In-circuit BIOS upgradability
- Memory:
  - — 32 Mbyte (4 Mbit x 72) DIMM included (3.3 V, 60 ns, single sided, unbuffered, EDO, ECC)
  - — 2 Slots (supports a maximum of 512 Mbytes of memory)

The peripherals feature set includes:

- On-board 3D Video with 2 Mbyte SGRAM (S3 Virge* GX)
- PC87307 Super I/O* with integrated Keyboard Controller and RTC
- Support for single IDE bus (Primary)
- Support for floppy drive

User-accessible on-board connectors include:

- Two serial RS-232 ports; COM1, COM2
- One EPP/ECP parallel port (DSUB 25)
- Supports PS/2 keyboard and PS/2 mouse (6-pin mini-DIN connector)
- Two USB ports
- VGA display connector (15-pin HD DShell)

- Four PCI expansion slots and two ISA expansion slots. Usage is limited to four PCI and one ISA or three PCI and two ISA.
- Standard ATX power supply connector

Miscellaneous features include:

- On-board post code debugger (Port 80)
- Reset push button
- Stand-off feet for table-top operation

Discovery software from the following companies is included in your kit:

- QNX Software Systems, Ltd.
- Radisys Corporation
- Intrinsic Software, Inc.
- Cogent Real-Time Systems, Inc.
- VenturCom, Inc.
- Spectron Microsystems, Inc.
- WindRiver Systems

2.2 Included Hardware

- Evaluation board
- Intel Embedded Processor Module
- Power Interposer Card
- 32-Mbyte DIMM
- One M-Systems 40-Mbyte DiskOnChip*
- Mounting hardware
- Schematics

2.3 Software Key Features

The software in the kit was chosen to facilitate development of real-time applications with the Embedded Processor Module and the evaluation platform. The tools in the kit are described in this section.

Note: Software in the kit has been provided free by the vendor and is only licensed for evaluation purposes. Customers using the tools that work with Microsoft products must have licensed those products. Any targets created by those tools should also have appropriate licenses.

WinCE* is not included in the kit, but it has been evaluated for the platform. The generic WinCE demo builds work on the evaluation platform without any modifications. Look for future WinCE tools which may be posted to the Intel developer's web site under product information for this kit.

2.3.1 QNX Software Systems, Ltd.

QNX Real Time Operating System for Intel Architecture.

- Small memory footprint of the QNX operating system with microGUI
- QNX microGUI is a full featured Graphical User Interface (GUI) and windowing system
- Photon Application Builder
- QNX Development kit provides the basic utilities to build and program Intel Flash
- Watcom C/C++ Development Suite: is a full featured development suite
- Includes compiler, assembler and debugger with full support for the QNX microGUI function library
- Makes development of the QNX executables fast, easy and optimized

2.3.2 Cogent Real-Time Systems, Inc.

Cogent's Slang* Programming Language for QNX and the Photon microGUI.

- Rapid Application Development language that significantly reduces the time-to-market and after-market maintenance
- Provides a programming environment similar to C and C++, but includes considerable functionality not available in these languages
- Simplifies QNX and Photon programming
- Allows developers to modify applications *on the fly*, without interrupting or restarting the target application

2.3.3 RadiSys Corporation

INtime*: Get real-time control with industry standard Windows NT.

- Field-proven real-time technology to maximize the reliability of your products
- Win32 API extensions provide real-time capabilities in a Windows NT environment
- Robust, non-intrusive integration with Windows NT ensures continued future compatibility with Windows NT
- Fully featured, high-end real-time capabilities for even the most demanding applications
- Fully integrated with Microsoft Visual Developer Studio C/C++, including real-time Wizard extensions
- Patented architecture provides protected real-time execution
- Full memory protection for real-time kernel and real-time tasks
- Ensures survival of real-time threads in event of total Windows failure

2.3.4 Intrinsyc Software, Inc.

Integration Expert* (IX): IX is an integrated software development environment that enables developers of Win32 embedded applications to improve design productivity while maximizing system reliability. IX provides software component analysis and management capabilities that simplify the tasks associated with embedded application development, operating system configuration, and target generation and deployment.

- Support for Win32 OS and versions: Windows 95 and NT
- Operating system and version independent
- Automated OS/application dependency analysis, conversion, and reduction
- Integration with Microsoft Developer Studio* and RadiSys' INtime
- Component gallery of commercial off-the-shelf software components
- Target Wizard: Configurable application options and proper definition of the target systems configuration
- Generate minimal bootable images for disk, flash, network, or CD-ROM

2.3.5 VenturCom, Inc.

2.3.5.1 Real-Time Extension* (RTX)

- Delivers real-time response for Windows NT applications
- Deterministic response times
- Fixed-priority scheduling with 128 priorities
- IPC with semaphores, mail slots, and shared memory objects
- Real-time process and thread management
- Memory locking, mapping and management functions
- High-speed clocks and timers
- Perform direct I/O register reads and writes
- Manage hardware interrupts

2.3.5.2 Component Integrator* (CI)

- Configuration management tools to efficiently build dedicated Windows NT systems
- Import custom applications and commercial-off-the-shelf components
- Build embedded Windows NT systems
- Utilize VenturCom's embedded and real-time extensions
- Analyze RAM and persistent storage requirements
- Validate system completeness
- Preconfigure operating system and applications

2.3.6 Phoenix Technologies, Ltd.

PhoenixPICO BIOS for the Intel Pentium® processor and Intel 430HX PCIset chipset

- Industry standard PhoenixPICO BIOS, PM*, and X^{ROM*} code
- Powerful PhoenixPICO software enhancements

2.3.7 Spectron Microsystems, Inc.

IA-SPOX* Real Time Native Signal Processing Software for Windows95.

IA-SPOX is based on Spectron's industry-standard SPOX* real-time operating system for digital signal processors. IA-SPOX brings a real-time multi-tasking kernel and other real-time services, including low latency device drivers, to Windows 95, enabling a new generation of real-time industrial control, soft instrumentation, test measurement, machine vision, servo controls, communications, multi-media, and other low latency signal processing applications.

2.3.8 WindRiver Systems

Tornado* Evaluation Kit 1.0.1; Tornado Development Environment

- A superior development and deployment platform for the embedded developer
- Makes all tools available regardless of target resources or connection strategy
- Runs on UNIX workstation or PCs using Microsoft Windows 95 or Windows NT
- Offers published APIs for easy customization and third-party tool integration
- Provides central "control panel" and productivity-enhancing GUI
- Supports industry standards including ANSI-C, POSIX, and Tcl
- Includes the proven, high-performance VxWorks* operating system
- Scalable across all real-time implementations

2.4 Before You Begin

Before you set up and configure your evaluation board, you may want to gather some additional hardware and software.

VGA Monitor	You can use any standard VGA or multi-resolution monitor. The setup instructions in this chapter assume that you are using a standard VGA monitor.
Power Supply	You must use an ATX-type PC power supply.
Keyboard	You need a keyboard with a PS/2 style connector or adapter.
Mouse	Optional. You can use a mouse with a PS/2 style connector or adapter.
Storage Device	Choose a storage device to load an operating system. • You can use the included DiskOnChip. Instructions for how to do this appear later in this chapter. • You can use an IDE hard disk drive. Two devices (master & slave) can be attached to the IDE connector. • You can use a floppy drive. You may have all these storage devices attached to the board at the same time.
Other Devices and Adapters	The Evaluation Board with an Intel Embedded Processor Module installed behaves much like a standard desktop computer motherboard. Most PC compatible peripherals can be attached and configured to work with the evaluation board. For example, you may want to install a sound card or an enhanced video adapter.

2.5 Setting up the Board

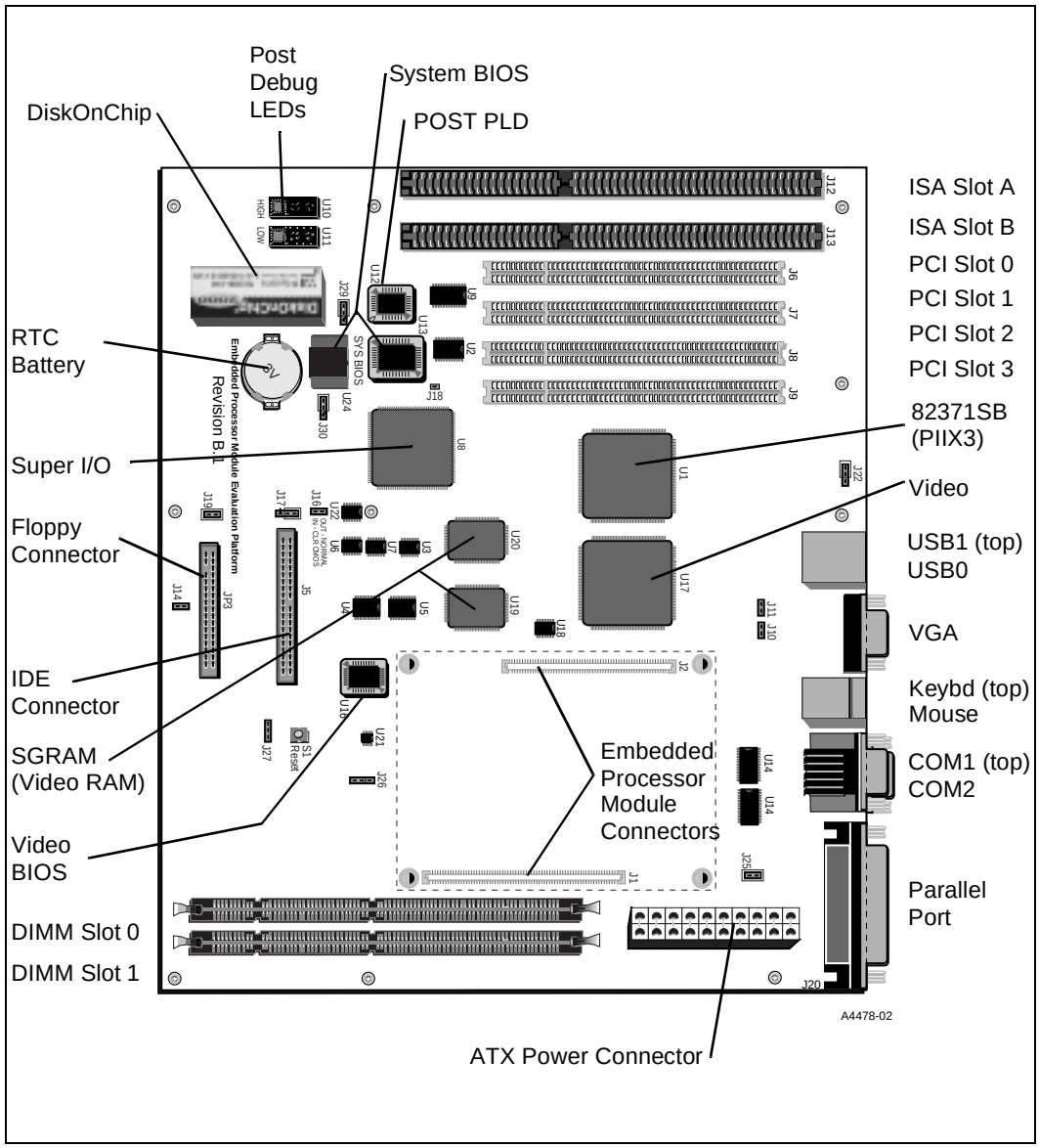
Once you have gathered the hardware described in the last section, follow the steps below to set up your evaluation board. This manual assumes you are familiar with basic concepts involved with installing and configuring hardware for a personal computer system.

Refer to Figure 2-1 for locations of connectors, jumpers, etc.

1. Make sure you are in a static-free environment before removing any components from their anti-static packaging. The evaluation board is susceptible to electro-static discharge damage; such damage may cause product failure or unpredictable operation.
2. Inspect the contents of your kit. Check for damage that may have occurred during shipment. Contact your sales representative if any items are missing or damaged.

Caution: Connecting the wrong cable or reversing the cable can damage the evaluation board and may damage the device being connected. Since the board is not in a protective chassis, use caution when preparing to connect cables to this product.

Figure 2-1. Embedded Processor Module Evaluation Board



3. Make sure the board's jumpers are set to the following default locations.
   - J10, J11, J14 and J16 — No jumper
   - J17, J22, J29 and J30 — Jumper pins 1-2
   - J26 — Refer to the datasheet for the module's voltage, then set the jumper as shown:
     - — For the Embedded Processor Module with 2.9 V core voltage, jumper pins 1-2
     - — For the Embedded Processor Module with 2.45 V core voltage, jumper pins 2-3
   - J19 and J25 — Both pins jumpered

4. Connect desired storage devices to the evaluation board:

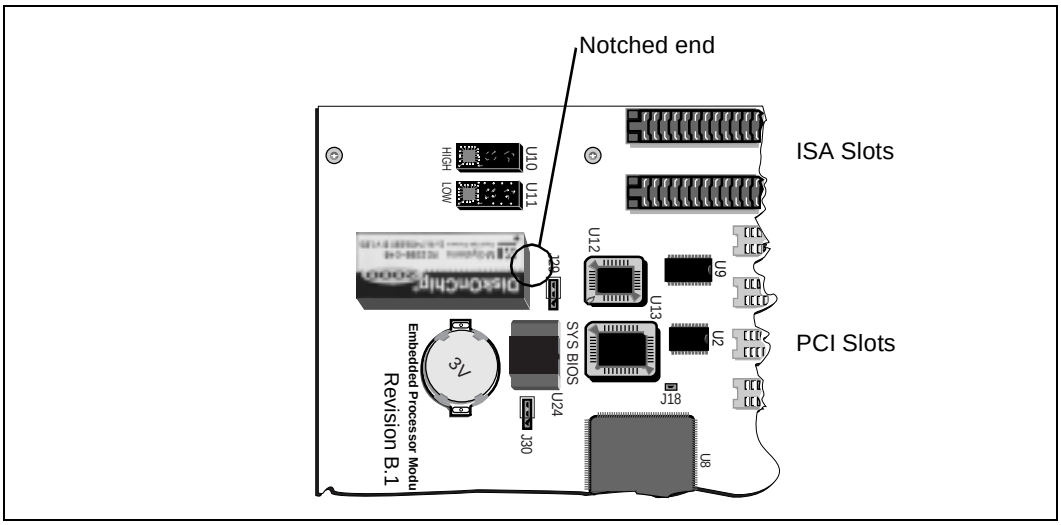
   The evaluation board supports a single (Primary) IDE interface that can host 1 or 2 devices (master/slave). When you are using 2 devices (such as a hard disk and a CD), make sure the hard disk has a jumper in the master position and the CD has a jumper in the slave position. When you are using a single IDE device with the evaluation board, be sure that there are no jumpers in either the master or slave positions on the hard disk.

   - Installing an IDE hard disk drive:
     - — Connect the hard drive's IDE connector to the J5 connector on the evaluation board. Be sure to align Pin 1 of the cable connector with pin 1 of J5.

Caution: Make sure the tracer on the ribbon cable is aligned with pin 1 on both the hard disk and the header. Connecting the cable backwards can damage the evaluation board.

   - — Connect the hard drive to the power supply.
   - — Format the hard disk according to the manufacturer's instructions.
   - — You may have to make changes to the system BIOS to enable this hard disk.
   - Installing the supplied DiskOnChip component:
     - — Orient the DiskOnChip component as shown in Figure 2-2.

Figure 2-2. Installing the DiskOnChip



   - — Insert the DiskonChip device into the socket at location U23 on the evaluation board. Ensure the device's pin 1 marking matches with the notched end of the socket at U23. This notched end of the socket is pointing toward the evaluation board's expansion PCI connectors.

Warning: Inserting the DiskonChip component onto the card without matching the device's pin 1 to the notched end of the socket at U23 can damage the DiskOnChip.

   - — To enable the DiskonChip, you'll have to make changes to the BIOS settings. The changes required are described in the M-Systems DiskOnChip manual included in your kit.

- Floppy drive: A floppy disk drive connected to the evaluation board is the most direct method for loading software.
  - — Insert floppy cable into JP3 (be sure to orient Pin 1 correctly).
  - — Connect a power cable to the floppy drive.
  - — You have to make changes to the system BIOS to enable this floppy disk.

5. Mount or install the evaluation board:
   - Table-top Operation: The evaluation board is shipped with standoff "feet" for use in a table-top environment. These feet are installed on the evaluation platform to raise it off the table surface.
   - The evaluation board can also be mounted in a standard ATX type chassis
6. Make sure the DRAM DIMM is installed in the socket labeled Slot 0. The board uses 3.3 V, EDO, single-sided, 60 ns DIMMs. The evaluation board is shipped with 32 Mbytes of ×72 ECC memory but can also support regular ×64 memory.
7. Connect a VGA monitor, PS/2 mouse and keyboard (see Figure 2-1 for connector locations).

Note: J15 is a stacked PS/2 connector. The bottom connector is for the mouse and the top is for the keyboard.

8. Install the Embedded Processor Module (EPM):

Warning: Always turn off the power before you insert or remove the module.

The Embedded Processor Module (shown in Figure 2-3), contains the processor, cache, 82439HX System Controller, clocks, and core voltage regulator. It is populated with an ITP connector to interface to an ITP debugger. The module connects to the evaluation board via two high density connectors (shown in Figure 2-4). One is a 140-pin connector and the other is a 120-pin connector.

- Hold the module with the silkscreen text facing up. Use the arrows in Figure 2-3 and Figure 2-4 to orient the module for insertion.
- (Optional) If you will be using the ITP debugger, insert the cable now. See "Post Code Debugger" on page 3-4 for more details on the debugger.
- (Optional) If you will be using the power interposer card, socket the EPM into the power interposer card. Make sure the EPM is inserted into the side of the interposer card labeled TOP: THIS SIDE UP. Now socket this assembly into the evaluation board. Support the evaluation board from underneath while inserting the assembly. See "Measuring Module Current" on page 3-6 for more information about using the power interposer card.
- Support the evaluation board from below and insert the module. Refer to Figure 2-3 and Figure 2-4 for proper board and module orientation. The connector size and orientation only allows you to insert the module one way. Excessive flexing of the evaluation board may cause damage.

Figure 2-3. Embedded Processor Module Detail

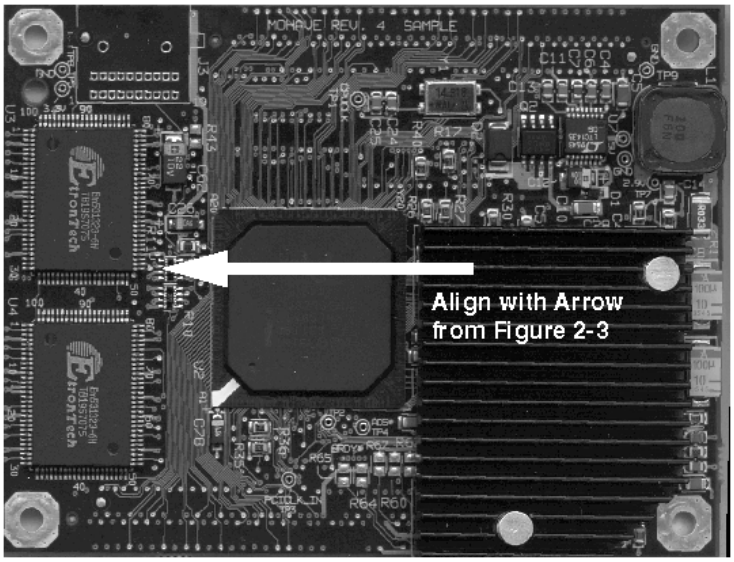
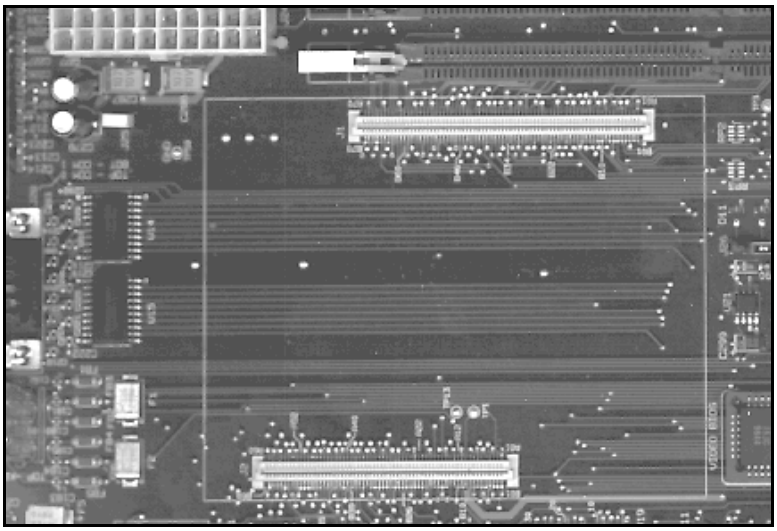


Figure 2-4. Evaluation Board Connector Detail



9. Install the fan included with your kit:
   a. Attach the fan onto the Embedded Processor Module heat-sink using the double-sided tape provided.
   b. Plug the fan's power connector into a power connector from the power supply.

10. Connect the power supply:

    You'll need a standard ATX PC power supply. Make sure the power supply is unplugged (or turned off), then connect the power supply cable to the power header (J24). See Figure 2-4 for connector orientation.

Note: Some ATX power supplies do not have an on/off switch. In this case remove jumper J25 before plugging in the ATX power connector. J25 controls an internal power supply on/off switch. When you are ready to apply power, insert the jumper. You may want to wire this header up to a toggle switch for convenience.

When the power is on you should see three power-indicator LEDs light up (located next to the ATX power connector in the upper right corner of the board, see Figure 2-1). The three LEDs show 5 V, 3.3 V and Core Voltage (in the case of the EPM this is either 2.45 V or 2.9 V). Check to see that the strap-on fan is operating.

Follow the instructions in the next section for entering the BIOS setup screens and configuring the BIOS according to your needs (hard drive parameters, floppy drive, operating system, etc.).

2.6 Configuring the BIOS

PhoenixPICO BIOS software is pre-loaded on the evaluation board. The BIOS defaults should work for most basic system configurations. You may have to make changes to the BIOS to enable other supported features (see next section). You can use the Setup program to modify BIOS settings and control the special features of the system. Setup options are configured through a menu-driven user interface. Chapter 5, "BIOS Quick Reference" contains a description of BIOS options.

BIOS updates may periodically be posted to the Developers' site at http://www.intel.com.

2.6.1 BIOS Defaults

By default the BIOS on the evaluation board is properly configured for the EPM Evaluation Platform Kit. There are two important exceptions:

- By Default ECC is Disabled — To enable ECC, press <F2> during startup to enter the BIOS setup screen. Select the Advanced menu and then the Advanced Chipset Control sub-menu. Highlight ECC/Parity Config and use the -/+ keys to select ECC.
- The evaluation board does not implement any power management features. This is despite the fact that a Power menu may appear during BIOS setup. All selections on this menu should be disabled with the exception of IRQ1.

2.7 DiskOnChip Setup Instructions

Refer to the M-Systems DiskOnChip manual included in your kit for installation instructions.

2.8 Changing the Default Video Drivers

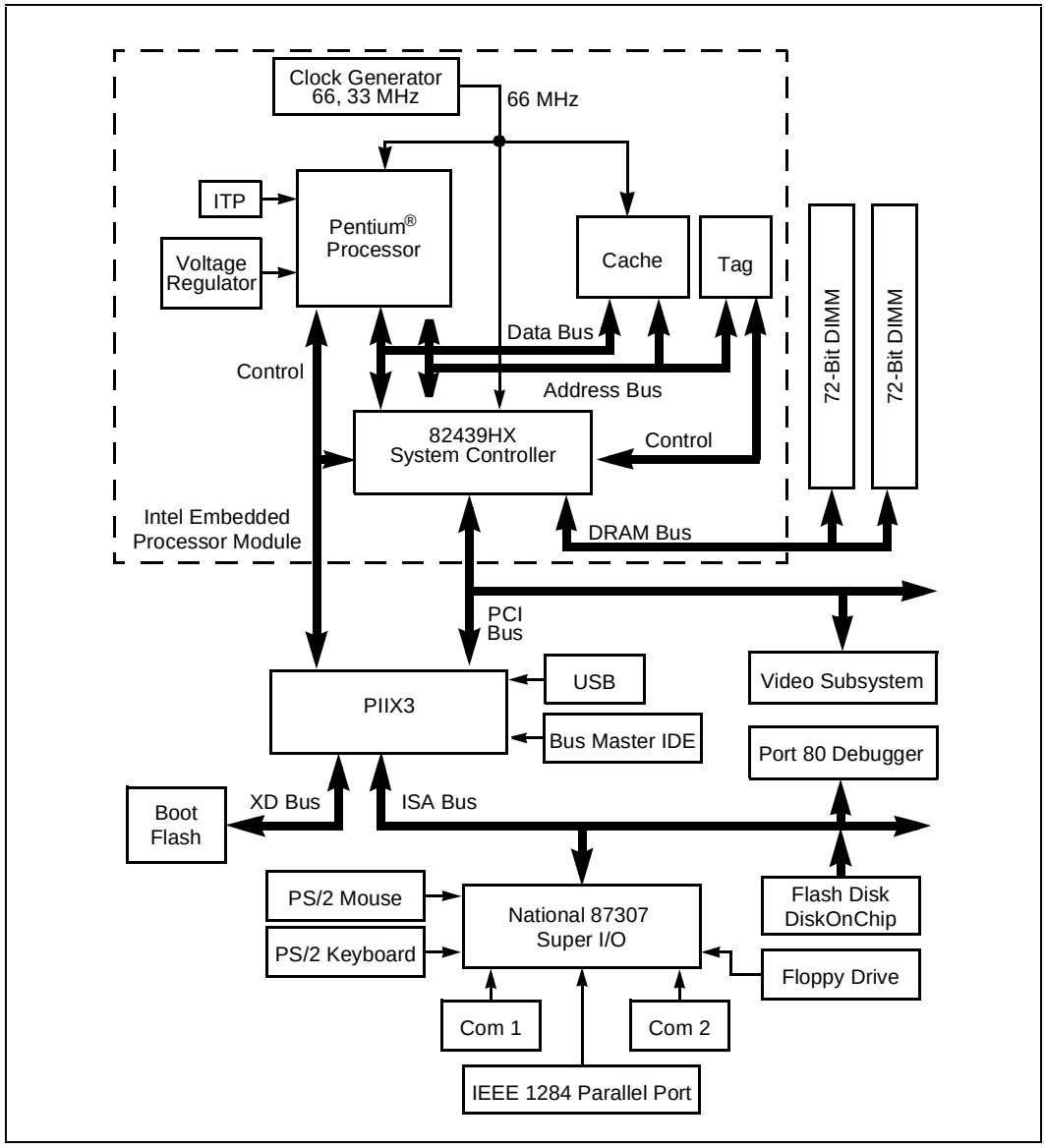
After you have set up the evaluation board using the instructions in this chapter and booted the operating system, you may want to change the default video drivers. The evaluation board is designed with 2 Mbytes of SGRAM and supports refresh rates up to 75 MHz.

To install new drivers, follow the instructions in your operating system documentation. Drivers for the Virge GX video are available from the S3 web page (http://www.s3.com).

Theory Of Operation 3

3.1 Block Diagram

Figure 3-1. Evaluation Board Block Diagram



3.2 System Operation

The Embedded Processor Module Evaluation Platform is a full featured ATX form-factor PC I/O module supporting the Embedded Processor Module. These modules simplify the design of Pentium® processor systems.

3.2.1 Embedded Processor Module

The Embedded Processor Module (EPM) is a high performance subsystem for use in embedded, industrial, and communication applications where flexibility and the ability to upgrade is important. The Embedded Processor Module Developer's Platform incorporates an Intel Pentium processor, a second level cache, a system controller, a clock generator and a voltage regulator on a single printed circuit board. Construction of the module consists of a six layer board 3" × 4". The module has two high-performance, low-profile connectors.

The two connectors carry power, clocks, the DRAM memory interface, and the 33 MHz PCI interface. All host bus devices (hence all the high speed design) are on the EPM provided by Intel. Both connectors are low profile (5 mm stacking height) high density (0.8 mm pitch) connectors. Other stacking heights are available from AMP and Berg.

3.3 V and 5 V power is provided to the EPM from the evaluation board. The EPM generates the core voltage. This core voltage is provided to the evaluation board for the power-on sequencing circuitry. This circuitry makes sure that all supplies are present before sending the PWOK signal to the system controller. The connectors also distribute the system clocks generated by the EPM.

The EPM is populated to allow ITP debugging.

3.2.2 82371SB PCI to ISA Bridge

The 82371SB is the PCI south bridge. The 82371SB connects to the EPM via the PCI bus. The 82371SB requests control of the PCI bus via the PHOLD# signal and becomes the PCI master upon receipt of the PHOLDA# signal from the Embedded Processor Module. The 82371SB contains the PCI and ISA interrupt controller, along with various ISA legacy functions such as a DMA controller, a Bus Master IDE interface, an ISA bus interface, an ISA bus clock control, an XD bus control, speaker control and boot ROM interface. It also provides a USB interface.

3.2.3 Video Subsystem

The evaluation board has a Virge GX high performance 3D graphics subsystem from S3 with 2 Mbytes of SGRAM. The video BIOS for this subsystem is contained in a socketed ROM local to the video chip (U16). Drivers are available at the S3 website (www.s3.com) for Windows 95, Windows NT 3.51, and Windows NT 4.0.

3.2.4 DRAM

The evaluation board provides connectors for two 168-pin JEDEC, DRAM DIMM modules. The supported DRAM DIMMS are 60 ns, single sided, unbuffered, 3.3 V EDO memory. The evaluation kit includes a single DIMM of 32 Mbyte, 72-bit memory. The DIMM connectors

provide a 64-bit or 72-bit interface directly to the Embedded Processor Module. DRAM parity or ECC may optionally be enabled using BIOS setup options. When parity or ECC is enabled, the 72-bit DIMMs must be used. When parity or ECC is disabled, 64-bit DIMMs may be used.

3.2.5 Power

The evaluation board uses an ATX-style connector to connect to an outside power supply. The evaluation board distributes the voltages to the board components as required, including the EPM module. The EPM generates its own core voltage from the voltages provided by the evaluation board.

3.2.6 Boot ROM

The system boot ROM installed at U24 is a 2 Mbit flash, 12 V programmable device. The system is set up for in-circuit reprogramming of the BIOS, but the flash device is also socketed. This device is addressable on the XD bus extension of the ISA bus. Control is provided through the 82371SB PCI-to-ISA bridge chip.

3.2.7 RTC/NVRAM

The RTC and NVRAM is contained within the National 87307 Super I/O* device. CMOS backup is provided by a 3.3 V battery.

3.2.8 Legacy I/O

Support for legacy I/O functions is provided by the 82371SB and the National 87307 Super I/O.

3.2.9 IDE

While the 82371SB is capable of hosting a primary and secondary IDE interface, the evaluation board supports only the primary IDE interface. This allows for up to two IDE devices (one master and one slave) to be supported via a single 40-pin IDE connector.

3.2.10 Floppy Disk Support

Floppy disk support is provided by the National 87307 Super I/O device. One 34-pin floppy connector is provided on the evaluation board.

3.2.11 Keyboard/Mouse

Keyboard and Mouse support is provided by the National 87307 Super I/O device. The keyboard and mouse connectors (J16) are PS/2 style, 6-pin stacked miniature DIN connectors. The bottom connector is for the mouse; the top connector is for the keyboard.

3.2.12 USB

The USB interface is implemented on the evaluation board, and is supported by the BIOS provided in your kit.

3.2.13 RS232 ports

Two serial I/O ports provided by the National 87307 Super I/O device. Two 9-pin RS232 connectors are provided on a single stacked connector (J28).

3.2.14 IEEE 1284 Parallel port

Parallel port support is provided by the National 87307 Super I/O device. One 25-pin IEEE 1284 Parallel port connector is provided on the evaluation board (J20).

3.2.15 PCI Connectors

In keeping with the ATX specification four 32-bit PCI connectors are provided on the evaluation board. These connectors support the 5 V PCI environment. Slot 0 is a shared slot with an ISA connector. All four PCI slots support a PCI slave or PCI master device.

3.2.16 ISA Connectors

Two 16-bit ISA connectors are provided on the evaluation board. ISA slot B is shared with a PCI connector.

3.2.17 Post Code Debugger

The evaluation board has an on-board Post Code Debugger. Data from any code that does an I/O write to 80H is latched on the two led displays (U10/U11). During BIOS startup, code is posted to these LEDs to indicate what the BIOS is doing. Application code can post its own data to these LEDs by writing to I/O address 80H.

The PLD code is included in Appendix A, “PLD Code Listing.”

3.2.18 On-Board 40-Mbyte Flash Disk

An onboard flash disk is implemented with M-Systems’ MD2200 DiskOnChip device configured for full boot operation.

3.2.19 Interrupt Map

Table 3-1. Interrupts

IRQ	System Resources
NMI	I/O Channel Check
0	Reserved, Interval Timer
1	Reserved, Keyboard buffer full
2	Reserved, Cascade interrupt from slave PIC
3	Serial Port 2
4	Serial Port 1
5	Parallel Port (PNP0 option)
6	Floppy
7	Parallel Port 1
8	Real Time Clock
9	IRQ2 Redirect
10	Reserved. Not supported.
11	Reserved. Not supported.
12	Onboard Mouse Port if present, else user available
13	Reserved, Math coprocessor
14	Primary IDE if present, else user available
15	Reserved. Not supported.

3.2.20 Memory Map

Table 3-2. Memory Map

Address Range (Hex)	Size	Description
100000-8000000	127.25M	Extended Memory
E0000-FFFFF	16K	BIOS
C8000-DFFFF		Available expansion BIOS area (Flash disk memory window)
A0000-C7FFF		Off-board video memory and BIOS
9FC00-9FFFF	1K	Extended BIOS Data (movable by QEMM, 386MAX)
80000-9FBFF	127K	Extended conventional
00000-7FFFF	512K	Conventional

3.2.21 Mechanical Design

The evaluation board conforms to the ATX form factor. For extra protection in a development environment users may want to install the evaluation board in an ATX chassis. The evaluation board has two ISA connectors, four PCI connectors and two DRAM DIMM connectors across the back. The I/O connectors are in the rear of the board in the defined ATX I/O window.

A single IDE and floppy drive connector are also provided.

The Embedded Processor Module connects to the evaluation board through two high-density connectors. Four mounting holes are provided on the module to allow mechanical fastening of the module to the evaluation board standoffs with 4/40 screws. The module provided has a passive heat sink. This heat sink interfaces to the EPM module with a thermal grease. The heat sink is also mechanically secured. For benchtop evaluation the evaluation kit provides a strap-on fan. For instructions on how to install the fan, see "Setting up the Board" on page 2-6.

3.3 Measuring Module Current

The Power Interposer Card was created to act as an interface between the evaluation board and the Embedded Processor Module. The Interposer Card passes all the signal connections straight through while providing the means to accurately measure the power dissipation of the IEPM. The Power Interposer Card measures 4" × 4" and has four metal layers. The two surface layers are electrical ground planes, and the two inner layers are 3.3 V and 5.0 V power planes (Figure 3-3). It was designed to accommodate two methods of power measurement: in-line current and current-loop.

Figure 3-2. Power Measurement Circuit Model

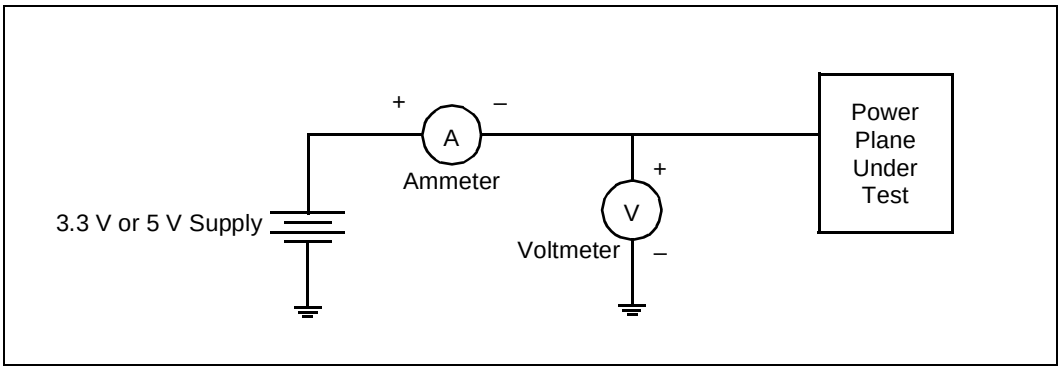
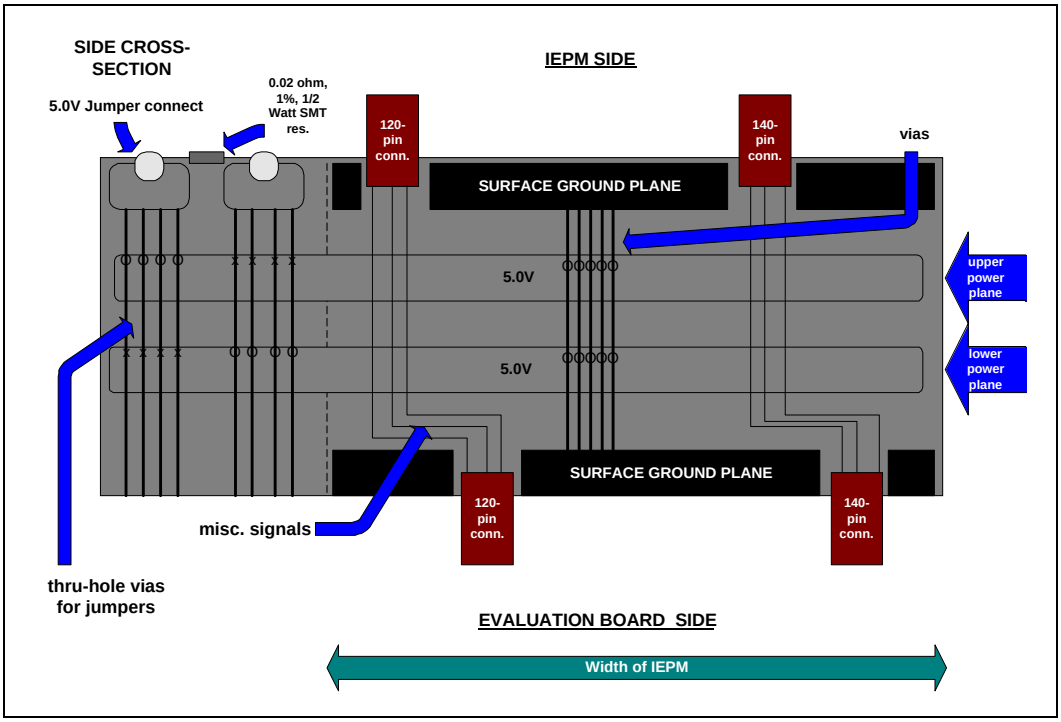


Figure 3-3. Interposer Card Cross Section



The 3.3 V and 5 V power supplies can be analyzed independently. Each power plane is divided into two areas (Figure 3-4). Part of the plane is dedicated to the 5 V supply and the rest of the plane is dedicated to the 3.3 V supply. The top of the card labeled “THIS SIDE UP” is called the “module side” because the IEPM plugs into this side (Figure 3-5).

Figure 3-4. Upper Power Plane - Top Down View

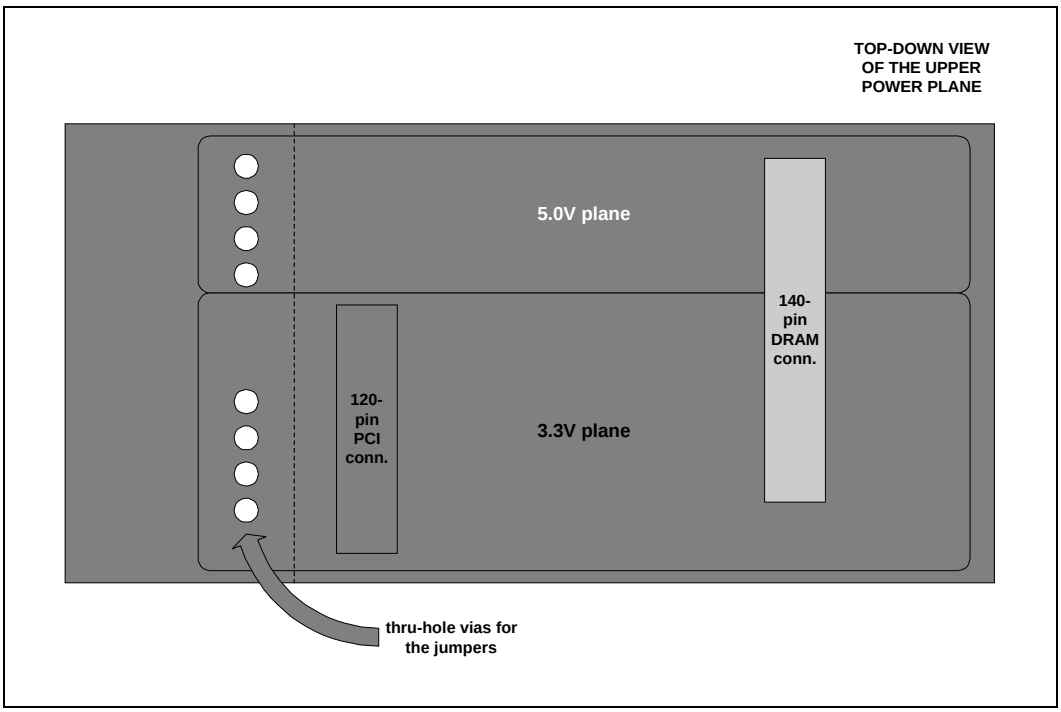
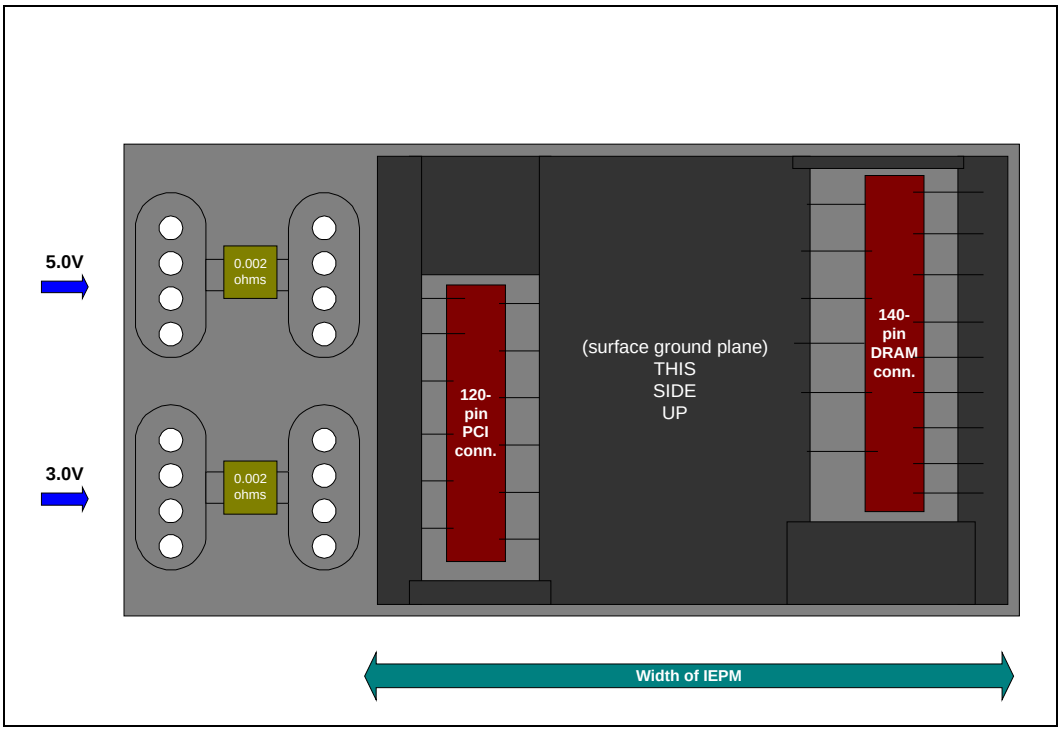


Figure 3-5. Interposer Board Layer 1 - Top View



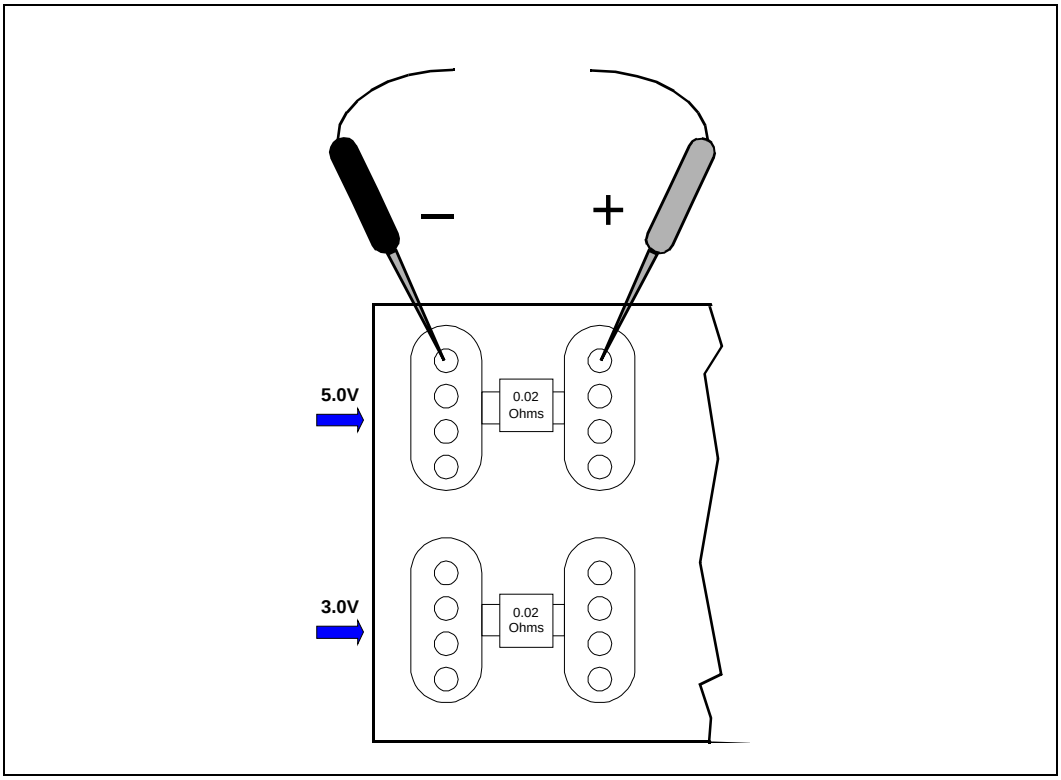
The bottom of the card is called the “board side” because the female connectors of the evaluation board plug into the interposer card. The voltage planes for each side (i.e., IEPM side, evaluation board side) are isolated within the card. On the top surface there are “jumpers” or connection paths where the current flows between power planes inside the Interposer Card. The jumpers consist of four groups of four 18 gauge holes (plated through-hole vias). Each set of four vias connects to a power plane within the board. This is where current and voltage measurements are made. A ½ W, 0.02 Ω, 1% precision resistor provides the connection across the jumper.

3.3.1 Measurement Techniques

3.3.1.1 In-Line

When performing the in-line current power measurement, use the through-hole vias as insertion points for the multimeter probes. Use a high precision digital multimeter (Keithley Model 2001 or similar) to measure the current and a lesser precision meter to simultaneously measure the voltage. The current flows from the contact closest to the leftmost side of the card (holes labeled either V3.3Y or V5.0Y) to the contact closer to the center of the card (labeled V3.3 or V5.0) so be sure to configure the multimeter probes properly (Figure 3-6).

Figure 3-6. Ammeter Probe Connections



3.3.1.2 Current Loop

To use the current-loop measurement method, insert one eighteen gauge copper wire into each hole in order to create a short circuit across the jumper. Then bunch and tie together the wires for each voltage so that the current-loop clamp can fit around the wires (see Figure 3-4). Monitor the current values using an oscilloscope with recording capability. Also measure the voltage with the same scope. Be sure to probe the voltage on the module side of the jumper (the V3.3 or V5.0) side. Calculate the power using P=VI.

3.3.1.3 Precision Resistor

Another method of calculating the instantaneous power consumption of the IEPM itself is to first use a precision digital multimeter to measure the value of the resistors between the jumpers. Second, measure the voltage drop across the resistors, then calculate the current using the equation I=V/R. At the same time, measure the voltage of the specific power supply (3.3 V or 5.0 V). Calculate the power using P=VI.

To calculate the amount of power consumed by the interposer card alone, use this value of I in the equation $P=I^2R$. This power is the power consumed by the 0.02 Ω resistor.

Note: When taking measurements, keep in mind that the 5 V power supply supplies mainly the core of the processor and the 3.3 V power supply powers the processor I/O, clock generator, SRAM and Tag RAM.

Hardware Reference 4

This section provides reference information on the system design. Included in this section is connector pinout information, jumper settings, and other system design information.

- Intel Embedded Processor Module
- In-Circuit BIOS Update
- Post Code Debugger
- ITP Debugger Port
- ISA and PCI Expansion Slots
- PCI Device Mapping
- System Clocks
- Connector Pinouts
- Jumpers
- Test Points

4.1 Embedded Processor Module

The Embedded Processor Module contains all of the host bus devices. This means that the high-speed design for the system is already done.

4.1.1 Power

The EPM draws 3.3 V and 5 V power from the evaluation board through its two high density connectors.

4.1.2 Connectors

The EPM connects to an application (in this case the evaluation board) via two high density connectors. One is a 120-pin connector and the other is a 140-pin connector. The connector placement is such that the EPM can only be socketed one way.

4.1.3 Interface Signals

The EPM interfaces to the an application (in this case the evaluation board) via two high performance connectors. These connectors are available in a variety of stacking heights from both AMP and Berg. These two connectors provide the 33 MHz PCI interface, the power connection to the module, the DRAM interface, and distribute clocking signals from the EPM to the evaluation board.

4.1.3.1 120-Pin Connector

The 120-pin connector from EPM carries the signals for the PCI interface, 3.3 V power, clocks, and signals associated with reset/power-on.

The EPM passes six copies of the PCI clock down to the evaluation board: PIIX3 (U1), Video (U17), Expansion slot 0, Expansion slot 1, Expansion slots 2/3 (share a clock). There is also a loopback clock. This clock is passed to the evaluation board through a length of trace and back to the EPM for clock de-skewing.

This connector also provides a 24 MHz clock and a 14 MHz clock to the system. On the evaluation board the 24 MHz clock is used for the USB clock reference (input to 82371SB System Controller south bridge).

On the evaluation board, the 14 MHz signal is buffered into three copies for the video chip (U17), 82371SB PCI/ISA south bridge, and two ISA expansion slots.

4.1.3.2 140-Pin Connector

The 140-pin connector from EPM provides the main memory interface. This connector supplies 5 V to the EPM and some additional 3.3 V pins as well.

4.2 In-Circuit Bios Update

The BIOS can be upgraded in-circuit. BIOS updates may periodically be posted to the Developers' site at http://www.intel.com.

To reprogram the BIOS:

1. Download the new BIOS upgrade file from Intel's Developer's web site.
2. Extract the BIOS upgrade zip file onto a bootable floppy.
3. Insert the floppy disk into the floppy drive attached to the evaluation board.
4. Reboot the evaluation board so that it reboots from the floppy.
5. Follow the on-screen instructions.

4.3 Post Code Debugger

The evaluation board has an on-board Post Code Debugger. Data from any code that does an I/O write to 80H is latched on the two led displays (U10/U11). During BIOS startup, code is posted to these LEDs to indicate what the BIOS is doing. Application code can post its own data to these LEDs by doing an I/O write to address 80H. The 22V10 PLD code used to implement this function is included in Appendix A, "PLD Code Listing."

4.4 ITP Debugger Port

The Embedded Processor Module included in your kit is populated with an ITP debugger. However, not all production versions have this port installed. This section tells you how to install the port if you purchase additional modules without the ITP port.

The ITP connector, two resistors, and a buffer must be populated on the Embedded Processor Module to support ITP. To populate your module for ITP debugging:

1. Make sure R43 on the module is depopulated
2. Populate U8 (74LVQ04)
3. Populate R43 with SM0805 0 Ohm resistor
4. Populate R21 with SM0805 1 KOhm resistor
5. Populate the J3 ITP connector (AMP104069-1)

When you are using the debugger port, plug the ITP cable into the Embedded processor module before you plug the module into the evaluation board.

4.5 ISA and PCI Expansion Slots

The evaluation board has four PCI expansion slots and two ISA slots. Per the ATX specification, PCI slot 0 and ISA slot B are shared. This means that one slot can be populated, but not both at once. PCI slots 2 and 3 share the same PCI clock. Expansion PCI slots 0, 1, 2 use REQ0#/GNT0#–REQ2#/GNT2# respectively. When J10 and J11 are jumpered, REQ3#/GNT3# is connected to PCI slot 3.

4.6 PCI Device Mapping

On the evaluation board the PCI devices are mapped to PCI device numbers by connecting an address line to the IDSEL signal of each PCI device. Table 4-1 shows the mapping of PCI devices.

Table 4-1. PCI Device Mapping

Device	Address Line	PCI Device
PIIX3	AD12	1
Video	AD13	2
PCI Slot 0	AD28	18
PCI Slot 1	AD29	19
PCI Slot 2	AD30	20
PCI Slot 3	AD31	21

4.7 System Clocks

The Embedded Processor Module generates the clocks for the system.

Table 4-2. System Clocks

Clock	Description
PCI_CLK0	De-skew Loopback
PCI_CLK1	82371SB System Controller (PIIX3)
PCI_CLK2	Video (Virge GX)
PCI_CLK3	PCI expansion Slot 0
PCI_CLK4	PCI expansion Slot 1
PCI_CLK5	PCI expansion Slots 2/3

4.7.1 Other Clocks

The EPM provides a 14.318 MHz clock to the evaluation board. On the evaluation board three buffered copies of this clock are generated and distributed to the ISA slots, Video device, and Super I/O device. The ISA SYSCLK is generated from the 82371SB PCI/ISA bridge on the evaluation board.

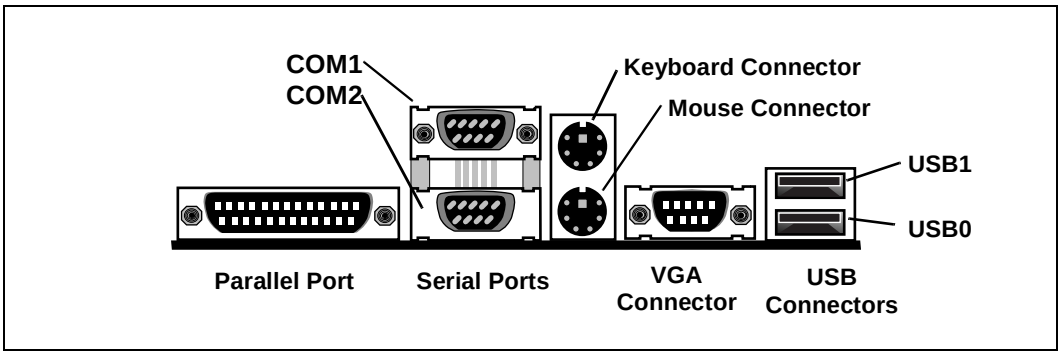
A 24 MHz clock is driven from the Embedded Processor Module to the 82371SB to support the USB unit.

Table 4-3. DMA Channels

DMA	Data Width	System Resources
0	8- or 16-bits	
1	8- or 16-bits	Parallel Port
2	8- or 16-bits	Floppy
3	8- or 16-bits	Parallel Port (for ECP/EPP Config.)
4		Reserved - Cascade Channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

4.8 Connector Pinouts

Figure 4-1. Connector Block — Side View



4.8.1 ATX Power Connector

Table 4-4 shows the signal that will be assigned to the ATX style power connector.

Table 4-4. Primary Power Connector (J24)

Pin	Name	Function
1	3.3 V	3.3 V
2	3.3 V	3.3 V
3	GND	Ground
4	+5V	+5 V VCC
5	GND	Ground
6	+5V	+5 V VCC
7	GND	Ground
8	PWRGD	Power Good
9	5VSB	Standby 5 V
10	+12 V	+12 V
11	3.3 V	3.3 V
12	–12 V	–12 V
13	GND	Ground
14	PS_ON#	Soft-off control
15	GND	Ground
16	GND	Ground
17	GND	Ground
18	–5 V	–5 Volts
19	+5 V	+5 V VCC
20	+5 V	+5 V VCC

4.8.2 ITP Debugger Connector

Table 4-5. ITP Connector Pin Assignment (J3)

Pin	Signal	Pin	Signal
1	INIT	11	PRDY
2	DBRESET	12	TDI
3	RESET	13	TDO
4	GND	14	TMS
5	N/C	15	GND
6	3.3V	16	TCLK
7	R/S#	17	GND
8	GND	18	TRST#
9	N/C	19	N/C
10	GND	20	N/C

4.8.3 Stacked USB

P0 is the bottom connector. P1 is on top.

Table 4-6. USB Connector Pinout (J21)

Pin	Signal Name
1	VCC
2	D-
3	D+
4	GND

4.8.4 VGA Connector

Table 4-7. VGA Connector (J23)

Pin	Signal Name
1	Red
2	Green
3	Blue
4	NC
5	GND
6	GND
7	GND
8	GND
9	V5_0
10	GND
11	NC
12	NC
13	
14	
15	NC

4.8.5 Mouse and Keyboard Connectors

The keyboard port is on top. The mouse port is on the bottom.

Table 4-8. Keyboard and Mouse Connector Pinouts (J15)

Pin	Signal Name
1	Data
2	No Connect
3	Ground
4	+5 V (fused)
5	Clock
6	No Connect

4.8.6 Parallel Port

Table 4-9. DB25 Parallel Port Connector Pinout (J20)

Pin	Signal Name	Pin	Signal Name
1	Strobe#	14	Auto Feed#
2	Data Bit 0	15	Fault#
3	Data Bit 1	16	INIT#
4	Data Bit 2	17	SLCT IN#
5	Data Bit 3	18	Ground
6	Data Bit 4	19	Ground
7	Data Bit 5	20	Ground
8	Data Bit 6	21	Ground
9	Data Bit 7	22	Ground
10	ACK#	23	Ground
11	Busy	24	Ground
12	Paper end	25	Ground
13	SLCT		

4.8.7 Serial Ports

COM0 is the top connector. COM1 is the bottom connector.

Table 4-10. Serial Port Connector Pinout (J28)

Pin	Signal Name
1	DCD
2	Serial In (SIN)
3	Serial Out (SOUT)
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

4.8.8 PCI IDE Connector

Table 4-11. PCI IDE Connector (J5)

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Host Data 7	4	Host Data 8
5	Host Data 6	6	Host Data 9
7	Host Data 5	8	Host Data 10
9	Host Data 4	10	Host Data 11
11	Host Data 3	12	Host Data 12
13	Host Data 2	14	Host Data 13
15	Host Data 1	16	Host Data 14
17	Host Data 0	18	Host Data 15
19	Ground	20	Key
21	DRQ3	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	BALE
29	DACK3#	30	Ground
31	IRQ14	32	IOCS16#
33	Addr 1	34	Ground
35	Addr 0	36	Addr 2
37	Chip Select 0#	38	Chip Select 1#
39	Activity	40	Ground

4.8.9 Floppy Drive Connector

Table 4-12. Diskette Drive Header Connector (JP3)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	FDHDIN
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	Index
9	Ground	10	Motor Enable A#
11	Ground	12	Drive Select B#
13	Ground	14	Drive Select A#
15	Ground	16	Motor Enable B#
17	Ground	18	DIR#
19	Ground	20	STEP#
21	Ground	22	Write Data#
23	Ground	24	Write Gate#
25	Ground	26	Track 00#
27	Ground	28	Write Protect#
29	Ground	30	Read Data#
31	Ground	32	Side 1 Select#
33	Ground	34	Diskette Change#

4.8.10 Embedded Processor Module - EPM Connector Pinouts

The following table shows the signal that will be assigned to the Embedded Processor Module PCI Connector (J1).

Table 4-13. 120-Pin Connector (Sheet 1 of 3)

Pin	Signal Name	Pin	Signal Name
A01	INIT	B01	3.3V
A02	CPURST	B02	STPCLK#
A03	3.3V	B03	SMI#
A04	A20M#	B04	GND
A05	INTR	B05	NMI
A06	IGNNE#	B06	FERR#
A07	GND	B07	N/C
A08	24MHZ	B08	3.3V
A09	N/C	B09	2.9V_SENSE
A10	12MHZ	B10	N/C
A11	3.3V	B11	14.318MHZ
A12	N/C	B12	GND
A13	PCICLK_1	B13	N/C

Table 4-13. 120-Pin Connector (Sheet 2 of 3)

Pin	Signal Name	Pin	Signal Name
A14	N/C	B14	PCICLK_2
A15	GND	B15	N/C
A16	PCICLK_3	B16	3.3V
A17	N/C	B17	PCICLK_4
A18	PCICLK_5	B18	N/C
A19	3.3V	B19	PCICLK_0
A20	DBRST	B20	GND
A21	N/C	B21	PCICLK_IN
A22	N/C	B22	N/C
A23	GND	B23	PCIRST#
A24	N/C	B24	3.3V
A25	AD30	B25	AD31
A26	AD28	B26	AD29
A27	3.3V	B27	AD27
A28	AD26	B28	GND
A29	PHLD#	B29	AD25
A30	AD23	B30	CBE3#
A31	GND	B31	AD22
A32	PHLDA#	B32	3.3V
A33	AD21	B33	LOCK#
A34	AD19	B34	AD20
A35	3.3V	B35	AD24
A36	FRAME#	B36	GND
A37	AD17	B37	AD18
A38	REQ0#	B38	AD16
A39	GND	B39	IRDY#
A40	CBE2#	B40	3.3V
A41	AD15	B41	CBE1#
A42	TRDY#	B42	GNT0#
A43	3.3V	B43	AD14
A44	AD13	B44	GND
A45	REQ1#	B45	AD12
A46	AD11	B46	DEVSEL#
A47	GND	B47	AD10
A48	AD9	B48	3.3V
A49	AD8	B49	GNT1#
A50	AD7	B50	CBE0#

Table 4-13. 120-Pin Connector (Sheet 3 of 3)

Pin	Signal Name	Pin	Signal Name
A51	3.3V	B51	REQ2#
A52	STOP#	B52	GND
A53	AD5	B53	AD6
A54	GNT2#	B54	AD4
A55	GND	B55	PAR
A56	AD3	B56	3.3V
A57	REQ3#	B57	AD2
A58	AD1	B58	SERR#
A59	3.3V	B59	GNT3#
A60	AD0	B60	GND

The following table shows the signals that will be assigned to the Embedded Processor Module connector (J2).

Table 4-14. 140-Pin Connector (Sheet 1 of 2)

Pin	Signal Name	Pin	Signal Name
A01	GND	B01	MWE#
A02	MAA1	B02	MAB1
A03	MAA0	B03	5.0V
A04	MAB0	B04	MA6
A05	5.0V	B05	MA5
A06	MA4	B06	MA3
A07	MA2	B07	5.0V
A08	MA8	B08	MA11
A09	GND	B09	MA7
A10	MA10	B10	MA9
A11	MD0	B11	5.0V
A12	MD32	B12	MD48
A13	5.0V	B13	MD16
A14	MD33	B14	MD17
A15	MD01	B15	GND
A16	MD49	B16	MD02
A17	5.0V	B17	MD34
A18	MD35	B18	MD18
A19	MD50	B19	5.0V
A20	MD03	B20	MD19
A21	GND	B21	MD36
A22	MD04	B22	MD51
A23	RAS7#	B23	5.0V
A24	RAS5#	B24	MD05
A25	5.0V	B25	MD52
A26	MD20	B26	RAS6#

Table 4-14. 140-Pin Connector (Sheet 2 of 2)

Pin	Signal Name	Pin	Signal Name
A27	RAS4#	B27	3.3V
A28	MD53	B28	MD21
A29	GND	B29	MD37
A30	CAS7#	B30	CAS3#
A31	MD22	B31	GND
A32	MD38	B32	MD06
A33	3.3V	B33	CAS1#
A34	MD39	B34	MD07
A35	MD54	B35	3.3V
A36	CAS5#	B36	CAS0#
A37	GND	B37	MPD2
A38	MD55	B38	MD23
A39	CAS4#	B39	GND
A40	CAS2#	B40	MPD4
A41	3.3V	B41	MPD0
A42	MPD6	B42	CAS6#
A43	RAS0#	B43	3.3V
A44	MPD7	B44	MPD1
A45	GND	B45	MPD5
A46	RAS2#	B46	RAS1#
A47	MD08	B47	GND
A48	MD40	B48	MPD3
A49	3.3V	B49	RAS3#
A50	MD25	B50	MD41
A51	MD24	B51	3.3V
A52	MD56	B52	MD30
A53	GND	B53	MD44
A54	MD26	B54	MD57
A55	MD09	B55	GND
A56	MD46	B56	MD11
A57	3.3V	B57	MD10
A58	MD42	B58	MD12
A59	MD59	B59	3.3V
A60	MD58	B60	MD60
A61	GND	B61	MD27
A62	MD43	B62	MD28
A63	MD61	B63	GND
A64	MD29	B64	MD45
A65	3.3V	B65	MD13
A66	MD62	B66	MD63
A67	MD14	B67	3.3V
A68	MD47	B68	MD31
A69	GND	B69	MD15
A70	N/C	B70	GND

4.8.11 PCI Slot Connector

Table 4-15. PCI Slots (J6, J7, J8, J9)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	VCC	B1	- 12V	A32	AD16	B32	AD17
A2	+ 12V	B2	GND	A33	3.3V	B33	CBE2#
A3	VCC	B3	GND	A34	FRAME#	B34	GND
A4	VCC	B4	No Connect	A35	GND	B35	IRDY#
A5	VCC	B5	VCC	A36	TRDY#	B36	3.3 V
A6	PIRQ1#	B6	VCC	A37	GND	B37	DEVSEL#
A7	PIRQ3#	B7	PIRQ2#	A38	STOP#	B38	GND
A8	VCC	B8	PIRQ0	A39	3.3 V	B39	LOCK#
A9	No Connect	B9	PRSNT1B#	A40	SDONE	B40	PERR#
A10	VCC	B10	No Connect	A41	SBO#	B41	3.3 V
A11	No Connect	B11	PRSNT2B#	A42	GND	B42	SERR#
A12	GND	B12	GND	A43	PAR	B43	3.3V
A13	GND	B13	GND	A44	AD15	B44	CBE1#
A14	No Connect	B14	No Connect	A45	3.3V	B45	AD14
A15	RST#	B15	GND	A46	AD13	B46	GND
A16	VCC	B16	PCLK3	A47	AD11	B47	AD12
A17	GNT1#	B17	GND	A48	GND	B48	AD10
A18	GND	B18	REQ#	A49	AD9	B49	GND
A19	Reserved	B19	VCC	A50	KEY	B50	KEY
A20	AD30	B20	AD31	A51	KEY	B51	KEY
A21	3.3V	B21	AD29	A52	CBEO#	B52	AD8
A22	AD28	B22	GND	A53	3.3 V	B53	AD7
A23	AD26	B23	AD27	A54	AD6	B54	3.3 V
A24	GND	B24	AD25	A55	AD4	B55	AD5
A25	AD24	B25	3.3 V	A56	GND	B56	AD3
A26	IDSEL	B26	CBE3#	A57	AD2	B57	GND
A27	3.3V	B27	AD23	A58	AD0	B58	AD1
A28	AD22	B28	GND	A59	VCC	B59	VCC
A29	AD20	B29	AD21	A60	REQ64#	B60	ACK64#
A30	GND	B30	AD19	A61	VCC	B61	VCC
A31	AD18	B31	3.3 V	A62	VCC	B62	VCC

4.8.12 ISA Slot Connector

Table 4-16. ISA Slots (J12, J13)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	IOCHK#	B1	GND	A26	SA5	B26	DACK2#
A2	SD7	B2	RSTSLOT	A27	SA4	B27	TC
A3	SD6	B3	VCC	A28	SA3	B28	BALE
A4	SD5	B4	IRQB9	A29	SA2	B29	VCC
A5	SD4	B5	–5V	A30	SA1	B30	OSC
A6	SD3	B6	DREQ2	A31	SA0	B31	GND
A7	SD2	B7	–12V	C1	SBHE#	D1	MEMCS16#
A8	SD1	B8	ZEROWS#	C2	LA23	D2	IOCS16#
A9	SD0	B9	+12V	C3	LA22	D3	IRQB10
A10	IOCHRDY	B10	GND	C4	LA21	D4	IRQB11
A11	AEN	B11	SMEMW#	C5	LA20	D5	IRQB11
A12	SA19	B12	SMEMR#	C6	LA19	D6	IRQ15
A13	SA18	B13	IOW#	C7	LA18	D7	IRQ14
A14	SA17	B14	IOR#	C8	LA17	D8	DACK0
A15	SA16	B15	DACK3#	C9	MEMR#	D9	DREQ0
A16	SA15	B16	DREQ3	C10	MEMW#	D10	DACK5
A17	SA14	B17	DACK1#	C11	SD8	D11	DREQ5
A18	SA13	B18	DREQ1	C12	SD9	D12	DACK6#
A19	SA12	B19	REFRESH#	C13	SD10	D13	DREQ6
A20	SA11	B20	SYSCLK	C14	SD11	D14	DACK7#
A21	SA10	B21	IRQA7	C15	SD12	D15	DREQ7#
A22	SA9	B22	IRQA6	C16	SD13	D16	VCC
A23	SA8	B23	IRQA5	C17	SD14	D17	MASTER#
A24	SA7	B24	IRQA4	C18	SD15	D18	GND
A25	SA6	B25	IRQA3				

4.9 Jumpers

Table 4-17 shows default Jumper settings.

Table 4-17. Jumper Configuration

Jumper	Default Setting	Other Configurations
J10/J11	OUT:Slot 3 DMA disabled	IN: REQ3#/GNT3# to Slot 3
J22	1–2 Video Chip (U17) B-Step	2–3 Video Chip (U17) C-Step
J26	1–2 2.7V Power Detect	2–3 2.4V Power Detect
J19	IN: +12v Flash Program Supply	OUT: System Flash Program Disabled
J17	1–2 BIOS boot normal	2–3 SA16 Invert
J18	Unconnected	
J25	IN: Power Supply ON	OUT: Power Supply Disabled
J29	1-2 Maps flash disk to C8000H	2-3 Maps flash disk to D0000H
J30	1-2 Boot BIOS from U24	2-3 Boot BIOS from U13

4.9.1 J10/J11/J22

The PCI REQ3#/GNT3# signals are shared by the video chip and PCI expansion slot 3. Since there can only be one master on a DMA line, provisions were made such that REQ3#/GNT3# could be provided to the expansion slot or the video chip. The current stepping of the video chip does not support DMA (B-Step Virge-GX from S3). To prevent the video chip from being connected to REQ3#/GNT3# 0 Ω resistors R101, R102 and R95 have not been populated on evaluation boards containing the B-step Virge-GX video chip. When the C-step is available, future versions of the evaluation board may include the C-step Virge-GX. At that time the required resistors will be populated. Until that time, Jumper J22 should always be in the 1-2 position.

Warning: A B-step video chip may be damaged if jumper J22 is placed in the 2-3 position and R95 is populated.

4.9.2 J26 Power Detect

The evaluation board provides power to the embedded processor module. The voltage regulator on the module generates the core voltage for the processor. In the case of the EPM this is nominally 2.9 V. For other modules this voltage may be different. J26 selects the reference voltage for the power-on sequencing circuitry and should be in the 1-2 position for use with the EPM. This circuitry makes sure that the power supply is within spec (PW_OK signal form ATX power supply) and that the 2.9 V core voltage from the EPM is within 80% of nominal before giving the PWOK signal to the system controller (82371SB System Controller).

4.9.3 J19 System Flash Programming Voltage

The system BIOS Flash device on the evaluation board requires 12 V for program/erase. This jumper must be populated for in-circuit BIOS updates.

4.9.4 J17

This jumper provides the ability to invert the SA16 signal (most significant bit of address presented to the system BIOS Flash device). In the past, some BIOS programs have used this in the implementation of in-circuit Flash reprogramming. The BIOS shipped with the evaluation board does not need this. J17 should always be in the 1-2 position.

4.9.5 J18

By default the boot block of the system BIOS flash device is locked to prevent accidental erasure.

4.9.6 J25

Jumpers the remote turn on/off switch of the ATX power supply. When this jumper is out the ATX power supply is off. When this jumper is in the ATX power supply is on.

4.9.7 J29

The M-Systems DiskOnChip device at U23 is mapped into the expansion BIOS area of the system memory map. The 1-2 (default) position selects C8000H as the starting address for the flash disk's 8 Kbyte memory window. Position 2-3 selects D0000H as the starting address.

4.9.8 J30

This jumper controls the chip enable signal to the system BIOS flash device. The 1-2 (default) position allows the board to boot from the 2 Mbit flash installed at U24. The 2-3 position allows boot from U13 when a 1 Mbit flash device is installed.

4.10 Test Points

Table 4-18 lists key test points. Refer to the schematics for the location of test and probe points.

Table 4-18. Key Test Points

Test Point	Signal Name
TP1	12 MHz
TP13	14.318 MHz
TP14	PCI Clock for 82371SB (PIIX3)
TP15	24 MHz
TP17	BIOSCS#
TP19	SYSCLK

BIOS Quick Reference 5

This section describes how to configure the BIOS for your system configuration. This section assumes that you have already followed the installation instructions provided in Chapter 2.

PhoenixPICO BIOS Software comes pre-loaded on the evaluation board. You can use the Setup program to modify BIOS settings and control the special features of the system. Setup options are configured through a menu-driven user interface.

5.1 Main Menu

To start SETUP:

1. Turn on or reboot your system. PhoenixPICO BIOS displays this message:
   `Press <F2> to enter SETUP`
2. Press <F2> to display the Main Menu. Figure 5-1 shows a sample menu.

Figure 5-1. The Main Menu

```
PhoenixPICO BIOS Setup - Copyright 1985-April 1998 Phoenix Technologies Ltd.
Main    Advanced    Security    Power Savings    Exit
Item Specific Help
   System Time:               [16:19:20]
   System Date: [03/02/1994] 3
   Disk A: [1.2 MB, 5¨"]
   Disk B:                [Not Installed]
 ➢ IDE Adapter 0 Master:    C:  121 MB
 ➢ IDE Adapter 0 Slave:        None
   Video System:                [EGA / VGA]
 ➢ Boot Options:
 ➢ Keyboard Features:

   System Memory:    640 KB
   Extended Memory:   1024 KB

F1  Help        ↑↓ Select Item              -/+   Change Values
F9  Setup Defaults
ESC Exit        ←→ Select Menu              Enter Select ➢ Sub-Menu
F10 Previous Values
```

5.1.1 Menu Bar

The Menu Bar at the top of the window lists these selections:

Main	Use this menu for basic system configuration (described in "Main Menu Selections" on page 17).
Advanced	Use this menu to set the Advanced Features available on your system's chipset (described in "Advanced Menu" on page 25).
Power	The evaluation board does not implement any power management features. This is despite the fact that a Power menu may appear during BIOS setup. All selections on this menu should be disabled with the exception of IRQ1.
Security	Use this menu to set User and Supervisor Passwords and the Backup and Virus-Check reminders (described in "Security Menu" on page 30).
Exit	Exits the current menu (described in "Exit Menu" on page 32).

Use the left/right arrow keys (← and →) to make a selection.

"Exit Menu" on page 5-19 explains how to exit the Main Menu.

5.1.2 Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. Table 5-1 describes the legend keys and their alternates.

Table 5-1. Legend Keys

Key	Function
<F1> or <Alt-H>	General Help window (see below).
<Esc>	Exit this menu.
← or → arrow keys	Select a different menu.
↑ or ↓ arrow keys	Move cursor up and down.
<Tab> or <Shift-Tab>	Cycle cursor up and down.
<Home> or <End>	Move cursor to top or bottom of window.
<PgUp> or <PgDn>	Move cursor to next or previous page.
<F5> or <->	Select the Previous Value for the field.
<F6> or <+> or <Space>	Select the Next Value for the field.
<F9>	Load the Default Configuration values for this menu.
<F10>	Load the Previous Configuration values for this menu.
<Enter>	Execute Command or Select *P* Submenu.
<Alt-R>	Refresh screen.

To select an item, use the arrow keys to move the cursor to the field you want. Then use the plus-and-minus value keys to select a value for that field. The Save Values commands in the Exit Menu save the values currently displayed in all the menus.

To display a sub menu, use the arrow keys to move the cursor to the submenu you want, then press <Enter>. A "➢" pointer marks all sub menus.

5.1.3 Field Help Window

The help window on the right side of each menu displays the help text for the currently selected field. As you move the cursor to each field, it updates the values.

5.1.4 General Help Window

Pressing <F1> or <Alt-H> on any menu displays the General Help window that describes the legend keys and their alternates:

Figure 5-2. General Help Window

```
General Help

 Setup changes system behavior by modifying the power on
 initialization parameters.  Selecting incorrect values
 may cause system boot failure; load Setup Default values
 to recover.

 <Up/Down> arrows select fields in current menu.
 <PgUp/PgDn> moves to previous/next page on scrollable
  menus.
 <Home/End> moves to top/bottom item of current menu.

 Within a field, <F5> or <-> selects next lower value and
 <F6>, <+>, or <Space> selects next higher value.

 <Left/Right> arrows select menus on menu bar.
 <Enter> displays more options for items marked with ÿ.

 <F9> loads factory-installed Setup Default values.
 <F10> restores previous values from CMOS.

 <ESC> or <Alt-X> exits Setup; in sub-menus, pressing
 these keys returns to the previous menu.
```

The scroll bar on the right of any window indicates that there is more than one page of information in the window. Use <PgUp> and <PgDn> to display all the pages. Pressing <Home> and <End> displays the first and last page. Pressing <Enter> displays each page and then exits the window.

Press <Esc> to exit the current window.

5.1.5 Main Menu Selections

You can make the following selections on the Main Menu. Use the sub menus for other selections.

Table 5-2. Main Menu Selections

Feature	Options	Description
System Time	HH:MM:SS	Set the system time
System Date	MM/DD/YYYY	Set the system date
Disk A: Disk B:	360KB, 5 ¼" 1.2MB, 5 ¼" 720KB, 3 ½" 1.44M, 3 ½" 2.88MB, 3 ½" Not installed	Select the type of floppy-disk drive installed in your system.
Video System	Monochrome *EGA/VGAVGA, CGA 40x25, CGA 80x25,	Select the default video device.
System Memory	N/A	Displays amount of conventional memory detected during bootup
Extended Memory	N/A	Displays the amount of extended memory detected during bootup

5.1.6 IDE Adapters

The IDE adapters control the hard disk drives. While PhoenixPICO BIOS supports up to two IDE adapters the evaluation board supports only one. The single adapter can support up to two devices (one master drive and one optional slave drive).

Use a separate sub menu to configure each hard disk drive.

5.1.6.1 Advanced Hard Disk Features—Not Installed

If Advanced Hard Disk Features are not installed, selecting one of the IDE Adapter sub-menus on the Main Menu displays a menu like this:

Figure 5-3. IDE Adapter Menu (Advanced Hard Disk Features—Not Installed)

```
PhoenixPICO BIOS Setup - Copyright 1985-April 1998 Phoenix Technologies Ltd.

Main
```

IDE Adapter 0 Master: C: 121 MB	Item Specific Help
Autotype Fixed Disk: [Press Enter] Type: [User] 121 MB Cylinders 762 Heads 8 Sectors/Track: 39 Write Precomp: None	Attempts to automatically detect the drive type for drives that comply with ANSI specifications

```
F1  Help      ↑↓   Select Item   -/+   Change Values      F9  Setup
Defaults
ESC Exit      ←→ Select Menu   Enter Select ▸ Sub-Menu  F10 Previous Values
```

Use the legend keys listed on the bottom to make your selections and exit to the Main Menu. Use the following chart to configure the hard disk.

Table 5-3. Hard Disk Selections

Feature	Options	Description
Autotype Fixed Disk	N/A	Pressing <Enter> causes the system to attempt to detect the type of ATA device. If successful, it fills in the remaining fields on this menu.
Type	1 to 39 User	1 to 39 fills in all remaining fields with values for predefined disk type. “User” prompts user to fill in remaining fields.
Cylinders	1 to 2048	Number of cylinders.
Heads	1 to 16	Number of read/write heads.
Sectors/Track	1 to 64	Number of sectors per track.
Write Precomp	1 to 2048 None	Number of the cylinder at which to change the write timing.

IDE drives do not require setting Landing Zone and Write Precomp.

Warning: Incorrect settings can cause your system to malfunction.

5.1.6.2 Advanced Hard Disk Features—Installed

If Advanced Hard Disk Features are installed, selecting one of the IDE Adapter sub menus on the Main Menu displays a menu like this:

Figure 5-4. IDE Adapter Menu (Advanced Hard Disk Features—Installed)

```
PhoenixPICO BIOS Setup - Copyright 1985-April 1998 Phoenix Technologies Ltd.

Main
```

IDE Adapter 0 Master: C: 121 MB	Item Specific Help
Autotype Fixed Disk: [Press Enter] Type: [User] 121 MB Cylinders: 762 Heads: 8 Sectors/Track: 39 Write Precomp: None Multi-Sector Transfers : Disabled LBA Control : Disabled 32 bit I/O : Enabled Transfer Mode : Standard	Attempts to automatically detect the drive type for drives that comply with ANSI specifications

```
F1  Help  ↑↓ Select Item    -/+   Change Values       F9  Setup Defaults
ESC Exit  ←→ Select Menu    Enter Select ➢ Sub-Menu  F10 Previous Values
```

Use the legend keys listed on the bottom to make your selections and exit to the Main Menu.

Use the following chart to configure the hard disk drive with Advanced Hard Disk Features:

Table 5-4. Advanced Hard Disk Features

Feature	Options	Description
Autotype Fixed Disk	N/A	Pressing <Enter> at this field attempts to read the hard disk parameters from the drive itself and sets the following options to their optimum setting. Sets “Type” field to “User” and allows editing of other fields.
Type	1 to 39 User Auto	1 to 39 fills in all remaining fields with values for predefined disk type. “User” prompts user to fill in remaining fields. “Auto” autotypes at each boot, displays settings in Setup menu and does not allow editing of remaining fields.
Cylinders	1 to 16,384	Number of cylinders.
Heads	1 to 16	Number of read/write heads.
Sectors/Track	1 to 63	Number of sectors per track.
Write Precomp	N/A	Obsolete
Multi-Sector Transfers	Auto 2 sectors 4 sectors 8 sectors 16 sectors	Auto sets the number of sectors per block at the highest number supported by the drive. This is not always the fastest option.
LBALBA Mode Control	Enabled Disabled	Enables Logical Block Access Default is Disabled.
32-Bit I/O	Enabled Disabled	Enables 32-bit communication between CPU and IDE card Requires PCI bus or local bus.
Transfer Mode	Standard Fast PIO 1 Fast PIO 2 Fast PIO 3 OR Standard Fast DMA A Fast DMA B Fast DMA F	Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform.

IDE drives do not require setting Landing Zone and Write Precomp.

Warning: Incorrect settings can cause your system to malfunction.

5.1.7 Memory Cache

Enabling cache saves time for the CPU by holding data most recently accessed in regular memory (dynamic RAM or DRAM) in a special storage area of static RAM (SRAM), which is faster. Before accessing regular memory, the CPU first accesses the cache. If it does not find the data it is looking for there, it accesses regular memory.

Selecting “Memory Cache” from the Advanced Setup menu displays a menu like the one shown here. The actual features displayed depend on your system’s hardware.

Figure 5-5. Memory Cache Menu

```
PhoenixPICO BIOS Setup - Copyright 1985-April 1998 Phoenix Technologies Ltd.
Main
```

Memory Cache :	Item Specific Help
External Cache: [Press Enter] Cache Interleave: [Disabled] Cache Write Back: [Disabled] Cache Read Cycles: [2T] Cache Write Cycles: [3T] Cache System BIOS: [Disabled] Cache Video BIOS: [Disabled] Cache E800 - EFFF: [Disabled] Cache E000 - E7FF: [Disabled] Cache D800 - DFFF: [Disabled] Cache D000 - D7FF: [Disabled] Cache C800 - CFFF: [Disabled] Non-cacheable Regions Region 0, start: [0 KB] Region 0, size: [Disabled] Region 1, start: [0 KB] Region 1, size: [Disabled]	Sets the state of the external system memory cache

```
F1  Help  ↑↓ Select Item    -/+   Change Values       F9  Setup Defaults
ESC Exit  ←→ Select Menu    Enter Select ➢ Sub-Menu  F10 Previous Values
```

Use the legend keys listed on the bottom to make your selections and exit to the Main Menu. For best performance both the internal and external caches should be set to ‘writeback’ mode. Use the following chart to configure the memory cache.

Table 5-5. Memory Cache Selections

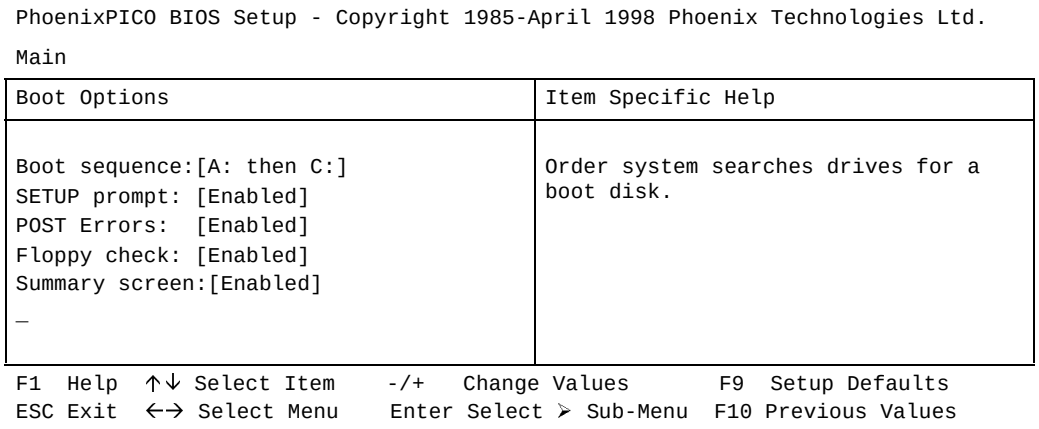
Feature	Options	Description
External Cache	Enabled Disabled	Generally enables or disables all memory caching.
Cache Interleave	Enabled Disabled	Interleaving multiple banks of static RAM improves CPU access.
Cache Write Back	Enabled Disabled	Enabled caches both reads and writes to memory. Disabled caches reads only.
Cache Read Cycles	Chipset Dependent	Sets the number of clock pulses for reading from the cache. Fewer pulses improves performance.
Cache Write Cycles	Chipset Dependent	Sets the number of clock pulses for writing to the cache. Fewer pulses improves performance.
Cache System BIOS	Enabled Disabled	Caches the system BIOS and improves performance.Cache
Cache Video BIOS	Enabled Disabled	Caches the video BIOS and improves performance.
Cache segments, e.g., E800-EFFF	Enabled Disabled	Controls caching of individual segments of memory usually reserved for shadowing system or option ROMs
Non-cacheable regions:		Specifies areas of regular and extended memory as non-cacheable regions.
Region 0, start	0 Multiples of 64	Multiples of 64 define start of non-cacheable region 0 in kilobytes.
Region 0, size	Disabled Multiples of 64	Disabling makes this region available for cache. Multiples of 64 define size of non-cacheable region 0 in kilobytes.
Region 1, start	0 Multiples of 64	Multiples of 64 define start of non-cacheable region 1 in kilobytes.
Region 1, size	Disabled Multiples of 64	Disabling makes this region available for cache. Multiples of 64 define size of non-cacheable region 1 in kilobytes.

Warning: Incorrect settings can cause your system to malfunction.

5.1.8 Boot Options

Selecting “Boot Options” on the Main Menu displays the Boot Options menu.

Figure 5-6. Boot Options Menu



Use the legend keys to make your selections and exit to the Main Menu.

Use the following chart to select your boot options.

Table 5-6. Boot Options

Feature	Options	Description
Boot sequence	A: then C; C: then A: C: only	The BIOS attempts to load the operating system from the disk drives in the sequence selected here.
Setup prompt	Enabled Disabled	Displays “Press <F2> for Setup” during bootup.
POST errors	Enabled Disabled	At boot error, pauses and displays “Press <F1> to resume, <F2> to Setup”.
Floppy seek	Enabled Disabled	Seeks disk drives during bootup. Disabling speeds boot time.
Summary screen	Enabled Disabled	Displays system summary screen during bootup.

5.1.9 Keyboard Features

Selecting “Keyboard Features” on the Main Menu displays the Keyboard Features menu:

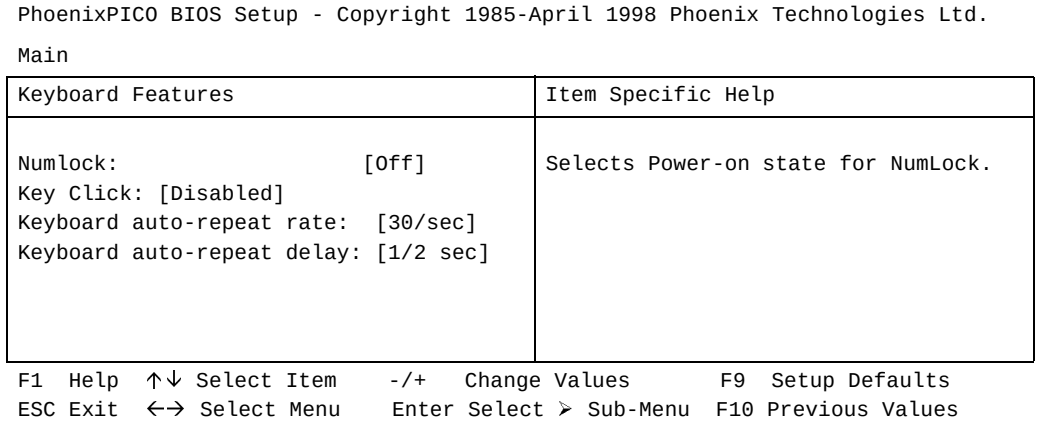


Figure 5-7. Keyboard Features Menu

Use the legend keys to make your selections and exit to the Main Menu.

Use the following chart to configure the keyboard features.

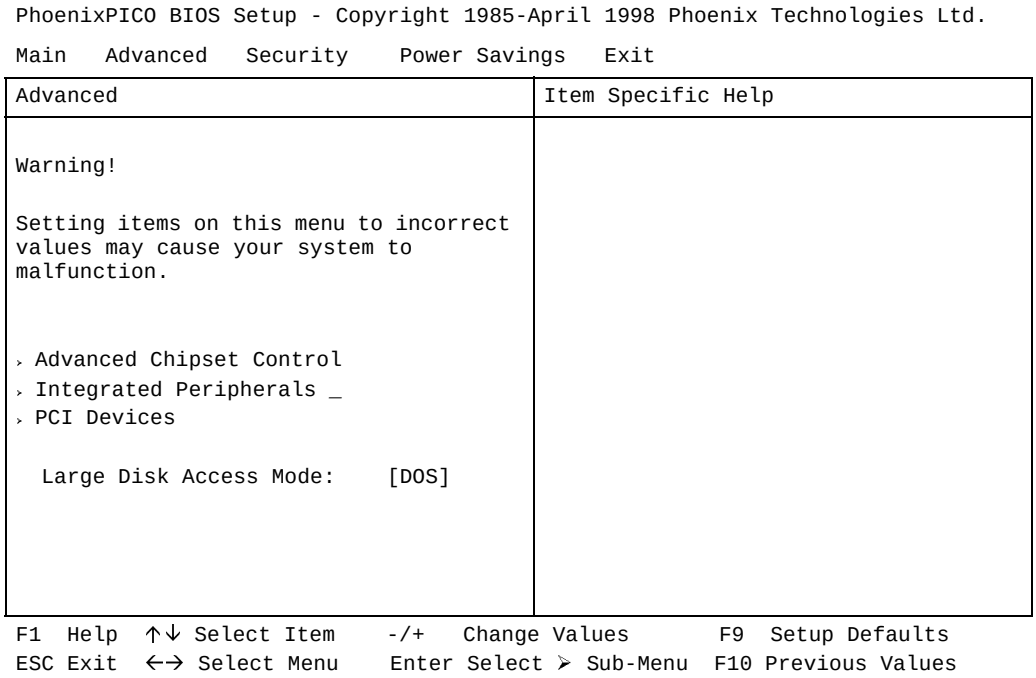
Table 5-7. Keyboard Features Selections

Feature	Options	Description
Numlock	On Off	On or Off turns NumLock on or off at bootup.
Key Click	Enabled Disabled	Turns audible key click on.
Keyboard auto-repeat rate	2/sec 6/sec 10/sec 13.3/sec 21.8/sec 26.7/sec 30/sec	Sets the number of times a second to repeat a keystroke when you hold the key down.
Keyboard auto-lag delay	¼ sec ½ sec ¾ sec 1 sec	Sets the delay time after the key is held down before it begins to repeat the keystroke.

5.2 Advanced Menu

Selecting “Advanced” from menu bar on the Main Menu displays a menu like this:

Figure 5-8. Advanced Menu



Use the legend keys to make your selections and exit to the Main Menu.

Table 5-8. Advanced Menu Selections

Feature	Options	Description
Large Disk Mode	DOS Other	Select DOS if you have DOS. Select Other if you have another operating system such as UNIX. A large disk is one that has more than 1024 cylinders, more than 16 heads, or more than 63 tracks per sector.

5.2.1 Advanced Chipset Control (No PCI)

The chipset is an integrated circuit that acts as an interface between the CPU and much of the system's hardware. You can use this menu to change the values in the chipset registers and optimize your system's performance.

Use the legend keys to make your selections, display the sub menus, and exit to the Main Menu.

Table 5-9. Chipset Options

Feature	Options	Description
Parity check	Enabled Disabled	Controls system memory parity checking.
Hidden refresh	Enabled Disabled	Refreshes regular memory without holding up the CPU.
Slow Refresh	Enabled Disabled	Slows memory refresh by a factor of 4.
Read wait states	0 to n	Sets the number of wait states added to reads from system memory. Chipset dependent.
Write wait states	0 to n	Sets the number of wait states added to writes to system memory. Chipset dependent.
Extra bus wait states	0 to n	Sets the number of wait states added to accesses of the AT bus. Chipset dependent.Wait state
Multiple ALE	Enabled Disabled	Determines whether to use single or multiple ALEs during cycle conversion.
Keyboard reset delay	Enabled Disabled	Enabled adds a 2 microsecond delay before resetting the system.

Note: The contents of this menu depend on the chipset installed on your motherboard. Chipsets vary widely. Consult your dealer or the chipset manual before changing the items on this menu. Incorrect settings can cause your system to malfunction.

5.2.2 Advanced Chipset Control Menu (PCI Chipset)

The PCI chipset is a computer chip that acts as an interface between the CPU and the system's hardware. You can use this menu to optimize the performance of your computer.

Use the legend keys to make your selections and exit to the Main Menu.

Use the following chart in configuring the chipset.

Table 5-10. PCI Chipset Options

Feature	Options	Description
Hidden Refresh	Disabled Enabled	Refreshes regular memory without holding up the CPU
Code Read Page Mode	Disabled Enabled	Improves performance when code contains mainly sequential instructions.
Write Page Mode	Disabled Enabled	Improves performance when data is written sequentially.
CPU to PCI Write Buffers	Disabled Enabled	Stores CPU data in buffers before writing to PCI.
PCI to DRAM Write Buffers	Disabled Enabled	Stores PCI data in buffers before writing to DRAM.
CPU to DRAM Write Buffers	Disabled Enabled	Stores CPU data in buffers before writing to DRAM.
Snoop Ahead	Disabled Enabled	Improves PCI bus master access to DRAM.
PCI Memory Burst Cycles	Disabled Enabled	Enables PCI memory burst write cycles.

Note: The contents of this menu depend on the chipset installed on your motherboard. Chip sets vary widely. Consult your dealer or the chipset manual before changing the items on this menu. Incorrect settings can cause your system to malfunction.

5.2.3 PCI Devices Menu

PCI Devices are devices equipped for operation with a PCI bus, a standardized hardware system that connects the CPU with other devices. Use this menu to configure the PCI devices installed on your system.

Use the legend keys to make your selections and exit to the Advanced menu.

Use the following chart in configuring the PCI devices.

Table 5-11. PCI Devices Options

Feature	Options	Description
PCI Device, Slots 1-n:		
Enable Device	Disabled Enabled	Enable selected device (Only for devices installed on the motherboard)
Enable Master	Disabled Enabled	Enables selected device as a PCI bus master. Not every device can function as a master. Check your device documentation.
Default Latency Timer	Yes No	Default uses minimum bus master clock rate. If yes, do not set the following field
Latency Timer	0000H to 0280H	Bus master clock rate. A high-priority, high-throughput device may benefit from a larger value.

Note: The contents of this menu depend on the devices installed on your system. Incorrect settings can cause your system to malfunction.

5.2.4 Integrated Peripherals Menu

Most chip sets manage the connections between the CPU and the I/O ports (COM: and LPT:), the floppy disks, and the hard-drive controllers. Some systems have a separate on-board chip for handling these items. If your system has a separate on-board I/O chip, selecting “Integrated Peripherals” menu on the Advanced Menu displays a menu like this:

Figure 5-9. Integrated Peripherals Menu

```
PhoenixPICO BIOS Setup - Copyright 1985-April 1998 Phoenix Technologies Ltd.
Main   Advanced   Security    Power Savings   Exit

Integrated Peripherals                  | Item Specific Help
                                        |
COM port: [3F8, IRQ 4]                  | Set COM port address.
COM port:   [2F8, IRQ 3]
LPT port:[378, IRQ 7]
Disk controller:[Enabled]
IDE controller: [Enabled]
ECP:[Disabled]

F1  Help  ↑↓ Select Item    -/+   Change Values       F9  Setup Defaults
ESC Exit  ←→ Select Menu    Enter Select ➢ Sub-Menu  F10 Previous Values
```

Use the legend keys to make your selections and exit to the Main Menu. Use the following chart in configuring the chipset.

Table 5-12. Integrated Peripherals Options

Feature	Options	Description
COM port	Disabled 3F8, IRQ 4 2F8, IRQ 3 338, IRQ 4 238, IRQ 3 3E8, IRQ 4 2E8, IRQ 3 2E8, IRQ 3 2E0, IRQ 3 220, IRQ 4 228, IRQ 3 Auto	Select a unique address and interrupt request for the listed COM ports. Auto selects the next available combination.
LPT port	Disabled 3BC, IRQ 7 378, IRQ, 7 278, IRQ 5	Select a unique address and interrupt request for the LPT port. Auto selects the next available combination.
Disk Controller	Disabled Enabled	Enables the on-board floppy disk controller.
IDE Controller	Disabled Enabled	Enables the on-board IDE controller
ECPECP	Enabled Disabled	Enables Extended Capabilities Parallel port, putting the LPT port above in ECP mode.

5.3 Security Menu

Selecting “Security” from the Main Menu displays a menu that resembles this one:

Figure 5-10. Security Menu

```
PhoenixPICO BIOS Setup - Copyright 1985-April 1998 Phoenix Technologies Ltd.
Main   Advanced   Security    Power Savings   Exit
```

Security	Item Specific Help
Supervisor Password is Disabled User Password is Disabled Set Supervisor Password[Press Enter] Set User PasswordPress Enter Password on boot:[Disabled] Disk access[Supervisor] Fixed disk boot sector:[Normal] System backup reminder:[Disabled] Virus check reminder:[Disabled]	Set COM port address.

```
F1  Help  ↑↓ Select Item    -/+   Change Values       F9  Setup Defaults
ESC Exit  ←→ Select Menu    Enter Select ➢ Sub-Menu  F10 Previous Values
```

Use the legend keys to make your selections and exit to the Main Menu. Security

Enabling “Supervisor Password” requires a password for entering Setup. The passwords are not case sensitive.

Pressing <Enter> at either Set Supervisor Password or Set User Password displays a dialog box like this:

```
Set Password

    Enter new password:  [        ]
    Re-enter new password:  [        ]
```

Figure 5-11. Set Password Dialog Box

Type the password and press <Enter>, then re-enter the password.

Use the following chart to configure the system-security and anti-virus options.

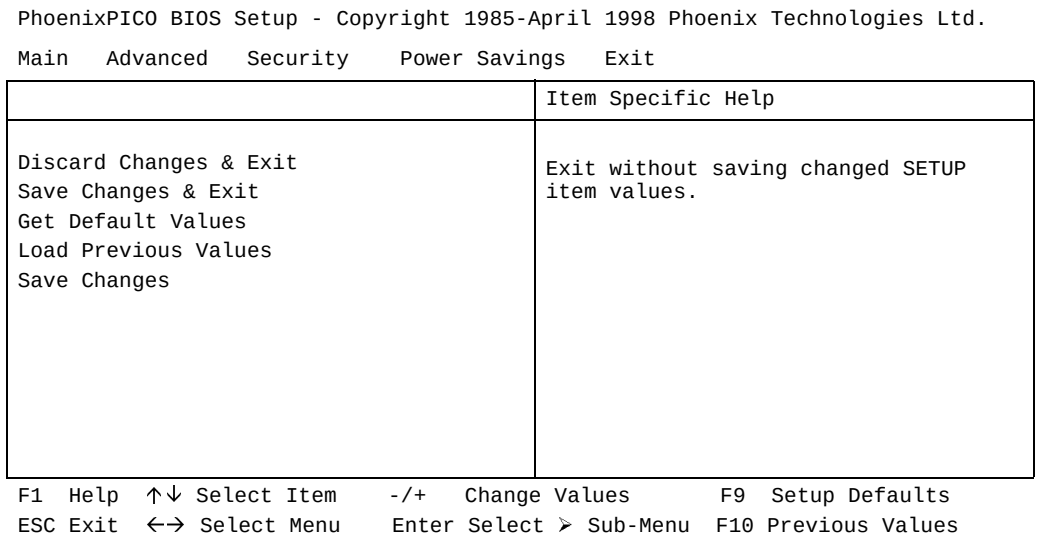
Table 5-13. Security Options

Feature	Options	Description
Supervisor Password	Up to seven alphanumeric characters	Pressing <Enter> displays dialog box for entering the supervisor password. This password gives full access to SETUP menus.
Set User Password	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. This password gives restricted access to SETUP menus. Requires prior setting of Supervisor password.
Password on boot	Enabled Disabled	Enabled requires a password on boot. Requires prior setting of the Supervisor password. If supervisor password is set and this option disabled, BIOS assumes user is booting.
Disk Access	Supervisor User	Supervisor restricts use of floppy drives to supervisor. Requires setting the Supervisor password.
Fixed disk boot sector	Normal Write Protected	Write protected helps prevent viruses.
System backup reminder Virus check reminder	Disabled Daily Weekly Monthly	Displays a message during bootup asking (Y/N) if you have backed up the system or scanned it for viruses. Message returns on each boot until you respond with “Y”. Daily displays the message on the first boot of the day, Weekly on the first boot after Sunday, and Monthly on the first boot of the month.

5.4 Exit Menu

Selecting “Exit” from the menu bar displays this menu:

Figure 5-12. The Exit Menu



The following sections describe each of the options on this menu. Note that <Esc> does not exit this menu. You must select one of the items from the menu or menu bar to exit.

5.4.1 Discard Changes and Exit

Use this option to exit SETUP without storing in CMOS any new selections you may have made. The selections previously in effect remain in effect.

5.4.2 Save Changes and Exit

After making your selections on the Setup menus, always select either “Save values & Exit” or “Save Current Values.” Both procedures store the selections displayed in the menus in CMOS (short for “battery-backed CMOS RAM”) a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS.

After you save your selections, the program displays this message:

```
Values have been saved to CMOS!
    Press <space> to continue
```

If you attempt to exit without saving, the program asks if you want to save before exiting.

During bootup, PhoenixPICO BIOS attempts to load the values saved in CMOS. If those values cause the system boot to fail, reboot and press <F2> to enter Setup. In Setup, you can get the Default Values (as described below) or try to change the selections that caused the boot to fail.

5.4.3 Get Default Values

To display the default values for all the Setup menus, select “Get Default Values” from the Main Menu. The program displays this message:

```
ROM Default values have been loaded!
    Press <space> to continue
```

During bootup, if the BIOS program detects a problem in the integrity of values stored in CMOS, it displays these messages:

```
System CMOS checksum bad - run SETUP
Press <F1> to resume,  <F2> to Setup
```

The CMOS values have been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS.

Press <F1> to resume the boot or <F2> to run Setup with the ROM default values already loaded into the menus. You can make other changes before saving the values to CMOS.

5.4.4 Load Previous Values

If, during a Setup Session, you change your mind about changes you have made and have not yet saved the values to CMOS, you can restore the values you previously saved to CMOS.

Selecting Load Previous Values on the Exit menu updates all the selections and displays this message:

```
CMOS values have been loaded!
    Press <space> to continue
```

5.4.5 Save Changes

Save Current Values saves all the selections without exiting Setup. You can return to the other menus if you want to review and change your selections.

PLD Code Listing A

The code listing below is for the 22V10 PLD (schematic location U12), and the DiskOnChip chip select.

```
TITLE       22V10 PORT 80 ADDRESS DECODER / FLASH DECODE
PATTERN     1
REVISION    B
AUTHOR      CHRIS BANYAI
COMPANY     INTEL CORPORATION
DATE        10/1/97

OPTIONS
    SECURITY = OFF


;  ( part was 22V10FN before conversion )
CHIP  P80B iPLD22V10N

PIN         19    IOWR_BAR
PIN          3    AEN
PIN      [6:7]    SA[0:1]
PIN     [9:13]    SA[2:6]
PIN         16    SA7
PIN      [5:4]    SA[8:9]
PIN    [26:23]    SA[19:16]
PIN    [21:20]    SA[15:14]
PIN          2    SEL

PIN         18   /CS_BAR
PIN         17   /CS_DOC
PIN         27    OX

EQUATIONS
CS_BAR = /IOWR_BAR * /AEN * /SA0 * /SA1 * /SA2 * /SA3 * /SA4 * /SA5 * /SA6
               * SA7 * /SA8 * /SA9
CS_BAR.TRST = VCC

CS_DOC = /SEL * /AEN * SA19 * SA18 * /SA17 * /SA16 * SA15 * /SA14
       + SEL * /AEN * SA19 * SA18 * /SA17 * SA16 * /SA15 * /SA14
CS_DOC.TRST = VCC

OX = /IOWR_BAR
OX.TRST = VCC

SIMULATION

    SETF /AEN /SA0 /SA1 /SA2 /SA3 /SA4 /SA5 /SA6 /SA7 /SA8 /SA9 IOWR_BAR
    SETF SA7 IOWR_BAR
    SETF /IOWR_BAR
```

```
SETF IOWR_BAR
SETF AEN /IOWR_BAR
SETF /AEN
SETF IOWR_BAR
SETF SA0 /IOWR_BAR
SETF /SA0 /IOWR_BAR
SETF IOWR_BAR
SETF /SA0 /SA1 /SA2 /SA3 /SA4 /SA5 /SA6 /SA7 /SA8 /SA9
SETF /SA19 /SA18 /SA17 /SA16 /SA15 /SA14
SETF /SEL
SETF SA19 SA18 /SA17 /SA16 SA15 /SA14
SETF /SEL
SETF /AEN
SETF /SA19
SETF SA19
SETF /SA18
SETF SA18
SETF SA17
SETF /SA17
SETF SA16
SETF /SA16
SETF /SA15
SETF SA15
SETF SA14
SETF /SA14
SETF /SEL
SETF SA19 SA18 /SA17 SA16 /SA15 /SA14
SETF /SEL
SETF /AEN
SETF SEL
SETF /SA19
SETF SA19
SETF /SA18
SETF SA18
SETF SA17
SETF /SA17
SETF /SA16
SETF SA16
SETF SA15
SETF /SA15
SETF SA14
SETF /SA14
SETF /SEL
```

Bill of Materials B

This list is provided as a service to our customers for reference only. The inclusion of this list should not be considered a recommendation or product endorsement by Intel Corporation.

Table B-1. Embedded Processor Module Bill of Materials (Sheet 1 of 6)

Item	Quan	Ref	Value	Package	Man	Man#	Volts	Tol
1	1	XBT1	HU 2032	SOCKET	Renata	HU-232	x	x
2	10	C1, C2, C3, C36, C38, C39, C44, C45, C46, C47	0.001µF	SM 0805	AVX	08055C102KAT1A	25V	x
3	32	C4, C24, C32, C33, C34, C35, C37, C48, C65, C73, C74, C85, C86, C103, C104, C115, C116, C141, C142, C153, C154, C177, C178, C179, C237, C240, C247, C249, C251, C256, C298, C302	0.01µF	SM 0805	AVX	08055C103KAT1A	25V	
4	150	C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C21, C22, C23, C25, C26, C27, C28, C29, C30, C31, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C64, C66, C67, C68, C70, C71, C72, C76, C77, C79, C80, C82, C83, C84, C88, C89, C91, C92, C93, C94, C95, C96, C100, C101, C102, C106, C107, C109, C110, C112, C113, C114, C118, C119, C121, C122, C123, C124, C125, C126, C129, C130, C132, C133, C135, C136, C138, C139, C140, C144, C145, C147, C148, C150, C151, C152, C171, C172, C173, C174, C175, C176, C189, C190, C191, C192, C193, C194, C196, C197, C198, C199, C200, C201, C202, C236, C239, C246, C248, C250, C252, C253, C255, C258, C259, C260, C261, C262, C263, C265, C266, C267, C276, C279, C292, C293, C294, C297, C301, C303, C304, C305, C307, C310, C313, C314, C315, C316 C285, C320, C156, C321, C322	0.1µF	SM 1206	AVX	12065C104KAT1A	25V	
5	10	C19, C20, C286, C287, C308, C309, C235, C238, C311, C312	100µF	Size-D	AVX	TPSD107M010R0080	10V	Tant 20%

Table B-1. Embedded Processor Module Bill of Materials (Sheet 2 of 6)

Item	Quan	Ref	Value	Package	Man	Man#	Volts	Tol
6	7	C40, C41, C42, C43, C131, C134, C146	10µF	D-Size	Pan TE	ECS-T1VD106R	35V	Tant 20%
	0	C62, C63, C97, C127, C155, C257, C317, C318, C319	NOT POPULATED	SM 0805			x	x
7	25	C69, C75, C78, C81, C87, C90, C99, C105, C108, C111, C117, C120, C128, C137, C143, C149, C169, C170, C245, C254, C264, C288, C295, C299, C300	10µF	B-Size	Pan TE	ECS-T1AX106R	10V	Tant 20%
8	2	C98, C274, C275	100pF	SM 0402	Pan Multi	ECU-E1H101JCQ	50V	
	0	C98	NOT POPULATED					
9	18	C157, C158, C159, C160, C161, C162, C163, C164, C165, C166, C167, C168, C268, C269, C270, C271, C272, C273	10pF	SM 0402	Pan Multi	ECUE1H100DCQ	50V	
10	25	C180, C181, C182, C183, C184, C185, C203, C204, C205, C206, C208, C209, C210, C211, C215, C216, C217, C218, C219, C220, C221, C222, C282, C283, C284	470pF	SM 0402	Pan Multi	ECU-E1E471KBQ	25V	10%
11	2	C188, C291	22µF	C-Size	Pan TE	ECS-T1AC226R	10V	Tant 20%
12	16	C207, C212, C213, C214, C223, C224, C225, C226, C227, C228, C229, C230, C231, C232, C233, C234	220pF	SM 0402	Pan Multi	ECU-E1H221JCQ	50V	5%
13	4	C241, C242, C243, C244	47pF	SM 0402	Pan Multi	ECU-E1H470JCQ	50V	5%
14	4	C277, C278, C280, C281	100µF	6.3X11.2mm	Pan M	ECA-1EM101	25V	20%
15	1	C289	4.7nF	SM 1206	AVX	12065C472KAT1A	25V	
16	2	C290, C296	1µF	A-Size	Pan TE	ECS-T1CY105R	16V	Tant 20%
17	1	C306	1000pF	SM 0402	Pan Multi	ECU-E1E102KBQ	25V	10%
18	4	D1, D7, D8, D9	LED	SOT23	Siemens	LGS260-DO	x	x
19	1	D2	(1N4148)	MMBD914 (SOT23)	Zetex	FMMD914	x	x
20	1	D3	LM4041EIM3-1.2	SOT23	National	LM4041EIM3-1.2	x	x
21	3	D4, D5, D6	(IN4148)	SOT-23 SERIES	Zetex	BAV99	x	x
22	1	D10	Zener	SOT-23	Philips	BZX84C2V7	1.3W	
23	1	D11	Zener	SOT-23	Philips	BZX84C2V4	1.3W	
24	6	FB1, FB2, FB3, FB4, FB5, FB6	Ferrite	SM 1806	Murata	BLM41A800S	x	x
25	4	FB7, FB8, FB9, FB10	Ferrite	SM 0805	Murata	BLM21B050S	x	x

Table B-1. Embedded Processor Module Bill of Materials (Sheet 3 of 6)

Item	Quan	Ref	Value	Package	Man	Man#	Volts	Tol
26	5	FB11, FB12, FB13, FB14, FB15	CB70 Ferrite	SM 1206	TDK	HF30ACB321611-T	x	x
27	4	F1, F2, F3, F4	Poly Fuse	Drawing	Raychem	SMD125-2	15V	1.24 Hold
28	1	F5	Poly Fuse	Drawing	Raychem	SMD100-2	15V	1.24 Hold
29	1	J28	Stacked Serial	drawing	FOXCONN	DM10156-73	x	x
30	1	JP3	FLOPPY 17X2		FOXCONN	HL07173-P4	x	x
31	1	JP4	1x4	25-mil sq /100-mil sp	3M	929647-09-04	x	x
32	1	J1	Mohave DRAM Conn	140-Pin Recept	AMP	177983-6	x	x
					Berg	61082-141-000		
33	1	J2	Mohave PCI Conn	120-Pin Recept	AMP	177983-5	x	x
					Berg	61082-121-000		
34	2	J4, J3	DIMM Connector		FOXCONN	AT08403-K8	x	x
35	1	J3	DRAM, 32M, DIMM		Micron	MT18LD472AG-6X		
36	1	J5	IDE Conn		FOXCONN	HL07206-D2	x	x
37	4	J6, J7, J8, J9	PCI Conn	EH06001-PC-W	FOXCONN	EH06001-PC-W	x	x
38	6	J10, J11, J14, J16, J19, J25,	1x2	25-mil sq /100-mil sp	3M	929647-09-02	x	x
39	2	J12, J13	ISA Conn A, B		FOXCONN	EQ04901-S6	x	x
40	1	J15	PS2 STACK		FOXCONN	MH11067-D2	x	x
41	6	J17, J22, J27, J26, J29, J30	1x3	25-mil sq /100-mil sp	3M	929647-09-03	x	x
42	1	J18	1x1	25-mil sq /100-mil sp	3M	929647-09-01	x	x
43	1	J20	DB25		FOXCONN	DT11323-R5T	x	x
44	1	J21	USB Stack		FOXCONN	UB1112C-D3	x	x
45	1	J23	DB15HD VGA		FOXCONN	DZ11A36-R5	x	x
46	1	J24	ATX POW CONN	x	FOXCONN	HM20100-P2	x	x
	0	RP1, RP2, RP3, RP4	NOT POPULATED	EXB-V	Pan	EXB-V8VR00OV	x	5%
47	4	RP5, RP6, RP45, RP49	22	EXB-V	Pan	EXB-V8V220JV	x	5%
48	14	RP7, RP17, RP18, RP20, RP21, RP25, RP30, RP32, RP34, RP36, RP38, RP39, RP40, RP41	10K	EXB-V	Pan	EXB-V8V103JV	x	5%
49	11	RP8, RP9, RP10, RP11, RP12, RP13, RP14, RP15, RP16, RP46, RP48	33	EXB-V	Pan	EXB-V8V330JV	x	5%
50	5	RP19, RP28, RP42, RP43, RP44	4.7K	EXB-V	Pan	EXB-V8V472JV	x	5%

Table B-1. Embedded Processor Module Bill of Materials (Sheet 4 of 6)

Item	Quan	Ref	Value	Package	Man	Man#	Volts	Tol
51	2	RP22, RP26	330	EXB-V	Pan	EXB-V8V331JV	x	5%
52	6	RP23, RP24, RP27, RP29, RP31, RP33	2.7K	EXB-V	Pan	EXB-V8V272JV	x	5%
53	2	RP35, RP37	5.6K	EXB-V	Pan	EXB-V8V562JV	x	5%
54	1	RP47	1K	EXB-V	Pan	EXB-V8V102JV	x	5%
55	2	RP50, RP51	220	EXB-V	Pan	EXB-V8V221JV	x	5%
56	4	R1, R65, R97, R98,	0	SM 0805	Pan	ERJ-6GEYOR00V	x	5%
	0	R2, R5, R7, R15, R25, R33, R34, R57, R58, R59, R60, R95, R96, R99, R101, R102, R123, R124, R125	NOT POPULATED					
57	11	R3, R6, R69, R81, R83, R85, R86, R87, R88, R106, R107	22	SM 0805	Pan	ERJ-6GEYJ220V	x	5%
	0	R82, R84	NOT POPULATED					
58	16	R4, R13, R48, R49, R51, R52, R53, R61, R63, R64, R91, R108, R109, R111, R116, R117	10K	SM 0805	Pan	ERJ-6GEYJ103V	x	5%
	0	R50, R110, R112	NOT POPULATED					
59	6	R8, R19, R20, R27, R28, R94	220	SM 0805	Pan	ERJ-6GEYJ221V	x	5%
60	18	R9, R10, R37, R38, R40, R42, R44, R45, R46, R47, R68, R79, R80, R89, R90, R127, R130, R131	4.7K	SM 0805	Pan	ERJ-6GEYJ472V	x	5%
61	3	R11, R14, R16	47	SM 0805	Pan	ERJ-6GEYJ470V	x	5%
62	1	R12	33	SM 0805	Pan	ERJ-6GEYJ330V	x	5%
63	6	R17, R36, R62, R70, R92, R126	1K	SM 0805	Pan	ERJ-6GEYJ102V	x	5%
64	2	R18, R113	215	SM 0805	Pan	ERJ-6ENFJ2150V	x	1%
65	9	R21, R22, R23, R24, R29, R30, R31, R32, R39	2.7K	SM 0805	Pan	ERJ-6GEYJ272V	x	5%
	0	R26	NOT POPULATED	SM 0805	Pan	ERJ-6GEYJ100V	x	5%
66	2	R41, R43	330	SM 0805	Pan	ERJ-6GEYJ331V	x	5%
67	1	R55	22	SM 0805	Pan	ERJ-6GEYJ220V	x	5%
68	1	R66	8.2K	SM 0805	Pan	ERJ-6GEYJ822V	x	5%
69	1	R67	20K	SM 0805	Pan	ERJ-6GEYJ203V	x	5%
70	4	R71, R72, R75, R76	27	SM 0805	Pan	ERJ-6GEYJ270V	x	5%
71	4	R73, R74, R77, R78	15K	SM 0805	Pan	ERJ-6GEYJ153V	x	5%
72	1	R93	147	SM 0805	Pan	ERJ-6ENF1470V	x	1%

Table B-1. Embedded Processor Module Bill of Materials (Sheet 5 of 6)

Item	Quan	Ref	Value	Package	Man	Man#	Volts	Tol
73	0	R100, R121, R122	NOT POPULATED	SM 1206	Pan	ERJ-8GEYJ102V	x	5%
74	3	R103, R104, R105	75	SM 0805	Pan	ERJ-6GEYJ750V	x	5%
75	1	R114	130	SM 0805	Pan	ERJ-6GEYJ131V	x	5%
76	1	R115	110	SM 0805	Pan	ERJ-6GEYJ111V	x	5%
77	1	R118	1K	SM 0805	Pan	ERJ-6GEYJ102V	x	5%
78	1	S1	RESET SWITCH	drawing	Pan	EVQ-PHP03T	x	
	0	TP1-158	No parts	x	x	x	x	x
79	1	U1	PIIX3	QFP 208	Intel	SB82371SB	x	x
80	3	U2, U4, U5	74ALS245	SOIC20	National	DM74ALS245AWM	x	x
81	1	U3	74HCT14	SOIC14	74HCT14D	PHILIPS	x	x
82	1	U6	74ALS08	SOIC14	National	DM74ALS08M	x	x
83	1	U7	74ALS00	SOIC14	National	DM74ALS00M	x	x
84	1	U8	Super I/O	NS VUL160A	Nat	PC87307IBU-VUL	x	x
85	1	U9	QS3384	SOIC 24	QSI	QS3384SO	x	x
86	2	XU11,XU10	TIL311 SOCKET	DIP14	MILLMAX	110-99-314-41-001	x	x
87	1	U12	GAL22V10	PLCC28	LATTICE	GAL22V10B-7LJ	x	x
88	1	XU13	Socket	PLCC 32 SOCKET	FOXCONN	PL01160-TM	x	x
89	2	U15, U14	GD75232SOP	SOIC	TI	GD75232DW	x	x
90	1	XU16	Video Bios Socket	PLCC 32 SOCKET	FOXCONN	PL01160-TM	x	x
91	1	U17	VIRGE GX	PQFP 208	S3	86C385Z	x	x
92	2	U20, U19	SGRAM	TQFP 100	NEC	UPD481850GFA-10	x	x
93	1	U21	TLC393C	SOP8	TI	TLC393CD	5V	x
94	1	Y1	32.768KHZ	MC-405	EPSON	MC-405	x	x
95	1	BATTERY BT1	3V 190mAH Li coin	(see item 1)	Renata	CR2032	3V	x
96	2	LED Display U10, U11	TIL311 PART	(see item 86)	TI	TIL311	x	x
	0	U13	NOT POPULATED	NOT POPULATED	Intel	28F001BX-T150	x	x
97	1	Video Bios Eprom U16	27LV512-15	(see item 90)	ATM	AT27LV512A-15JC	x	x
98	10	Screw for foot	4-40X5/16 PHP ZINC		HSV FAST	PAN M/S TYPE F ZINC		
99	10	1” HEX SPACER, STANDOFF			Richco	HS4-8		
100	7	Shunt Jumper .1CTR 10µin Au			3M	929955-06		
101	1	XU12	IC SOCKET	PLCC 28 SOCKET	AMP	822271-1		
102	1	PC Board	Raw Card		Details	4617-23-0001		

Table B-1. Embedded Processor Module Bill of Materials (Sheet 6 of 6)

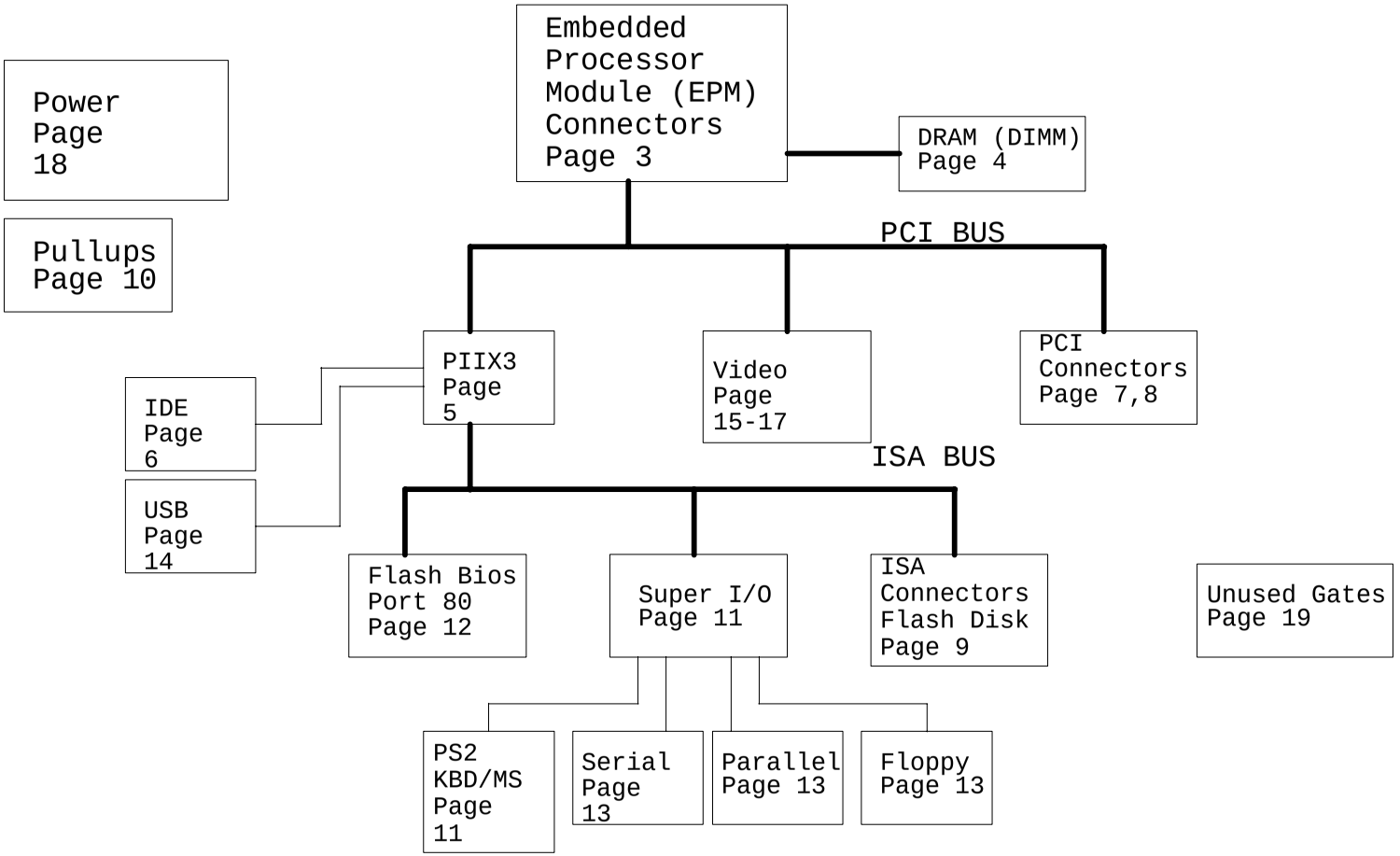
Item	Quan	Ref	Value	Package	Man	Man#	Volts	Tol
103	1	R120	22 ohm	SM1206	Pan	ERJ-8GEYJ220V	x	5%
104	2	R128, R129	2.2K	SM 0805	Pan	ERJ-6GEYJ222V	x	5%
105	1	U22	74ACT05	SO14	Motorola	MC74ACT05DR	x	
					Harris	CD74ACT05M96		
106	1	R54	22M	SM1206	KOA	RM73B2BT226K	x	10%
107	1	C186	10pF+/-.5pF	SM0805	Murata	GRM40COG100D50V		
108	1	C187	15pF 5%	SM0805	Murata	GRM40COG150J50V		
109	1	R56	120K	SM0805	Pan	ERJ-6GEYJ124V		
					Dale	CRCW0805124JRT1		
110	1	U18	74ACT04	SOIC	National	74ACT04SC		
111	1	R35	68ohm	SM0805	Pan	ERJ-6GEYJ680V		
112	10		Washer, Yuma standoff	.281OD .125ID .022TK	HSV FAST	#4 SPE F/W ZINC		
113	1	AV-THT-38-426	Label, Bios Rev	U24, U12, U16	Brady	THT-38-426		
114	1	XU23	IC SOCKET	DIP, SMT, 32-PIN	Samtec	ICF632SO		
115	1	U23	40 Mbyte	DiskOnChip, socketed	M-Systems	MD2200-D40		
116	1	U24 SYS BIOS FLASH	28F002BC-T120	TSOP, 40 lead	Intel	E28F002BC-T120		

Schematics C

Schematics are provided for the following items:

- Block Diagram
- Embedded Processor Module Connectors
- DRAM DIMM socket
- PIIX3
- IDE interface
- PCI slots 0 and 1
- PCI slots 2 and 3
- ISA sockets flash disk
- PCI and ISA pullup/pulldown
- Super I/O
- Flash BIOS/Port 80
- I/O connectors
- USB ports
- Video
- SGRAM
- Video VGA connector
- Power
- Extra gates

PRELIMINARY



NOTE 1: Note NC denotes "no connect"
Do not connect NC's together in layout.

NOTE 2: Note DU denotes "do not use"
Do not connect DU's together in layout.

NOTE 3: 10-Layer (6 signal, 4 power/gnd)

NOTE 4: Test points are hole/via that can accept a 25-mil square post. Test points should be inline (no stubs)

Title: EVEPMDEVBD: Block Diagram		
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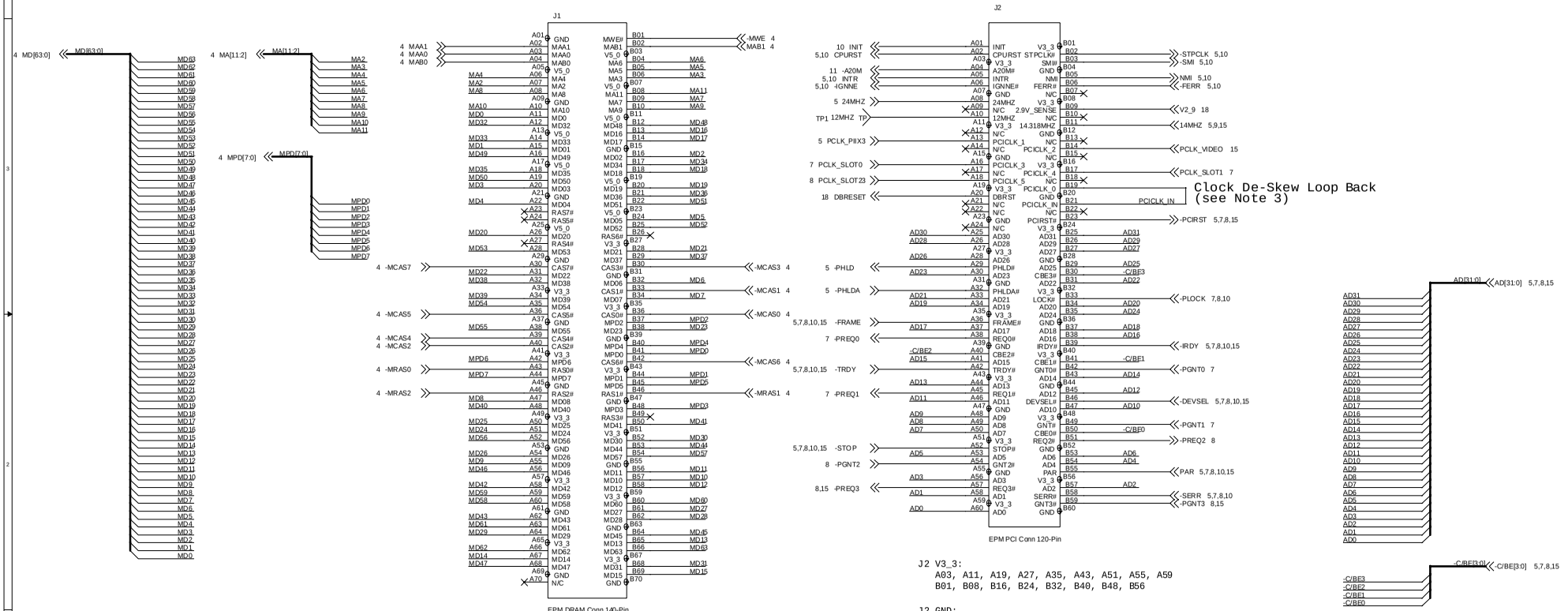
Embedded Processor Module (EPM) Connectors

PRELIMINARY

DRAM

ADDRESS/DATA/CLOCKS



J1 V5_0:
A05, A13, A17, A25
B03, B07, B11, B19, B23

J1 V3_3:
A33, A41, A49, A57, A65
B27, B35, B43, B51, B59, B67

J1 GND:
A01, A09, A21, A29, A37, A45, A53, A61, A69
B15, B31, B39, B47, B55, B63, B70

J2 V3_3:
A03, A11, A19, A27, A35, A43, A51, A55, A59
B01, B08, B16, B24, B32, B40, B48, B56

J2 GND:
A07, A15, A23, A31, A39, A47
B12, B20, B28, B36, B44, B52, B60

24MHZ/14MHZ/SYSCLK
24MHZ (3v): PIIX3(USBCLK), X1(Super I/O)
14MHZ (3v): PIIX3(OSC), ISA Slots (OSC)
SYSCLK 8.25MHZ (PIIX3) -> ISA Slots

PCI Clock Distribution (33MHZ)	
PCICLK_0	(B19) De-Skew Loopback
PCICLK_1/PCLK_PIIX3	(A13) PIIX3
PCICLK_2/PCLK_VIDEO	(B14) Video (Virge GX)
PCICLK_3/PCLK_SLOT0	(A16) PCI Expansion Slot 0
PCICLK_4/PCLK_SLOT1	(B17) PCI Expansion Slot 1
PCICLK_5/PCLK_SLOT23	(A18) PCI Expansion Slots 2/3

NOTE 0: Connectors are female
NOTE 1: PCLK_PIIX3, PCLK_VIDEO, PCLK_SLOT0, PCLK_SLOT2, PCLK_SLOT23 must be equal length.
NOTE 3: PCLK_0 to PCICLK_IN roundtrip must be same length as signals in NOTE 1.
NOTE 4: Split PCLK_SLOT23 to supply both PCI SLOT 2 and PCI SLOT 3 as close to the PCI slots as possible. Stubs must be of equal length.
NOTE 5: Separate all clocks from any other trace by 10 mil. (SYSCLK, 25MHZ, 14MHZ, PCLK_PIIX3, PCLK_VIDEO, PCLK_SLOT0, PCLK_SLOT1, PCLK_SLOT23

Title: EVEPMDEVBD - EPM CONNECTORS		
Size: C	Document Number: CB1	Rev: B.1
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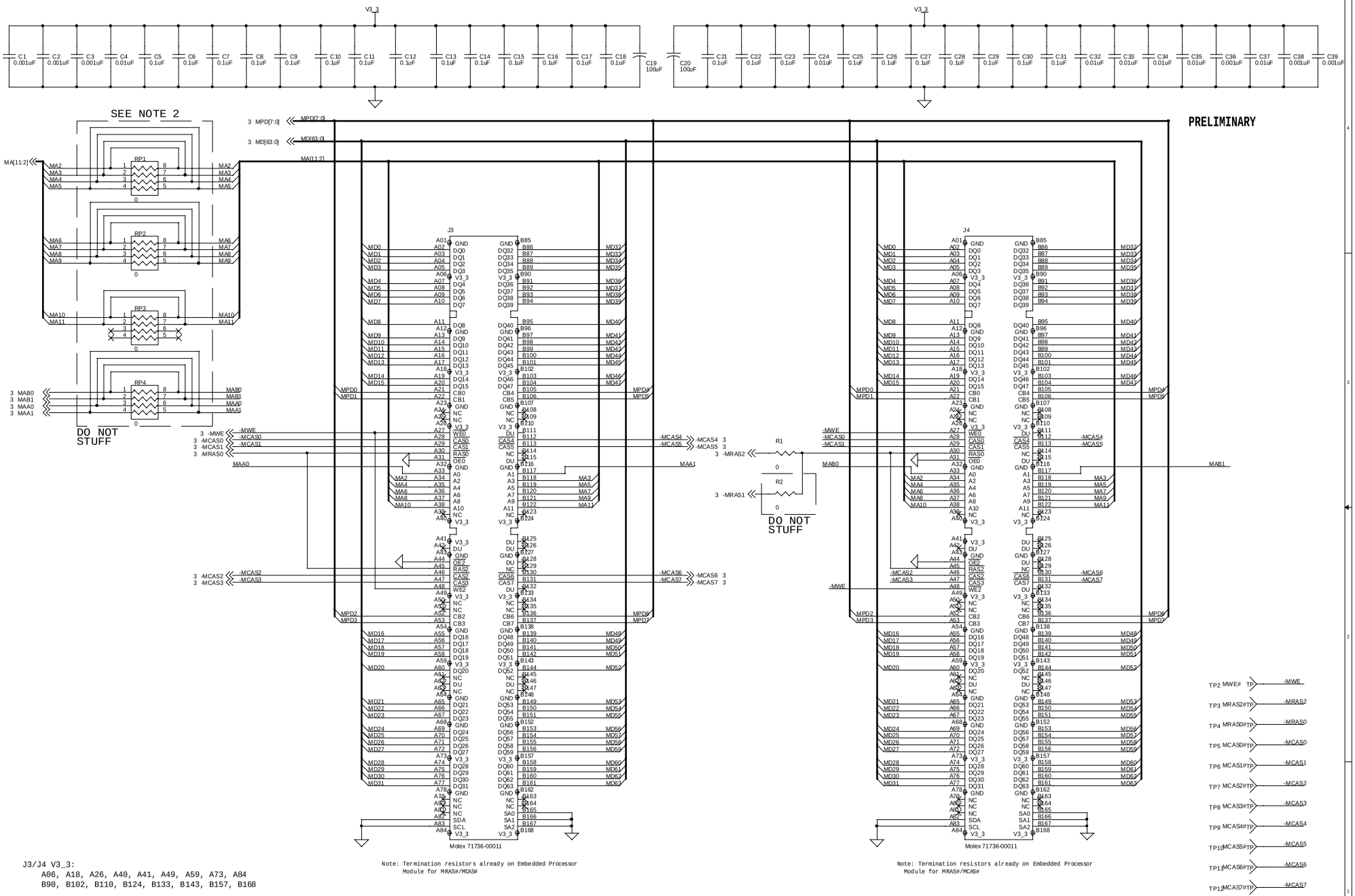

Note: Termination resistors already on Embedded Processor Module for MRAS#/MCAS#

Note: Termination resistors already on Embedded Processor Module for MRAS#/MCAS#

J3/J4 V3_3:
A06, A18, A26, A40, A41, A49, A59, A73, A84
B90, B102, B110, B124, B133, B143, B157, B168

J3/J4 GND:
A01, A12, A23, A32, A43, A54, A64, A68, A78 | A31, A44, A82, A83
B85, B96, B107, B116, B127, B138, B148, B152, B162 | B165, B166, B167

J3/J4 NC:
A24, A25, A39, A50, A51, A61, A63, A79, A80, A81
B108, B109, B114, B123, B129, B135, B145, B147, B163, B164

J3/J4 DU: A42, A62
B111, B115, B125, B126, B128, B132, B134, B135, B146

NOTE 1: Place Test Points close to J3/J4 DIMM Connectors
NOTE 2: Use R-PACK pad geometry. Shunt pads with trace. Route on surface (cuttable)

Title	EVEPMDEVBD - DRAM DIMM Sockets		
Size C	Document Number CB1		Rev B.1
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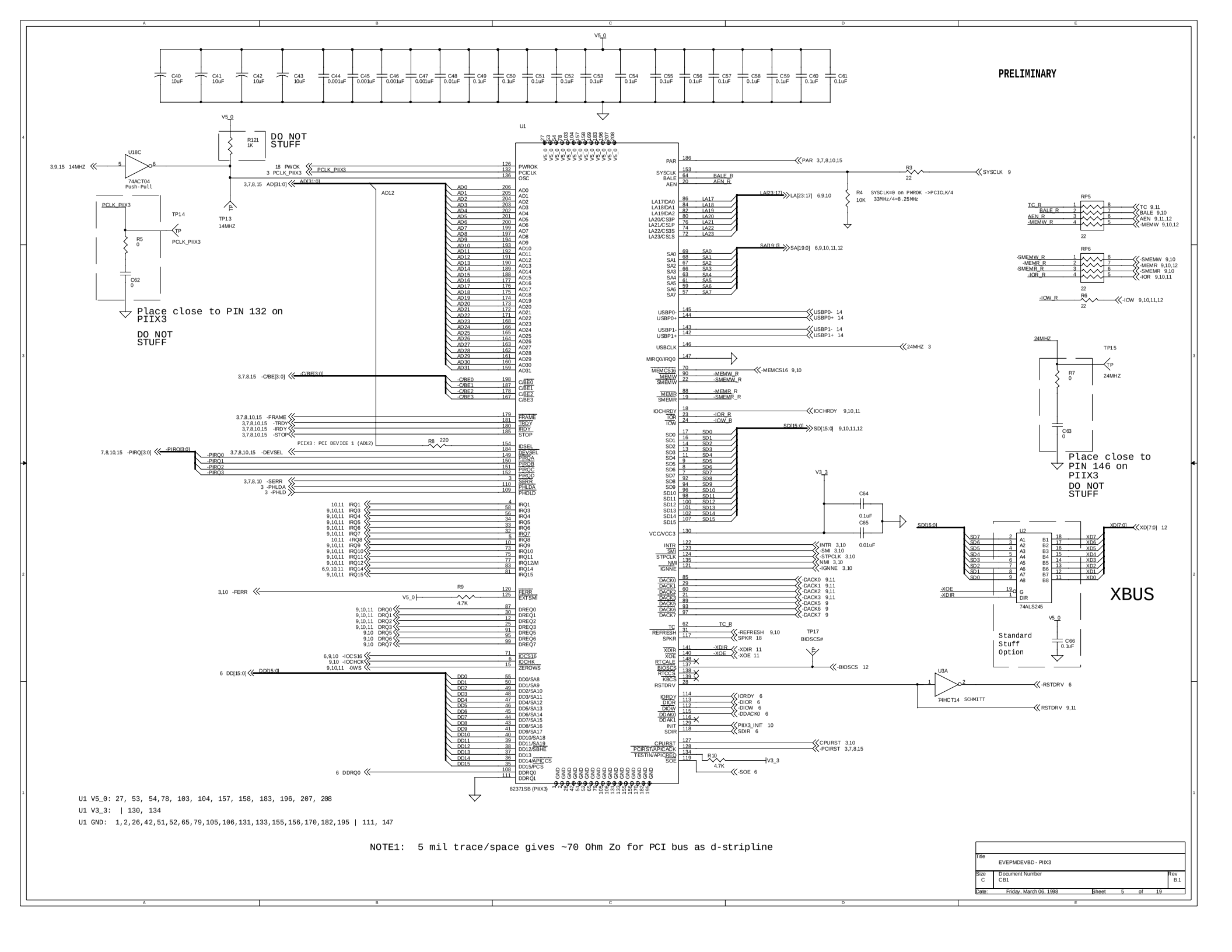
PRELIMINARY
V5_0
C40 10uF
C41 10uF
C42 10uF
C43 10uF
C44 0.001uF
C45 0.001uF
C46 0.001uF
C47 0.001uF
C48 0.01uF
C49 0.1uF
C50 0.1uF
C51 0.1uF
C52 0.1uF
C53 0.1uF
C54 0.1uF
C55 0.1uF
C56 0.1uF
C57 0.1uF
C58 0.1uF
C59 0.1uF
C60 0.1uF
C61 0.1uF
R121 1K
DO NOT STUFF
U18C
74ACT04 Push-Pull
3,9,15 14MHZ
TP13 14MHZ
PCLK_PIIX3
TP14
R5 0
C62 0
Place close to PIN 132 on PIIX3
DO NOT STUFF
U1
82371SB (PIIX3)
PWROK
PCICLK
OSC
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
C/BE0
C/BE1
C/BE2
C/BE3
FRAME
TRDY
IRDY
STOP
IDSEL
DEVSEL
PIRQA
PIRQB
PIRQC
PIRQD
SERR
PHLDA
PHOLD
IRQ1
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
IRQ8
IRQ9
IRQ10
IRQ11
IRQ12/M
IRQ14
IRQ15
FERR
EXTSMI
DREQ0
DREQ1
DREQ2
DREQ3
DREQ5
DREQ6
DREQ7
IOCS16
IOCHK
ZEROWS
DD0/SA8
DD1/SA9
DD2/SA10
DD3/SA11
DD4/SA12
DD5/SA13
DD6/SA14
DD7/SA15
DD8/SA16
DD9/SA17
DD10/SA18
DD11/SA19
DD12/SBHE
DD13
DD14/APICCS
DD15/PCS
DDRQ0
DDRQ1
PIIX3: PCI DEVICE 1 (AD12)
R8 220
R9 4.7K
PAR
SYSCLK
BALE_R
AEN_R
R3 22
SYSCLK 9
R4 SYSCLK=0 on PWROK ->PCICLK/4
10K 33MHz/4=8.25MHz
LA17/DA0
LA18/DA1
LA19/DA2
LA20/C3BP
LA21/C1LP
LA22/C3BS
LA23/C1LS
LA[23:17]
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA[19:0]
USBP0-
USBP0+
USBP1-
USBP1+
USBCLK
24MHZ 3
MIRQ0/IRQ0
MEMCS16
MEMW
SMEMW
MEMR
SMEMR
IOCHRDY
IOR
IOW
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
SD8
SD9
SD10
SD11
SD12
SD13
SD14
SD15
SD[15:0]
VCC/VCC3
INTR
SMI
STPCLK
NMI
IGNNE
DACK0
DACK1
DACK2
DACK3
DACK5
DACK6
DACK7
TC
REFRESH
SPKR
XDIR
XOE
RTCALE
BIOSCS
RTCCS
KBCS
RSTDRV
IORDY
DIOR
DIOW
DDACK0
DDAK1
INIT
SDIR
CPURST
PCIRST/APICACK
TESTIN/APICREQ
SOE
R10 4.7K
V3_3
C64 0.1uF
C65 0.01uF
TP17 BIOSCS#
U3A 74HCT14 SCHMITT
-RSTDRV 6
RSTDRV 9,11
RP5
RP6
R6 22
24MHZ
TP15
R7 0
C63 0
Place close to PIN 146 on PIIX3
DO NOT STUFF
U2
74ALS245
XBUS
Standard Stuff Option
C66 0.1uF
GND
U1 V5_0: 27, 53, 54,78, 103, 104, 157, 158, 183, 196, 207, 208
U1 V3_3: | 130, 134
U1 GND: 1,2,26,42,51,52,65,79,105,106,131,133,155,156,170,182,195 | 111, 147
NOTE1: 5 mil trace/space gives ~70 Ohm Zo for PCI bus as d-stripline
Title
EVEPMDEVBD - PIIX3
Size C
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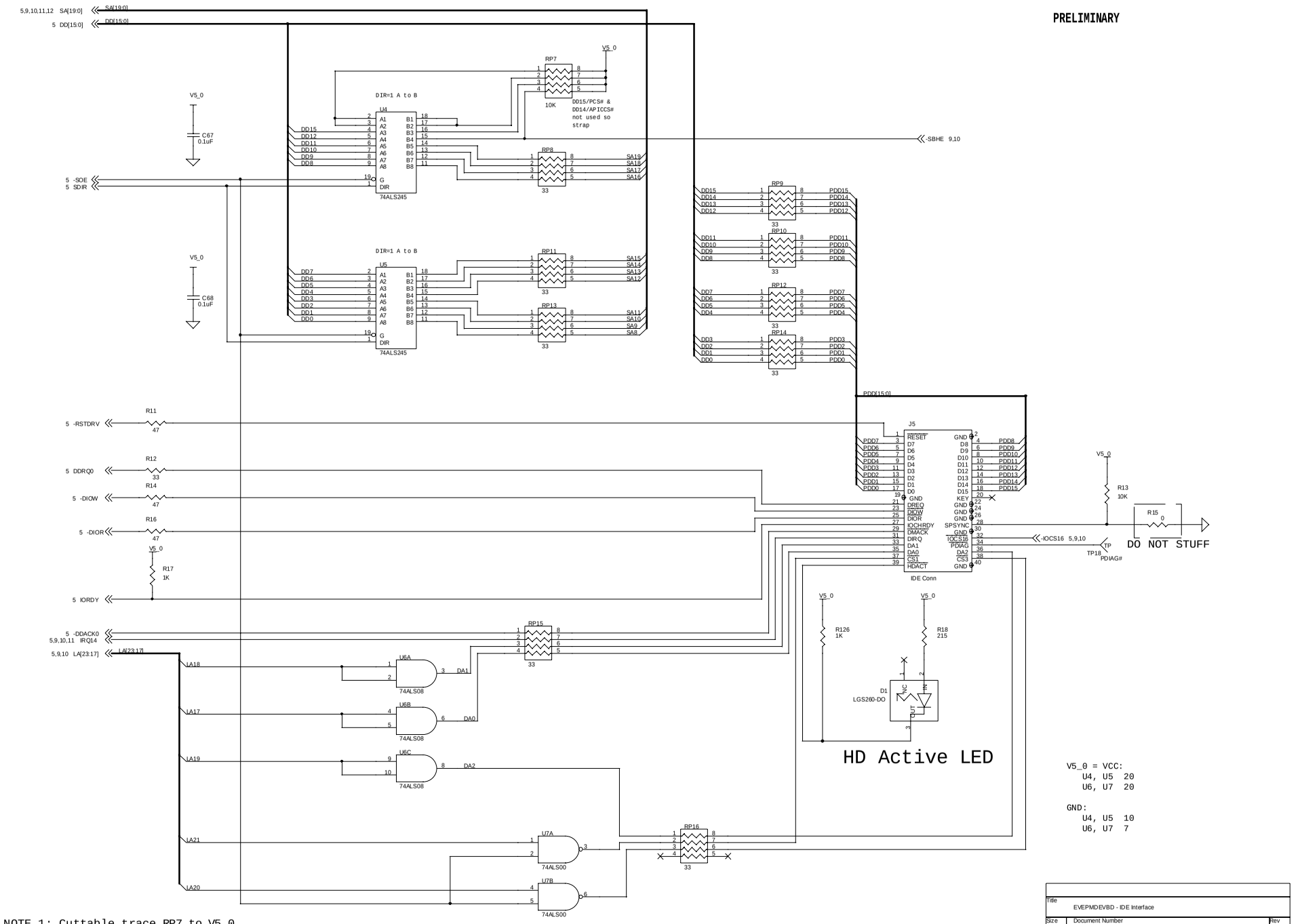
Sheet 5 of 19

IDE Interface

PRELIMINARY



V5_0 = VCC:
U4, U5 20
U6, U7 20

GND:
U4, U5 10
U6, U7 7

NOTE 1: Cuttable trace RP7 to V5_0

Title: EVEPMDEVBD - IDE Interface		
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J6/J7 V5_0:
    A5, A8, A10, A16, A59, A61, A62 | A1, A3, A4
    B5, B6, B19, B22, B59, B61, B62

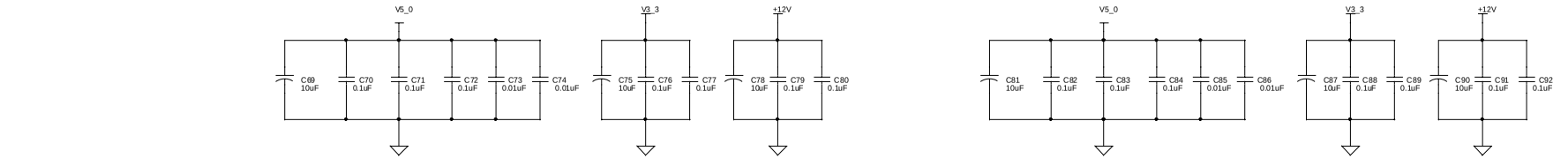
J6/J7 V3_3:
    A21, A27, A33, A39 A45, A53
    B25, B31, B36, B41, B43, B54

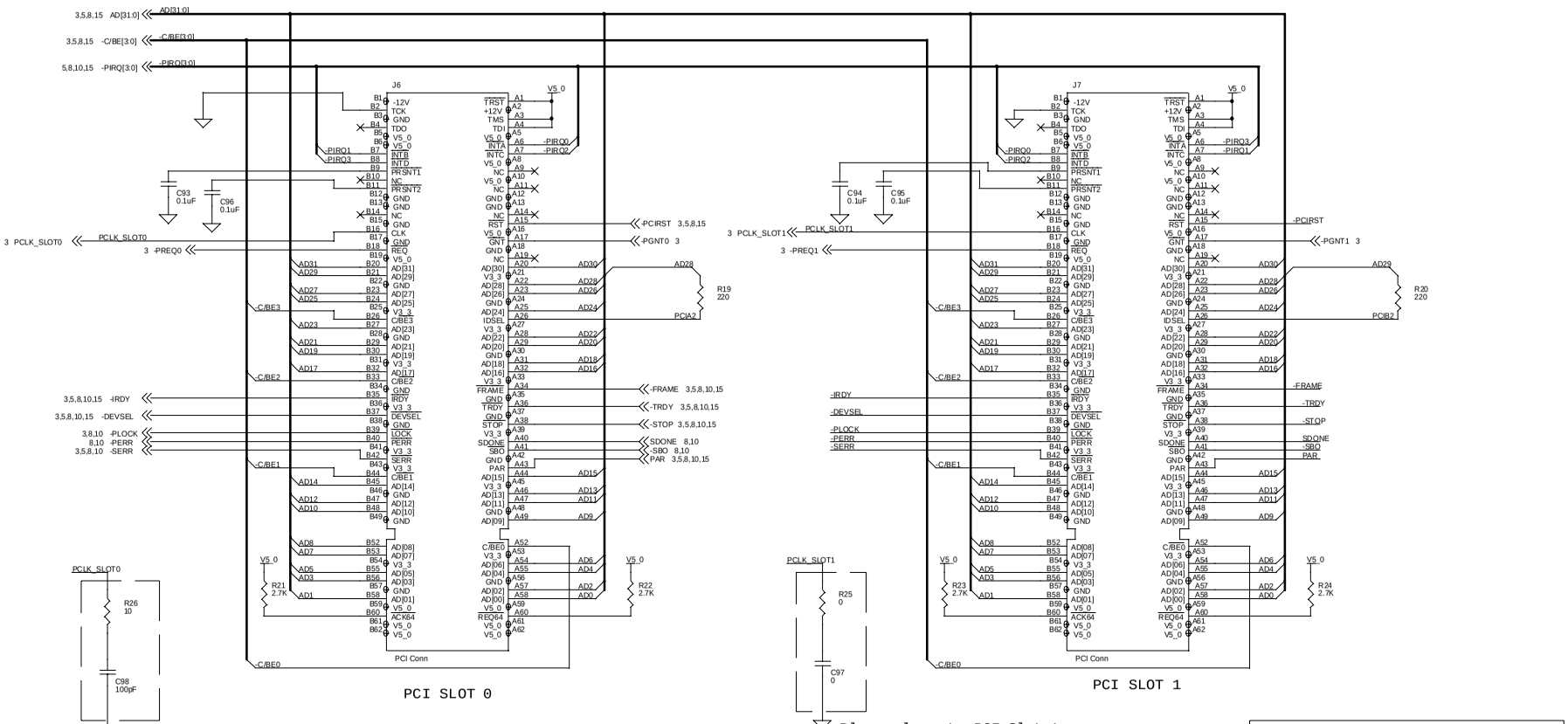
J6/J7 NC:
    A9, A11, A14, A19
    B10, B14

J6/J7 GND:
   A12, A13, A18, A24, A30, A35, A37, A42, A48, A56
   B3, B12, B13, B15, B17, B28, B34, B38, B46, B49, B57 | B2

J6/J7 +12V: A2
      -12V: B1

PRELIMINARY





Place close to PCI Slot 0
DO NOT
STUFF

Place close to PCI Slot 1
DO NOT
STUFF

Title	EVEPMDEVBD - PCI Slots 0 & 1	
Size C	Document Number CB1	Rev B.1
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J8/J9 V5_0:
    A5, A8, A10, A16, A59, A61, A62 | A1, A3, A4
    B5, B6, B19, B22, B59, B61, B62

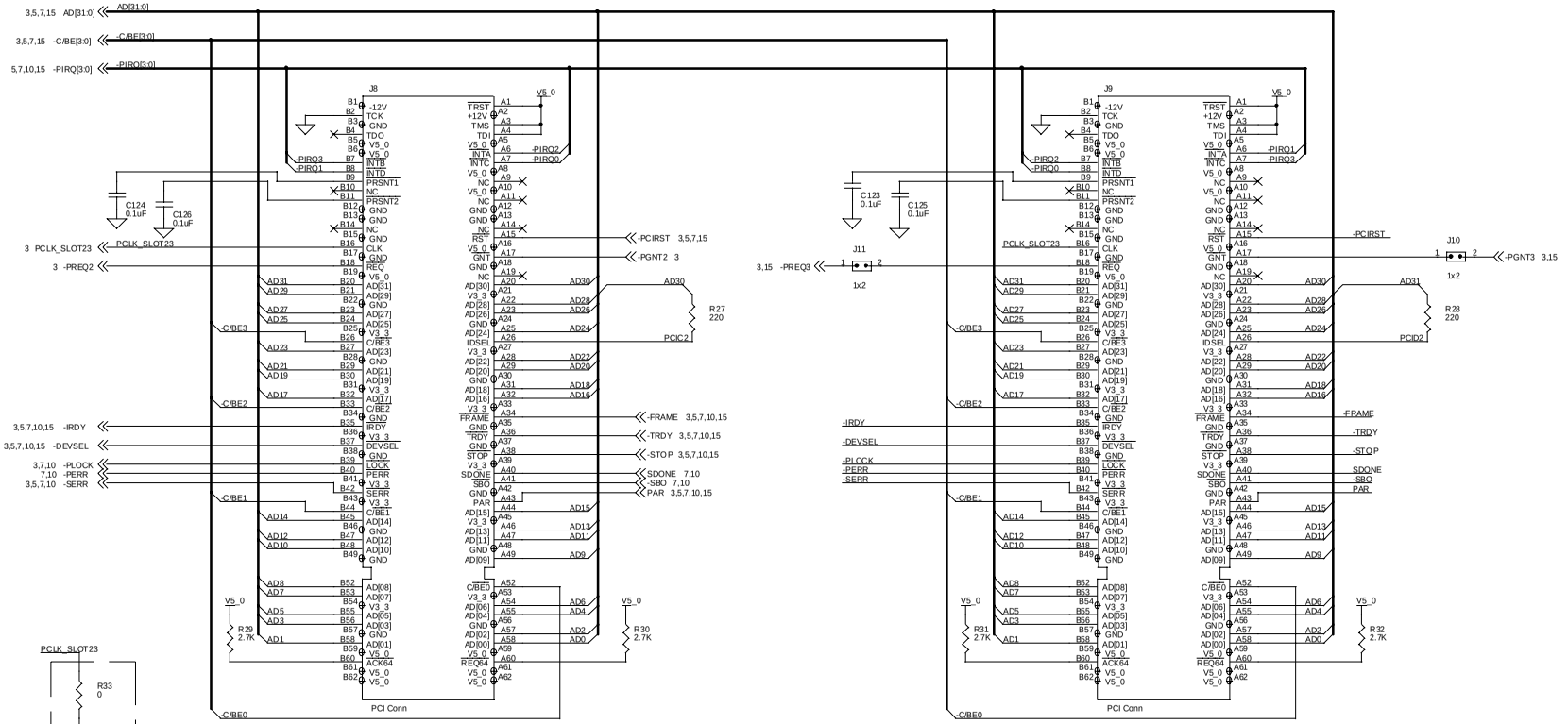
J8/J9 V3_3:
    A21, A27, A33, A39 A45, A53
    B25, B31, B36, B41, B43, B54

J8/J9 NC:
    A9, A11, A14, A19
    B10, B14

J8/J9 GND:
   A12, A13, A18, A24, A30, A35, A37, A42, A48, A56
   B3, B12, B13, B15, B17, B28, B34, B38, B46, B49,
B57 | B2

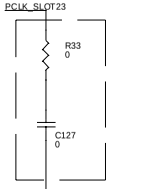
J8/J9 +12V: A2
      -12V: B1

PRELIMINARY



PCI SLOT 2

PCI SLOT 3



Place between PCI Slots 23 close to PCLK_SLOT23
DO NOT STUFF

NOTE: Slot 3 user notes.
1. Clock (PCLK_SLOT23) is shared w/ slot 2
2. Primary interrupt INTA (-PIRQ1) shared with Video
3. Slot 3 OR Video may use DMA but not both
   If video using DMA 3, pull jumpers out
   Virge GX B-step do not use DMA, C-step ok
   (see video page C-step stuff options)
4. If PCI Video card is used put it in slot 3

Title: EVEPMDEVBD - PCI Slots 2 & 3		
Size: C	Document Number: CB1	Rev: B.1
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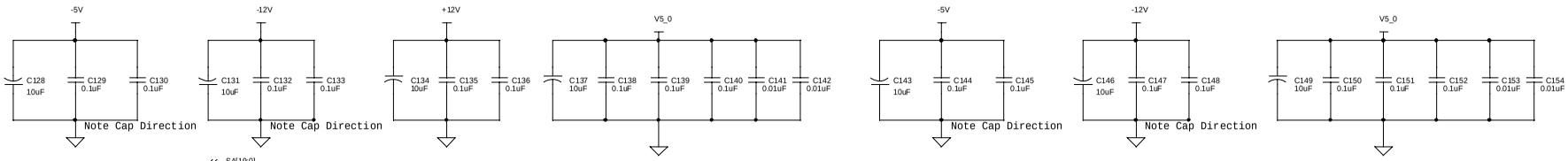
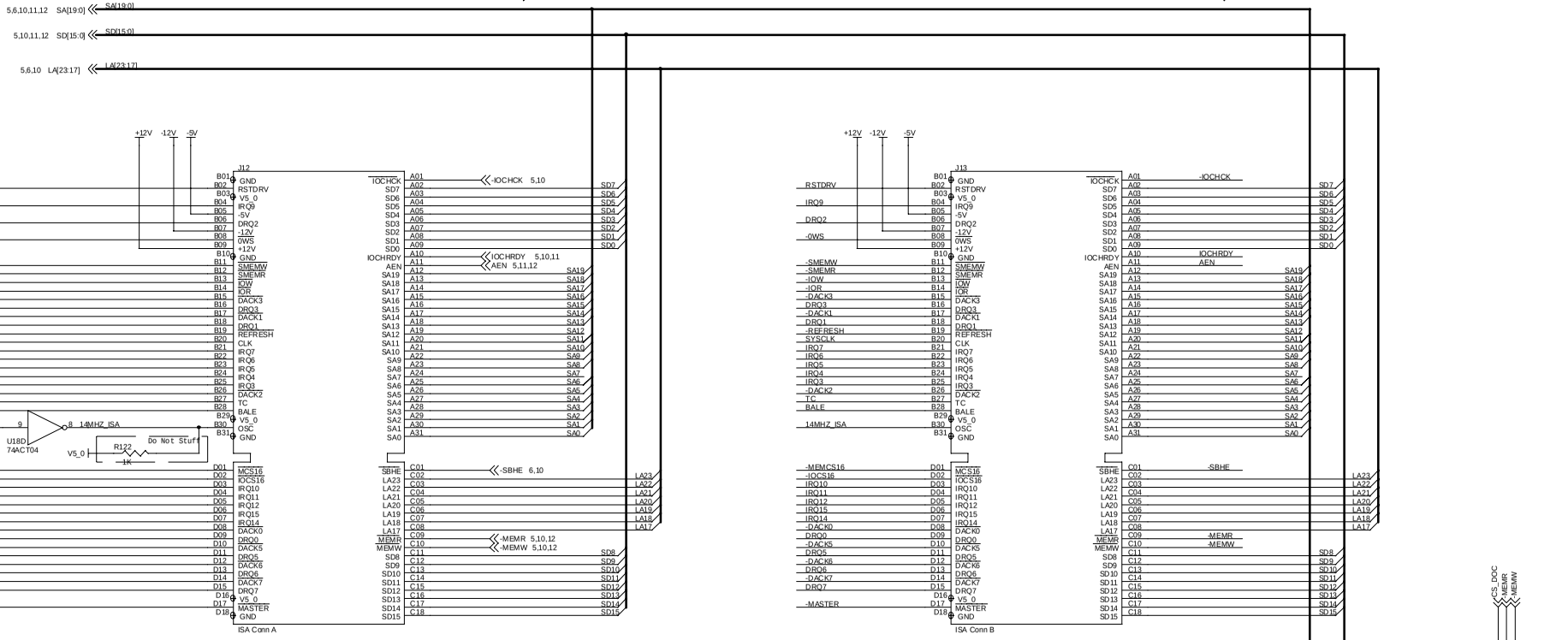
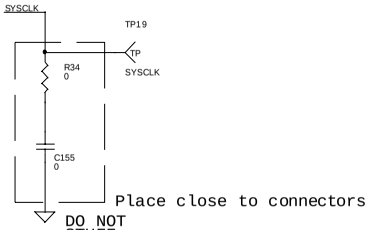
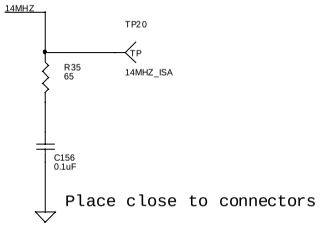
ISA Slots
Flash Disk

PRELIMINARY







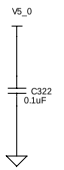


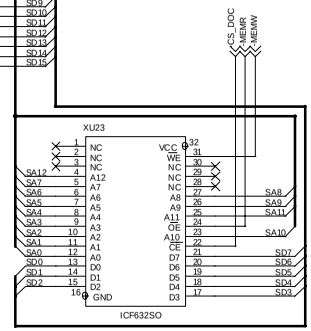
J10/11 V5_0:
B03, B29, B31, D16

J10/11 GND:
B01, B10, D18

J10/11: +12V B09
-12V B07
-5V B05

NOTE 1: ISA Conn B is a shared slot with PCI slot 3 (see ATX spec)





Title	EVEPMDEVBD - ISA Sockets Flash Disk		
Size C	Document Number CB1		Rev B.1
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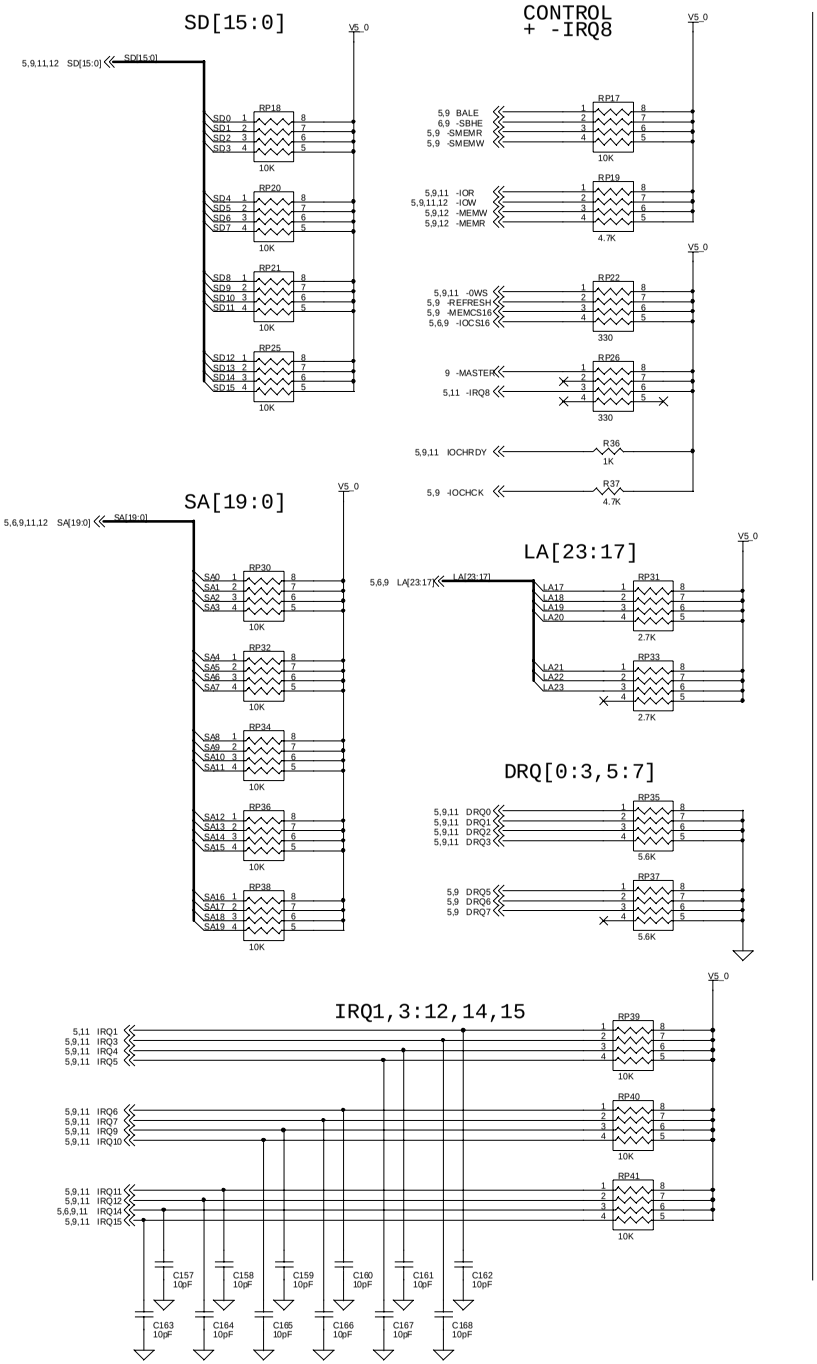
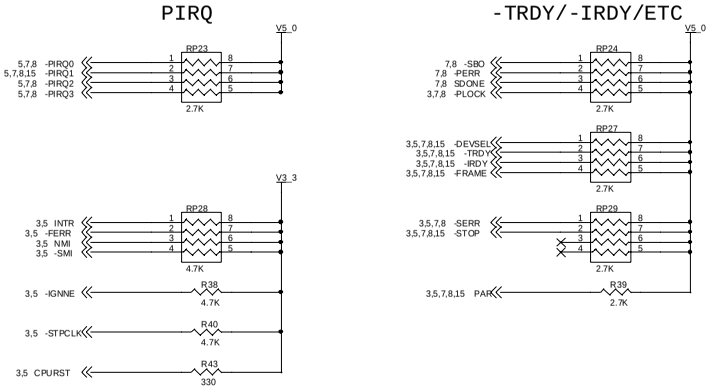
ISA Pullup/Pulldown

PRELIMINARY

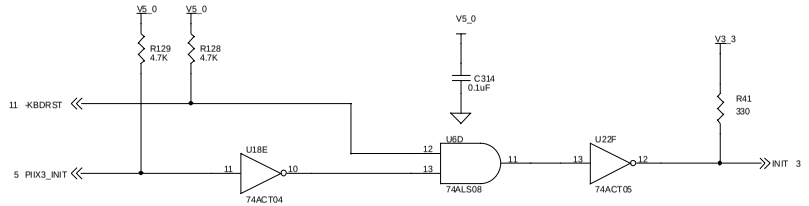


PCI Pullup/Pulldown



Note: 64-BIT PCI Strap Off At PCI Connectors

Note: Pullups on Embedded Processor
Module-PREQ/PGNT[3:0]



Title	EVEPMDEVBD - ISA Pullup/Pulldown	
Size C	Document Number CB1	Rev B.1
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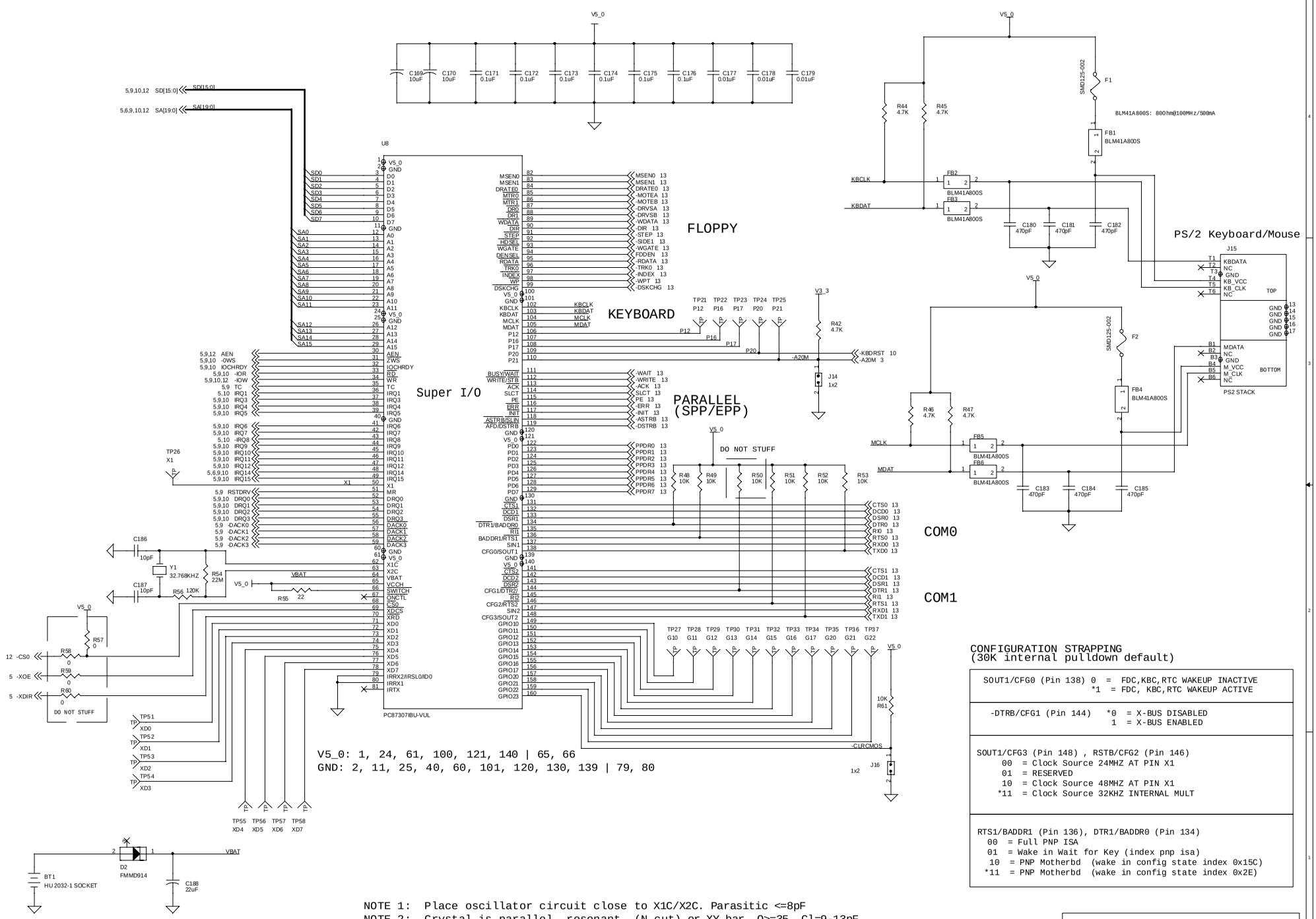

CONFIGURATION STRAPPING
(30K internal pulldown default)

SOUT1/CFG0 (Pin 138) 0 = FDC,KBC,RTC WAKEUP INACTIVE *1 = FDC, KBC,RTC WAKEUP ACTIVE
-DTRB/CFG1 (Pin 144) *0 = X-BUS DISABLED 1 = X-BUS ENABLED
SOUT1/CFG3 (Pin 148) , RSTB/CFG2 (Pin 146) 00 = Clock Source 24MHZ AT PIN X1 01 = RESERVED 10 = Clock Source 48MHZ AT PIN X1 *11 = Clock Source 32KHZ INTERNAL MULT
RTS1/BADDR1 (Pin 136), DTR1/BADDR0 (Pin 134) 00 = Full PNP ISA 01 = Wake in Wait for Key (index pnp isa) 10 = PNP Motherbd (wake in config state index 0x15C) *11 = PNP Motherbd (wake in config state index 0x2E)

NOTE 1: Place oscillator circuit close to X1C/X2C. Parasitic <=8pF
NOTE 2: Crystal is parallel, resonant, (N cut) or XY bar, Q>=35, Cl=9-13pF
NOTE 3: Test points are a hole/via such that a 25-mil square pin can be inserted.

Title	EVEPMDEVBD - Super I/O		
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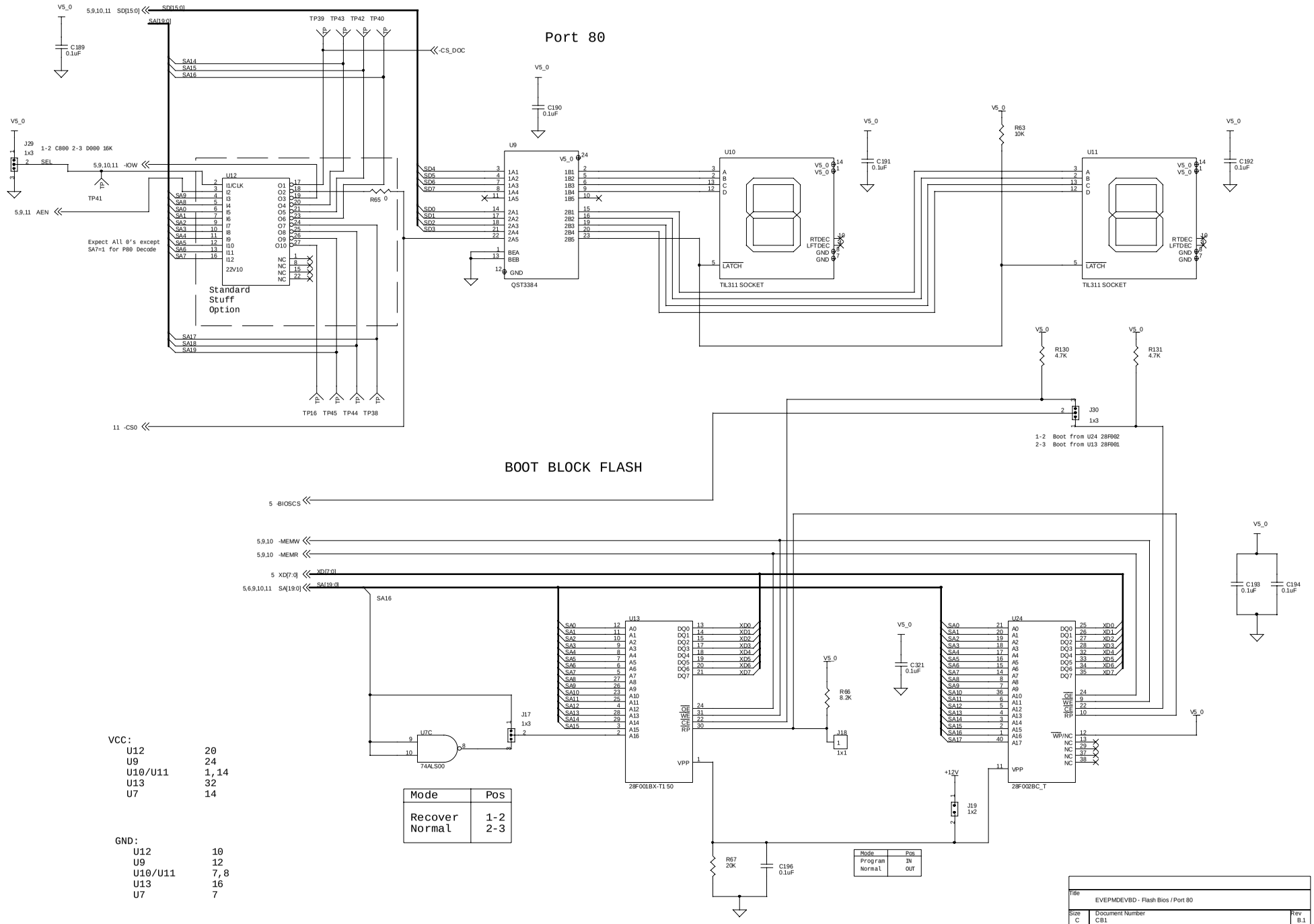
Port 80
BOOT BLOCK FLASH
Standard Stuff Option
Expect All 0's except SA7=1 for P80 Decode
TIL311 SOCKET
QST3384
28F001BX-T150
28F002BC_T
74ALS00
1-2 Boot from U24 28F002
2-3 Boot from U13 28F001
VCC:
U12 20
U9 24
U10/U11 1,14
U13 32
U7 14
GND:
U12 10
U9 12
U10/U11 7,8
U13 16
U7 7
Mode Pos
Recover 1-2
Normal 2-3
Mode Pos
Program IN
Normal OUT
Title EVEPMDEVBD - Flash Bios / Port 80
Size C
Document Number CB1
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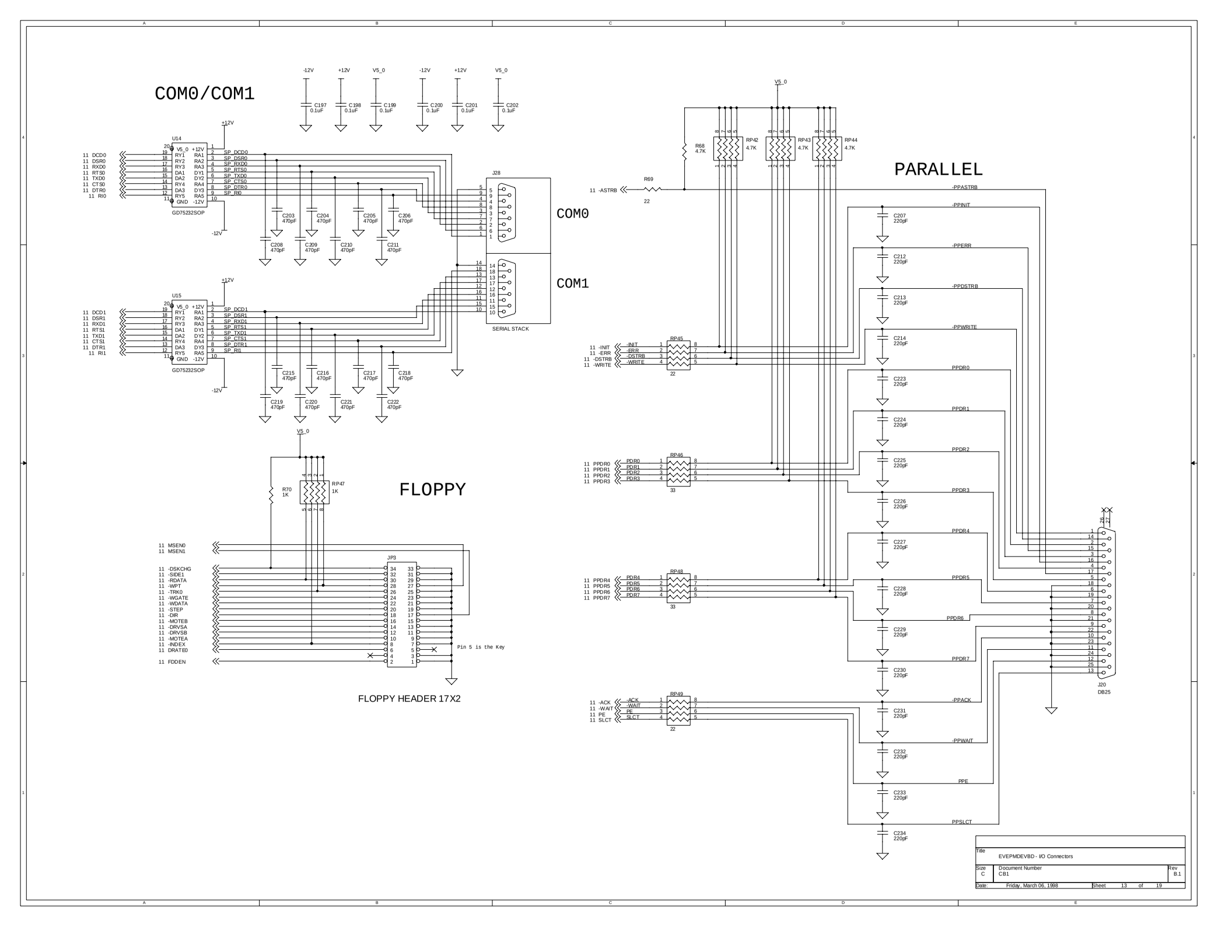
COM0/COM1
-12V
+12V
V5_0
C197 0.1uF
C198 0.1uF
C199 0.1uF
C200 0.1uF
C201 0.1uF
C202 0.1uF
U14
GD75232SOP
SP_DCD0
SP_DSR0
SP_RXD0
SP_RTS0
SP_TXD0
SP_CTS0
SP_DTR0
SP_RI0
C203 470pF
C204 470pF
C205 470pF
C206 470pF
C208 470pF
C209 470pF
C210 470pF
C211 470pF
J28
COM0
COM1
SERIAL STACK
U15
SP_DCD1
SP_DSR1
SP_RXD1
SP_RTS1
SP_TXD1
SP_CTS1
SP_DTR1
SP_RI1
C215 470pF
C216 470pF
C217 470pF
C218 470pF
C219 470pF
C220 470pF
C221 470pF
C222 470pF
FLOPPY
R70 1K
RP47 1K
JP3
MSEN0
MSEN1
-DSKCHG
-SIDE1
-RDATA
-WPT
-TRK0
-WGATE
-WDATA
-STEP
-DIR
-MOTEB
-DRVSA
-DRVSB
-MOTEA
-INDEX
DRATE0
FDDEN
Pin 5 is the Key
FLOPPY HEADER 17X2
PARALLEL
R68 4.7K
RP42 4.7K
RP43 4.7K
RP44 4.7K
R69
22
-ASTRB
-PPASTRB
-PPINIT
-PPERR
-PPDSTRB
-PPWRITE
C207 220pF
C212 220pF
C213 220pF
C214 220pF
C223 220pF
C224 220pF
C225 220pF
C226 220pF
C227 220pF
C228 220pF
C229 220pF
C230 220pF
C231 220pF
C232 220pF
C233 220pF
C234 220pF
RP45
-INIT
-ERR
-DSTRB
-WRITE
RP46
PDR0
PDR1
PDR2
PDR3
33
RP48
PDR4
PDR5
PDR6
PDR7
RP49
-ACK
-WAIT
PE
SLCT
PPDR0
PPDR1
PPDR2
PPDR3
PPDR4
PPDR5
PPDR6
PPDR7
-PPACK
-PPWAIT
PPE
PPSLCT
J20
DB25
Title
EVEPMDEVBD - I/O Connectors
Size
C
Document Number
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Rev
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Date:
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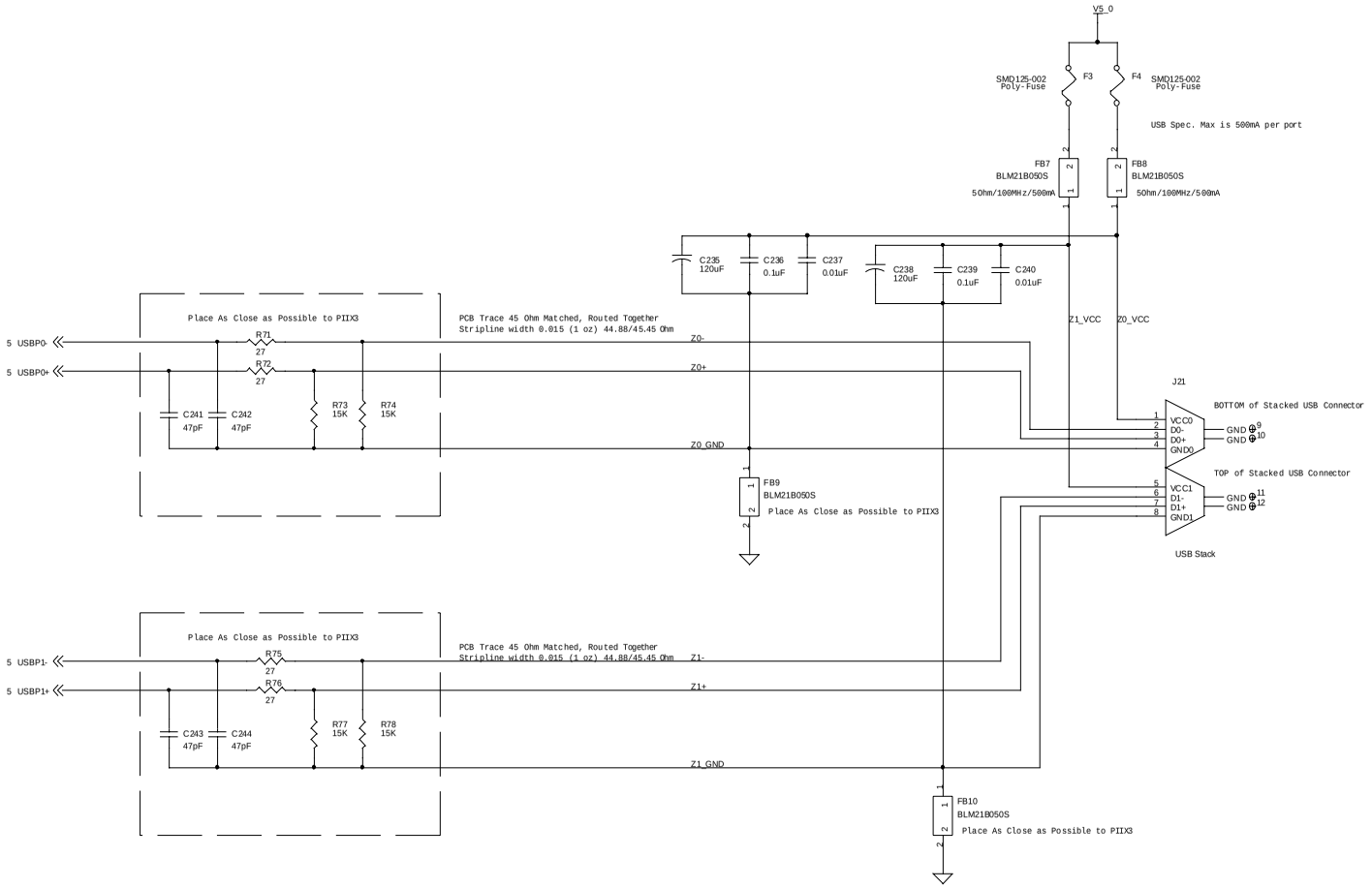
USB



NOTE 1: USB differential traces route together (Z0- & Z0+) and (Z1- & Z1+).
Must be 45 Ohm Matched
Stripline width 0.015 (for 1 oz)->44.88/45.45 Ohm.

NOTE 2: Protect differential traces w/ guard traces or
double space to any other signal.

NOTE 3: Place ferrites and C210-C215 at connector.

NOTE 4: Poly-fuse max 500mA

Title: EVEPMDEVBD - USB Ports		
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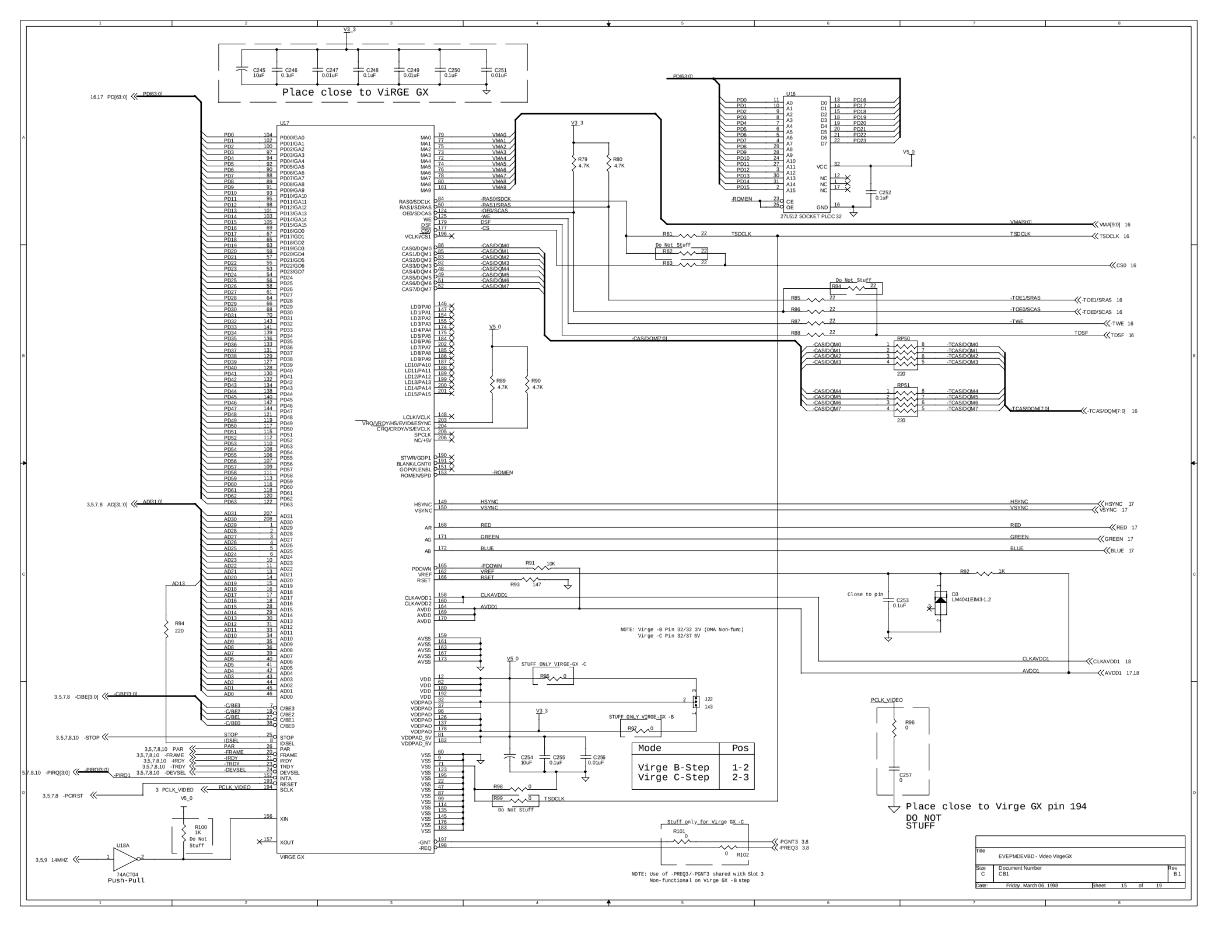
Place close to ViRGE GX
C245 10uF
C246 0.1uF
C247 0.01uF
C248 0.1uF
C249 0.01uF
C250 0.1uF
C251 0.01uF
V3_3
U17
PD[63:0]
VMA[9:0]
TSDCLK
-CS0
-TOE1/SRAS
-TOE0/SCAS
-TWE
TDSF
-CAS/DQM[7:0]
-TCAS/DQM[7:0]
HSYNC
VSYNC
RED
GREEN
BLUE
-PDOWN
VREF
RSET
CLKAVDD1
AVDD1
-ROMEN
-PGNT3 3,8
-PREQ3 3,8
U16
27L512 SOCKET PLCC 32
-ROMEN
V5_0
C252 0.1uF
RP50
RP51
220
R79 4.7K
R80 4.7K
R81 22
R82 22
R83 22
R84 22
R85 22
R86 22
R87 22
R88 22
Do Not Stuff
R89 4.7K
R90 4.7K
R91 10K
R92 1K
R93 147
R94 220
C253 0.1uF
D3 LM4041EIM3-1.2
Close to pin
NOTE: Virge -B Pin 32/32 3V (DMA Non-func)
Virge -C Pin 32/37 5V
STUFF ONLY VIRGE-GX -C
R95 0
STUFF ONLY VIRGE-GX -B
R97 0
J22 1x3
C254 10uF
C255 0.1uF
C256 0.01uF
R98 0
R99 0
Do Not Stuff
Mode | Pos
Virge B-Step | 1-2
Virge C-Step | 2-3
PCLK_VIDEO
R96 0
C257 0
Place close to Virge GX pin 194
DO NOT STUFF
R100 1K Do Not Stuff
U18A
74ACT04
Push-Pull
14MHZ
XIN
XOUT
VIRGE GX
Stuff only for Virge GX -C
R101 0
R102 0
NOTE: Use of -PREQ3/-PGNT3 shared with Slot 3
Non-functional on Virge GX -B step
Title
EVEPMDEVBD - Video VirgeGX
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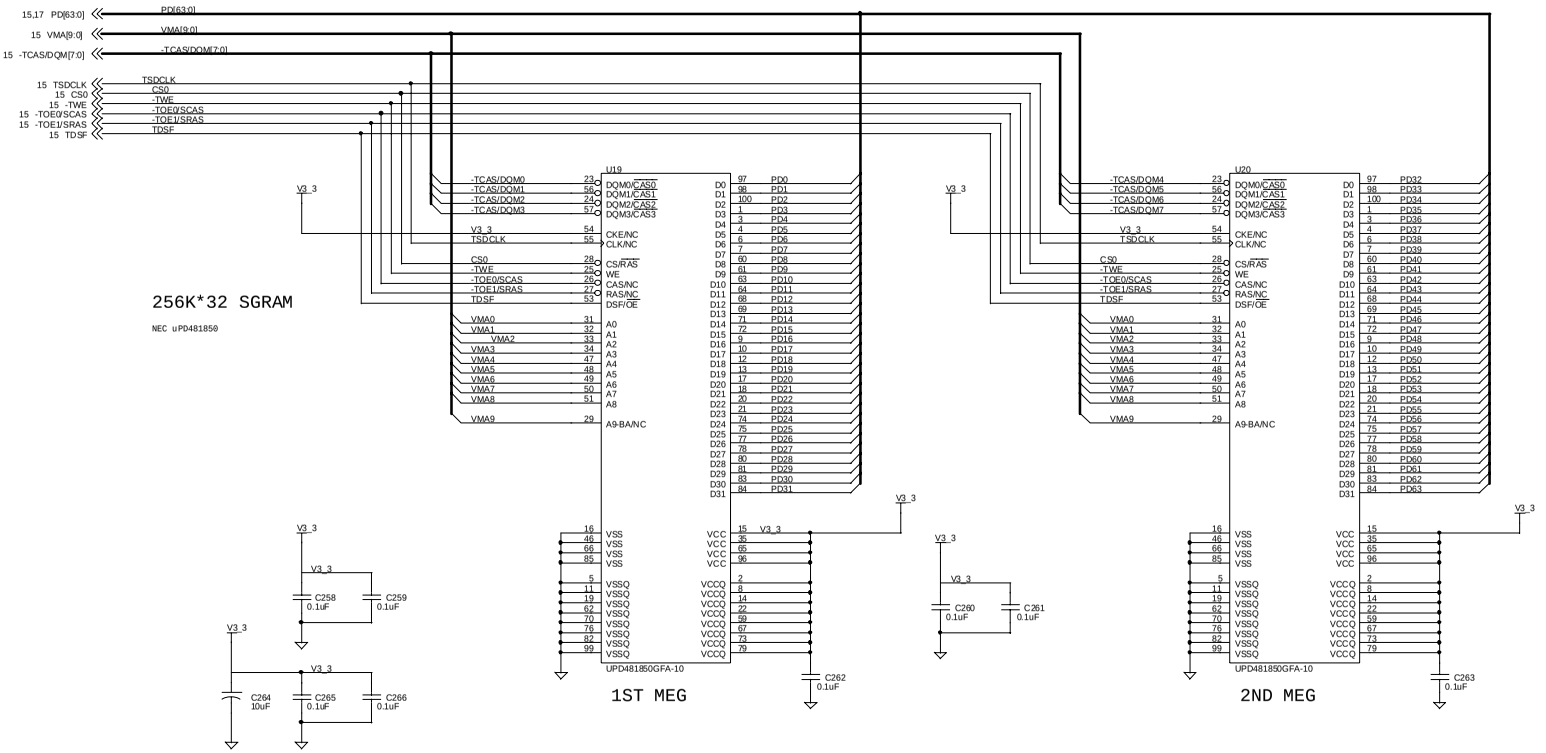

Title	EVEPMDEVBD - Video SGRAM	
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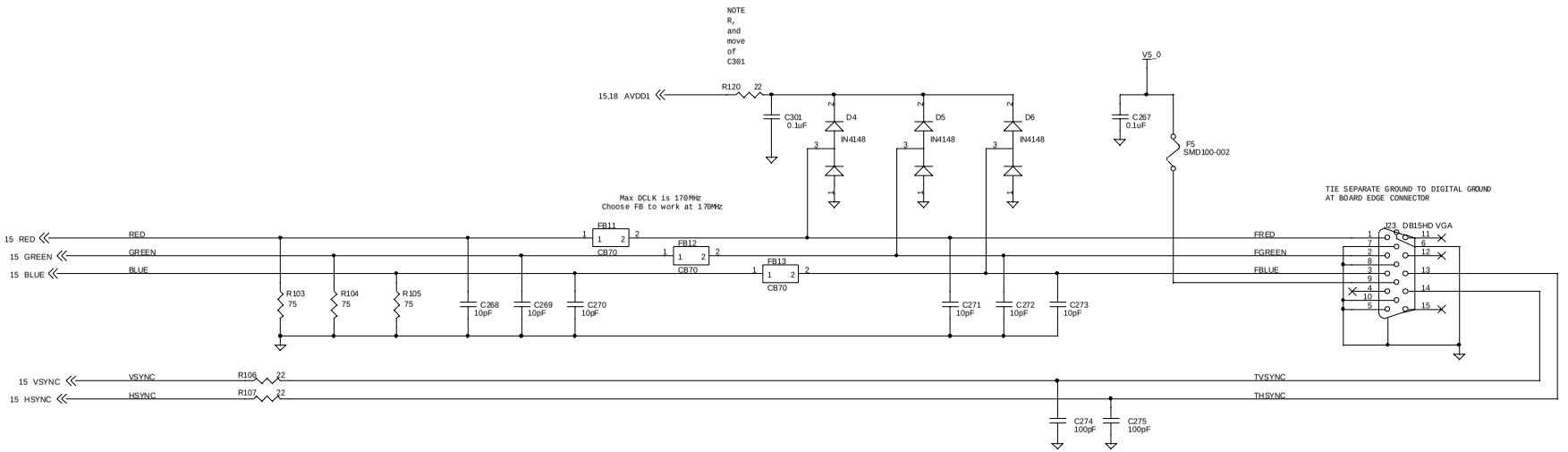
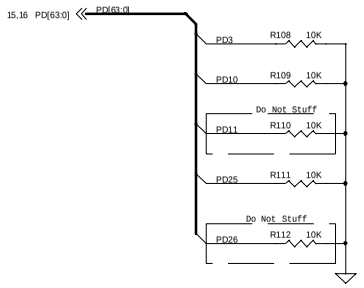


STRAPPING RESISTORS



RESISTOR	OPTION L-H	FUNCTION
PD3/2	IN/OUT*	SGRAM
PD9	OUT*	ViRGE GX IN TEST MODE
PD10	IN	READ PCI SUBSYS ID FROM ROM
PD11	OUT*	INTERNAL CLOCK SELECT
PD17/16	OUT*/OUT*	0 UNITS CAS/OE STRETCH
PD18	OUT*	3.5 MCLKS RAS LOW
PD19	OUT*	2.5 MCLKS RAS PRE-CHARGE
PD24	OUT*	GX BONDOUT OPTION
PD25	IN OUT*	MMFF20 AT I/O ADDRESS 000E8H MMFF20 AT I/O ADDRESS 000E2H
PD26	IN OUT*	MMFF20 ACCESS AT I/O OR MMIO MMFF20 ACCESS AT MMIO ONLY
PD28/27	OUT*/OUT*	0 UNITS WE DELAY
NOTE: * = Default pullup by Virge GX		

Title: EVEPMDEVBD - Video VGA Connector		
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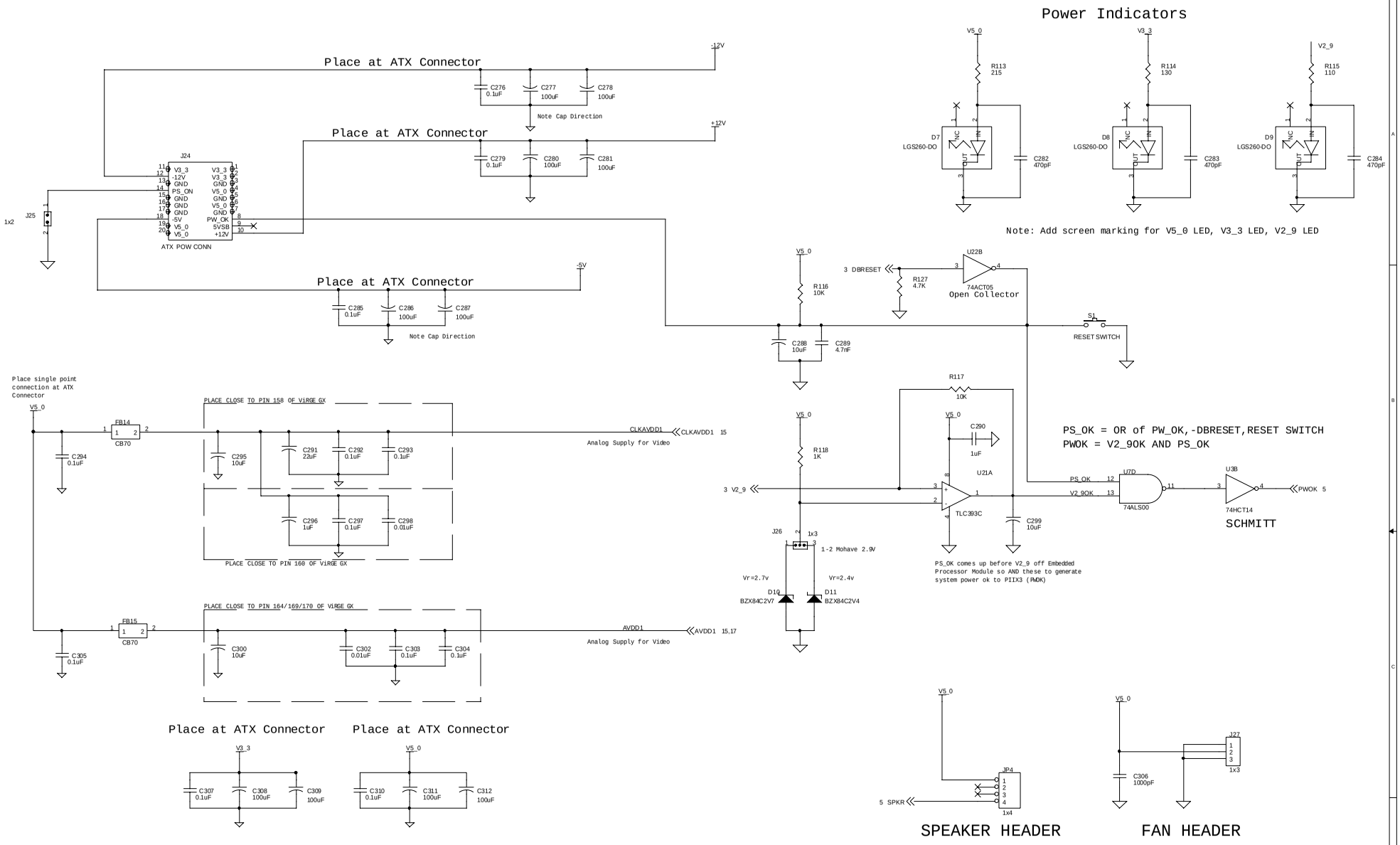

NOTE 1: Place R128/R129 side by side.
NOTE 2: Locate Fan Header next to Embedded Processor Module PCI Connector
Note 3: Connect V5_0 feed for analog supplies AVDD1 and CLKAVDD1 at one point only on PCB
Note 4: Place power connector decoupling at ATX connector
NOTE 5: Note direction of caps on -12V, -5V supplies.

Title	EVEPMDEVBD - Power	
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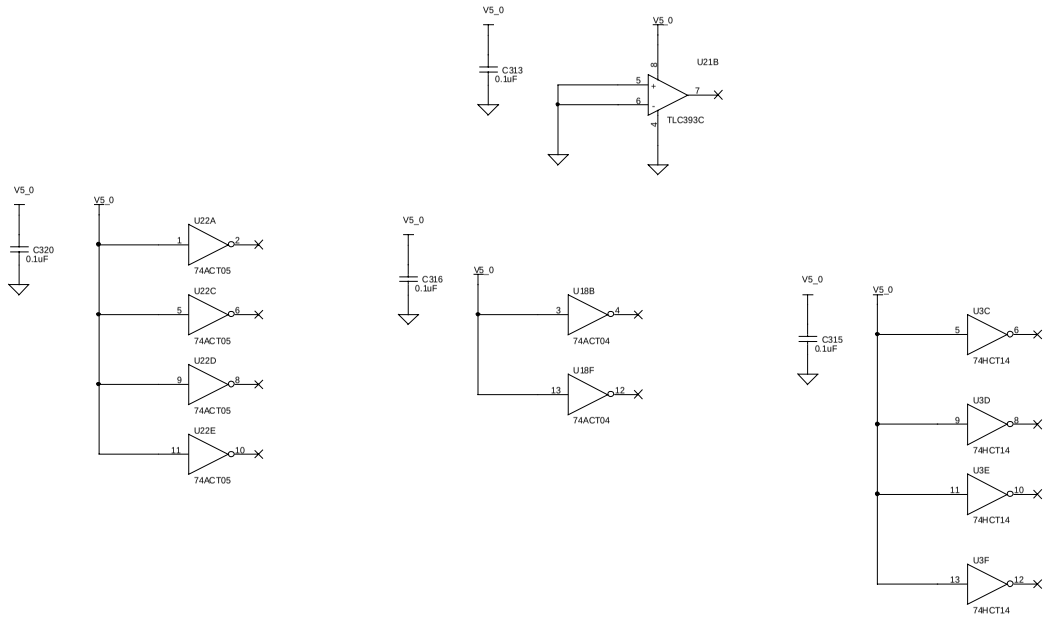

10-Layer Stackup
1. Top Signal
2. GND
3. X1 Signal
4. Y1 Signal
5. Vcc (5v)
6. GND
7. X2 Signal
8. Y2 Signal
9. Voltage (3V/5V)
10. Bottom Signal

NOTE 1: Make inputs to spare gates traces (not vias) so they can be cut and used.

Revisions:

B.1
1. Added DIP 32 Socket to ISA bus for flash disk
2. Added flash disk decode to 22V10
   -Added SA14-SA19, CS_DOC, SEN
   -Revised PLD code for decode
3. Added TSOP footprint for larger flash bios

A.3
Removed R32
R100, R121, R122 package
changed from 0805 to 1206
U18 nets altered to make
14MHZ_ISA, 14MHZ_U17
14MHZ_U1
GND test points added

A.2
1. Revision A.2 updated in data block of all pages
2. Resistor changed from 5.1M to 4.7M
3. Resistor changed from 20M to 10M
4. Added connection dots for C193 (page 12) and R67
5. J26 value attribute changed from 1x2 to actual 1x3
6. Parallel port -INIT and PCI INIT signals incorrectly connected, fixed. U1, J2, R41 are INIT. U8 and RP45 are -INIT
7. PAR and -FRAME incorrectly connected at U17, fixed
8. U18 (74HCT05) changed to 74ALS05
9. D2 symbol changed to reflect SOT23
10. D4,D5,D6 pins changed to reflect selected SOT23
11. Deleted TP16

A.1
1. Added J29 1x3 jumper so Virge GX can be held in reset
2. Removed JP1/JP2 serial headers & replaced with stacked serial connector J28, connecting nets altered for change

Note: Some layout packages cannot handle alpha characters in the pin name (ie A01, B05, etc.) and therefore require hand edits to the netlist to convert such symbols into purely numeric pin names.

Future uses of J6, J7, J8, J9, J12 and J13, may want to move the pin names Ax, Bx, ect. to the pin label and just number the pins without "A" and "B". This would make it easier for some layout packages to use the netlist directly.

Title: EVEPMDEVBD - Extra Gates		
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