PRELIMINARY

Pentium® PROCESSORS AT iCOMP® INDEX 1110\133, 1000\120, 815\100 MHz WITH VOLTAGE REDUCTION TECHNOLOGY

SmartDie™ Product Specification

- **Compatible with Large Software Base**
  - **MS-DOS*, Windows*, OS/2*, UNIX***
- **32-Bit CPU with 64-Bit Data Bus**
- **Superscalar Architecture**
  - **Two Pipelined Integer Units Are Capable of 2 Instructions/Clock**
  - **Pipelined Floating Point Unit**
- **Separate Code and Data Caches**
  - **8 Kbyte Code, 8 Kbyte Writeback Data**
  - **MESI Cache Protocol**
- **Advanced Design Features**
  - **Branch Prediction**
  - **Virtual Mode Extensions**
- **Low-Voltage BiCMOS Silicon Technology**
- **4 Mbyte Pages for Increased TLB Hit Rate**
- **IEEE 1149.1 Boundary Scan**
- **Internal Error Detection Features**
- **SL Enhanced Power Management Features**
  - **System Management Mode**
  - **Clock Control**
- **Voltage Reduction Technology**
  - **2.9 V V_{CC} for Core Supply**
  - **3.3 V V_{CC} for I/O Buffer Supply**
- **Fractional Bus Operation**
  - **100-MHz Core/66-MHz Bus**
  - **120-MHz Core/60-MHz Bus**
  - **133-MHz Core/66-MHz Bus**
- **Intel SmartDie™ Product**
  - **Full AC/DC Testing at Die Level**
  - **0°C to 105°C (Junction) Temperature Range**

NOTICE: This document contains preliminary information on new products in production. It is valid for the devices indicated in "DEVICE NOMENCLATURE" on page 17. This specification is subject to change without notice. Verify with your local Intel sales office that you have the latest product specification before finalizing a design.

REFERENCE INFORMATION: The information in this document is provided as a supplement to the standard package datasheet on a specific product. Please refer to the standard package datasheet (order number 242557) for product information and specifications not found in this document.

*Other brands and names are the property of their respective owners.

March 1996 Order Number: 272825-001

Pentium® PROCESSORS AT iCOMP® INDEX 1110\133, 1000\120, 815\100 MHz WITH VOLTAGE REDUCTION TECHNOLOGY

SmartDie™ Product Specification

1.0 DIE SPECIFICATIONS

The die photo below and the plot on page 2 indicate the orientation of the die in the GEL-PAK* shipping container. Die are aligned as shown relative to a 45° notch in one corner of the GEL-PAK. An Intel internal manufacturing name “80502” appears on the die. Table 1 describes the bond pad number and pad center data for each signal.

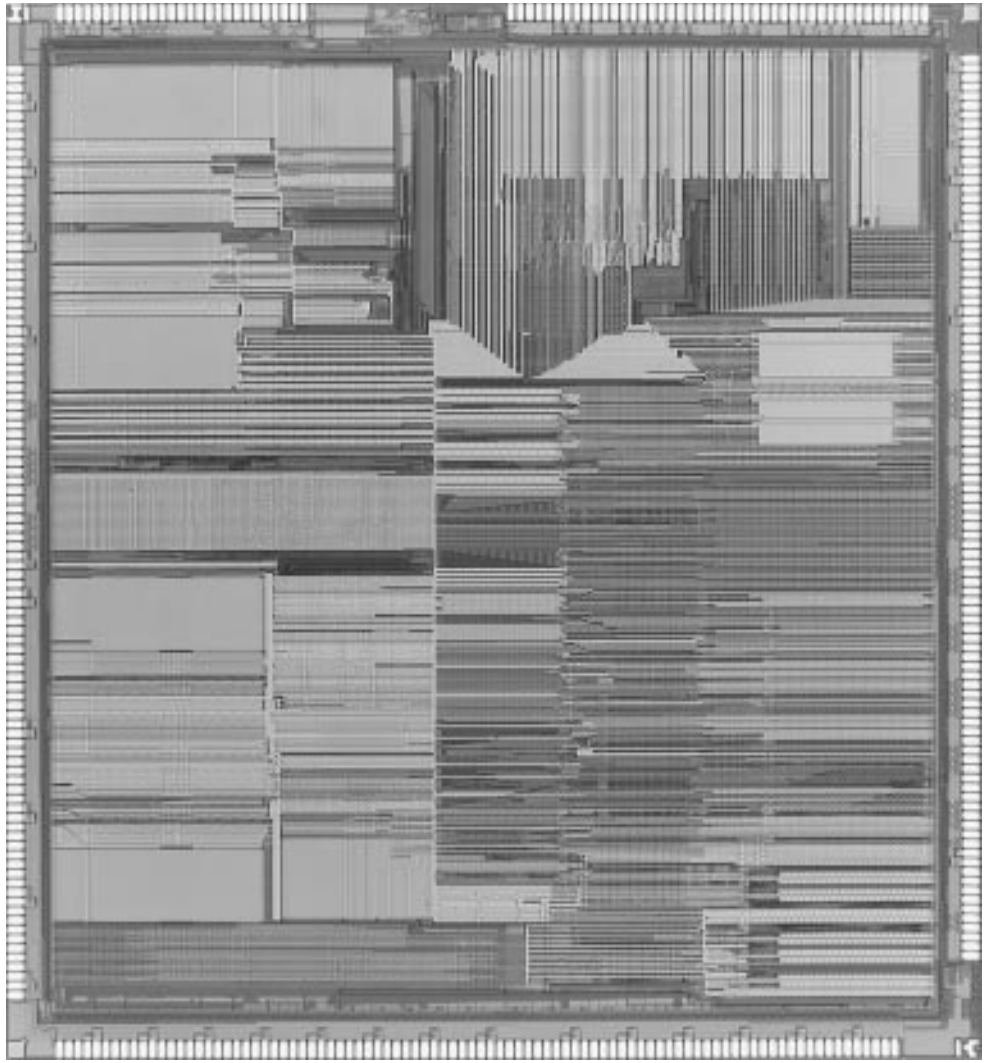


Figure 1. Pentium® Processor Die Photo

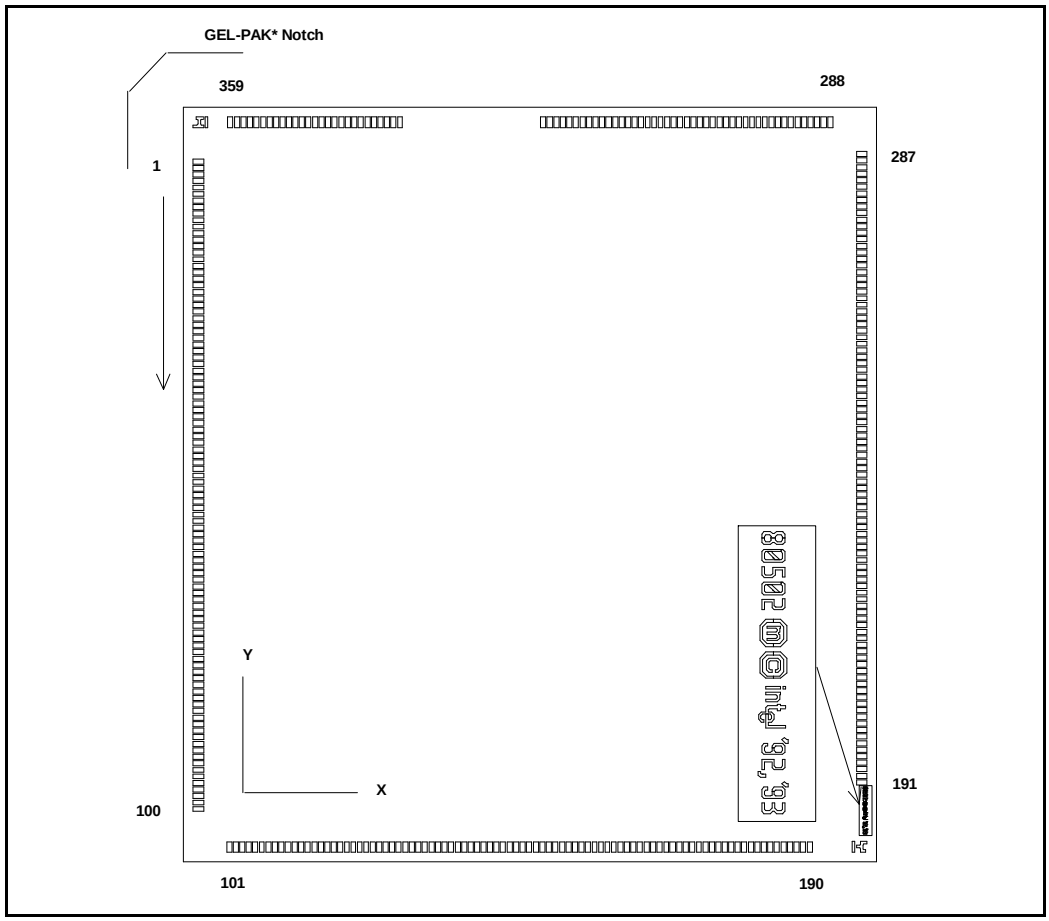


Figure 2. Pentium® Processor Die/Bond Pad Layout

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 1 of 12)

PAD#	SIGNAL[2,3,4]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
001	D/C#	-173.1	168.1	-4396	4271
002	PWT	-173.1	164.7	-4396	4184
003	PCD	-173.1	161.3	-4396	4098
004	V_{CC}_3.3	-173.1	157.9	-4396	4011
005	V_{SS}	-173.1	154.5	-4396	3925
006	N.C.	-173.1	151.1	-4396	3839
007	LOCK#	-173.1	147.7	-4396	3752
008	V_{CC}_2.9	-173.1	144.3	-4396	3666
009	V_{CC}_2.9	-173.1	140.9	-4396	3579
010	V_{SS}	-173.1	137.5	-4396	3493
011	V_{CC}_3.3	-173.1	134.1	-4396	3407
012	V_{SS}	-173.1	130.7	-4396	3320
013	AP	-173.1	127.3	-4396	3234
014	V_{CC}_2.9	-173.1	123.9	-4396	3147
015	V_{CC}_2.9	-173.1	120.5	-4396	3061
016	V_{SS}	-173.1	117.1	-4396	2975
017	HLDA	-173.1	113.7	-4396	2888
018	BREQ	-173.1	110.3	-4396	2802
019	V_{CC}_3.3	-173.1	106.9	-4396	2715
020	V_{SS}	-173.1	103.5	-4396	2629
021	APCHK#	-173.1	100.1	-4396	2543
022	PCHK#	-173.1	96.7	-4396	2456
023	V_{CC}_2.9	-173.1	93.3	-4396	2370
024	V_{CC}_2.9	-173.1	89.9	-4396	2283
025	V_{SS}	-173.1	86.5	-4396	2197
026	PRDY	-173.1	83.1	-4396	2111
027	SMIACT#	-173.1	79.7	-4396	2024
028	N.C.	-173.1	76.3	-4396	1938
029	V_{CC}_3.3	-173.1	72.9	-4396	1851
030	V_{SS}	-173.1	69.5	-4396	1765
031	N.C.	-173.1	66.1	-4396	1679

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 2 of 12)

PAD#	SIGNAL[2,3,4]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
032	N.C.	-173.1	62.7	-4396	1592
033	N.C.	-173.1	59.3	-4396	1506
034	V_{SS}	-173.1	55.9	-4396	1419
035	V_{CC}_2.9	-173.1	52.5	-4396	1333
036	V_{CC}_2.9	-173.1	49.1	-4396	1247
037	HOLD	-173.1	45.7	-4396	1160
038	WB/WT#	-173.1	42.3	-4396	1074
039	V_{CC}_2.9	-173.1	38.9	-4396	987
040	V_{CC}_2.9	-173.1	35.5	-4396	901
041	V_{SS}	-173.1	32.1	-4396	815
042	NA#	-173.1	28.7	-4396	728
043	BOFF#	-173.1	25.3	-4396	642
044	N.C.	-173.1	21.9	-4396	555
045	BRDY#	-173.1	18.5	-4396	469
046	V_{CC}_2.9	-173.1	15.1	-4396	383
047	V_{CC}_2.9	-173.1	11.7	-4396	296
048	V_{SS}	-173.1	8.3	-4396	210
049	KEN#	-173.1	4.9	-4396	123
050	AHOLD	-173.1	1.5	-4396	37
051	INV	-173.1	-1.9	-4396	-49
052	EWBE#	-173.1	-5.3	-4396	-136
053	V_{CC}_3.3	-173.1	-8.7	-4396	-222
054	V_{SS}	-173.1	-12.2	-4396	-309
055	CACHE#	-173.1	-15.6	-4396	-395
056	M/IO#	-173.1	-19.0	-4396	-481
057	V_{CC}_3.3	-173.1	-22.4	-4396	-568
058	V_{SS}	-173.1	-25.8	-4396	-654
059	BP3	-173.1	-29.2	-4396	-741
060	V_{SS}	-173.1	-32.6	-4396	-827
061	V_{CC}_2.9	-173.1	-36.0	-4396	-913
062	V_{CC}_2.9	-173.1	-39.4	-4396	-1000

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 3 of 12)

PAD#	SIGNAL[2,3,4]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
063	BP2	-173.1	-42.8	-4396	-1086
064	PM1/BP1	-173.1	-46.2	-4396	-1173
065	PM0/BP0	-173.1	-49.6	-4396	-1259
066	FERR#	-173.1	-53.0	-4396	-1345
067	V_{SS}	-173.1	-56.4	-4396	-1432
068	V_{CC}_2.9	-173.1	-59.8	-4396	-1518
069	V_{CC}_2.9	-173.1	-63.2	-4396	-1605
070	IERR#	-173.1	-66.6	-4396	-1691
071	V_{CC}_3.3	-173.1	-70.0	-4396	-1777
072	V_{SS}	-173.1	-73.4	-4396	-1864
073	DP7	-173.1	-76.8	-4396	-1950
074	D63	-173.1	-80.2	-4396	-2037
075	D62	-173.1	-83.6	-4396	-2123
076	D61	-173.1	-87.0	-4396	-2209
077	V_{CC}_2.9	-173.1	-90.4	-4396	-2296
078	V_{CC}_2.9	-173.1	-93.8	-4396	-2382
079	V_{SS}	-173.1	-97.2	-4396	-2469
080	V_{CC}_3.3	-173.1	-100.6	-4396	-2555
081	V_{SS}	-173.1	-104.0	-4396	-2641
082	D60	-173.1	-107.4	-4396	-2728
083	D59	-173.1	-110.8	-4396	-2814
084	D58	-173.1	-114.2	-4396	-2901
085	D57	-173.1	-117.6	-4396	-2987
086	V_{CC}_2.9	-173.1	-121.0	-4396	-3073
087	V_{CC}_2.9	-173.1	-124.4	-4396	-3160
088	V_{SS}	-173.1	-127.8	-4396	-3246
089	V_{CC}_3.3	-173.1	-131.2	-4396	-3333
090	V_{SS}	-173.1	-134.6	-4396	-3419
091	D56	-173.1	-138.0	-4396	-3505
092	DP6	-173.1	-141.4	-4396	-3592
093	D55	-173.1	-144.8	-4396	-3678

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 4 of 12)

PAD#	SIGNAL[2,3,4]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
094	D54	-173.1	-148.2	-4396	-3765
095	V_{CC}_2.9	-173.1	-151.6	-4396	-3851
096	V_{CC}_2.9	-173.1	-155.0	-4396	-3937
097	V_{SS}	-173.1	-158.4	-4396	-4024
098	V_{CC}_3.3	-173.1	-161.8	-4396	-4110
099	V_{SS}	-173.1	-165.2	-4396	-4197
100	D53	-173.1	-168.6	-4396	-4283
101	D52	-157.0	-188.4	-3988	-4786
102	D51	-153.6	-188.4	-3902	-4786
103	D50	-150.2	-188.4	-3816	-4786
104	V_{CC}_3.3	-146.8	-188.4	-3729	-4786
105	V_{SS}	-143.4	-188.4	-3643	-4786
106	D49	-140.0	-188.4	-3556	-4786
107	D48	-136.6	-188.4	-3470	-4786
108	DP5	-133.2	-188.4	-3384	-4786
109	D47	-129.8	-188.4	-3297	-4786
110	V_{CC}_3.3	-126.4	-188.4	-3211	-4786
111	V_{SS}	-123.0	-188.4	-3124	-4786
112	D46	-119.6	-188.4	-3038	-4786
113	D45	-116.2	-188.4	-2952	-4786
114	D44	-112.8	-188.4	-2865	-4786
115	D43	-109.4	-188.4	-2779	-4786
116	V_{CC}_3.3	-106.0	-188.4	-2692	-4786
117	V_{SS}	-102.6	-188.4	-2606	-4786
118	D42	-99.2	-188.4	-2520	-4786
119	D41	-95.8	-188.4	-2433	-4786
120	D40	-92.4	-188.4	-2347	-4786
121	DP4	-89.0	-188.4	-2260	-4786
122	V_{CC}_3.3	-85.6	-188.4	-2174	-4786
123	V_{SS}	-82.2	-188.4	-2088	-4786
124	D39	-78.8	-188.4	-2001	-4786

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 5 of 12)

PAD#	SIGNAL(2,3,4)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
125	D38	-75.4	-188.4	-1915	-4786
126	D37	-72.0	-188.4	-1828	-4786
127	D36	-68.6	-188.4	-1742	-4786
128	V_{CC}_3.3	-65.2	-188.4	-1656	-4786
129	V_{SS}	-61.8	-188.4	-1569	-4786
130	D35	-58.4	-188.4	-1483	-4786
131	D34	-55.0	-188.4	-1396	-4786
132	D33	-51.6	-188.4	-1310	-4786
133	D32	-48.2	-188.4	-1224	-4786
134	V_{CC}_3.3	-44.8	-188.4	-1137	-4786
135	V_{SS}	-41.4	-188.4	-1051	-4786
136	DP3	-38.0	-188.4	-964	-4786
137	D31	-34.6	-188.4	-878	-4786
138	D30	-31.2	-188.4	-792	-4786
139	D29	-27.8	-188.4	-705	-4786
140	V_{CC}_3.3	-24.4	-188.4	-619	-4786
141	V_{SS}	-21.0	-188.4	-532	-4786
142	D28	-17.6	-188.4	-446	-4786
143	D27	-14.2	-188.4	-360	-4786
144	D26	-10.8	-188.4	-273	-4786
145	D25	-7.4	-188.4	-187	-4786
146	V_{CC}_3.3	-4.0	-188.4	-100	-4786
147	V_{SS}	-0.6	-188.4	-14	-4786
148	V_{CC}_2.9	2.9	-188.4	72	-4786
149	V_{CC}_2.9	6.3	-188.4	159	-4786
150	V_{SS}	9.7	-188.4	245	-4786
151	D24	13.1	-188.4	332	-4786
152	DP2	16.5	-188.4	418	-4786
153	D23	19.9	-188.4	504	-4786
154	D22	23.3	-188.4	591	-4786
155	V_{CC}_3.3	26.7	-188.4	677	-4786

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 6 of 12)

PAD#	SIGNAL[2,3,4]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
156	V_{SS}	30.1	-188.4	764	-4786
157	D21	33.5	-188.4	850	-4786
158	D20	36.9	-188.4	936	-4786
159	D19	40.3	-188.4	1023	-4786
160	D18	43.7	-188.4	1109	-4786
161	V_{CC}_3.3	47.1	-188.4	1196	-4786
162	V_{SS}	50.5	-188.4	1282	-4786
163	D17	53.9	-188.4	1368	-4786
164	D16	57.3	-188.4	1455	-4786
165	DP1	60.7	-188.4	1541	-4786
166	D15	64.1	-188.4	1628	-4786
167	V_{CC}_3.3	67.5	-188.4	1714	-4786
168	V_{SS}	70.9	-188.4	1800	-4786
169	D14	74.3	-188.4	1887	-4786
170	D13	77.7	-188.4	1973	-4786
171	D12	81.1	-188.4	2060	-4786
172	D11	84.5	-188.4	2146	-4786
173	V_{CC}_3.3	87.9	-188.4	2232	-4786
174	V_{SS}	91.3	-188.4	2319	-4786
175	D10	94.7	-188.4	2405	-4786
176	D9	98.1	-188.4	2492	-4786
177	D8	101.5	-188.4	2578	-4786
178	DP0	104.9	-188.4	2664	-4786
179	V_{CC}_3.3	108.3	-188.4	2751	-4786
180	V_{SS}	111.7	-188.4	2837	-4786
181	D7	115.1	-188.4	2924	-4786
182	D6	118.5	-188.4	3010	-4786
183	D5	121.9	-188.4	3096	-4786
184	D4	125.3	-188.4	3183	-4786
185	V_{CC}_3.3	128.7	-188.4	3269	-4786
186	V_{SS}	132.1	-188.4	3356	-4786

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 7 of 12)

PAD#	SIGNAL(2,3,4)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
187	D3	135.5	-188.4	3442	-4786
188	D2	138.9	-188.4	3528	-4786
189	D1	142.3	-188.4	3615	-4786
190	D0	145.7	-188.4	3701	-4786
191	V_{CC}_2.9	173.1	-154.7	4396	-3930
192	V_{CC}_2.9	173.1	-151.3	4396	-3844
193	V_{SS}	173.1	-147.9	4396	-3757
194	N.C.	173.1	-144.5	4396	-3671
195	N.C.	173.1	-141.1	4396	-3584
196	N.C.	173.1	-137.7	4396	-3498
197	V_{CC}_2.9	173.1	-134.3	4396	-3412
198	V_{CC}_2.9	173.1	-130.9	4396	-3325
199	V_{SS}	173.1	-127.5	4396	-3239
200	N.C.	173.1	-124.1	4396	-3152
201	V_{SS}	173.1	-120.7	4396	-3066
202	V_{CC}_3.3	173.1	-117.3	4396	-2980
203	TCK	173.1	-113.9	4396	-2893
204	TDO	173.1	-110.5	4396	-2807
205	TDI	173.1	-107.1	4396	-2720
206	TMS	173.1	-103.7	4396	-2634
207	TRST#	173.1	-100.3	4396	-2548
208	V_{CC}_2.9	173.1	-96.9	4396	-2461
209	V_{CC}_2.9	173.1	-93.5	4396	-2375
210	V_{SS}	173.1	-90.1	4396	-2288
211	N.C.	173.1	-86.7	4396	-2202
212	V_{CC}_3.3	173.1	-83.3	4396	-2116
213	N.C.	173.1	-79.9	4396	-2029
214	V_{SS}	173.1	-76.5	4396	-1943
215	V_{CC}_2.9	173.1	-73.1	4396	-1856
216	V_{CC}_2.9	173.1	-69.7	4396	-1770
217	N.C.	173.1	-66.3	4396	-1684

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 8 of 12)

PAD#	SIGNAL[2,3,4]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
218	N.C.	173.1	-62.9	4396	-1597
219	N.C.	173.1	-59.5	4396	-1511
220	V_{CC}_3.3	173.1	-56.1	4396	-1424
221	V_{SS}	173.1	-52.7	4396	-1338
222	V_{CC}_2.9	173.1	-49.3	4396	-1252
223	V_{CC}_2.9	173.1	-45.9	4396	-1165
224	N.C.	173.1	-42.5	4396	-1079
225	STPCLK#	173.1	-39.1	4396	-992
226	N.C.	173.1	-35.7	4396	-906
227	V_{SS}	173.1	-32.3	4396	-820
228	V_{CC}_2.9	173.1	-28.9	4396	-733
229	V_{CC}_2.9	173.1	-25.5	4396	-647
230	N.C.	173.1	-22.1	4396	-560
231	N.C.	173.1	-18.7	4396	-474
232	BF	173.1	-15.3	4396	-388
233	V_{SS}	173.1	-11.9	4396	-301
234	V_{CC}_2.9	173.1	-8.5	4396	-215
235	V_{CC}_2.9	173.1	-5.1	4396	-128
236	V_{SS}	173.1	-1.7	4396	-42
237	N.C.	173.1	1.7	4396	44
238	N.C.	173.1	5.1	4396	131
239	PEN#	173.1	8.6	4396	217
240	INIT	173.1	12.0	4396	304
241	IGNNE#	173.1	15.4	4396	390
242	V_{SS}	173.1	18.8	4396	476
243	V_{CC}_2.9	173.1	22.2	4396	563
244	V_{CC}_2.9	173.1	25.6	4396	649
245	SMI#	173.1	29.0	4396	736
246	V_{CC}_2.9	173.1	32.4	4396	822
247	V_{CC}_2.9	173.1	35.8	4396	908
248	V_{SS}	173.1	39.2	4396	995

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 9 of 12)

PAD#	SIGNAL(2,3,4)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
249	INTR	173.1	42.6	4396	1081
250	R/S#	173.1	46.0	4396	1168
251	NMI	173.1	49.4	4396	1254
252	N.C.	173.1	52.8	4396	1340
253	V_{CC}_2.9	173.1	56.2	4396	1427
254	V_{CC}_2.9	173.1	59.6	4396	1513
255	V_{SS}	173.1	63.0	4396	1600
256	A21	173.1	66.4	4396	1686
257	A22	173.1	69.8	4396	1772
258	A23	173.1	73.2	4396	1859
259	V_{SS}	173.1	76.6	4396	1945
260	V_{CC}_3.3	173.1	80.0	4396	2032
261	V_{CC}_2.9	173.1	83.4	4396	2118
262	V_{CC}_2.9	173.1	86.8	4396	2204
263	V_{SS}	173.1	90.2	4396	2291
264	A24	173.1	93.6	4396	2377
265	A25	173.1	97.0	4396	2464
266	A26	173.1	100.4	4396	2550
267	A27	173.1	103.8	4396	2636
268	V_{SS}	173.1	107.2	4396	2723
269	V_{CC}_3.3	173.1	110.6	4396	2809
270	A28	173.1	114.0	4396	2896
271	A29	173.1	117.4	4396	2982
272	A30	173.1	120.8	4396	3068
273	A31	173.1	124.2	4396	3155
274	V_{SS}	173.1	127.6	4396	3241
275	V_{CC}_3.3	173.1	131.0	4396	3328
276	V_{CC}_2.9	173.1	134.4	4396	3414
277	V_{SS}	173.1	137.8	4396	3500
278	A3	173.1	141.2	4396	3587
279	V_{SS}	173.1	144.6	4396	3673

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 10 of 12)

PAD#	SIGNAL[2,3,4]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
280	V_{CC}_3.3	173.1	148.0	4396	3760
281	A4	173.1	151.4	4396	3846
282	A5	173.1	154.8	4396	3932
283	V_{SS}	173.1	158.2	4396	4019
284	V_{CC}_2.9	173.1	161.6	4396	4105
285	V_{SS}	173.1	165.0	4396	4192
286	V_{CC}_3.3	173.1	168.4	4396	4278
287	A6	173.1	171.8	4396	4364
288	A7	156.5	188.4	3975	4786
289	V_{SS}	153.1	188.4	3889	4786
290	V_{CC}_3.3	149.7	188.4	3802	4786
291	A8	146.3	188.4	3716	4786
292	V_{CC}_2.9	142.9	188.4	3629	4786
293	V_{CC}_2.9	139.5	188.4	3543	4786
294	V_{SS}	136.1	188.4	3457	4786
295	A9	132.7	188.4	3370	4786
296	V_{SS}	129.3	188.4	3284	4786
297	V_{CC}_3.3	125.9	188.4	3197	4786
298	A10	122.5	188.4	3111	4786
299	A11	119.1	188.4	3025	4786
300	V_{SS}	115.7	188.4	2938	4786
301	V_{CC}_3.3	112.3	188.4	2852	4786
302	A12	108.9	188.4	2765	4786
303	V_{CC}_2.9	105.5	188.4	2679	4786
304	V_{CC}_2.9	102.1	188.4	2593	4786
305	V_{SS}	98.7	188.4	2506	4786
306	A13	95.3	188.4	2420	4786
307	V_{SS}	91.9	188.4	2333	4786
308	V_{CC}_3.3	88.5	188.4	2247	4786
309	A14	85.1	188.4	2161	4786
310	V_{CC}_2.9	81.7	188.4	2074	4786

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 11 of 12)

PAD#	SIGNAL(2,3,4)	Pad Center(1)			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
311	V_{CC}_2.9	78.3	188.4	1988	4786
312	V_{SS}	74.9	188.4	1901	4786
313	A15	71.5	188.4	1815	4786
314	V_{SS}	68.1	188.4	1729	4786
315	V_{CC}_3.3	64.7	188.4	1642	4786
316	A16	61.3	188.4	1556	4786
317	A17	57.9	188.4	1469	4786
318	V_{SS}	54.5	188.4	1383	4786
319	V_{CC}_3.3	51.1	188.4	1297	4786
320	A18	47.6	188.4	1210	4786
321	V_{CC}_2.9	44.2	188.4	1124	4786
322	V_{CC}_2.9	40.8	188.4	1037	4786
323	V_{SS}	37.4	188.4	951	4786
324	A19	34.0	188.4	865	4786
325	V_{SS}	30.6	188.4	778	4786
326	V_{CC}_3.3	27.2	188.4	692	4786
327	A20	23.8	188.4	605	4786
328	V_{CC}_2.9	20.4	188.4	519	4786
329	V_{SS}	17.0	188.4	433	4786
330	V_{CC}_2.9	13.6	188.4	346	4786
331	V_{SS}	10.2	188.4	260	4786
332	RESET	6.8	188.4	173	4786
333	N.C.	-68.1	188.4	-1729	4786
334	CLK	-71.5	188.4	-1815	4786
335	SCYC	-74.9	188.4	-1902	4786
336	V_{SS}	-78.3	188.4	-1988	4786
337	V_{CC}_3.3	-81.7	188.4	-2074	4786
338	BE7#	-85.1	188.4	-2161	4786
339	BE6#	-88.5	188.4	-2247	4786
340	BE5#	-91.9	188.4	-2334	4786
341	BE4#	-95.3	188.4	-2420	4786

Table 1. Pentium® Processor Bond Pad Center Data (Sheet 12 of 12)

PAD#	SIGNAL[2,3,4]	Pad Center[1]			
		Mils (=0.001 inch)		Microns	
		X	Y	X	Y
342	V_{SS}	-98.7	188.4	-2506	4786
343	V_{CC}_3.3	-102.1	188.4	-2593	4786
344	BE3#	-105.5	188.4	-2679	4786
345	BE2#	-108.9	188.4	-2766	4786
346	BE1#	-112.3	188.4	-2852	4786
347	BE0#	-115.7	188.4	-2938	4786
348	A20M#	-119.1	188.4	-3025	4786
349	FLUSH#	-122.5	188.4	-3111	4786
350	BUSCHK#	-125.9	188.4	-3198	4786
351	W/R#	-129.3	188.4	-3284	4786
352	V_{SS}	-132.7	188.4	-3370	4786
353	V_{CC}_3.3	-136.1	188.4	-3457	4786
354	HIT#	-139.5	188.4	-3543	4786
355	HITM#	-142.9	188.4	-3630	4786
356	V_{SS}	-146.3	188.4	-3716	4786
357	V_{CC}_3.3	-149.7	188.4	-3802	4786
358	ADS#	-153.1	188.4	-3889	4786
359	EADS#	-156.5	188.4	-3975	4786

NOTES:

1. X-Y coordinates represent pad centers and are relative to center of die.
2. N.C. signifies no connect. These pads must not be connected.
3. The symbol “#” is used to denote active low signals.
4. Boundary Scan (JTAG) is implemented through the following pads:
   204 (TDO), 203 (TCK), 205 (TDI), 206 (TMS), 207 (TRST)

2.0 INTEL DIE PRODUCTS PROCESSING

2.1 Test Procedure

Intel has instituted full-speed functional testing at the die level for all SmartDie products. This level of testing is ordinarily performed only after assembly into a package. Each die is tested to the same electrical limits as the equivalent packaged unit.

2.2 Wafer Probe

Wafer probing is performed on every wafer produced in Intel Fabs. The process consists of specific electrical tests and device-specific functionality tests.

At the wafer level, built-in test structures are probed to verify that device electrical characteristics are in control and meet specifications. Measurements are made of transistor threshold voltages and current characteristics; poly and contact resistance; gate oxide and junction integrity; and specific parameters critical to the particular technology and device type. Wafer-to-wafer, across-the-wafer run-to-run variation and conformance to spec limits are checked.

The actual devices on each wafer are then probed for both functionality and performance to specifications. Additional reliability tests are also included in the probe steps.

2.3 Wafer Saw

Probed wafers are transferred to Intel's assembly sites to be sawed. The saw cuts totally through the wafer.

2.4 Die Inspection

Upon completion of the wafer saw, the die are moved to pick and place equipment that removes reject die. The remaining die are submitted to the same visual inspection as standard packaged product. The compliant die are then transferred to GEL-PAKs for shipment.

2.5 Packing Procedure

Intel will ship all Intel die products in GEL-PAKs. GEL-PAKs eliminate the die edge damage usually associated with die cavity plates or chip trays.

The backside of each die adheres to the gel membrane in the GEL-PAK, eliminating the risk of damage to the active die surface. A simple vacuum release mechanism allows for pick and place removal at the customer's site.

Only die from the same wafer lot are packaged together in a GEL-PAK, and all die are placed in the GEL-PAKs with a consistent orientation. The GEL-PAKs are then sealed and labeled with the following information:

- Intel SmartDie
- Intel Part Number
- Assembly Process Order / Spec
- ROM Code (if applicable)
- Customer Part Number (if applicable)
- Assembly Lot Traveler Number
- Finished Product Order Number
- Quantity
- Seal Date
- Country of Origin

NOTE:

GEL-PAKs require a Vacuum Release Station. Contact Vichem* Corporation for more information.

2.6 Inspection Steps

Multiple inspection steps are performed during the die fabrication and packing flow. These steps are performed according to the same specifications and criteria established for Intel's standard packaged product. Specific inspection steps include a wafer saw visual as well as a final die visual just before die are sealed in moisture barrier bags.

2.7 Storage Requirements

Intel die products will be shipped in GEL-PAKs and sealed in a moisture-barrier anti-static bag with a desiccant. No special storage procedures are required while the bag is still unopened. Once opened, the GEL-PAK should be stored in a dry, inert atmosphere to prevent corrosion of the bond pads.

2.8 Electro-Static Discharge (ESD)

Components are ESD sensitive.

3.0 SPECIFICATIONS

Specifications within this document are specific to a particular die revision and are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

3.1 Physical Specifications

Table 2 defines Pentium® Processor physical specifications.

Table 2. Pentium® Processor Physical Specifications

Die Revision:	C-0
Post-Saw Die Dimensions:	Mils: X = 361 ± 0.5, Y = 391 ± 0.5 See Figure 2 for X, Y orientation.
Die Thickness:	17 ± 1 mils
Minimum Pad Pitch:	85 microns (3.3 mils)
Pad Passivation Opening Size:	Mils: 2.6 x 5.6 (single pads) Microns: 67 x 141 (single pads)
Bond Pad Metallization: (outermost layer first)	16,800 Angstroms Aluminum (0.5% Copper), 1000 Angstroms Titanium
Pads per Die:	359
Die Backside Material: (outermost layer first)	1600 Angstroms Gold, 345 Angstroms Titanium
Passivation: (outermost layer first)	3.3 microns polyimide, 0.75 microns nitride
Intel Fabrication Process:	BiCMOS (min. feature size 0.4 microns)

3.2 DC Specifications

ABSOLUTE MAXIMUM RATINGS†

GEL-PAK Storage Temperature ..... 0°C to +70°C
Junction Temperature Under Bias ..... -65°C to +110°C
3 V Supply Voltage wrt. V_{SS} ..... -0.5 V to +4.6 V
2.9 V Supply Voltage wrt. V_{SS} ..... -0.5 V to +4.1 V
3 V Only Buffer DC Input Voltage..... -0.5 V to $V_{CC}3$+0.5 V not to exceed 4.6 V(1)
5 V Safe Buffer DC Input Voltage..... 0.5 V to +6.5 V(2)

OPERATING CONDITIONS†

$V_{CC}3$ (I/O Supply Voltage) .....3.3 V ± 165 mV
$V_{CC}2$ (Core Supply Voltage) .....2.9 V ± 165 mV
T_J (Junction Temperature Under Bias) ..... 0°C to + 105°C(3)
Substrate Bias..... Float (Self Biasing to V_{SS}), Alternative is to Drive V_{SS}
Core Operating Frequency..... 100, 120, 133 MHz (66, 60, 66 MHz Bus)

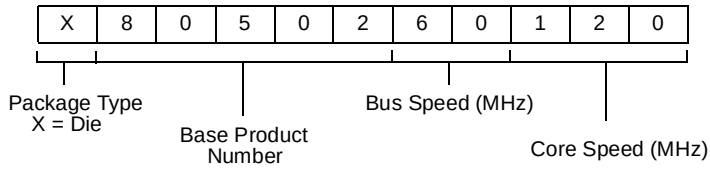
NOTES:

1. Applies to all Pentium® processors with voltage reduction technology inputs except CLK
2. Applies to CLK
3. Average die surface temperature

NOTICE: This datasheet contains preliminary information on new products in production. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

†***WARNING:*** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.0 DEVICE NOMENCLATURE



VALID COMBINATIONS:
X8050266100
X8050260120
X8050266133

5.0 REFERENCE INFORMATION

Document Title	Order #
Pentium® Processors at iComp® Index 1110\133, 1000\120, 815\100, 735\90, 610\75 with Voltage Reduction Technology datasheet	242557
Pentium® Processors and Related Products databook	241732
AP-479 Pentium® Processor Clock Design Application Note	241574
AP-480 Pentium® Processor Thermal Design Guidelines Application Note	241575

6.0 REVISION HISTORY

Revision	Date	Description
001	3/96	Initial Release