PRELIMINARY

Intel486™ DX CPU-CACHE CHIP SET

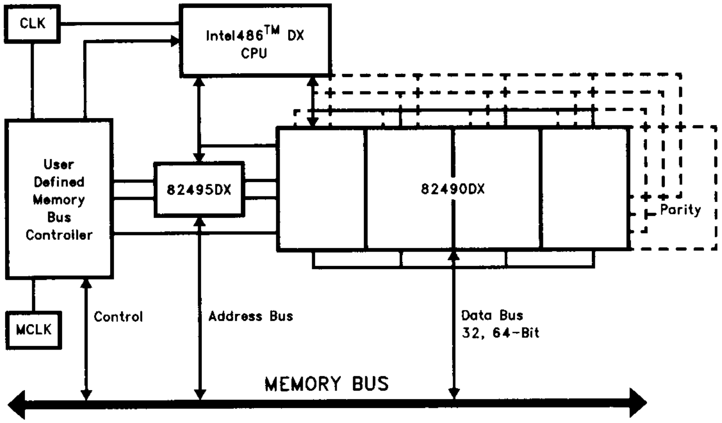
50 MHz Intel486™ DX Microprocessor, 82495DX Cache Controller, and 82490DX Dual Ported Intelligent Cache SRAM

- **50 MHz Intel486™ DX CPU**
  - RISC Integer Core with Frequent Instructions Executing in One Clock
  - 160 Mbyte/Sec Burst Bus
  - 41 Dhrystone MIPs
  - 11.5M Double Precision Whetstones/Sec.
  - On-Chip Cache and FPU
- **Highly Flexible**
  - Supports 128 Kbyte and 256 Kbyte Configurations
  - Complete MESI Protocol Support
  - 32- or 64-Bit Memory Bus Width
  - Synchronous, Asynchronous, and Strobed Memory Bus Protocols
  - Variable Cache Line Sizes and Sectoring
  - Cache Data Parity Option
- **High Performance Second Level Cache**
  - Two-Way Set Associative
  - Write-Back or Write Through Cache
  - Zero Wait State Cache Access
  - Concurrent CPU Bus, Memory Bus, and Internal Array Operation
- **Full Multiprocessing Support**
  - Implements MESI Write-Back Cache Protocol
  - Low Bus Utilization
  - Automatically Maintains 1st Level Cache Consistency
  - Supports Read-for-Ownership, Write-Allocation, and Cache-to-Cache Transfers

The 50 MHz Intel486 DX CPU-Cache Chip Set provides a high performance solution for servers and high-end desktop systems. This binary compatible solution has been optimized to provide 50 MHz, zero wait state performance. The CPU-Cache chip set combines the 50 MHz Intel486 Microprocessor with the 82495DX/82490DX cache subsystem. It delivers integer performance of 41 V1.1 Dhrystone MIPs and a SPEC integer rating of 27.9. The cache subsystem features the 82495DX Cache Controller and the 82490DX Dual Ported Data RAM. Dual ported buffers and registers of the 82490DX allow the 82495DX Cache Controller to concurrently handle CPU bus, memory bus, and internal cache operations for maximum performance.

The CPU-Cache Chip Set offers many features that are ideal for multiprocessor based systems. The Write-Back feature provides efficient memory bus utilization by reducing bus traffic through eliminating unnecessary writes to main memory. The CPU-Cache chip set also supports MESI protocol and monitors the memory bus to guarantee cache coherency.

The 50 MHz Intel486 DX CPU and 82495DX/82490DX Cache subsystem are produced on Intel's latest CHMOS V process which features submicron technology and triple layer metal.



241084-1

October 1992
Order Number: 241084-003

Intel486™ DX CPU-Cache Chip Set

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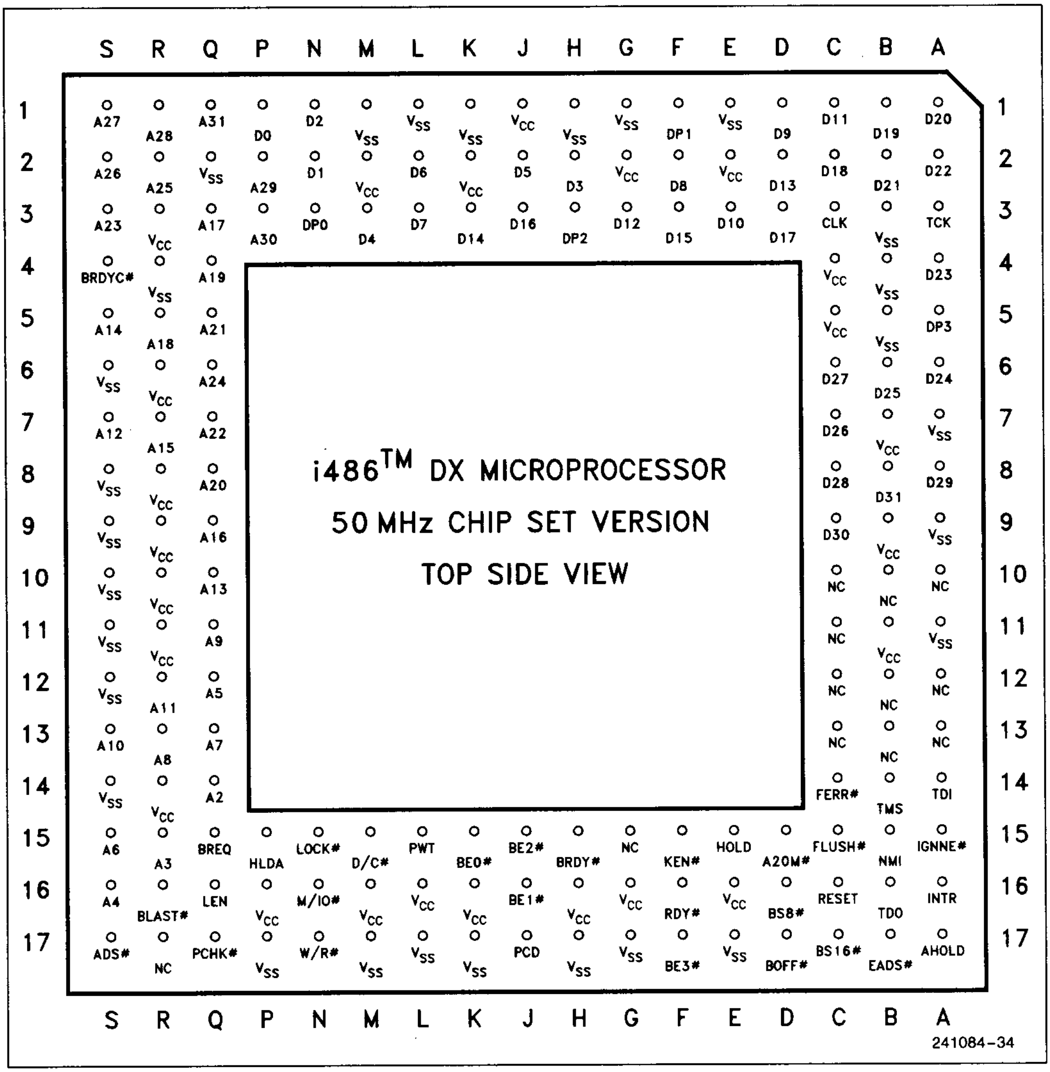
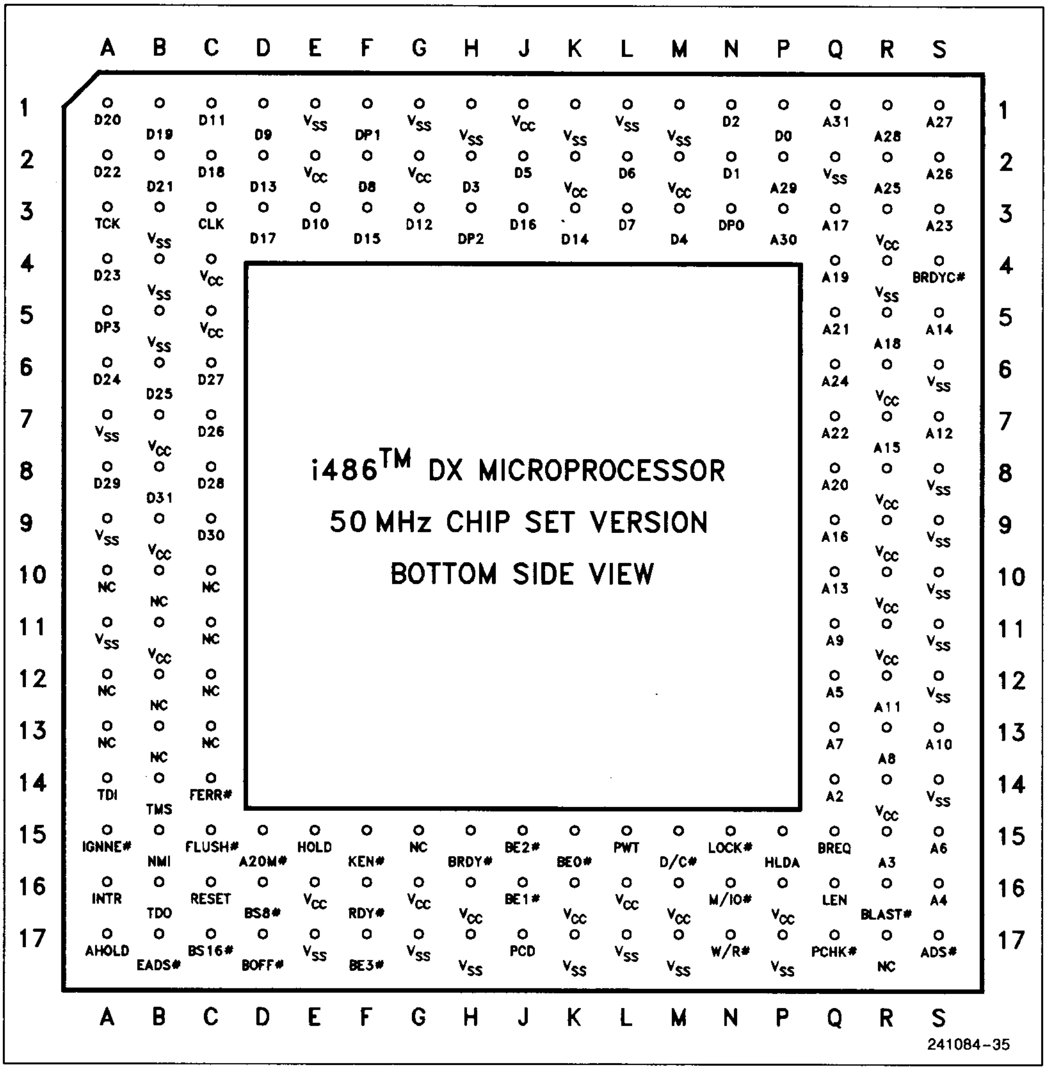
1.0 PINOUTS

1.1 i486™ DX CPU Pinouts


S R Q P N M L K J H G F E D C B A
1 A27 A28 A31 D0 D2 V_{SS} V_{SS} V_{SS} V_{CC} V_{SS} V_{SS} DP1 V_{SS} D9 D11 D19 D20 1
2 A26 A25 V_{SS} A29 D1 V_{CC} D6 V_{CC} D5 D3 V_{CC} D8 V_{CC} D13 D18 D21 D22 2
3 A23 V_{CC} A17 A30 DP0 D4 D7 D14 D16 DP2 D12 D15 D10 D17 CLK V_{SS} TCK 3
4 BRDYC# V_{SS} A19 V_{CC} V_{SS} D23 4
5 A14 A18 A21 V_{CC} V_{SS} DP3 5
6 V_{SS} V_{CC} A24 D27 D25 D24 6
7 A12 A15 A22 D26 V_{CC} V_{SS} 7
8 V_{SS} V_{CC} A20 D28 D31 D29 8
9 V_{SS} V_{CC} A16 D30 V_{CC} V_{SS} 9
10 V_{SS} V_{CC} A13 NC NC NC 10
11 V_{SS} V_{CC} A9 NC V_{CC} V_{SS} 11
12 V_{SS} A11 A5 NC NC NC 12
13 A10 A8 A7 NC NC NC 13
14 V_{SS} V_{CC} A2 FERR# TMS TDI 14
15 A6 A3 BREQ HLDA LOCK# D/C# PWT BE0# BE2# BRDY# NC KEN# HOLD A20M# FLUSH# NMI IGNNE# 15
16 A4 BLAST# LEN V_{CC} M/IO# V_{CC} V_{CC} V_{CC} BE1# V_{CC} V_{CC} RDY# V_{CC} BS8# RESET TDO INTR 16
17 ADS# NC PCHK# V_{SS} W/R# V_{SS} V_{SS} V_{SS} PCD V_{SS} V_{SS} BE3# V_{SS} BOFF# BS16# EADS# AHOLD 17
S R Q P N M L K J H G F E D C B A
i486™ DX MICROPROCESSOR
50 MHz CHIP SET VERSION
TOP SIDE VIEW
241084-34

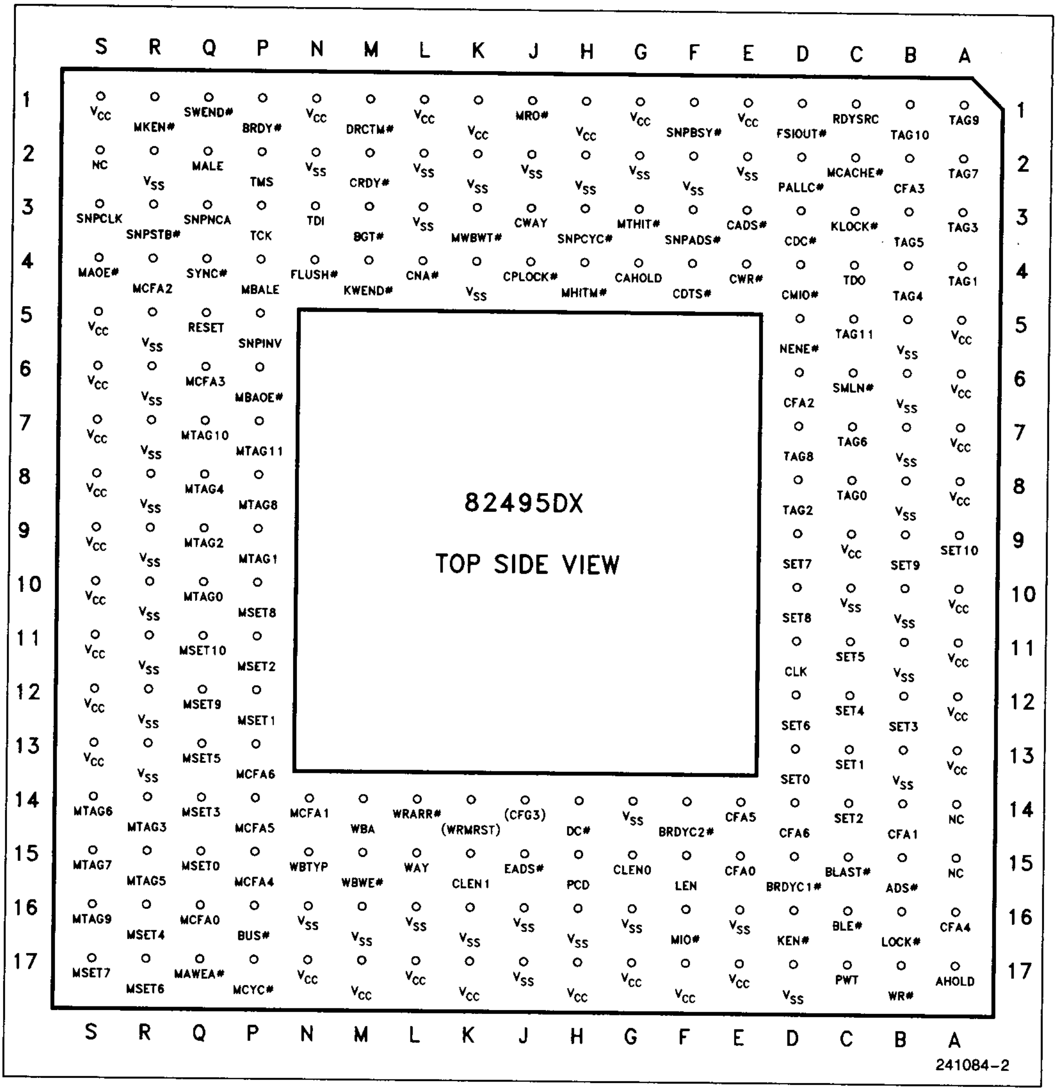
Intel486™ DX CPU Pinout (Top View)



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S
1	D20	D19	D11	D9	V_{SS}	DP1	V_{SS}	V_{SS}	V_{CC}	V_{SS}	V_{SS}	V_{SS}	D2	D0	A31	A28	A27
2	D22	D21	D18	D13	V_{CC}	D8	V_{CC}	D3	D5	V_{CC}	D6	V_{CC}	D1	A29	V_{SS}	A25	A26
3	TCK	V_{SS}	CLK	D17	D10	D15	D12	DP2	D16	D14	D7	D4	DP0	A30	A17	V_{CC}	A23
4	D23	V_{SS}	V_{CC}												A19	V_{SS}	BRDYC#
5	DP3	V_{SS}	V_{CC}												A21	A18	A14
6	D24	D25	D27												A24	V_{CC}	V_{SS}
7	V_{SS}	V_{CC}	D26												A22	A15	A12
8	D29	D31	D28												A20	V_{CC}	V_{SS}
9	V_{SS}	V_{CC}	D30												A16	V_{CC}	V_{SS}
10	NC	NC	NC												A13	V_{CC}	V_{SS}
11	V_{SS}	V_{CC}	NC												A9	V_{CC}	V_{SS}
12	NC	NC	NC												A5	A11	V_{SS}
13	NC	NC	NC												A7	A8	A10
14	TDI	TMS	FERR#												A2	V_{CC}	V_{SS}
15	IGNNE#	NMI	FLUSH#	A20M#	HOLD	KEN#	NC	BRDY#	BE2#	BE0#	PWT	D/C#	LOCK#	HLDA	BREQ	A3	A6
16	INTR	TDO	RESET	BS8#	V_{CC}	RDY#	V_{CC}	V_{CC}	BE1#	V_{CC}	V_{CC}	V_{CC}	M/IO#	V_{CC}	LEN	BLAST#	A4
17	AHOLD	EADS#	BS16#	BOFF#	V_{SS}	BE3#	V_{SS}	V_{SS}	PCD	V_{SS}	V_{SS}	V_{SS}	W/R#	V_{SS}	PCHK#	NC	ADS#

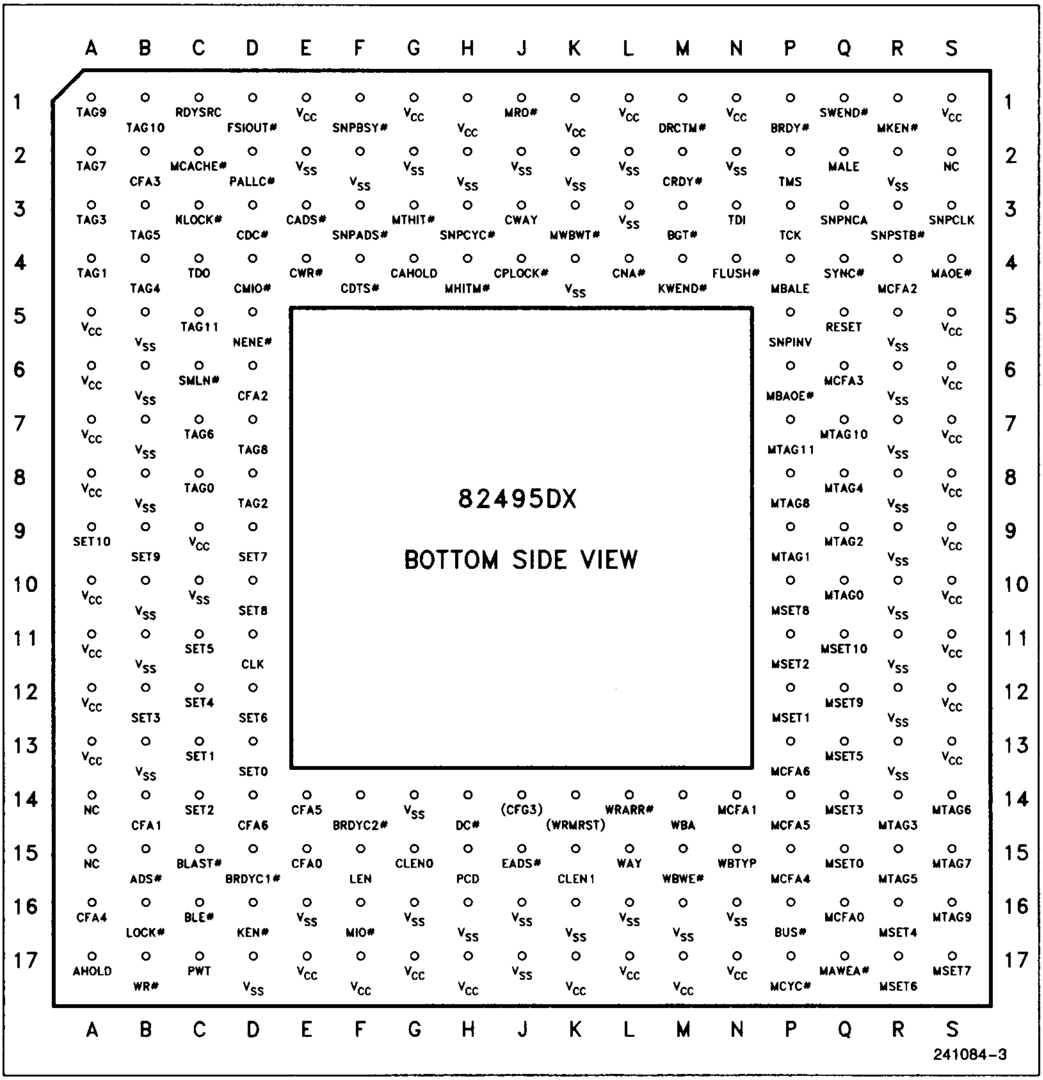
Intel486™ DX CPU Pinout (Bottom View)

1.2 82495DX Pinouts



82495DX Pinout (Top View)

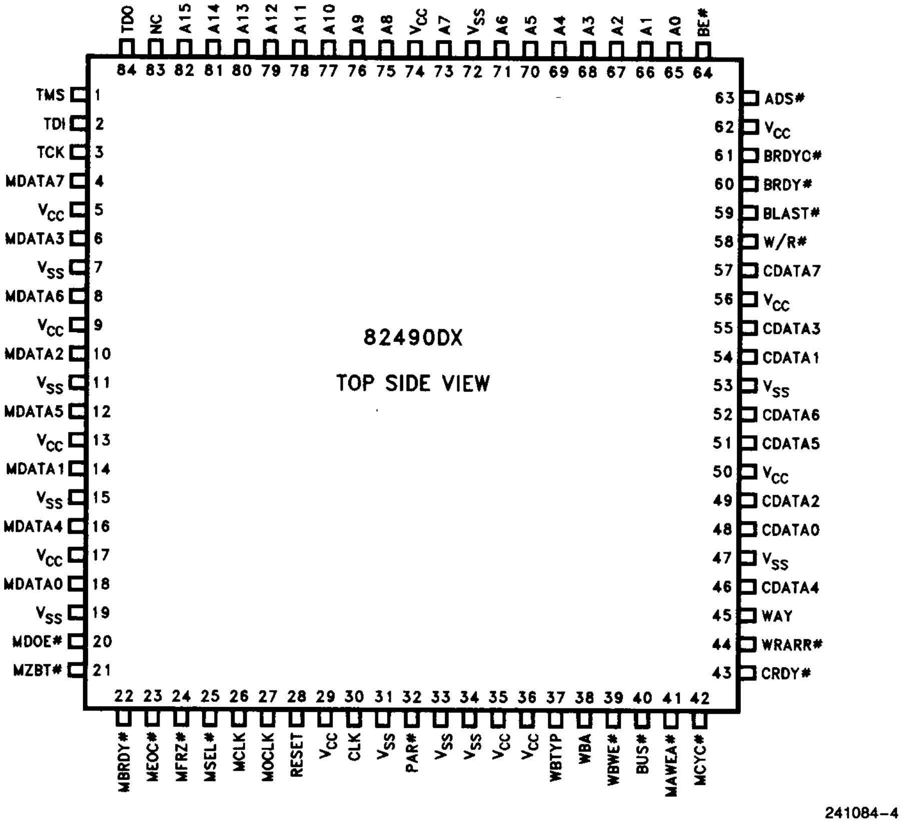
	S	R	Q	P	N	M	L	K	J	H	G	F	E	D	C	B	A
1	V_{CC}	MKEN#	SWEND#	BRDY#	V_{CC}	DRCTM#	V_{CC}	V_{CC}	MRO#	V_{CC}	V_{CC}	SNPBSY#	V_{CC}	FSIOUT#	RDYSRC	TAG10	TAG9
2	NC	V_{SS}	MALE	TMS	V_{SS}	CRDY#	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	PALLC#	MCACHE#	CFA3	TAG7
3	SNPCLK	SNPSTB#	SNPNCA	TCK	TDI	BGT#	V_{SS}	MWBWT#	CWAY	SNPCYC#	MTHIT#	SNPADS#	CADS#	CDC#	KLOCK#	TAG5	TAG3
4	MAOE#	MCFA2	SYNC#	MBALE	FLUSH#	KWEND#	CNA#	V_{SS}	CPLOCK#	MHITM#	CAHOLD	CDTS#	CWR#	CMIO#	TDO	TAG4	TAG1
5	V_{CC}	V_{SS}	RESET	SNPINV										NENE#	TAG11	V_{SS}	V_{CC}
6	V_{CC}	V_{SS}	MCFA3	MBAOE#										CFA2	SMLN#	V_{SS}	V_{CC}
7	V_{CC}	V_{SS}	MTAG10	MTAG11										TAG8	TAG6	V_{SS}	V_{CC}
8	V_{CC}	V_{SS}	MTAG4	MTAG8										TAG2	TAG0	V_{SS}	V_{CC}
9	V_{CC}	V_{SS}	MTAG2	MTAG1										SET7	V_{CC}	SET9	SET10
10	V_{CC}	V_{SS}	MTAG0	MSET8										SET8	V_{SS}	V_{SS}	V_{CC}
11	V_{CC}	V_{SS}	MSET10	MSET2										CLK	SET5	V_{SS}	V_{CC}
12	V_{CC}	V_{SS}	MSET9	MSET1										SET6	SET4	SET3	V_{CC}
13	V_{CC}	V_{SS}	MSET5	MCFA6										SET0	SET1	V_{SS}	V_{CC}
14	MTAG6	MTAG3	MSET3	MCFA5	MCFA1	WBA	WRARR#	(WRMRST)	(CFG3)	DC#	V_{SS}	BRDYC2#	CFA5	CFA6	SET2	CFA1	NC
15	MTAG7	MTAG5	MSET0	MCFA4	WBTYP	WBWE#	WAY	CLEN1	EADS#	PCD	CLEN0	LEN	CFA0	BRDYC1#	BLAST#	ADS#	NC
16	MTAG9	MSET4	MCFA0	BUS#	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	MIO#	V_{SS}	KEN#	BLE#	LOCK#	CFA4
17	MSET7	MSET6	MAWEA#	MCYC#	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{SS}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{SS}	PWT	WR#	AHOLD



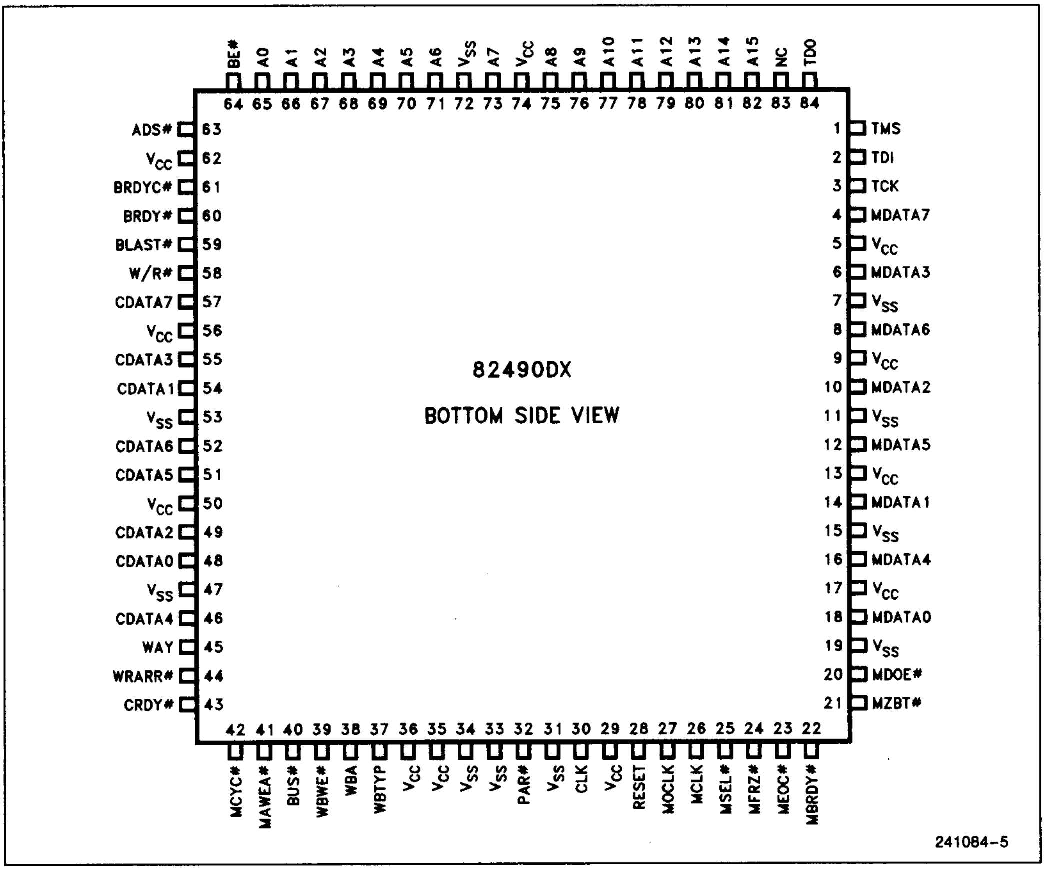
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S
1	TAG9	TAG10	RDYSRC	FSIOUT#	V_{CC}	SNPBSY#	V_{CC}	V_{CC}	MRO#	V_{CC}	V_{CC}	DRCTM#	V_{CC}	BRDY#	SWEND#	MKEN#	V_{CC}
2	TAG7	CFA3	MCACHE#	PALLC#	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	CRDY#	V_{SS}	TMS	MALE	V_{SS}	NC
3	TAG3	TAG5	KLOCK#	CDC#	CADS#	SNPADS#	MTHIT#	SNPCYC#	CWAY	MWBWT#	V_{SS}	BGT#	TDI	TCK	SNPNCA	SNPSTB#	SNPCLK
4	TAG1	TAG4	TDO	CMIO#	CWR#	CDTS#	CAHOLD	MHITM#	CPLOCK#	V_{SS}	CNA#	KWEND#	FLUSH#	MBALE	SYNC#	MCFA2	MAOE#
5	V_{CC}	V_{SS}	TAG11	NENE#										SNPINV	RESET	V_{SS}	V_{CC}
6	V_{CC}	V_{SS}	SMLN#	CFA2										MBAOE#	MCFA3	V_{SS}	V_{CC}
7	V_{CC}	V_{SS}	TAG6	TAG8										MTAG11	MTAG10	V_{SS}	V_{CC}
8	V_{CC}	V_{SS}	TAG0	TAG2										MTAG8	MTAG4	V_{SS}	V_{CC}
9	SET10	SET9	V_{CC}	SET7										MTAG1	MTAG2	V_{SS}	V_{CC}
10	V_{CC}	V_{SS}	V_{SS}	SET8										MSET8	MTAG0	V_{SS}	V_{CC}
11	V_{CC}	V_{SS}	SET5	CLK										MSET2	MSET10	V_{SS}	V_{CC}
12	V_{CC}	SET3	SET4	SET6										MSET1	MSET9	V_{SS}	V_{CC}
13	V_{CC}	V_{SS}	SET1	SET0										MCFA6	MSET5	V_{SS}	V_{CC}
14	NC	CFA1	SET2	CFA6	CFA5	BRDYC2#	V_{SS}	DC#	(CFG3)	(WRMRST)	WRARR#	WBA	MCFA1	MCFA5	MSET3	MTAG3	MTAG6
15	NC	ADS#	BLAST#	BRDYC1#	CFA0	LEN	CLEN0	PCD	EADS#	CLEN1	WAY	WBWE#	WBTYP	MCFA4	MSET0	MTAG5	MTAG7
16	CFA4	LOCK#	BLE#	KEN#	V_{SS}	MIO#	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	BUS#	MCFA0	MSET4	MTAG9
17	AHOLD	WR#	PWT	V_{SS}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{SS}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	MCYC#	MAWEA#	MSET6	MSET7

82495DX Pinout (Bottom View)

1.3 82490DX Pinouts


TDO 84
NC 83
A15 82
A14 81
A13 80
A12 79
A11 78
A10 77
A9 76
A8 75
V_{CC} 74
A7 73
V_{SS} 72
A6 71
A5 70
A4 69
A3 68
A2 67
A1 66
A0 65
BE# 64
TMS 1
TDI 2
TCK 3
MDATA7 4
V_{CC} 5
MDATA3 6
V_{SS} 7
MDATA6 8
V_{CC} 9
MDATA2 10
V_{SS} 11
MDATA5 12
V_{CC} 13
MDATA1 14
V_{SS} 15
MDATA4 16
V_{CC} 17
MDATA0 18
V_{SS} 19
MDOE# 20
MZBT# 21
63 ADS#
62 V_{CC}
61 BRDYC#
60 BRDY#
59 BLAST#
58 W/R#
57 CDATA7
56 V_{CC}
55 CDATA3
54 CDATA1
53 V_{SS}
52 CDATA6
51 CDATA5
50 V_{CC}
49 CDATA2
48 CDATA0
47 V_{SS}
46 CDATA4
45 WAY
44 WRARR#
43 CRDY#
82490DX
TOP SIDE VIEW
22 MBRDY#
23 MEOC#
24 MFRZ#
25 MSEL#
26 MCLK
27 MOCLK
28 RESET
29 V_{CC}
30 CLK
31 V_{SS}
32 PAR#
33 V_{SS}
34 V_{SS}
35 V_{CC}
36 V_{CC}
37 WBTYP
38 WBA
39 WBWE#
40 BUS#
41 MAWEA#
42 MCYC#
241084-4

82490DX Pinout (Top View)


82490DX
BOTTOM SIDE VIEW
BE# 64
A0 65
A1 66
A2 67
A3 68
A4 69
A5 70
A6 71
V_SS 72
A7 73
V_CC 74
A8 75
A9 76
A10 77
A11 78
A12 79
A13 80
A14 81
A15 82
NC 83
TDO 84
1 TMS
2 TDI
3 TCK
4 MDATA7
5 V_CC
6 MDATA3
7 V_SS
8 MDATA6
9 V_CC
10 MDATA2
11 V_SS
12 MDATA5
13 V_CC
14 MDATA1
15 V_SS
16 MDATA4
17 V_CC
18 MDATA0
19 V_SS
20 MDOE#
21 MZBT#
ADS# 63
V_CC 62
BRDYC# 61
BRDY# 60
BLAST# 59
W/R# 58
CDATA7 57
V_CC 56
CDATA3 55
CDATA1 54
V_SS 53
CDATA6 52
CDATA5 51
V_CC 50
CDATA2 49
CDATA0 48
V_SS 47
CDATA4 46
WAY 45
WRARR# 44
CRDY# 43
42 MCYC#
41 MAWEA#
40 BUS#
39 WBWE#
38 WBA
37 WBTYP
36 V_CC
35 V_CC
34 V_SS
33 V_SS
32 PAR#
31 V_SS
30 CLK
29 V_CC
28 RESET
27 MOCLK
26 MCLK
25 MSEL#
24 MFRZ#
23 MEOC#
22 MBRDY#
241084-5

82490DX Pinout (Bottom View)

1.4 Pin Cross Reference Tables

1.4.1 Intel486™ DX MICROPROCESSOR CHIP SET VERSION PIN TABLE

Pin	Location
A2	Q14
A3	R15
A4	S16
A5	Q12
A6	S15
A7	Q13
A8	R13
A9	Q11
A10	S13
A11	R12
A12	S7
A13	Q10
A14	S5
A15	R7
A16	Q9
A17	Q3
A18	R5
A19	Q4
A20	Q8
A21	Q5
A22	Q7
A23	S3
A24	Q6
A25	R2
A26	S2
A27	S1
A28	R1
A29	P2
A30	P3
A31	Q1
A20M#	D15
ADS#	S17
AHOLD	A17
BE0#	K15
NC	A10, A12, A13, B10, B12, B13, C10, C11, C12, C13, G15, R17

Pin	Location
BE1#	J16
BE2#	J15
BE3#	F17
BLAST#	R16
BOFF#	D17
BRDY#	H15
BRDYC#	S4
BREQ	Q15
BS16#	C17
BS8#	D16
CLK	C3
D/C#	M15
D0	P1
D1	N2
D2	N1
D3	H2
D4	M3
D5	J2
D6	L2
D7	L3
D8	F2
D9	D1
D10	E3
D11	C1
D12	G3
D13	D2
D14	K3
D15	F3
D16	J3
D17	D3
D18	C2
D19	B1
D20	A1
D21	B2
D22	A2
VCC	B11, B7, B9, C4, C5, E16, E2, G16, G2, H16, J1, K16, K2, L16, M16, M2, P16, R10, R11, R14, R3, R6, R8, R9

Pin	Location
D23	A4
D24	A6
D25	B6
D26	C7
D27	C6
D28	C8
D29	A8
D30	C9
D31	B8
DP0	N3
DP1	F1
DP2	H3
DP3	A5
EADS#	B17
FERR#	C14
FLUSH#	C15
HLDA	P15
HOLD	E15
IGGNE#	A15
INTR	A16
KEN#	F15
LEN	Q16
LOCK#	N15
M/IO#	N16
NMI	B15
PCD	J17
PCHK#	Q17
PWT	L15
RDY#	F16
RESET	C16
TCK	A3
TDI	A14
TDO	B16
TMS	B14
W/R#	N17
VSS	A11, A7, A9, B3, B4, B5, E1, E17, G1, G17, H1, H17, K1, K17, L1, L17, M1, M17, P17, Q2, R4, S10, S11, S12, S14, S6, S8, S9

1.4 Pin Cross Reference Tables (Continued)

1.4.2 82495DX QUICK REFERENCE BY NAME

Signal	Location
(CFG3)	J14
ADS#	B15
AHOLD	A17
BGT#(CLDRV)	M03
BLAST#	C15
BLE#	C16
BRDY#	P01
BRDYC1#	D15
BRDYC2#	F14
BUS#	P16
CADS#	E03
CAHOLD	G04
CD/C#	D03
CDTS#	F04
CFA0	E15
CFA1	B14
CFA2	D06
CFA3	B02
CFA4	A16
CFA5	E14
CFA6	D14
CLEN0	G15
CLEN1	K15
CLK	D11
CM/IO#	D04
CNA#(CFG0)	L04
CPLOCK# (PLOCKEN)	J04
CRDY#(SLFTST#)	M02
CWAY	J03
CW/R#	E04
D/C#	H14
DRCTM#	M01
EADS#	J15
FLUSH#	N04
FSIOUT#	D01
KEN#	D16
KLOCK#	C03

Signal	Location
KWEND#(CFG2)	M04
LEN	F15
LOCK#	B16
MALE(WWOR#)	Q02
MAOE#	S04
MAWEA#	Q17
MBALE(HIGHZ#)	P04
MBAOE#	P06
MCACHE#	C02
MCFA0	Q16
MCFA1	N14
MCFA2	R04
MCFA3	Q06
MCFA4	P15
MCFA5	P14
MCFA6	P13
MCYC#	P17
MHITM#	H04
M/IO#	F16
MKEN#	R01
MRO#	J01
MSET0	Q15
MSET1	P12
MSET2	P11
MSET3	Q14
MSET4	R16
MSET5	Q13
MSET6	R17
MSET7	S17
MSET8	P10
MSET9	Q12
MSET10	Q11
MTAG0	Q10
MTAG1	P09
MTAG2	Q09
MTAG3	R14
MTAG4	Q08
MTAG5	R15

Signal	Location
MTAG6	S14
MTAG7	S15
MTAG8	P08
MTAG9	S16
MTAG10	Q07
MTAG11	P07
MTHIT#	G03
MWB/WT#	K03
NENE#	D05
PALLC#	D02
PCD	H15
PWT	C17
RDYSRC	C01
RESET	Q05
SET0	D13
SET1	C13
SET2	C14
SET3	B12
SET4	C12
SET5	C11
SET6	D12
SET7	D09
SET8	D10
SET9	B09
SET10	A09
SMLN#	C06
SNPADS#	F03
SNPBSY#	F01
SNPCLK(SNPMD)	S03
SNPCYC#	H03
SNPINV	P05
SNPNCA	Q03
SNPSTB#	R03
SWEND#(CFG1)	Q01
SYNC#(MALDRV)	Q04
TAG0	C08
TAG1	A04
TAG2	D08

1.4.2 82495DX QUICK REFERENCE BY NAME (Continued)

Signal	Location
TAG3	A03
TAG4	B04
TAG5	B03
TAG6	C07
TAG7	A02
TAG8	D07
TAG9	A01
TAG10	B01
TAG11	C05
TCK	P03
TDI	N03
TDO	C04
TMS	P02
WAY	L15
WBA (SEC2#)	M14
WBTYP (LR0)	N15
WBWE# (LR1)	M15
(WRMRST)	K14
W/R#	B17
WRARR#	L14
NC	A14, A15, S02
V_{CC}	A05–A08, A10–A13, C09, E01, E17, F17, G01, G17, H01, H17, K01, K17, L01, L17, M17, N01, N17, S01, S05–S13
V_{SS}	B05–B08, B10–B11, B13, C10, D17, E02, E16, F02, G02, G14, G16, H02, H16, J02, J16, J17, K02, K04, K16, L02–L03, L16, M16, N02, N16, R02, R05–R10, R11–R13

1.4.3 82490DX QUICK REFERENCE BY NAME

Signal	Location
A0	65
A1	66
A2	67
A3	68
A4	69
A5	70
A6	71
A7	73
A8	75
A9	76
A10	77
A11	78
A12	79
A13	80
A14	81
A15	82
ADS#	63
BE#	64
BLAST#	59
BRDY#	60
BRDYC#	61
BUS#	40
CDATA0	48
CDATA1	54
CDATA2	49
CDATA3	55
CDATA4	46
CDATA5	51
CDATA6	52
CDATA7	57
CLK	30
CRDY#	43
MAWEA#	41
MBRDY# (MISTB)	22
MCLK (MSTBM)	26
MCYC#	42
MDATA0	18
MDATA1	14
MDATA2	10
MDATA3	6
MDATA4	16
MDATA5	12
MDATA6	8
MDATA7	4
MDOE#	20
MEOC#	23
MFRZ# (MDLDRV)	24
MOCLK (MOSTB)	27
MSEL# (MTR4/8#)	25
MZBT# (MX4/8#)	21
PAR#	32
RESET	28
TCK	3
TDI	2
TDO	84
TMS	1
WAY	45
WBA	38
WBTYP	37
WBWE#	39
W/R#	58
WRARR#	44
NC	83
V_{CC}	5, 9, 13, 17, 29, 35, 36, 50, 56, 62, 74
V_{SS}	7, 11, 15, 19, 31, 33, 34, 47, 53, 72

2.0 QUICK PIN REFERENCE

What follows is a brief pin description of the memory bus controller interface. Parentheses refer to signal function at reset. For detailed signal descriptions, please refer to the product hardware reference manuals, 50 MHz Intel486™ DX CPU-Cache Module HRM (Order #241091), 50 MHz Intel486™ DX CPU-Cache Chip Set HRM (Order #241172).

Symbol	Type	Name and Function
A20M#	I	**A20 MASK** is connected to the A20M# pin of the Intel486™ CPU. Please refer to the Intel486 DX CPU data sheet for details.
BGT# (CLDRV)	I	**BUS GUARANTEED TRANSFER (Cache LOW Drive)** is generated by the memory bus controller (MBC) to indicate that it is committed to completing a given memory bus cycle. Until BGT# is active, the CPU-cache chip set owns the cycle and may abort the cycle upon an intervening bus snoop. Once BGT# is asserted, the MBC owns the cycle, freeing the chip set for other operations. For proper operation, BGT# must meet the setup and hold time t_{30} and t_{31}. During RESET, BGT# becomes the CLDRV input. CLDRV determines the driving strength of the connections between the internal components. Please refer to the chip set layout specifications for information how to use CLDRV. For proper operation, CLDRV must meet the setup and hold times t_{10} and t_{31}.
BLE#	O I	The 82495DX asserts **Byte Latch Enable** to latch PCD, PWT, and BE0#–BE3# from the CPU. BLE is an output of the 82495DX and an input to the F377 latch.
BRDY#	I	**BURST READY** is generated by the memory bus controller (MBC) to strobe data into or out of the Intel486 CPU. The MBC BRDY# is internally connected to all of the CPU-cache chip set components. BRDY# provides the same function as described in the Intel486 DX CPU data sheet. The CPU-cache chip set also uses BRDY# for burst tracking to increment the CPU latch burst counter. For proper operation, BRDY# must meet the setup and hold times $t_{30,\ a,\ b}$ and $t_{31,\ a}$.
CADS#	O	**CACHE ADDRESS STROBE** is generated by the CPU-cache chip set to request that the memory bus controller execute a memory bus cycle. When active, CADS# indicates that the cache address, control and attribute signals are valid.
CAHOLD	O	**CACHE AHOLD** is generated by the CPU-cache chip set to track the CPU AHOLD signal during warm reset and LOCKed sequences. CAHOLD also provides information relevant to 82495DX built-in self-test (BIST).
CD/C#	O	**CACHE DATA/CONTROL** is driven by the CPU-cache chip set to indicate whether a requested memory bus cycle needs data or code. CD/C# is valid with CADS#.
CDTS#	O	**CACHE DATA STROBE** indicates to the memory bus controller that the data path is ready. In read cycles, CDTS# indicates that the memory bus controller can generate the first BRDY# in the next CLK. For write cycles, CDTS# indicates that data is available on the memory bus in the next cycle. CDTS# permits independent data and address strobes (CADS#, SNPADS#).
(CFG3)	I	**CACHE CONFIGURATION BITS** 0–3 are used to configure the CPU-cache chip set in any of four modes that determine chip set/Intel486 CPU line ratio, cache tag size (4K or 8K) and lines per sector. For proper operation, CFG3 must meet the setup and hold times t_{10} and t_{11}.
CLEN0-1	O	The **CYCLE LENGTH INDICATION** bits are memory bus controller interface signals which indicate the length of a CPU-initiated memory bus cycles. CLEN0 and CLEN1 are valid with CADS# and are used to indicate cycles of one, two or four transfers in length.
CLK	I	**CLOCK** provides fundamental timing for the CPU-cache chip set and all of its components. The chip set's clock inputs must be provided with minimal skew.
CM/IO#	O	**CACHE MEMORY/IO** is driven by the CPU-cache chip set to indicate whether a requested memory bus cycle is for memory or for I/O. CM/IO is valid with CADS#.

2.0 QUICK PIN REFERENCE (Continued)

Symbol	Type	Name and Function
CNA# (CFG0)	I	**NEXT ADDRESS REQUEST (Configuration Pin 0)** is driven by the memory bus controller to dynamically pipeline CPU-cache chip set cycles. If a cycle is pending and CNA# is given, a new CADS# is driven with the new cycle information. For proper operation, CNA# must meet the setup and hold times t_{30} and t_{31}. During the falling edge of RESET, CNA# functions as the chip set's CFG0 input. Cache Configuration Bits 0–3 are used to configure the CPU-cache chip set in any of four modes that determine chip set/Intel486 CPU line ratio, cache tag size (4K or 8K) and lines per sector. For proper operation, CFG0 must meet the setup and hold times t_{10} and t_{11}.
CPLOCK# (PLOCKEN)	O	**CACHE PLOCK# (Enable PLOCK Function)** tracks the CPU PLOCK# output but is only generated for write cycles. If write cycles are PLOCKed together, snooping is disabled between these cycles. PLOCK# can be disabled by setting CPLOCK LOW during reset. For proper operation, PLOCKEN must meet the setup and hold times t_{10} and t_{11}.
CRDY# (SLFTST#)	I	**CACHE MEMORY BUS READY (CPU-cache Self Test)** is generated by the memory bus controller to indicate to the CPU-cache chip set that a memory bus cycle has completed and make chip set resources available for the next cycle. For proper operation, CRDY# must meet the setup and hold times t_{28} and t_{29}. If SLFTST# is sampled LOW (active) during the falling edge of RESET while MBALE is HIGH (active), chip set self-test is invoked. For proper operation, SLFTST# must meet the setup and hold times t_{10} and t_{11}.
CWAY	O	**CACHE WAY** is driven by the CPU-cache chip set to indicate to the memory bus controller in which cache "way" the line will be loaded during line fills or during write-backs. CWAY is valid with CADS# and is used to facilitate external tracking tags.
CW/R#	O	**CACHE WRITE/READ** is driven by the CPU-cache chip set to indicate a requested memory bus cycle requires a read or a write. CW/R# is valid with CADS#.
DRCTM#	I	**MEMORY BUS DIRECT TO [M] STATE** allows the memory bus to inform the CPU-cache chip set of a request to skip the [E] state and move a line directly to the [M] state. DRCTM# allows the chip set to support read-for-ownership and cache-to-cache transfers (without main memory updates), and is sampled when SWEND# is asserted. For proper operation, DRCTM# must meet the setup and hold times t_{67} and t_{68} only during SWEND# assertion.
FERR#	O	**FLOATING-POINT ERROR** is connected to the Intel486 CPU FERR# pin. Please refer to the Intel486 DX CPU data sheet for details.
FLUSH#	I	**The 82495DX FLUSH#** input causes the CPU-Cache chip set to execute a write-back to main memory of any modified cache lines and then invalidate all cache tag locations within the 82495DX. For proper operation, FLUSH# must meet the setup and hold times t_{12} and t_{13}, or t_{14} if used asynchronously. Asserting the FLUSH# input on the 82495DX will not invalidate the cache tags in the CPU's cache directory. **The Intel486 DX CPU FLUSH#** input must be asserted to invalidate the tags of the CPU's on-chip cache. See the Intel486 DX CPU data book for details.
FSIOUT#	O	**FLUSH/SYNC/INITIALIZATION OUTPUT** indicates the start and end of Flush, Sync and Initialization operations.
HOLD/HLDA	I/O	**Intel486 CPU HOLD/HLDA** are connected to the Intel486 CPU and used during warm-reset to ensure that the Intel486 CPU has completed any current cycle before resetting. Please refer to the Intel486 DX CPU data sheet for details.

2.0 QUICK PIN REFERENCE (Continued)

Symbol	Type	Name and Function
IGNNE#	I	**IGNORE NUMERIC ERROR** is connected to the Intel486 CPU IGNNE# pin. Please refer to the Intel486 DX CPU data sheet for details.
INTR	I	**INTERRUPT REQUEST** is connected to the Intel486 CPU INTR pin. Please refer to the Intel486 DX CPU data sheet for details.
KLOCK#	O	**CACHE LOCK#** indicates to the memory bus controller that a request for atomic read-modify-write sequences is present. KLOCK# tracks the LOCK# signal of the Intel486 CPU.
KWEND# (CFG2)	I	**CACHEABILITY WINDOW END (Configuration Pin 2)** is generated by the memory bus controller to indicate to the CPU-cache chip set that the cacheability window (the period during which cacheability is determined) has expired. When KWEND# is asserted, the CPU-cache chip set latches the memory cacheability signal (MKEN#) and makes determinations based on the cacheability attribute (e.g. whether a line is cacheable, is read-only, requires a replacement, requires an allocation). The Memory Read-Only Signal (MRO#) is also sampled at this point. For proper operation, KWEND# must meet the setup and hold times t_{30} and t_{31}. During the falling edge of RESET, KWEND# becomes the CFG2 input. Cache Configuration Bits 0–3 are used to configure the CPU-cache chip set in any of four modes that determine chip set/Intel486 CPU line ratio, cache tag size (4K or 8K) and lines per sector. For proper operation, CFG2 must meet the setup and hold times t_{10} and t_{11}.
LMBE0–3#	O	**LATCHED MEMORY BYTE ENABLES** are latched versions of the Intel486 CPU byte enable outputs, BE0#–BE3#. They are driven through a SN74F377D latch. Please see the Intel486 CPU data sheet for details.
LPCD	O	**LATCHED PAGE CACHEABILITY ATTRIBUTE** is the latched Intel486 CPU PCD attribute to give the memory bus controller direct access. It is driven through a SN74F377D latch. PCD is used to determine cacheability and overrides MKEN#. Please refer to the Intel486 DX CPU data sheet for more information about PCD.
LPWT	O	**LATCHED PAGE WRITE-THROUGH ATTRIBUTE** is the latched CPU PWT attribute to give the memory bus controller direct access. It is driven through a SN74F377D latch. PWT is used to determine write-through and overrides MWB/WT#. Please refer to the Intel486 DX CPU data sheet for more information about PWT.
MALE (WWOR#)	I	**MEMORY BUS ADDRESS LATCH ENABLE (Weak Write Ordering)** is generated by the memory bus controller to control transparent address latches (resembling 373-series TTL logic) within the CPU-cache chip set. CADS# generates a new address at the input of the internal address latch. If MALE and MAOE# are both active, the address flows to the memory bus. When MALE becomes inactive (LOW), the address is latched. WWOR# configures the CPU-cache chip set into strong and weak write ordering modes. In strong ordering mode, the chip set writes data to memory in the order in which it was received from the Intel486 CPU. For proper operation, WWOR# must meet the setup and hold times t_{10} and t_{11}.
MAOE#	I	**MEMORY BUS ADDRESS OUTPUT ENABLE** is generated by the memory bus controller to control the output buffers of the CPU-cache chip set's memory bus address latches. If MAOE# is active (LOW), the chip set drives the memory bus address lines. If MAOE# is inactive (HIGH), the CPU-cache chip set's address inputs are driven to the hi-z state. Snoops are enabled only while MAOE# is inactive. MAOE# must meet setup times $t_{62a, b, c}$ and hold times $t_{63a, b, c}$ during snoop cycles for proper operation.

2.0 QUICK PIN REFERENCE (Continued)

Symbol	Type	Name and Function
MBALE (HIGHZ#)	I	**MEMORY BUS 82495DX SUB-LINE-ADDRESS LATCH ENABLE (HIGH-Impedance Output)** functions like MALE but only controls the CPU-cache chip set's sub-line addresses. MBALE is generated by the memory bus controller to control transparent address latches (resembling 373-series TTL logic) within the CPU-cache chip set. CADS# generates a new address at the internal address latch input. If MBALE and MBAOE# are both active, the sub-line address flows to the memory bus. If MBALE becomes inactive (LOW), the sub-line address is latched. A separate subline control input is provided because the CPU-cache chip set only provides the starting sub-line address. If active along with SLFTST#, HIGHZ# causes the chip set to float its MSET, MTAG, and MCFA address outputs. For proper operation, HIGHZ# must meet the setup and hold times t_{10} and t_{11}.
MBAOE#	I	**MEMORY BUS SUB-LINE ADDRESS OUTPUT ENABLE** functions like MAOE# but only controls the CPU-cache chip set's sub-line addresses. If MBAOE# is active (LOW), the chip set drives the sub-line portion of the address onto the memory bus. Otherwise, the CPU-cache chip set's sub-line address is driven to the hi-z state. MBAOE# is also sampled during snoop cycles. If MBAOE# is sampled inactive in conjunction with SNPSTB#, snoop write-back cycles begin at the sub-line address provided. If MBAOE# is sampled active with SNPSTB#, snoop write-back cycles begin at sub-line address 0. A separate sub-line control input is provided because the CPU-cache chip set only provides the starting sub-line address. MBAOE# must meet setup time $t_{62a, b, c}$ and hold times $t_{63a, b, c}$ during snoop cycles for proper operation.
MBRDY# MISTB	I	**MEMORY BUS READY (Memory Input Strobe)** is used to clock data into and out of the CPU-cache chip set. When active (LOW), MBRDY# indicates that the CPU-cache chip set will increment the burst counter and output or accept the next data. For proper operation, MBRDY# must meet the setup and hold time t_{38} and t_{39}. In strobed memory bus mode, MISTB is the CPU-cache chip set's input data strobe. On each edge of MISTB, the chip set latches data and increments the burst counter. MISTB must meet high and low times t_{85} and t_{86} for proper operation.
MCACHE#	O	**CACHE INTERNAL CACHEABILITY** is driven during read cycles to indicate whether the current cycle is potentially cacheable. During write operations, MCACHE# is only active for write-back cycles. MCACHE# is inactive during I/O, special and locked cycles.
MCLK (MSTBM)	I	**MEMORY BUS CLOCK (Memory Bus Strobed Mode)** is the memory bus clock input to the CPU-cache chip set while in clocked memory bus mode. Here, memory bus signals and data are sampled on the rising edge of MCLK. During clocked memory bus writes, data is driven off MCLK or MOCLK, depending on configuration. MCLK inputs to each 82490DX must be within proper skew specifications. If HIGH during reset, MSTBM indicates that the memory bus will be strobed. If MSTBM is toggling at reset, the memory bus will be clocked. For proper operation, MSTBM must meet the setup and hold times t_{10} and t_{11}.
MDATA7-0	I/O	The **MEMORY DATA PINS** are each of the CPU-cache chip set's 82490DX data I/O pins. Together with other 82490DX components, they form a 32-, 64-, or 128-bit wide memory bus. In clocked memory bus mode, MDATA is sampled with the rising edge of MCLK. New data is driven out on these pins with MEOC#, with the rising edge of MCLK or with MOCLK while MBRDY# is active. In strobed memory bus mode, MDATA is sampled on each MISTB edge. New data is driven with each MOSTB edge. In clocked mode MDATA must follow setup and hold times t_{42} and t_{43}, and in strobed mode, t_{100} and t_{101}.

2.0 QUICK PIN REFERENCE (Continued)

Symbol	Type	Name and Function
MDOE#	I	**MEMORY DATA OUTPUT ENABLE** controls the way the CPU-cache chip set drives data onto the memory bus. When MDOE# is inactive (HIGH), the MDATA pins are tristated. When MDOE# is active (LOW), the MDATA pins drive data. Because it is unrelated to CLK and MCLK, MDOE# functions the same during strobed and clocked memory bus operations.
MDPTY3-0	I/O	The **MEMORY DATA PARITY** pins provide the four bits needed to store parity information for the CPU-cache chip set's parity option. MDPTY bits are sampled and driven exactly as MDATA bits are. In clocked mode MDPTY3-0 must follow setup and hold times t_{42} and t_{43}, and in strobed mode, t_{100} and t_{101}.
MEOC#	I	**MEMORY END OF CYCLE** ends the current cycle. Because it is synchronous with the memory bus, MEOC# can end a memory bus cycle and begin a new cycle without waiting for Intel486 CPU CLK synchronization. MEOC# also causes data to be latched or driven and resets the memory burst counter. In clocked mode MEOC# must follow setup and hold times t_{38} and t_{39}, and in strobe mode, high and low times t_{87} and t_{88}.
MFRZ# (MDLDRV)	I	**MEMORY FREEZE (Memory Data Bus LOW Drive)** is used during write cycles that could cause allocation cycles. When MFRZ# is active (LOW), write data is latched within the CPU-cache chip set. The subsequent allocation will not overwrite latched data, thereby avoiding the memory write on the memory bus. Because memory is not updated, the allocated line must be cached in the [M] state. In clocked mode MFRZ# must follow setup and hold times t_{40} and t_{41}, and in strobed mode, t_{98} and t_{99}. During the falling edge of RESET, MDLDRV is sampled to indicate the memory data bus driver strength of the CPU-cache chip set, which offers normal and HIGH drive capability buffers. For proper operation, MDLDRV must meet the setup and hold times t_{10} and t_{11}.
MHITM#	O	**MEMORY BUS HIT TO MODIFIED LINE** is driven during snoop cycles to indicate whether snooping addresses hit a modified cache line within the CPU-cache chip set. When snoop hits to [M] occur, the chip set automatically schedules the write-back of modified lines. MHITM# is valid in the CLK following SNPCYC# and remains valid until the next SNPSTB#.
MKEN#	I	**MEMORY BUS CACHEABILITY** is driven by the memory bus controller to indicate to the CPU-cache chip set whether the current memory bus cycle is cacheable to both the CPU cache and chip set cache. MKEN# is sampled when KWEND# is asserted. For proper operation MKEN# must meet the setup and hold times t_{67} and t_{68} only during KWEND# assertion.
MOCLK (MOSTB)	I	**MEMORY OUTPUT CLOCK (Memory Output Strobe)** controls a transparent latch at the CPU-cache chip set's data outputs. MDATA hold time may be increased through a clock input skewed from MCLK. MOCLK must be within the proper skew specifications. In strobe bus mode, each edge of MOSTB outputs new data to the memory bus.
MRO#	I	**MEMORY BUS READ-ONLY** indicates to the CPU-cache chip set that an accessed line is READ-ONLY. READ-ONLY lines are non-cacheable in the first level cache and are cached within the chip set in the [S] state if MKEN# is sampled active during KWEND#. MRO# is sampled with KWEND# assertion. Subsequent writes to read-only lines are not updated but instead posted to the memory system. For proper operation, MRO# must meet the setup and hold times t_{67} and t_{68} only during KWEND# assertion.

2.0 QUICK PIN REFERENCE (Continued)

Symbol	Type	Name and Function
MSEL# (MTR4/8#)	I	**MEMORY SELECT (Memory Transfer)** is a chip select input which provides three functions. (1) MSEL# qualifies the MBRDY# CPU-cache chip set input. (2) If MSEL# is active with MEOC#, MZBT# is sampled for the next cycle. (3) If MSEL# is inactive, the CPU-cache chip set's memory burst counter is reset. In clocked mode MSEL# must follow setup and hold times t_{38} and t_{39}, and in strobed mode, t_{92}, t_{93} and t_{94}. MTR4/8# determines the number of transfers needed on the memory bus for each cache line. If MTR4/8# is HIGH, there are four transfers for each cache line; if LOW, there are eight transfers. For proper operation, MTR4/8# must meet the setup and hold times t_{10} and t_{11}.
MSET10–0 MTAG11–0 MCFA6–0	I/O	The **MEMORY ADDRESS** lines are used along with the CPU-cache chip set's byte enables to define the areas of memory or I/O to be accessed. They are driven during normal memory bus cycles and are inputs during snoop operations. The memory address outputs must meet setup times $t_{62a, b, c}$ and hold times $t_{63a, b, c}$ during snoop cycles for proper operation.
MTHIT#	0	**MEMORY BUS TAG HIT** is driven by the CPU-cache chip set during snoop cycles to indicate whether a snooping address hits an exclusive, shared or modified cache line. MTHIT# is valid in the CLK following SNPCYC# and remains valid until the next SNPSTB#.
MWB/WT#	I	**MEMORY BUS WRITE POLICY** allows the memory bus to dynamically indicate to the CPU-cache chip set whether the write policy is write-through or write-back. MWB/WT# is also asserted to change the tag state to shared when the line is detected in another cache. MWB/WT# is sampled when SWEND# becomes active. For proper operation, MWB/WT# must meet the setup and hold times t_{67} and t_{68} only during SWEND# assertion.
MZBT# (MX4/8#)	I	When sampled active with MSEL# or MEOC#, **MEMORY ZERO BASED TRANSFER (Memory I/O Bit)** indicates that burst location 0 of the memory bus cycle should be the starting sub-line address independent of the sub-line address requested by the Intel486 CPU. In clocked mode MZBT# must follow setup and hold times t_{40} and t_{41}, and in strobed mode, t_{96} and t_{97}. MX4/8# determines the number of I/O pins to be used for the memory bus. If MX4/8# is HIGH, four I/O pins are used. If MX4/8# is LOW, eight I/O pins are used. For proper operation, MX4/8# must meet the setup and hold times t_{10} and t_{11}.
NENE#	O	**NEXT NEAR** allows the memory bus controller (MBC) to take advantage of paged or static column DRAMs by indicating whether a requested memory address is "near" the previously generated address (i.e. within the same 2K DRAM page). NENE# is valid with CADS#.
NMI	I	**NON-MASKABLE INTERRUPT** is connected to the Intel486 CPU NMI pin. Please refer to the Intel486 DX CPU data sheet for details.
PALLC#	O	**POTENTIAL ALLOCATE** indicates to the memory bus controller that the current write cycle could allocate a cache line. PALLC# is active for miss cycles in which LOCK#, PCD and PWT are inactive.
(PAR#)	I	**PARITY CONFIGURATION,** when sampled active during RESET, causes the 82490DX to be configured solely as a parity device. PAR# must meet setup and hold times t_{10} and t_{11} for proper operation.
PCHK#	O	**PARITY CHECK** is the Intel486 CPU'S parity check output. Please refer to the Intel486 DX CPU data sheet for details.
RDYSRC	O	**READY SOURCE** indicates the source of Intel486 CPU BRDY generation. If RDYSRC is HIGH, the memory bus controller must generate BRDY#; if RDYSRC is LOW, the CPU-cache chip set generates BRDY#.

2.0 QUICK PIN REFERENCE (Continued)

Symbol	Type	Name and Function
RESET	I	**RESET** is asynchronous to the CPU-cache chip set. RESET initiates chip set execution at a known state. The falling edge samples the state of the configuration pins. For proper operation, RESET must meet the setup and hold times t_7 and t_8 or t_9 if used asynchronously. The following CPU-cache pins are sampled during the falling edge of RESET: CNA# (CFG0). CFG0 line of the configuration inputs. SWEND# (CFG1). CFG1 line of the configuration inputs. KWEND# (CFG2). CFG2 line of the configuration inputs. (CFG3). Used to configure CPU-cache chip set cache parameters—define lines per sector, line ration, number of tags. CRDY# (SLFTST#). Invokes Built in Self Test (BIST) if zero. CPLOCK# (PLOCKEN). Permits handling of PLOCK# cycles—active HIGH. BGT# (C8LDRV). Indicates driving strength of internal CPU-cache chip set interface. SYNC# (MALDRV). Indicates the CPU-cache chip set's memory address bus driving strength. SNPCLK (SNPMD). Indicates whether the snoop mode is synchronous clocked, or strobed. MALE (WWOR#). Enforces strong or weak write ordering consistency. MBALE (HIGHZ#). Tristates CPU-cache chip set outputs if active with SLFTST#. MZBT# (MX4/8#). Determines whether each 82490DX uses 4 or eight I/O pins on the memory bus. MSEL# (MTR4/8#). Determines the number of memory bus transfers needed to fill each cache line—four transfers if HIGH, eight if LOW. MCLK (MSTBM). Indicates the memory bus configuration—strobed if inactive (HIGH), clocked if toggling. MFRZ# (MDLDRV). Indicates the CPU-cache chip set's memory data bus driving strength. (PAR#). Configures the 82490DX as a parity device.
SMLN#	O	**SAME CACHE LINE** indicates to the memory bus controller that the current cycle accesses the same CPU-cache chip set line as the previous memory (not I/O) cycle. SMLN# is valid with CADS# and can be used to selectively activate SNPSTB# for other caches. For example, SMLN# can prevent consecutive snoops to the same line.
SNPADS#	O	**CACHE SNOOP ADDRESS STROBE** functions exactly like CADS# but is generated only on snoop write-back cycles. Because snoop write-back cycles must be immediately serviced on the memory bus, the separate address strobe eases memory bus controller (MBC) implementation. When SNPADS# is active, the MBC aborts all pending cycles (i.e. those for which BGT# has not been issued; after BGT#, snoops are not acknowledged). The CPU-cache chip set may re-issue cycles following snoop completion.
SNPBSY#	O	When active (LOW), **SNOOP BUSY** indicates that the CPU-cache chip set is not ready to accept another snoop cycle. SNPBSY# is activated when a snoop hits a modified line or when back-invalidation is needed for a snoop in progress. CPU-cache does not perform lookups until SNPBSY# is deactivated.
SNPCLK (SNPMD)	I	**SNOOP CLOCK (Snoop Mode)** provides the CPU-cache chip set with a snoop clock so the MBC can snoop at its own rate. During clocked mode, SNPSTB#, SNPINV, SNPNCA, MBAOE#, MAOE# and all address lines are sampled by SNPCLK. When HIGH during reset, SNPMD indicates strobed snooping mode. If LOW during reset, SNPMD indicates synchronous snooping mode. In clocked snooping mode, SNPCLK is connected to the snoop clock source.

2.0 QUICK PIN REFERENCE (Continued)

Symbol	Type	Name and Function
SYPCYC#	O	**SNOOP CYCLE** indicates when a snoop look-up is occurring within the CPU-cache chip set's tag RAM. MHITM# and MTHIT# are valid during the clock following SNPCYC#.
SNPINV	I	**SNOOP INVALIDATION** is sampled with SNPSTB# and indicates the state of a cache line following a snoop hit cycle. If active, SNPSTB# forces the line to become invalid. SNPINV must meet setup times $t_{62a, b, c}$ and hold times $t_{63a, b, c}$ during snoop cycles for proper operation.
SNPNCA	I	**SNOOP NON-CACHING DEVICE ACCESS** is sampled with SNPSTB# and indicates to the CPU-cache chip set whether a bus master is a non-caching device (e.g. a DMA controller). SNPNCA helps prevent the chip set from unnecessarily changing cache line states from exclusive to shared. SNPNCA must meet setup times $t_{62a, b, c}$ and hold times $t_{63a, b, c}$ during snoop cycles for proper operation.
SNPSTB#	I	**SNOOP STROBE** causes the snoop address and parameters to be latched and initiates a snoop. The CPU-cache chip set supports clocked, strobed and synchronous latching modes. In clocked mode, address and attribute signals are latched when SNPSTB# becomes active with the rising edge of SNPCLK. In strobed mode, addresses and attributes are latched at the falling edge of SNPSTB#. In synchronous mode, address and attribute signals are latched when SNPSTB# becomes active with the rising edge of CLK. SNPSTB# must meet setup times t_{62a} and t_{62c} and hold times t_{63a} and t_{63c} for proper operation.
SWEND# (CFG1)	I	**SNOOP WINDOW END (Configuration Pin 1)** is generated to the memory bus controller to indicate to the CPU-cache chip set that the snoop window has expired. When SWEND# is asserted, the chip set latches the Write Policy (MWB/WT#) and Direct to Memory Transfer (DRCTM#) attributes. By the end of the window, all devices have snooped the bus master address and generated bus address caching attributes. When a cycle begins, the chip set prevents snooping until it receives SWEND#. The chip set can then update its tag RAM. For proper operation, SWEND# must meet the setup and hold times t_{30} and t_{31}. During the falling edge of RESET, SWEND# becomes the CFG1 input. **Cache Configuration Bits** 0–3 are used to configure the CPU-cache chip set in any of four modes that determine chip set/Intel486 CPU line ratio, cache tag size (4K or 8K) and lines per sector. For proper operation, CFG1 must meet the setup and hold times t_{10} and t_{11}.
SYNC# (MALDRV)	I	**SYNCHRONIZE CPU-CACHE (Memory Address Bus LOW Drive)** synchronizes the CPU-cache chip set tag array with main memory. All cache lines modified by the CPU-cache chip set are written back to main memory. SYNC# differs from FLUSH# in that it does not invalidate the CPU-cache chip set or the Intel486 CPU tag array. All E, I and S state lines remain in the E, I and S states while all modified cache lines (M state) become non-modified (E state). For proper operation, SYNC# must meet the setup and hold times t_{12} and t_{13} or t_{14} if used asynchronously. During the falling edge of RESET, MALDRV is sampled to determine the CPU-cache chip set's memory address bus driving strength. For proper operation, MALDRV must meet the setup and hold times t_{10} and t_{11}.
TCK	I	**TESTABILITY CLOCK** is the boundary scan testability clock for all CPU-cache chip set components.
TDI	I	**TESTABILITY SERIAL INPUT** is the boundary scan serial test data input for all CPU-cache chip set components. For proper operation, TDI must meet the setup and hold times t_{126} and t_{127}.
TDO	O	**TESTABILITY SERIAL OUTPUT** is the boundary scan serial test data output for all CPU-cache chip set components.
TMS	I	**TESTABILITY CONTROL** is the boundary scan test mode select input for all CPU-cache chip set components. For proper operation, TMS must meet the setup and hold times t_{126} and t_{127}.
WRMRST	I	**WARM-RESET** is an input to the 82495DX that indicates that the Intel486 CPU is being reset without the rest of the cache chip set. WRMRST must be connected to the RESET pin of the Intel486 CPU.

2.1 Quick Pin Reference (Optimized Interface)

The table below lists and describes the pins that comprise the optimized interface. This is the interface between the i486 CPU, 82495DX Cache Controller, and the 82490DX SRAM that has been refined and optimized to allow zero wait state operation at 50 MHz.

Intel provides a recommended Intel486 DX CPU-Cache chip set layout for each possible cache size. Intel strongly recommends that this layout be used. The information provided in the table below is helpful in identifying the pins that make up the optimized interface to facilitate interface layout and debugging.

Symbol	Type		Name and Function
A2–A31 A0–A15	O I	i486 490	The i486 CPU **Address** Outputs A2–A31 are connected to the 82495DX address inputs of SET, TAG and CFA. The lower Bits of the CPU Address are also connected to the 82490DX address inputs A0–A15. The actual connectons of the CPU Address lines to the 82490DX and 82495DX are determined by the cache configuration used.
ADS#	O I I	i486 495 490	The i486 CPU **Address Strobe** output is connected to the 82495DX and 42490DX ADS# inputs and indicates the start of a CPU cycle. Please refer to the i486 DX CPU data sheet for details.
AHOLD	I O	i486 495	**Address Hold** is driven by the 82495DX to the i486 CPU AHOLD input during back-invalidation cycles. Please refer to the i486 DX CPU data sheet for details.
BE0#–BE3# BE#	O I I	i486 latch 490	The i486 CPU **Byte Enable** outputs are driven to an external latch controlled by the 82495DX. Each byte enable also goes to an 82490DX to control partial write cycles. Please refer to the i486 DX CPU data sheet for details.
BLAST#	N/C O I	i486 495 490	The 82495 DX **Burst Last** output is driven to indicate the end of a cycle. It is connected to the 82490DX BLAST# input.
BOFF#	I	i486	The BOFF# input is sampled by the i486 CPU during RESET to enable Chip Set Mode. BOFF# may not be used in any other way.
BRDYC#	I I	i486 490	**Burst Ready Cache** is a second BRDY# input to the i486 CPU from the cache used for cache hit cycles. It is connected to the 82495DX BRDYC1# output. BRDYC# is an input to the 82490DX that is connected to the 82495DX BRDYC2# output and is used for tracking these hit cycles.
BRDYC1#	O	495	**Burst Ready Cache 1** is output by the 82495DX to the i486 CPU BRDYC# input during cache hit and posted cycles.
BRDYC2#	O	495	**Burst Ready Cache 2** is output by the 82495DX to the 82490DX BRDYC# input during cache hit and posted cycles.
BS16#	I	i486	The BS16# input is sampled by the i486 CPU during RESET to enable Chip Set Mode. BS16# may not be used in any other way.
BS8#	I	i486	The BS8# input is sampled by the i486 CPU during RESET to enable Chip Set Mode. BS8# may not be used in any other way.
BUS#	O I	495 490	The **Bus/Array Select** output of the 82495DX multiplexes either the memory bus path or array path to the CPU bus of the 82490DX.
CDATA0-7	I/O	490	**Cache Data** I/O pins are the 8 bits comprising the I/O data bus interface between each 82490DX and the i486 CPU data bus.
CFA0–CFA6	I/O	495	**Cache Function and Address** pins of the 82495DX are multiplexed to the i486 CPU address according to the 82495DX configuration.
D/C#	O I	i486 495	The **Data/Code** output of the i486 CPU is used by the 82495DX to decode special cycles. Please refer to the i486 DX CPU data sheet for details.
D0–D31	I/O	i486	The i486 CPU **Data Bus** pins are distributed to each 82490DX. Please refer to the i486 DX CPU data sheet for details.

2.1 Quick Pin Reference (Optimized Interface) (Continued)

Symbol	Type		Name and Function
DP0–DP3	I/O	i486	The i486 CPU **Data Parity Bus** pins are distributed to each 82490DX. Please refer to the i486 DX CPU data sheet for details.
EADS#	I O	i486 495	The i486 CPU **External Invalidation Address Strobe** is driven by the 82495DX during back-invalidation cycles to maintain inclusion. Please refer to the i486 DX CPU data sheet for details.
KEN#	I O	i486 495	The i486 CPU **Cache Enable** input is driven by the 82495DX during cacheable cycles. Please refer to the i486 DX CPU data sheet for details.
LEN	O I	i486 495	The i486 CPU drives the **Length** pin active to indicate a cycle of 2 transfers. With LEN inactive, the cycle length is 1 transfer. If a cycle is cacheable, LEN is undefined and the cycle length is 4 transfers. LEN is only defined for read cycles.
LOCK#	O I	i486 495	The **Cycle Lock** pin of the i486 CPU is driven to the 82495DX which in turn drives the memory bus KLOCK# output. Please refer to the i486 DX CPU data sheet for details.
M/IO#	O I	i486 495	The i486 CPU **Memory/IO** pin is used by the 82495DX to decode memory and I/O cycles. Please refer to the i486 DX CPU data sheet for details.
MAWEA#	O I	495 490	The 82495DX asserts **Memory Bus Array Write Enable or Allocation** signal to the 82490DX to indicate that the data in the memory buffers should be written to the array, or that an allocation should occur.
MCYC#	O I	495 490	The 82495DX asserts **Memory Bus Cycle** to the 82490DX to indicate that the current cycle will use the memory buffers.
PCD	O I I	i486 495 latch	The i486 CPU **Page Cacheability Disable** attribute bit is driven on PCD to indicate cacheability. PCD active causes the 82495DX to make the current cycle non-cacheable. Please refer to the i486 DX CPU data sheet for details.
PWT	O I I	i486 495 latch	The i486 CPU **Page Write-Through** attribute is driven on PWT to indicate write-through. PWT active causes the 82495DX to make the current cycle write-through. Please refer to the i486 DX CPU data sheet for details.
RDY#	I	i486	The RDY# pin must remain unused and unconnected.
SET0–10	I/O	495	The 82495DX **Set Address** pins are connected to 11 bits of the CPU address. The actual connection is configuration dependent.
TAG0–11	I/O	495	The 82495DX **Tag Address** pins are connected to 12 bits of the CPU address. The actual connection is configuration dependent.
W/R#	O I I	i486 495 490	The i486 CPU **Write/Read** pin is driven to the 82495DX and 82490DX to indicate a read or write cycle. Please refer to the i486 DX CPU data sheet for details.
WAY	O I	495 490	The 82495DX **Way** indication is used by the 82490DX to properly load and store buffers as well as update the MRU bit.
WBA (SEC2#)	O I	495 490	The **Write Back Buffer Address (2 lines per sector)** pin is driven by the 82495DX to indicate which line is loaded by the 82490DX. The 82495DX drives SEC2# during RESET to the 82490DX to pass along lines/sector information. If active, SEC2# indicates 2 lines per sector.
WBTYP (LR0)	O I	495 490	The 82495DX **Write Back Cycle Type (Line Ratio 0)** pin is driven to the 82490DX to indicate a write-back or snoop write-back cycle. LR0 is driven by the 82495DX to the 82490DX at RESET to pass along line ratio information.
WBWE# (LR1)	O I	495 490	The 82495DX **Write-Back Buffer Write Enable (Line Ratio 1)** pin is used in conjunction with the WBA pin to load the write-back buffers. LR1 is driven by the 82495DX to the 82490DX at RESET to pass along line ratio information.
WRARR#	O I	495 490	The 82495DX **Write to 82490DX Array** signal controls the writing of data into the 82490DX array and updating of the MRU bit.

The following pins have internal pull-ups and will be disabled during the tri-state output testing sequence:

82495DX:

ADS#
BGT#
CNA#
CPLOCK#
DRCTM#
FLUSH#
KWEND#
MRO#
SNPCLK
SNPSTB#
SWEND#
SYNC#
TCK
TDI
TMS

82490DX:

ADS#
BOFF#
MCLK
MFRZ#
MOCLK
MZBT#
PAR#
TMS
TDI
TCK

The following signals are glitch-free and are always valid following RESET:

CADS#
CDTS#
SNPADS#
SNPCYC#
KLOCK#

Table 2.1. Pin State During RESET

Pin Name	Pin State During RESET
CADS#, CDTS#, SNPADS#	High
CW/R#, CD/C#, CM/IO#, MCACHE#, CLEN0, CLEN1	Undefined
RDYSRC, PALLC#, CWAY	Undefined
NENE#, SMLN#	Undefined
KLOCK#	High
MSET, MTAG, MCFA	Undefined
CAHOLD	(Note 1)
MHITM#, MTHIT#	High
SNPCYC# FSIOUT#, SNPBSY#	High Low
TDO	(Note 2)

NOTES:
1. The state of CAHOLD depends on whether selt-test is selected.
2. The state of TDO is determined by boundary scan which is independent of all other signals including RESET.

Table 2.2. CPU-Cache Chip Set Output Pins

Name	Active
TDO	—
FERR#	Low
LPCD	High
LPWT	High
CADS#	Low
SNPADS#	Low
CDTS#	Low
CW/R#	Low
CD/C#	Low
CM/IO#	Low
MCACHE#	Low
KLOCK#	Low
SNPCYC#	Low
PCHK#	Low
RDYSRC	High
CLEN0	—
CLEN1	—
CWAY	—
NENE#	Low
SMLN#	Low
PALLC#	Low
CAHOLD	High
FISOUT#	Low
SNPBSY#	Low
MHITM#	Low
MTHIT#	Low
LMBE0–3#	Low
HLDA	High

Table 2.3. CPU-Cache Chip Set Input/Output Pins

Name	Active	Synch/Asynch	When Floated
MSET, MTAG, MCFA	—	(Note 2)	MAOE# = High
MDATA	—	(Note 2)	MDOE# = High, Reset
MDPTY	—	(Note 2)	MDOE# High, Reset
CPLOCK# (PLOCKEN)	—		

Table 2.4. CPU-Cache Chip Set Input Pins

Name	Active	Synch/Asynch
CLK	—	—
RESET	High	Asynchronous
CFG3	—	—
MCLK	—	—
TCK	—	—
TDI	—	(Note 3)
TMS	—	(Note 3)
HOLD	High	Synchronous
NMI	High	Asynchronous
INTR	High	Asynchronous
IGNNE#	Low	Asynchronous
A20M#	Low	Asynchronous
BRDY#	Low	Synchronous
CNA# (CFG0)	Low	Synchronous
MKEN#	Low	(Note 1)
MWB/WT#	—	(Note 1)
DRCTM#	Low	(Note 1)
MRO#	Low	(Note 1)
BGT# (CLDRV)	Low	Synchronous
KWEND# (CFG2)	Low	Synchronous
SWEND# (CFG1)	Low	Synchronous
CRDY# (SLFTST#)	Low	Synchronous
FLUSH#	Low	Asynchronous
SYNC# (MALDRV)	Low	Asynchronous
MAOE#	Low	(Note 4)
MBAOE#	Low	(Note 4)
MALE	High	Asynchronous
MBALE	High	Asynchronous
MDOE#	Low	Asynchronous
MSEL# (MTR4/8#)	Low	(Note 2)
MEOC#	Low	(Note 2)
MOCLK	—	—
MFRZ#	Low	(Note 2)
MZBT# (MX4/8#)	Low	(Note 2)
MBRDY# (MSTBM)	Low	(Note 2)
SNPCLK (SNPMD)	—	—
SNPSTB#	Low	(Note 4)
SNPINV	High	(Note 4)
SNPNCA	High	(Note 4)

NOTES:

1. MWB/WT# and DRCTM# must be synchronous to CLK while SWEND# is active. MKEN# and MRO# must be synchronous to CLK while KWEND# is active.
2. In clocked memory bus mode, these pins are synchronous to MCLK. In strobed memory bus mode, these pins are asynchronous.
3. These signals are synchronous with TCK.
4. These signals are sampled differently depending on the snoop mode.

3.0 ARCHITECTURAL OVERVIEW

3.1 Introduction

The Intel486™ CPU-cache chip set provides a tightly coupled processing engine based on the Intel486 microprocessor and a cache subsystem comprised of the 82495DX cache controller and multiple 82490DX cache components. Figure 3.1 diagrams the basic configuration.

The cache subsystem provides a gateway between the CPU and the memory bus. All CPU accesses that can be serviced locally are transparent to the memory bus and serve to avoid bus traffic. As a result, the cache chip set reduces memory bus bandwidth to both increase Intel486 processor performance and support efficient multiprocessor systems.

The cache subsystem also decouples the CPU from the memory bus to provide zero-wait-state operation at high clock frequencies while allowing relatively slow and inexpensive memories.

The CPU-cache chip set prevents latency and bandwidth bottlenecks across a variety of uniprocessor and multiprocessor designs. The processor's on-chip cache supports a very wide CPU data bus and high-speed data movement. The second-level cache greatly extends the capabilities of the on-chip cache resources, enabling a larger portion of memory cycles to be satisfied independently of the memory bus.

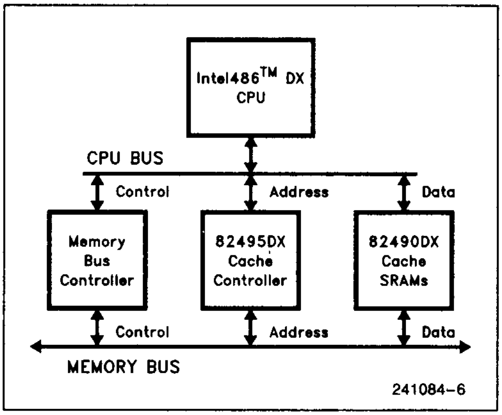


Figure 3.1. Basic CPU-Cache Subsystem

3.2 CPU-Cache Chip Set Description

The chip set is comprised of three functional blocks:

3.2.1 CPU

The chip set includes a special version of the Intel486™DX microprocessor at 50 MHz. The Intel486™DX Microprocessor Data Sheet provides complete component specifications.

3.2.2 CACHE CONTROLLER

The 82495DX cache controller is the main control element for the chip set, providing tags and line states, and determining cache hits and misses. The 82495DX executes all CPU bus requests and coordinates all main memory accesses with the memory bus controller (MBC).

The 82495DX controls the data paths of the 82490DX cache components for cache hits and misses and furnishes the CPU with needed data. The controller dynamically adds wait states as needed using the most recently used (MRU) prediction algorithm.

The 82495DX also performs memory bus snoop operations in shared memory systems and drives the cycle address and other attributes during memory bus accesses. Figure 3.2 diagrams the 82495DX.

3.2.3 CACHE SRAM

Multiple 82490DX cache components provide the cache SRAM and data path. Each component includes the latches, muxes and logic needed to work in lock step with the 82495DX to efficiently serve both hit and miss accesses. The 82490DX components take full advantage of VLSI silicon flexibility to exceed the capabilities of discrete implementations. The 82490DX components support zero-wait-state hit accesses and concurrent CPU and memory bus accesses, and they replicate MRU bits for autonomous way prediction. During memory bus cycles, the 82490DX components act as a gateway between CPU and memory buses. Figure 3.3 diagrams an 82490DX cache component.

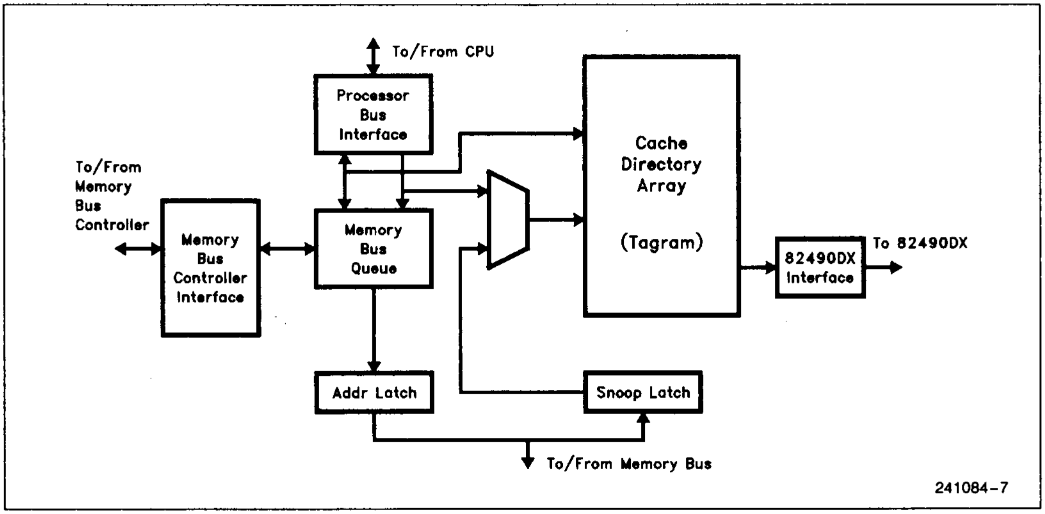

To/From CPU
Processor
Bus
Interface
Cache
Directory
Array
(Tagram)
To/From
Memory
Bus
Controller
Memory
Bus
Controller
Interface
Memory
Bus
Queue
82490DX
Interface
To 82490DX
Addr Latch
Snoop Latch
To/From Memory Bus
241084-7

Figure 3.2. 82495DX Block Diagram

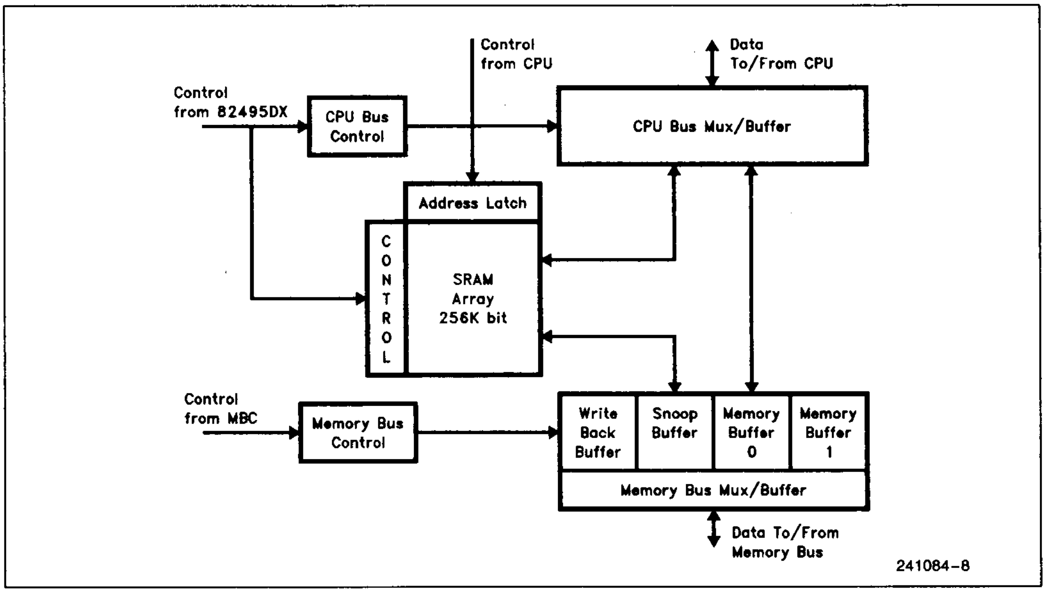

Control
from CPU
Data
To/From CPU
Control
from 82495DX
CPU Bus
Control
CPU Bus Mux/Buffer
Address Latch
C
O
N
T
R
O
L
SRAM
Array
256K bit
Control
from MBC
Memory Bus
Control
Write
Back
Buffer
Snoop
Buffer
Memory
Buffer
0
Memory
Buffer
1
Memory Bus Mux/Buffer
Data To/From
Memory Bus
241084-8

Figure 3.3. 82490DX Block Diagram

3.3 Secondary Cache Features

The 82495DX cache controller and 82490DX cache components provide a unified, software transparent secondary data and instruction cache. The cache enables a high-speed processor core that provides efficient performance even when paired with a significantly slower memory bus.

The secondary cache interprets CPU bus cycles and can service most memory read and write cycles without accessing main memory. I/O and other special cycles are passed directly to the memory bus. The cache has a dual-port structure that permits concurrent CPU and memory bus operation.

The 82495DX cache controller contains the 8K tag entries and logic needed to support a cache as large as 256K. Combinations of between 4 and 9 82490DX cache SRAMs are used to create caches ranging from 128K to 256K, with or without data parity.

The MBC provides logic needed to interface the CPU, 82495DX and 82490DX to the memory bus. Because the MBC also affects system performance, its design can be the basis of product differentiation.

The secondary cache offers the following major features:

- Tracks the speed of the Intel486 microprocessor
- 4K or 8K tags
- 1 or 2 lines per sector
- 4 or 8 transactions per line
- 32- or 64-bit memory bus
- 128K or 256K cache
- Data parity support
- Write-Back cache with full multiprocessing consistency support
- Supports MESI cache consistency protocol
- Monitors memory bus to ensure cache consistency
- Maintains inclusion
- Write-protection
- Two-way set-associativity with MRU prediction algorithm
- Zero-wait-state hit cycles on MRU way, one wait-state on MRU misses
- Concurrent CPU and memory bus transactions
- Supports synchronous, clocked and strobed memory bus architectures
- Strong and weak write ordering enforcement
- Single-level write posting
- Optional single-level memory bus pipelining

The secondary cache is highly flexible, providing many configuration options. The system designer can select among physical configurations (such as line size and sectoring), snooping modes and memory bus modes. The cache can be used in a variety of design applications spanning uniprocessor, dual processor and large-scale multiprocessor systems.

Cache configurations are determined by the 82495DX and 82490DX pin settings at reset only. To conserve pins, a number of configuration inputs become 82495DX and 82490DX I/O pins following reset.

The physical cache can be organized to support a number of basic cache configurations as shown in Figure 3.4.

3.4 Chip Set Design and Operation

The Intel486™DX microprocessor, 82495DX and 82490DX are specifically designed to enable a high-performance chip set. The component interfaces have been carefully evaluated by Intel to arrive at an optimal layout. The memory bus definition is, however, completely determined by the system designer.

3.5 CPU Bus Interface

The CPU bus interface connects the 82495DX and 82490DX to the CPU. This interface is optimized to provide zero-wait-state accesses at 50 MHz. Intel provides a proven high-performance layout recommendation. If a different layout is required, limited A.C. Timings and a set of design rules are provided in Section 4.5.

3.6 Secondary Cache Interface

Intel has carefully optimized the interface between the 82495DX cache controller and 82490DX cache memories to provide a high-speed interconnect that supports zero-wait-state operations. The interface enables the 82495DX to control how the 82490DX components load, store and move data between their internal buffers, the CPU bus and the memory bus.

The secondary cache interface is considered highly optimized, and Intel strongly recommends its example layout specification.

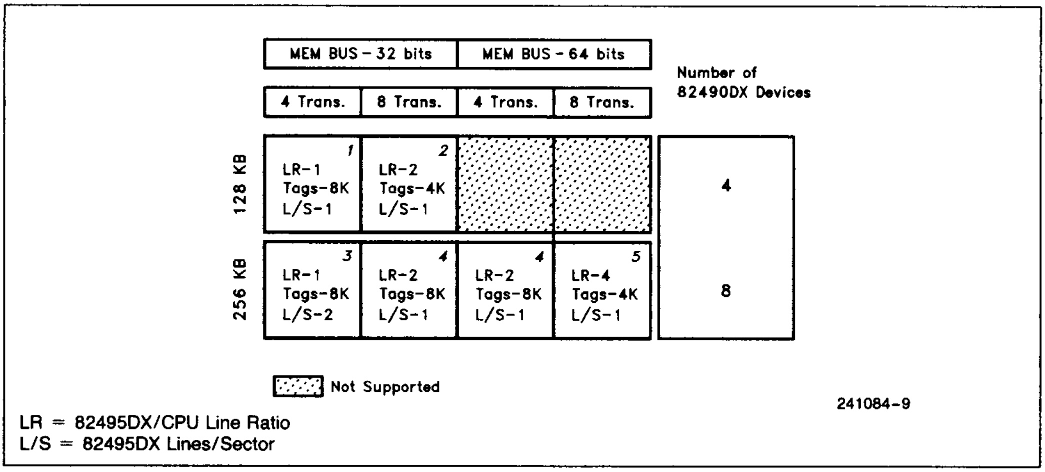

MEM BUS - 32 bits
MEM BUS - 64 bits
4 Trans.
8 Trans.
4 Trans.
8 Trans.
Number of 82490DX Devices
128 KB
1
LR-1
Tags-8K
L/S-1
2
LR-2
Tags-4K
L/S-1
4
256 KB
3
LR-1
Tags-8K
L/S-2
4
LR-2
Tags-8K
L/S-1
4
LR-2
Tags-8K
L/S-1
5
LR-4
Tags-4K
L/S-1
8
Not Supported
241084-9
LR = 82495DX/CPU Line Ratio
L/S = 82495DX Lines/Sector

Figure 3.4. Cache Configurations

3.7 Memory Bus/MBC Interface

The MBC is a user-implemented set of components that adapt the CPU and cache subsystem to a specific memory bus protocol. While the 82495DX and 82490DX provide address and data paths, the MBC provides the basic path for control signals accessing the memory bus and the system. The MBC controls cycle sequencing and accommodates the timing requirements of the cache, CPU and other devices on the memory bus.

MBC design complexity can vary according to the application, from single-CPU systems employing a write-through cache to complex multiprocessor systems with external tags. The CPU-cache chip set is highly flexible, and its precise operation is largely determined by the design of the MBC.

The MBC adapts the CPU-cache chip set to a specific memory bus protocol and coordinates with the 82495DX for operations such as line fills, flushes and write-backs. The controller also handles all cycle control, data transfers, snooping and any needed synchronization. The MBC invites product differentiation and allows the designer to easily adapt the 82495DX cache subsystem to specific architectures. Figure 3.5 diagrams one of many possible MBC designs.

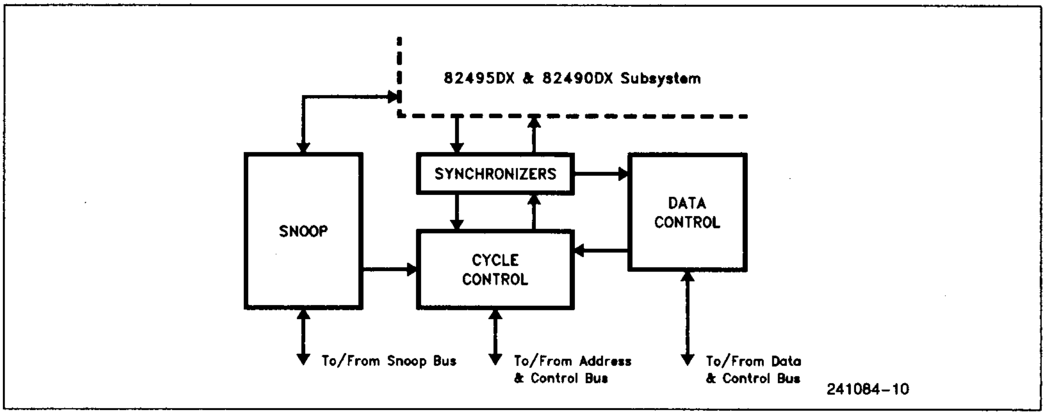

82495DX & 82490DX Subsystem
SYNCHRONIZERS
SNOOP
DATA CONTROL
CYCLE CONTROL
To/From Snoop Bus
To/From Address & Control Bus
To/From Data & Control Bus
241084-10

Figure 3.5. MBC Block Diagram Example

3.8 Test

The cache subsystem supports built-in self-test (BIST) and boundary scan. The designer may elect to use BIST as part of the system test procedure, to be initiated along with Intel486 processor BIST at RESET. Boundary scan utilizes dedicated 82495DX boundary scan pins which provide test hooks that conform to the IEEE Standard Test Access Port and Boundary Scan Architecture (IEEE Std. 1149.1).

4.0 ELECTRICAL DATA

4.1 Background

The 82495DX cache controller provides four main interfaces, one each to the CPU bus, memory bus controller, memory bus and 82490DX cache components. The memory bus controller (MBC) is typically implemented using programmable logic devices (PLDs). As a result, MBC interface signal timings are generated based on readily available PLD specifications. The memory bus interface is specified to suit a generic memory interface that operates at frequencies as high as the CPU frequency.

In the chip set implementation, the Intel486 CPU provides the following inputs and outputs, which are accessed by the MBC: CLK, RESET, PCHK# HOLD, HLDA, BRDY#, A20M#, FLUSH#, NMI, FERR#, IGGNE#, INTR, BS8#, BS16# and BOFF#. The AC and DC characteristics of these signals are listed here but are not valid for the 50 MHz Intel486 DX component version.

The following A.C. and D.C. parameters are not tested but rather are guaranteed by design characterization:

V_{IL} min
V_{IH} max
Pin Capacitance
Clock Rise and Fall Times
Clock Stability
Float Delays

4.2 Maximum Ratings

Table 4.1 refers to stress ratings only, and functional operation at these maximum ratings cannot be guaranteed. Functional operation is given by the AC and DC specifications.

Table 4.1a. Absolute Maximum Ratings 82495DX and 82490DX

Case Temperature Under Bias	−65°C to +100°C
Storage Temperature	−65°C to +150°C
Pin Voltage with Respect to Ground	−0.5V to V_{CC} +0.5V
Supply Voltage with Respect to V_{SS}	−0.5V to +6.5V

4.3 DC Specifications

Table 4.1. DC Specifications

$V_{CC} = 5V \pm 5\%, T_{CASE} = 0°C$ to $+75°C$					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Notes**
V_{IL}	Input Low Voltage	−0.3	+0.8	V	TTL Level
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	TTL Level
V_{OL}	Output Low Voltage		0.45	V	TTL Level(1)
V_{OH}	Output High Voltage	2.4		V	TTL Level(2)
I_{CC}	Power Supply Current		1000 600 300 480	mA	i486DX CPU @ 50 MHz(3) 82495DX @ 50 MHz(3) 82490DX @ Typical Cycle Mix @ 50 MHz(4) 82490DX @ Atypical Cycle Mix @ 50 MHz(4)
I_{LI}	Input Leakage Current		±15	μA	$0 < V_{IN} < V_{CC}$
I_{LO}	Output Leakage Current		±15	μA	$0 \leq V_{OUT} \leq V_{CC}$ Tristate
I_{IL}	Input Leakage Current		200	μA	$V_{IN} = 0.45V$(5)
C_{IN}	Input Capacitance		13 14 5	pF	for i486 DX CPU for 82495DX for 82490DX
C_O	Output Capacitance		17 18 15	pF	for i486 DX CPU for 82495DX for 82490DX
$C_{I/O}$	I/O Capacitance		17 18 15	pF	for i486 DX CPU for 82495DX for 82490DX
C_{CLK}	CLK Input Capacitance		15 11 5	pF	for i486 DX CPU for 82495DX for 82490DX
C_{TIN}	Test Input Capacitance		15 15 10	pF	for i486 DX CPU for 82495DX for 82490DX
C_{TOUT}	Test Output Capacitance		20 15 10	pF	for i486 DX CPU for 82495DX for 82490DX
C_{TCK}	Test Clock Capacitance		15 15 10	pF	for i486 DX CPU for 82495DX for 82490DX

NOTES:

1. Parameter measured at 4 mA I_{load}. For MCFA6–MCFA0, MSET10–MSET0, and MTAG11–MTAG0, this parameter is measured at 12 mA I_{load}.
2. Parameter measured at 1 mA I_{load}. For MCFA6–MCFA0, MSET10–MSET0, and MTAG11–MTAG0, this parameter is measured at 2 mA I_{load}.
3. Represents maximum power consumption given a worst case cycle mix.

4. The 82490DX's maximum I_{CC} varies depending on the type of cycles performed. The 82490DX consumes the **atypical cycle mix maximum I_{CC}** by running back-to-back single word read cycles. Normally, applications will not exercise the 82490DX in this way over sustained periods of time. the **typical cycle mix maximum I_{CC}** is defined for an instruction mix of 1/3 read hits, 1/3 write hits and 1/3 idle cycles. One MRU read hit cycle (two clocks), one Write-Back write hit (two cycles) and two idle clocks implements this mix. The table below illustrates a typical 82490DX's supply current for various cycle types under typical conditions (V_{CC} = 5V, T_{CASE} = 25°C):

Cycle Type	I_{CC}*
Idle	77 mA
Read hit; Burst = 1 (Atypical Cycle Mix)	388 mA
Read hit; Burst = 4	304 mA
Write hit; Burst = 1	223 mA
Write hit; Burst = 4	240 mA
Write Through; non-cacheable; Burst = 1	180 mA
Line fill; Cacheable; Burst = 4	275 mA
Cache Flush	117 mA
Typical Cycle Mix (1/3 Read, 1/3 Write, 1/3 Idle)	244 mA

*These values are neither tested nor guaranteed by Intel.

5. This parameter is for input with pullup.

4.4 AC Specifications

All TTL timing specifications are measured at 1.5V for logic levels 0 and 1.

Table 4.2. Clock, Reset and Configuration

V_{CC} = 5V ±5%, T_{CASE} = 0°C to +75°C, C_L = 0 pF Unless Otherwise Specified. All Inputs and Outputs are TTL Level.

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_0	CLK Frequency	33	50	MHz		1 × clock
t_{0a}	MCLK, MOCLK Frequency	25	50	MHz		
t_1	CLK, MCLK, MOCLK Stability		0.1	%		
t_2	CLK Period	20	30	ns		
t_{2a}	MCLK, MOCLK Period	20	40	ns		
t_3	CLK, MCLK, MOCLK High Time	7		ns	4.1	(Note 1)
t_4	CLK, MCLK, MOCLK Low Time	7		ns	4.1	(Note 1)
t_5	CLK, MCLK, MOCLK Rise Time		2	ns		(Note 1)
t_6	CLK, MCLK, MOCLK Fall Time		2	ns		(Note 1)
t_7	RESET Setup Time	6		ns	4.4	
t_8	RESET Hold Time	2		ns	4.4	
t_9	RESET Duration	8 × t_2 15 × t_2		ns	4.4	for 82495DX(2) for 82490DX and i486 DX CPU
t_{10}	All Configurations CFG3-CFG0, SNPMD, PLOCKEN, MALDRV, MDLDRV, CLDRV, HIGHZ#, SLFTST# Setup Time	10 × t2		ns	4.4	(Notes 3, 4, 9)
t_{11}	All Configurations CFG3-CFG0, SNPMD, PLOCKEN, MALDRV, MDLDRV, CLDRV, HIGHZ#, SLFTST# Hold Time	0		ns	4.4	(Notes 3, 5, 9)
t_{12}	FLUSH#, SYNC# Setup Time	8		ns	4.3	for 82495DX(5)
t_{13}	FLUSH#, SYNC# Hold Time	1		ns	4.3	for 82495DX(7)
t_{14}	FLUSH#, SYNC# Duration	2 × t_2		ns		(Note 8)
t_{15}	MOCLK Falling Edge to Rising Edge of MCLK	2		ns		

Table 4.2. Clock, Reset and Configuration (Continued)

V_{CC} = 5V ±5%, T_{CASE} = 0°C to +75°C, C_L = 0 pF Unless Otherwise Specified. All Inputs and Outputs are TTL Level.						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{16}	FLUSH#, A20M#, NMI, INTR, IGNNE#, BS8#, BS16#, BOFF# Setup Time	5		ns	10-3	for i486 DX CPU
t_{17}	FLUSH#, A20M#, NMI, INTR, IGNNE#, BS8#, BS16#, BOFF# Hold Time	2		ns	10-3	for i486 DX CPU
t_{18}	FERR#, HLDA Valid Delay	2	12	ns	10-2	
t_{19}	FERR#, HLDA Float Delay		20	ns		
t_{20}	HOLD Setup Time	5		ns	10-3	
t_{21}	HOLD Hold Time	2		ns	10-3	

NOTES:

1. Rise/Fall, High/Low times measured between 0.8V and 2.0V.
2. Power-up reset duration should be 1 ms after V_{CC} and CLK become stable. If configuration inputs with pullups are left floated, 10 μs RESET duration is required.
3. Timing is referenced to the falling edge of reset.
4. 9 ns setup time is required to guarantee recognition on next clock.
5. 4 ns hold time is required to guarantee recognition on next clock.
6. To guarantee recognition on next clock.
7. Synchronous mode only.
8. Asynchronous mode only. To guarantee recognition.
9. CFG3 is a CMOS level input.

Table 4.3. 82495DX/82490DX Memory Bus Controller Interface

V_{CC} = 5V ±5%, T_{CASE} = 0°C to +75°C C_L = 0 pF Unless Otherwise Specified. All Inputs and Outputs are TTL Level.						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{30}	BRDY#, CRDY#, KWEND#, SWEND#, BGT#, CNA#, [WRMRST] Setup Time	8		ns	4.3	82495DX
t_{30a}	BRDY#, CRDY# Setup	7		ns	4.3	82490DX
t_{30b}	BRDY# Setup	5		ns	4.3	i486 DX CPU
t_{31}	BRDY#, CRDY#, KWEND#, SWEND#, BGT#, CNA#, [WRMRST] Hold Time	1		ns	4.3	
t_{31a}	BRDY# Hold	2		ns	4.3	i486 DX CPU
t_{32}	CW/R#, CD/C#, CMI/O#, CLEN0, CLEN1, RDYSRC, MCACHE#, KLOCK#, BLE#, CPLOCK#, PALLC#, CAHOLD, CWAY, FSIOUT#, CADS#, CDTS#, SNPADS# Valid Delay	2	10	ns	4.2	
t_{33}	NENE#, SMLN# Valid Delay	2	14	ns	4.2	
t_{34}	MDATA Setup to CLK (Clock before BRDY# Active)	6		ns	4.3	(Note 1)
t_{35}	MDATA Valid Delay from CLK (CLK from CDTS# Valid, MDOE# Active)	2	12	ns	4.2	
t_{36}	MDATA Valid Delay from MDOE# Active		8	ns	4.2	
t_{37}	MDATA Float Delay from MDOE# Inactive	0	14	ns		

NOTE:

1. Even if MBRDY# or MISTB is not used for this cycle, the data still must be held according to t_{43}.

Table 4.4. 82495DX Memory Interface

V_{CC} = 5V ±5%, T_{CASE} = 0°C to +75°C C_L = 0 pF Unless Otherwise Specified. All Inputs and Outputs are TTL Level.						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{50}	SNPCLK Frequency	8	50	MHz		1 × clock(10)
t_{51}	SNPCLK Period	20	125	ns	4.1	(Note 11)
t_{52}	SNPCLK High Time	7		ns	4.1	
t_{53}	SNPCLK Low Time	7		ns	4.1	
t_{54}	SNPCLK Rise Time		2	ns		(Note 1)
t_{55}	SNPCLK Fall Time		2	ns		(Note 1)
t_{56}	MCFA6–MCFA0, MSET10–MSET0, MTAG11–MTAG0 Valid Delay	2	11	ns	4.5	(Notes 2, 3)
t_{57}	MCFA6–MCFA0, MSET10–MSET0, MTAG11–MTAG0 Float Delay	2	15	ns	4.5	(Note 4)
t_{58}	MCFA6–MCFA0, MSET10–MSET0, MTAG11–MTAG0 Valid Delay	2	13	ns	4.5	(Note 5)
t_{60}	MCFA6–MCFA0, MSET10–MSET0, MTAG11–MTAG0 Valid Delay	2	13	ns	4.2	(Note 6)
t_{62a}	MCFA6–MCFA0, MSET10–MSET0, MTAG11–MTAG0, SNPINV, SNPNCA, MAOE#, MBAOE#, SNPSTB# Setup Time	8		ns	4.3	(Note 7a)
t_{62b}	MCFA6–MCFA0, MSET10–MSET0, MTAG11–MTAG0, SNPINV, SNPNCA, MAOE#, MBAOE# Setup Time	1		ns	4.3	(Note 7b)
t_{62c}	MCFA6–MCFA0, MSET10–MSET0, MTAG11–MTAG0, SNPINV, SNPNCA, MAOE#, MBAOE#, SNPSTB# Setup Time	8		ns	4.3	(Note 7c)
t_{63a}	MCFA6–MCFA0, MSET10–MSET0, MTAG11–MTAG0, SNPINV, SNPNCA, MAOE#, MBAOE#, SNPSTB# Hold Time	1		ns	4.3	(Note 7a)
t_{63b}	MCFA6–MCFA0, MSET10–MSET0, MTAG11–MTAG0, SNPINV, SNPNCA, MAOE#, MBAOE# Hold Time	8		ns	4.3	(Note 7b)
t_{63c}	MCFA6–MCFA0, MSET10–MSET0, MTAG11–MTAG0, SNPINV, SNPNCA, MAOE#, MBAOE#, SNPSTB# Hold Time	1		ns	4.3	(Note 7c)
t_{64}	SNPSTB# Setup Time	8		ns	4.3	(Note 8)
t_{65}	SNPSTB# Hold Time	1		ns	4.3	(Note 8)
t_{66}	SNPSTB# Active/Inactive Time	8		ns	4.3	(Note 9)
t_{67}	MRO#, MKEN#, DRCTM#, MWB/WT# Setup Time	8		ns	4.3	

Table 4.4. 82495DX Memory Interface (Continued)

V_{CC} = 5V ±5%, T_{CASE} = 0°C to +75°C C_L = 0 pF Unless Otherwise Specified. All Inputs and Outputs are TTL Level.						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{68}	MRO#, MKEN#, DRCTM#, MWB/WT# Hold Time	1		ns	4.3	
t_{69}	MTHIT#, MHITM#, SNPBSY# Valid Delay	2	12	ns	4.2	
t_{69a}	SNPCYC# Valid Delay	2	10	ns	4.2	

NOTES:

1. Rise/fall times measured between 0.8V and 2.0V.
2. See capacitive derating curves for additional loading delay.
3. Valid delay from MAOE#, MBAOE# going active (low).
4. Float delay from MAOE#, MBAOE# going inactive (high).
5. Valid delay from MALE or MBALE if both MAOE#, MBAOE# are active.
6. Valid delay from CLK only if MALE or MBALE, MAOE# and MBAOE# are active.

7a. In clocked mode referenced to SNPCLK rising edge.

7b. In strobed mode referenced to SNPSTB# falling edge.

7c. In synchronous mode, refer to CLK.

8. Asynchronous clocked mode only. Timings referenced to SNPCLK.
9. Asynchronous signal. Time to guarantee recognition on next clock.
10. SNPCLK is only used for the clocked memory bus mode. SNPCLK Min frequency is not tested.
11. $t_{51} \geq t_2$

Table 4.5. 82490DX Clocked Mode

V_{CC} = 5V ±5%, T_{CASE} = 0°C to +75°C C_L = 0 pF Unless Otherwise Specified. All Inputs and Outputs are TTL Level.						
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Figure**	**Notes**
t_{38}	MBRDY#, MSEL#, MEOC# Setup to MCLK	5		ns	4.3	
t_{39}	MBRDY#, MSEL#, MEOC#, Hold from MCLK	2		ns	4.3	
t_{40}	MZBT#, MFRZ# Setup to MCLK	5		ns	4.3	
t_{41}	MZBT#, MFRZ# Hold from MCLK	2		ns	4.3	
t_{42}	MDATA Setup to MCLK	5		ns	4.3	
t_{43}	MDATA Hold from MCLK	2		ns	4.3	
t_{44}	MDATA Valid Delay from MCLK•MBRDY#	2	14	ns	4.2	
t_{45}	MDATA Valid Delay from MCLK•MEOC# MCLK•MSEL#	2	20	ns	4.2	(Notes 1, 2)
t_{46}	MDATA Valid Delay from MOCLK	2	10	ns	4.2	(Note 3)

NOTES:

1. Since MEOC# causes the 82490DX to end a cycle and switch to the next pending cycle, MDATA may be driven from the next MCLK•MEOC edge.
2. Since MSEL# can be used to restart a cycle (by resetting the burst counter), MDATA may be driven from the MCLK•MSEL#•MRDY# edge.
3. Since MOCLK controls a transparent latch on MDATA, MOCLK activation may be the gating signal for MDATA valid.

Table 4.6. 82490DX Strobed Mode

V_{CC} = 5V ±5%, T_{CASE} = 0°C to +75°C
C_L = 0 pF Unless Otherwise Specified.
All Inputs and Outputs are TTL Level.

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{85}	MISTB, MOSTB High Time	12		ns	4.6	(Note 2)
t_{86}	MISTB, MOSTB Low Time	12		ns	4.6	
t_{87}	MEOC# High Time	8		ns	4.6	
t_{88}	MEOC# Low Time	8		ns	4.6	
t_{89}	MxSTB, MEOC# Rise Time		2	ns		(Notes 1, 2)
t_{90}	MxSTB, MEOC# Fall Time		2	ns		
t_{91}	MSEL# High Time for Restart	8		ns	4.6	
t_{92}	MSEL# Setup before Transition on MxSTB	5		ns	4.8	(Note 2)
t_{93}	MSEL# Hold after Transition on MxSTB	10		ns	4.8	
t_{94}	MSEL# Hold after Transition on MEOC#	2		ns	4.8	
t_{95}	MxSTB Transition to/from MEOC# Falling Transition	10		ns		
t_{96}	MZBT# Setup to MSEL# or MEOC# Falling Edge	5		ns	4.7	
t_{97}	MZBT# Hold from MSEL# or MEOC# Falling Edge	2		ns	4.7	
t_{98}	MFRZ# Setup to MEOC# Falling Edge	5		ns	4.7	
t_{99}	MFRZ# Hold from MEOC# Falling Edge	2		ns	4.7	
t_{100}	MDATA Setup to MISTB Transition or MEOC# Falling Edge	5		ns	4.7	
t_{101}	MDATA Hold from MISTB Transition or MEOC# Falling Edge	2		ns	4.7	
t_{102}	MDATA Valid Delay from MOSTB Transition	2	14	ns	4.9	
t_{103}	MDATA Valid Delay from MEOC# Falling Transition or MSEL# Deactivation	2	20	ns	4.9	

NOTES:
1. Rise/fall times measured between 0.8V and 2.0V.
2. Strobed Mode timings are not tested.

Table 4.7. Test Mode All Components

V_{CC} = 5V ±5%, T_{CASE} = 0°C to +75°C
C_L = 0 pF Unless Otherwise Specified.
All Inputs and Outputs are TTL Level.

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{120}	TCK Frequency		25	MHz		1 × clock
t_{121}	TCK Period	40		ns		
t_{122}	TCK High Time	10		ns		
t_{123}	TCK Low Time	10		ns		
t_{124}	TCK Rise Time		4	ns		(Note 1)
t_{125}	TCK Fall Time		4	ns		(Note 1)
t_{126}	TDI, TMS Setup Time	16		ns	4.10	
t_{127}	TDI, TMS Hold Time	12		ns	4.10	
t_{128}	TDO Valid Delay	0	20	ns	4.10	
t_{129}	TDO Float Delay		20			(Note 1)
t_{130}	All Outputs Valid Delay	0	25	ns	4.10	
t_{131}	All Outputs Float Delay		36	ns	4.10	(Note 1)
t_{132}	All Input Setup Time	17		ns		
t_{133}	All Input Hold Time	12		ns		

NOTE:
1. Not tested.

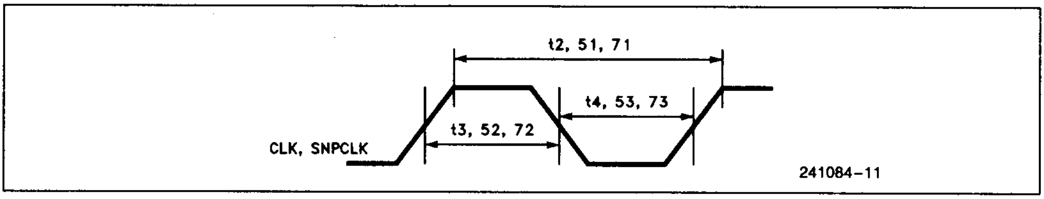


Figure 4.1. Clock Waveform

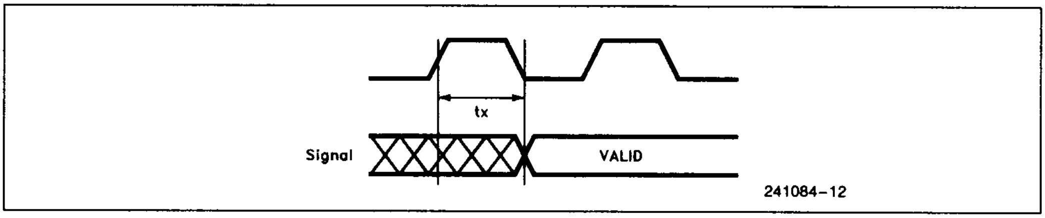
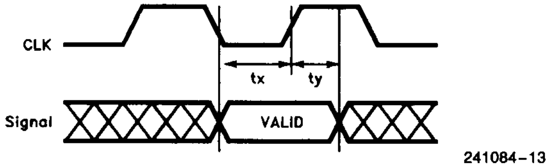


Figure 4.2. Valid Delay Timings


CLK
tx
ty
Signal
VALID
241084-13

tx = t_{30}, 62a, 62c, 64, 67, 76, 85
ty = t_{31}, 63a, 63c, 65, 68, 77, 86

Figure 4.3. Setup and Hold Timings

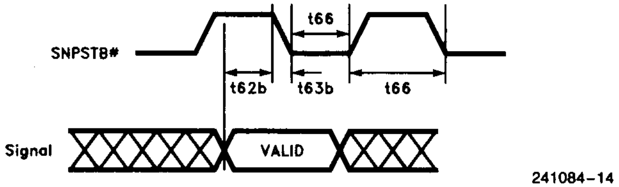

SNPSTB#
t66
t62b
t63b
t66
Signal
VALID
241084-14

Figure 4.3a. Setup and Hold Timings in Strobed Snooping Mode

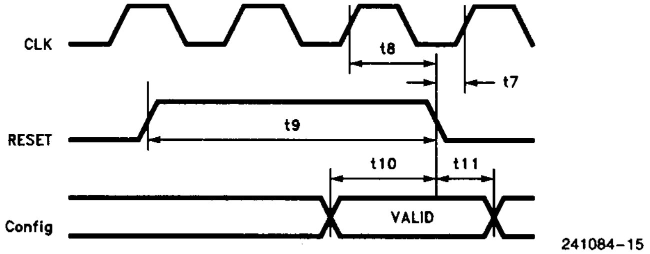

CLK
t8
t7
RESET
t9
t10
t11
Config
VALID
241084-15

Figure 4.4. Reset and Configuration Timings

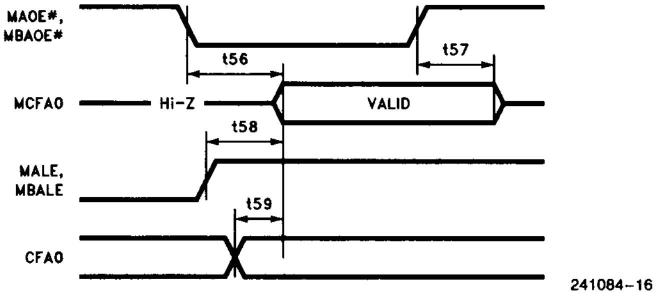

MAOE#,
MBAOE#
t56
t57
MCFA0
Hi-Z
VALID
t58
MALE,
MBALE
t59
CFA0
241084-16

Figure 4.5. Memory Interface Signals

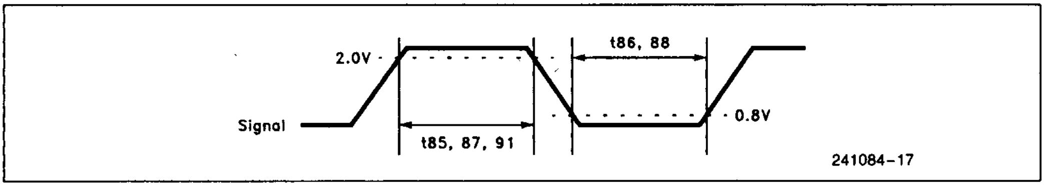

2.0V
Signal
t85, 87, 91
t86, 88
0.8V
241084-17

Figure 4.6. Active/Inactive Timing

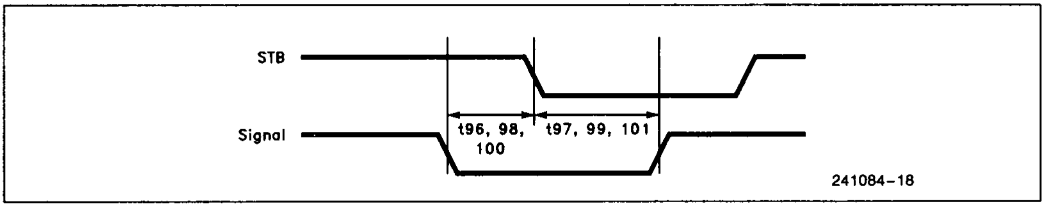

STB
Signal
t96, 98, 100
t97, 99, 101
241084-18

Figure 4.7. Setup and Hold Timing

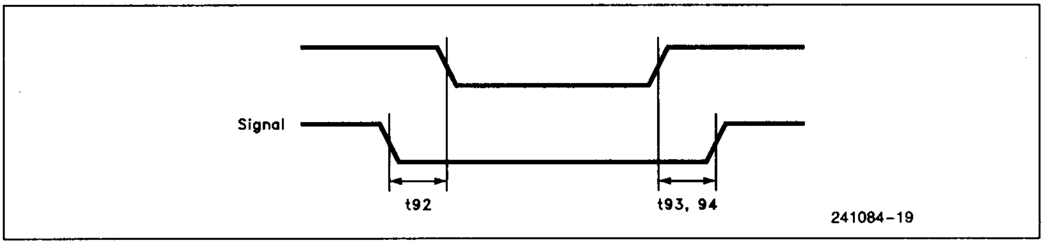

Signal
t92
t93, 94
241084-19

Figure 4.8. Setup and Hold Timing

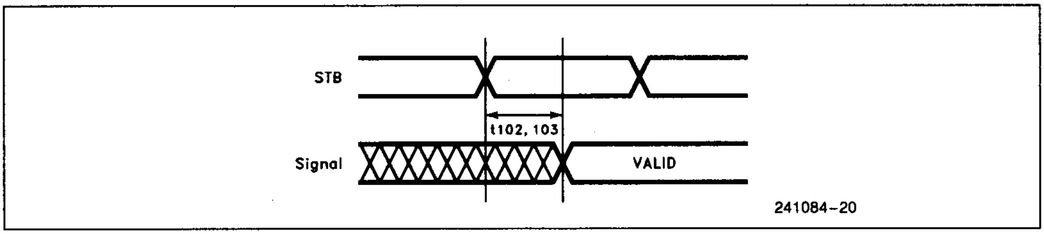

STB
Signal
t102, 103
VALID
241084-20

Figure 4.9. Valid Delay Timing

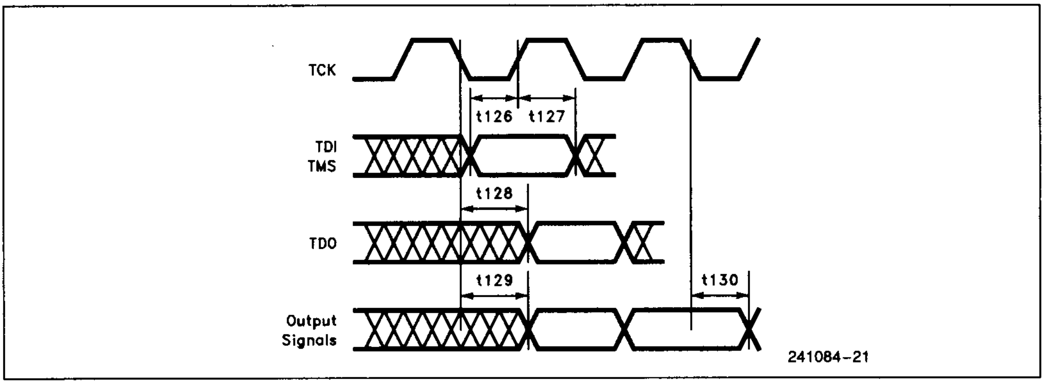

TCK
t126
t127
TDI
TMS
t128
TDO
t129
t130
Output Signals
241084-21

Figure 4.10. Test Timings

4.5 Optimized and External Interface Specifications

OPTIMIZED INTERFACE

The Optimized Interface is the high-performance interconnect between the Intel486 DX CPU, 82495DX Cache Controller and the 82490DX SRAMs. This interface is tuned for the known configuration options of the chip set and includes specially designed (non-standard) input and output buffers optimized for the defined electrical environment of each signal path. The specification of this interface is also non-standard and requires some new definitions which will be explained in the following sections.

The Intel486 DX CPU-Cache Chip Set Hardware Reference Manual (HRM) details recommended layouts for the different cache size configurations. These layouts have been thoroughly tested and are available in industry standard formats. Check with your local Intel sales office for specific information on these documents. The system designer may choose an alternate component layout; in designing this layout the designer must ensure that each of the optimized signal interface paths is carefully simulated and that signal timings and quality achieve the specified limits. This section explains the new specifications defined for the Optimized Interface and shows the steps involved to extract these parameters when simulating an alternate layout.

Each path in the Optimized Interface has specific requirements. As outlined in Table 4.8, there are three classes of specifications: Flight Time to guarantee signal timing; Signal Quality to guarantee reliable operation; and Buffer Models to specify completely Flight Time and Signal Quality.

The worst case simulation corners (slow and fast) come from plotting power supply voltage (V_{CC}) and operating temperature on a graph as shown in Figure 4.11. A device will have its slowest signal rise times and internal propagation delays when V_{CC} is at its minimum and temperature is at it's maximum allowed value. This corresponds to the slow simulation corner. Conversely, a device will have its fastest signal rise times and internal propagation delays when V_{CC} is at its maximum and temperature is at its minimum allowed value. This corresponds to the fast simulation corner. The fast and slow corners are the two extreme operating conditions which need to be simulated. All other point on the graph will fall between these two extremes, and do not need to be simulated to guarantee operation.

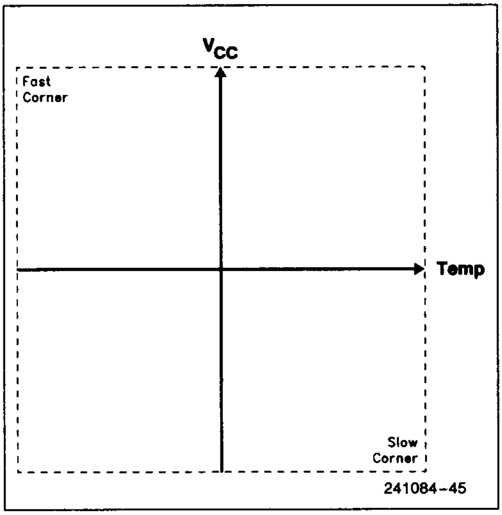


Figure 4.11. Determining the Simulation Corners

Table 4.8. The Three Specification Classes of the Optimized Interface, their Purpose and the New Parameters

Specification Class	Purpose	Parameters
Flight Time	Guarantee Timing	Maximum Flight Time
Signal Quality	Guarantee Reliable Operation	Maximum Signal Overshoot (Undershoot) Maximum Signal Ring-back Maximum Settling Time
Buffer Models	Completely Specify Flight Time and Signal Quality	C_{IN}—Input Capacitance Lp—Package Inductance Cp—Package Capacitance dV/dt—Voltage Source Rate of Change R_O—Output Impedance C_O—Output Capacitance

FLIGHT TIME

Flight Time is essentially the maximum propagation delay of a signal from a driving component to any receiving component. It is defined to be the time difference between the $V_{CC}/2$ (50%) level of an unloaded output signal and the $V_{CC}/2$ (50%) level of a receiving signal whose 50% V_{CC} to 60% V_{CC} rise time is greater than or equal to 1 V/ns (**T_{50-50}**, Figure 4.12). Receiving signals with slower rise times mut be de-rated where the 60% V_{CC} point is extrapolated back to the 50% V_{CC} point using a 1 V/ns reference slope (**Textrapolated,** Figure 4.13). Thus Flight Time is defined to be the greater of these two values, **T_{50-50}** or **Textrapolated.** (Although the figures only show a low to high transition, Flight Time is the worst case of both low to high and high to low transitions.) The Flight Time specifications must be met to insure proper signal timings between all components participating in the Optimize Interface. Please see the notes to the designer on page 45 for additional information regarding Flight Time measurements.

Figure 4.14 shows how to measure Flight Time in a system environment. Note that this particular figure shows the measurement being made from the 60% V_{CC} threshold. This only applies if the slope of the receiving signal is less than 1 V/ns from the 50% V_{CC} to 60% V_{CC} points. If the slope is greater than 1 V/ns in this region, then the Flight Time would be measured to the 50% V_{CC} point.

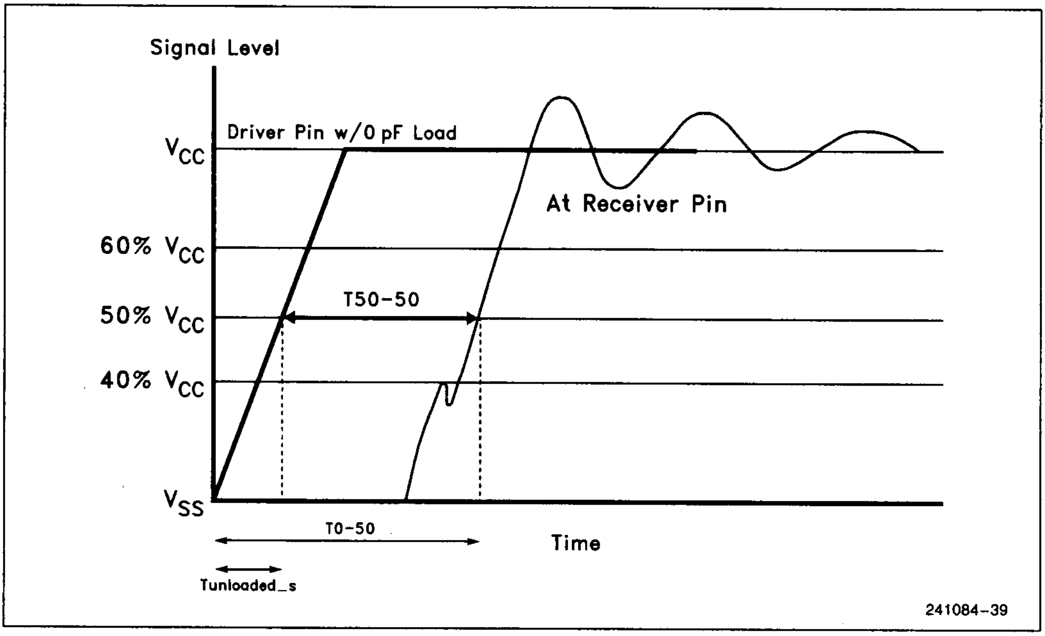


Figure 4.12. How to measure Flight Time (T_{50-50}) when the 50% V_{CC} to 60% V_{CC} slope is faster than 1 V/ns for Low to High transitions. (Use the 50% V_{CC} to 40% V_{CC} slope for High to Low transitions).

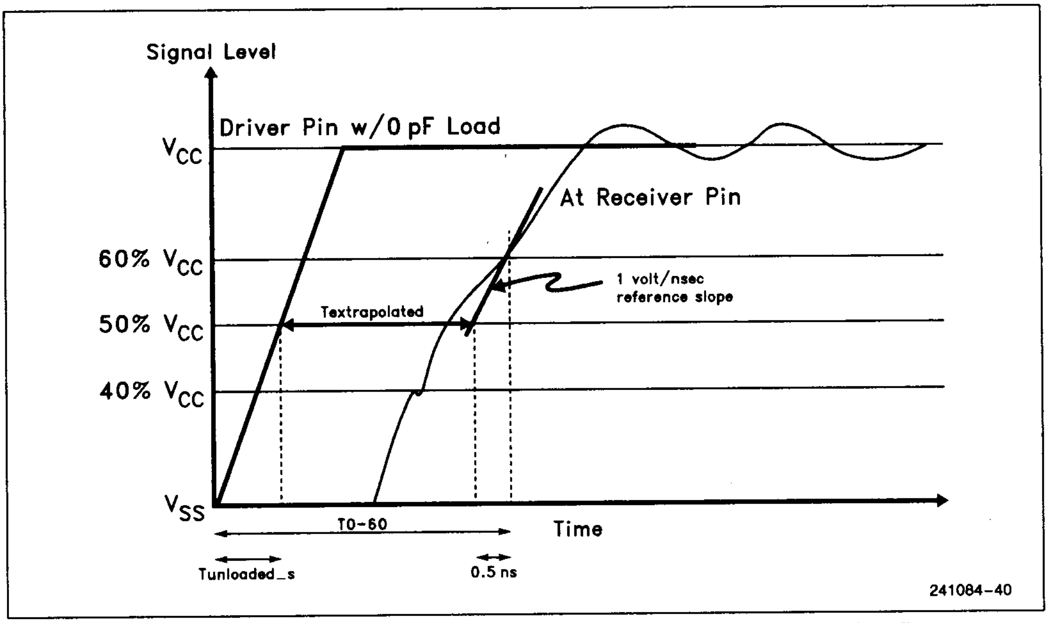


Figure 4.13. Determining Flight Time based on a 1 V/ns slope (Textrapolated) for Low to High transitions. (For High to Low transitions extrapolate from the 40% V_{CC} point back to the 50% V_{CC} point with a −1 V/ns slope.)

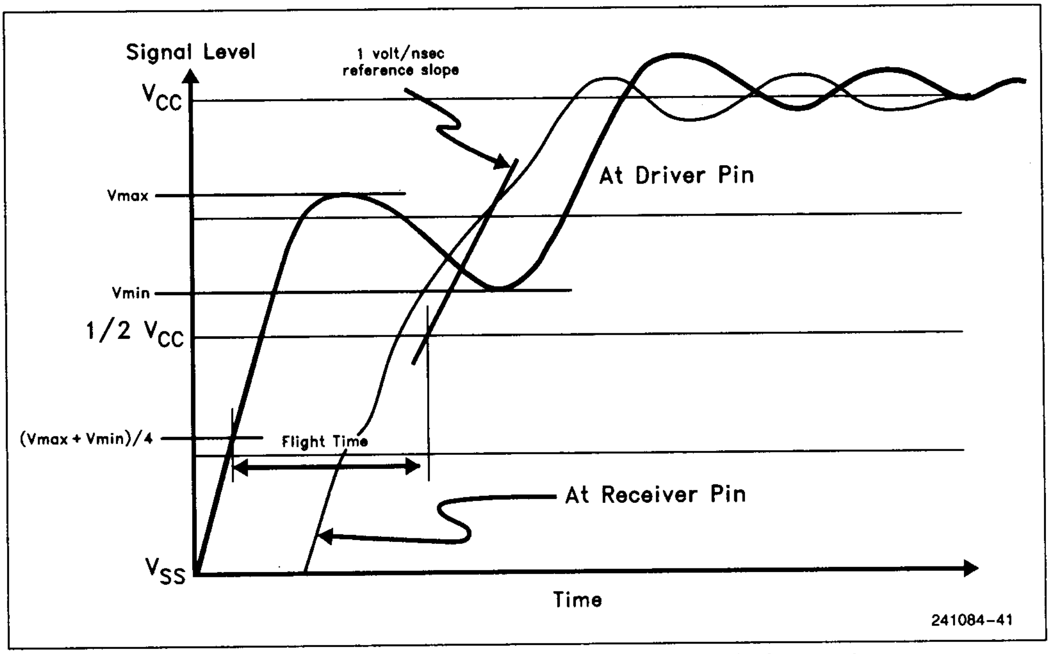


Figure 4.14. How to Measure Flight Time in a System Environment

Table 4.9 describes the maximum flight time and clock skew specifications. Tables 4.10 to 4.13 list the maximum flight time and clock skew specifications for each driver-receiver network in the Optimized Interface (256 Kbyte version). Tables 4.14–4.17 list similar information for the 128 Kbyte version. For each net, the first order buffer model driver and receiver type are also listed. (See Tables 4.21 and 4.22 for the parameters that define the drivers and receivers.)

Table 4.9. Description of Maximum Flight Time and Clock Skew

Parameter	Description
Maximum Flight Time	Maximum time a signal may take traveling from the driver to the input pin of the receiving component. It includes the time to traverse the PC board trace and any added output delay on the output buffer due to the trace and receiving component loading and is dependent on rise time at the receiving component.
Maximum Clock Skew	Maximum difference in time between the clock signal arriving at different components. It is measured at 1.5V.

Table 4.10. Flight Times, Signal Group: CPU to Cache RAM (CPU-CRAM) (256 Kbyte Version)

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
i486 D0–D31	82490 CDATA0–3	1.0	2.05	ZD2	ZR9
i486 DP0–3	82490 CDATA0–3	1.0	2.05	ZD2	ZR9
82490 CDATA0–3	i486 D0–D31	1.0	2.25	ZD10	ZR3
82490 CDATA0–3	i486 DP0–31	1.0	2.25	ZD10	ZR3

Table 4.11. Flight Times, Signal Group: CPU to Cache (CPU-Cache) (256 Kbyte Version)

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
i486 A2–A3	82495 CFA0–1	0.5	3.6	ZD4	ZR6
i486 A4–A5	82495 CFA5–6	0.5	3.6	ZD4	ZR6
i486 A6–A16	82495 SET0–10	0.5	3.6	ZD4	ZR6
i486 A2–A16	82490 A1–A15	1.0	4.6	ZD4	ZR7
82495 CFA5–6	i486 A4–A5	0.5	11.0	ZD6	ZR4
82495 SET0–10	i486 A6–A16	0.5	11.0	ZD6	ZR4
82495 CFA0–1	82490 A1–A2	1.0	11.0	ZD6	ZR7
82495 CFA5–6	82490 A3–4	1.0	11.0	ZD6	ZR7
82495 SET0–10	82490 A5–A15	1.0	11.0	ZD6	ZR7
i486 ADS#	82495 ADS#	0.5	3.5	ZD5	ZR5
i486 ADS#	82490 ADS#	1.0	4.2	ZD5	ZR8
i486 W/R#	82495 W/R#	0.5	3.8	ZD5	ZR5
i486 W/R#	82490 W/R#	1.0	4.2	ZD5	ZR8
i486 BE0–3#	82490 BE#	1.0	3.8	ZD1	ZR8
i486 BE0–3#	82490 CDATA4–7	1.0	3.8	ZD1	ZR9

Table 4.12. Flight Times, Signal Group: CPU to Cache Controller (CPU-CCTL) (256 Kbyte Version)

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
i486 A17–A20	82495 TAG0–3	0.5	1.5	ZD4	ZR6
i486 A21–A28	82495 TAG4–11	0.5	1.5	ZD1	ZR6
i486 A29–A31	82495 CFA2–4	0.5	1.5	ZD1	ZR6
82495 TAG0–3	i486 A17–A20	0.5	2.1	ZD6	ZR4
82495 TAG4–11	i486 A21–A28	0.5	2.1	ZD6	ZR2
82495 CFA2–4	i486 A29–A31	0.5	2.1	ZD6	ZR2
i486 D/C#	82495 D/C#	0.5	1.4	ZD3	ZR5
i486 LEN	82495 LEN	0.5	1.3	ZD3	ZR5
i486 LOCK#	82495 LOCK#	0.5	1.3	ZD3	ZR5
i486 M/IO#	82495 M/IO#	0.5	1.4	ZD3	ZR5
i486 PCD	82495 PCD	0.5	2.8	ZD3	ZR5
i486 PWT	82495 PWT	0.5	2.8	ZD3	ZR5
82495 AHOLD	i486 AHOLD	0.5	1.8	ZD7	ZR1
82495 BRDYC1#	i486 BRDYC#	0.5	1.25	ZD7	ZR1
82495 EADS#	i486 EADS#	0.5	1.8	ZD7	ZR1
82495 KEN#	i486 KEN#	0.5	1.8	ZD7	ZR1

Table 4.13. Flight Times, Signal Group: Cache Controller to Cache RAM (CCTL-CRAM) (256 Kbyte Version)

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
82495 BLAST#	82490 BLAST#	1.0	2.1	ZD9	ZR8
82495 BRDYC2#	82490 BRDYC#	1.0	2.0	ZD9	ZR8
82495 BUS#	82490 BUS#	1.0	2.4	ZD9	ZR8
82495 MAWEA#	82490 MAWEA#	1.0	2.4	ZD9	ZR8
82495 MCYC#	82490 MCYC#	1.0	2.4	ZD9	ZR8
82495 WAY	82490 WAY	1.0	2.2	ZD9	ZR8
82495 WBA	82490 WBA	1.0	3.2	ZD9	ZR8
82495 WBTYP	82490 WBTYP	1.0	2.3	ZD9	ZR8
82495 WBWE#	82490 WBWE#	1.0	2.3	ZD9	ZR8
82495 WRARR#	82490 WRARR#	1.0	2.2	ZD9	ZR8

Table 4.14. Signal Group: CPU to Cache RAM (CPU-CRAM) (128 Kbyte Version)

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
i486 D0–D31	82490 CDATA0–7	1.0	2.05	ZD2	ZR9
i486 DP0–3	82490 CDATA0–3	1.0	2.05	ZD2	ZR9
82490 CDATA0–7	i486 D0–D31	1.0	2.25	ZD10	ZR3
82490 CDATA0–3	i486 DP0–31	1.0	2.25	ZD10	ZR3

Table 4.15. Signal Group: CPU to Cache (CPU-Cache) (128 Kbyte Version)

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
i486 A2–A3	82495 CFA0–1	0.5	3.6	ZD4	ZR6
i486 A4	82495 CFA6	0.5	3.6	ZD4	ZR6
i486 A5–A15	82495 SET0–10	0.5	3.6	ZD4	ZR6
i486 A2–A15	82490 A2–A15	1.0	4.6	ZD4	ZR7
82495 CFA6	i486 A4	0.5	11.0	ZD6	ZR4
82495 SET0–10	i486 A5–A15	0.5	11.0	ZD6	ZR4
82495 CFA0–1	82490 A2–A3	1.0	11.0	ZD6	ZR7
82495 CFA6	82490 A4	1.0	11.0	ZD6	ZR7
82495 SET0–10	82490 A5–A15	1.0	11.0	ZD6	ZR7
i486 ADS#	82495 ADS#	0.5	3.5	ZD5	ZR5
i486 ADS#	82490 ADS#	1.0	4.2	ZD5	ZR8
i486 W/R#	82495 W/R#	0.5	3.8	ZD5	ZR5
i486 W/R#	82490 W/R#	1.0	4.2	ZD5	ZR8
i486 BE0–3#	82490 BE#	1.0	3.8	ZD1	ZR8
i486 BE0–3#	82490 CDATA4–7	1.0	3.8	ZD1	ZR9

Table 4.16. Signal Group: CPU to Cache Controller (CPU-CCTL) (128 Kbyte Version)

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
i486 A16-A20	82495 TAG0-4	0.5	1.5	ZD4	ZR6
i486 A21-A27	82495 TAG5-11	0.5	1.5	ZD1	ZR6
i486 A28-A31	82495 CFA2-5	0.5	1.5	ZD1	ZR6
82495 TAG0-4	i486 A16-A20	0.5	2.1	ZD6	ZR4
82495 TAG5-11	i486 A21-A27	0.5	2.1	ZD6	ZR2
82495 CFA2-5	i486 A28-A31	0.5	2.1	ZD6	ZR2
i486 D/C#	82495 D/C#	0.5	1.4	ZD3	ZR5
i486 LEN	82495 LEN	0.5	1.3	ZD3	ZR5
i486 LOCK#	82495 LOCK#	0.5	1.3	ZD3	ZR5
i486 M/IO#	82495 M/IO#	0.5	1.4	ZD3	ZR5
i486 PCD	82495 PCD	0.5	2.8	ZD3	ZR5
i486 PWT	82495 PWT	0.5	2.8	ZD3	ZR5
82495 AHOLD	i486 AHOLD	0.5	1.8	ZD7	ZR1
82495 BRDYC1#	i486 BRDYC#	0.5	1.25	ZD7	ZR1
82495 EADS#	i486 EADS#	0.5	1.8	ZD7	ZR1
82495 KEN#	i486 KEN#	0.5	1.8	ZD7	ZR1

Table 4.17. Signal Group: Cache Controller to Cach RAM (CCTL-CRAM) (128 Kbyte Version)

Driver	Receiver	Max CLK Skew (ns)	Max Flight Time (ns)	Driver Buffer Type	Receiver Buffer Type
82495 BLAST#	82490 BLAST#	1.0	2.1	ZD9	ZR8
82495 BRDYC2#	82490 BRDYC#	1.0	2.0	ZD9	ZR8
82495 BUS#	82490 BUS#	1.0	2.4	ZD9	ZR8
82495 MAWEA#	82490 MAWEA#	1.0	2.4	ZD9	ZR8
82495 MCYC#	82490 MCYC#	1.0	2.4	ZD9	ZR8
82495 WAY	82490 WAY	1.0	2.2	ZD9	ZR8
82495 WBA	82490 WBA	1.0	3.2	ZD9	ZR8
82495 WBTYP	82490 WBTYP	1.0	2.3	ZD9	ZR8
82495 WBWE#	82490 WBWE#	1.0	2.3	ZD9	ZR8
82495 WRARR#	82490 WRARR#	1.0	2.2	ZD9	ZR8

Notes to the Designer:

1. The method of measuring Flight Times discussed earlier in this section assumes that the signal at the receiving pin is increasing monotonically at the 50% and 60% V_{CC} threshold voltages for low to high transitions (decreasing monotonically at the 50% and 40% V_{CC} threshold voltages for the high to low transitions). If the signal wave form at a receiving input does not increase monotonically through these threshold voltages, but instead has some "ringing" as shown in Figure 4.15 then the proper measurement point for determining Flight Time is the last crossing of the specified measurement voltage (50% and 60% V_{CC} for low to high transitions, 50% and 40% V_{CC} for high to low transitions). **Do not confuse the use of the term "ringing" as it is used here with the Signal Quality specification, Ringback, which is discussed in the next section.**

   One exception where you do not measure the Flight Time from the last crossing of the threshold voltage is shown in Figure 4.16. This condition occurs when the signal wave form at the receiving input transitions to a high enough voltage before "ringing" to allow the input buffer to switch, yet does not "ring back" to a low enough voltage, or for a long enough period to allow the input buffer to switch back to its original value. In this exception case, the signal must transition monotonically up to a minimum of 3.5V (V_{CC} = 5V) before "ringing". The falling transition must not drop below 2.8V, and the signal may not stay below the 60% V_{CC} threshold (3.0V) for more than 1.0 ns. (For the high to low transition case, the signal must transition monotonically down to 1.5V before "ringing". The rising transition must not rise above 2.2V, and the signal may not stay above the 40% V_{CC} threshold (2.0V) for more than 1.0 ns.)

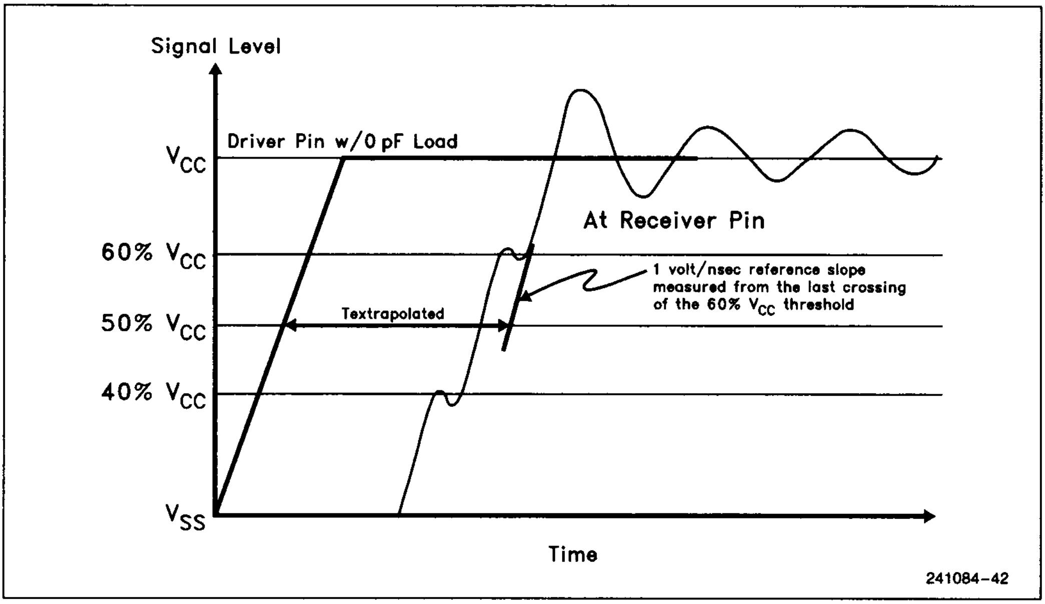


Figure 4.15. How to Measure Flight Time with Multiple Crossings of the Threshold Voltage

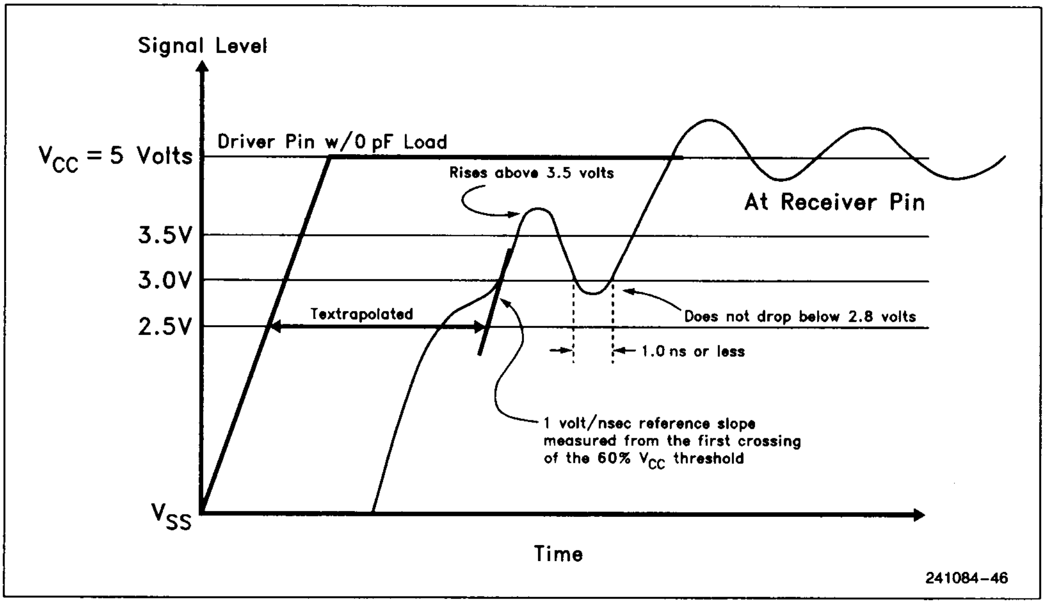

Signal Level
V_{CC} = 5 Volts
Driver Pin w/0 pF Load
Rises above 3.5 volts
At Receiver Pin
3.5V
3.0V
2.5V
Textrapolated
Does not drop below 2.8 volts
1.0 ns or less
1 volt/nsec reference slope measured from the first crossing of the 60% V_{CC} threshold
V_{SS}
Time
241084-46

Figure 4.16. Exception case where you can measure the Flight Time from the first crossing of the 60% point (3.0V in this example) instead of the last crossing.

2. Decreasing the maximum clock skew in your system can increase the allowed maximum Flight Time. The maximum Flight Times listed in Tables 4.10 to 4.17 assume that the maximum clock skew, also listed in the tables, is present in the system. If the system designer can guarantee a clock skew smaller than those listed in the tables, the maximum Flight Time specifications can be increased by an equal amount. For example, the first signal listed in Table 4.13, BLAST#, has a Flight Time of 2.1 ns and a maximum clock skew between the 82495DX and the 82490DX of 1.0 ns. If the system designer guarantees the clock skew between the 82495DX and all 82490DX components is no greater than 0.5 ns, then the maximum allowable Flight Time for the signal BLAST# can be increased to 2.6 ns.

SIGNAL QUALITY

Acceptable signal quality must be maintained over all operating conditions to insure reliable operation. Signal quality is defined by three parameters: Settling Time, Over/Undershoot and Ringback. Figure 4.17 illustrates the parameters used to verify signal quality. Table 4.18 describes each of these parameters. The Under/Overshoot parameter must be measured without the ESD input protection diodes present. This implies that this parameter can only be accurately compared with the specification in a simulation environment. The two other parameters can be measured either with or without the diodes i.e., with simulations and/or in a system environment.

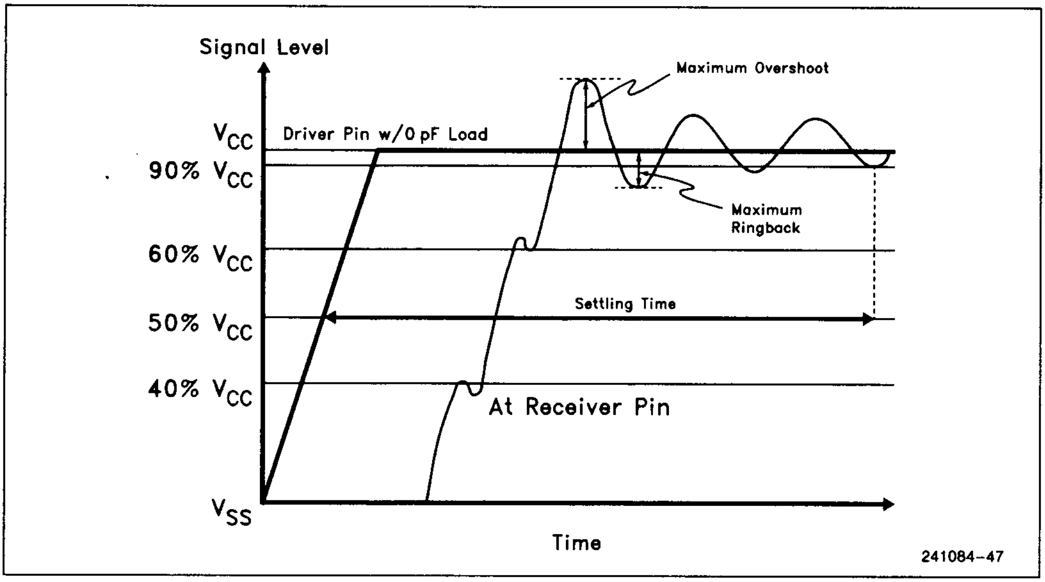

Signal Level
Maximum Overshoot
V_{CC}
Driver Pin w/0 pF Load
90% V_{CC}
Maximum Ringback
60% V_{CC}
Settling Time
50% V_{CC}
40% V_{CC}
At Receiver Pin
V_{SS}
Time
241084-47

Figure 4.17. Driver and Receiver Signal Wave Forms Showing Signal Quality Parameters

Table 4.18. Specifications for Signal Quality (Optimized Interface)

Parameter	Description	Specification
Maximum Signal Overshoot (Undershoot)	Maximum absolute voltage a signal extends above V_{CC} or below V_{SS} (without diodes present).	3.0V
Maximum Settling Time	The total time required for a signal at the receiver to stabilize within 10% of its final voltage (above 4.5V or below 0.5V for V_{CC} = 5V, V_{SS} = 0V). It is referenced to the time the unloaded driver pin crosses the 50% V_{CC} threshold.	15.0 ns
Maximum Signal Ringback	The maximum absolute value, in volts, allowed for a signal at the receiving pin, below V_{CC} or above V_{SS}, following an overshoot or undershoot event respectively.	1.75V

I/O BUFFER MODELS

The first order I/O buffer model is a simplified representation of the complex input and output buffers used in the Intel486 DX CPU, 82495DX, and 82490DX. Figure 4.18 shows the structure of the input buffer model and Figure 4.19 shows the output buffer model. Tables 4.19 and 4.20 shows the parameters used to specify these models.

The package parameters of the input buffer model, Cp and Lp, will vary from pin to pin depending on the location of the pin on the package and the trace length from the pin to the bonding pad. The input capacitance, Cin, will vary depending on the routing of traces on the die, the type of buffers connected to the pin and the processing of any particular die.

The output model parameters dV/dt, Ro, Co and to will vary with the type of output buffer used for a given signal output, the processing conditions of any given die, the V_{CC} level and the temperature.

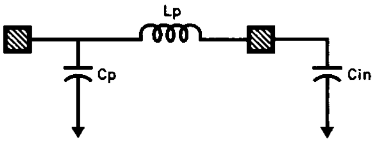


Figure 4.18. First Order Input Buffer

Table 4.19. The Parameters Used in the Specification of the First Order Input Buffer Model

Parameter	Description
Cin	Minimum and Maximum value of the capacitance of the input buffer model.
Lp	Minimum and Maximum value of the package inductance.
Cp	Minimum and Maximum value of the package capacitance.

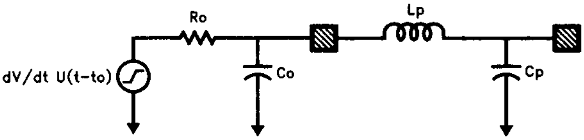


Figure 4.19. First Order Output Buffer

Table 4.20. The Parameters Used in the Specification of the First Order Output Buffer Model

Parameter	Description
dV/dt	Minimum and maximum value of the rate of change of the open circuit voltage source used in the output buffer model.
Ro	Minimum and Maximum value of the output buffer impedance.
Co	Minimum and Maximum value of the output buffer capacitance.
Lp	Minimum and Maximum value of the package inductance.
Cp	Minimum and Maximum value of the package capacitance.

OPTIMIZED INTERFACE BUFFERS

The values shown in Tables 4.21 and 4.22 represent the minimum and maximum values for each of the buffer model parameters. These values are guaranteed by Intel and should be used in worst case analysis for Flight Time (slow corner) and Signal Quality (fast corner).

The following outputs of the 82495DX have selectable output driver sizes:

- BLAST#
- BRDYC2#
- BUS#
- MAWEA#
- MCYC#
- WAY
- WBA
- WBTYP
- WBWE#
- WRARR#

These outputs can have either a Large or X-Large sized driver (ZD8 or ZD9). It is recommended that for both 128 Kbyte and 256 Kbyte caches, the X-Large driver (ZD9) be used. To select the larger driver, the signal BGT# (Cache Low Drive) must be held low during the falling edge of reset. CLDRV must meet the proper setup and hold times t_{10} and t_{11}.

Table 4.21. Input Buffer Model Parameters (Optimized Interface)

Buffer Type	Component	Pin Type	Cp (pF)		Lp (nH)		Cin (pF)	
			Min	Max	Min	Max	Min	Max
ZR1	Intel486 DX	Input Only	5.6	9.0	11.7	20.0	1.5	1.9
ZR2	Intel486 DX	I/O–ZD1 driver	4.7	8.1	7.8	15.6	3.0	4.3
ZR3	Intel486 DX	I/O–ZD2 driver	3.6	7.2	7.7	16.5	3.5	4.3
ZR4	Intel486 DX	I/O–ZD4 driver	4.0	8.1	7.1	16.2	5.5	7.3
ZR5	82495DX	Input Only	5.2	8.5	7.6	17.5	2.1	4.2
ZR6	82495DX	I/O–ZD6 driver	5.2	10.3	6.6	17.7	3.8	4.6
ZR7	82490DX	Input Only	0.9	1.1	7.3	9.8	1.5	1.9
ZR8	82490DX	Input Only	0.9	1.1	7.5	10.6	1.5	2.2
ZR9	82490DX	I/O–ZD10 Driver	0.9	1.1	7.7	10.0	3.5	4.3

Table 4.22. Output Buffer Model Parameters (Optimized Interface)

Buffer Type	Component	Driver Size	dV/dt (V/ns)		Ro (Ω)		Co (pF)		Lp (nH)		Cp (pF)	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
ZD1	Intel486 DX	Small	2.8	5	25.5	76.5	3.0	4.3	7.8	15.6	4.7	8.1
ZD2	Intel486 DX	Small	2.8	5	25.5	76.5	3.5	4.3	7.7	16.5	3.6	7.2
ZD3	Intel486 DX	Small	2.8	5	25.5	76.5	3.0	3.6	8.5	17.8	5.4	11.1
ZD4	Intel486 DX	Large	3.8	7.1	14	44	5.5	7.3	7.1	16.2	4.0	8.1
ZD5	Intel486 DX	Large	3.8	7.1	14	44	5.5	6.7	7.7	16.0	5.9	7.3
ZD6	82495DX	Small	2.8	5	25.5	85	3.8	4.6	6.6	17.7	5.2	10.3
ZD7	82495DX	Small	2.8	5	25.5	85	5.3	8.7	7.6	16.5	5.3	8.7
ZD8	82495DX	Large	3.8	6.3	14	44	3.4	10.2	7.5	13.9	5.3	7.9
ZD9	82495DX	X-Large	3.8	6.3	11.4	28.5	3.4	10.2	7.5	13.9	5.3	7.9
ZD10	82490DX	Small	2.8	5	25.5	85	3.5	4.3	7.7	10.0	0.9	1.1

EXTERNAL INTERFACE BUFFERS

The external interface is the interface between the chip set components and the memory bus controller, memory address bus, and memory data bus. Intel supplies buffer models for this interface to aid system designers simulation of this section of their design. Unlike the optimized interface, Intel supplies the AC Specifications of output valid delay and input setup and hold times.

Each valid delay is specified for a 0 pF load. The system designer should use I/O buffer modeling or lumped capacitance derating curves to account for signal flight time delays. I/O buffer modeling is recommended since it is a more exact method of determining flight times. Table 4.23 lists the buffer type to be used for each signal in the external interface. Lumped capacitance derating curves can be found in the Intel486 DX CPU-Cache Chip Set data sheet.

The values shown in Tables 4.24 and 4.25 represent the minimum and maximum values for each of the buffer model parameters. These values are not guaranteed Intel, but represent a very close approximation of the actual values. These values should be used in worst case analysis for Flight Time (slow corner) and Signal Quality (fast corner). Typical values for each individual pin can be found in Appendix E.

Table 4.26 outlines the 82495DX and 82490DX external interface signals which have selectable output buffer sizes based on the value of MALDRV and MDLDRV, respectively, during the falling edge of reset. The size of driver used should be determined by the capacitive load placed on each group of signals. MALDRV and MDLDRV must meet the proper setup and hold times t_{10} and t_{11}.

Table 4.23. External Interface Signal Buffer Assignment

Device	Signals	Type	Driver Buffer Type	Receiver Buffer Type
Intel486 DX	A20M#, BOFF#, BRDY#, BS8, CLK, FLUSH#, HOLD, IGGNE#, INTR, NMI, RESET, TCK, TDI, TMS (BS16#, RDY#—See Note 1)	I	NA	ER1
	HLDA, FERR#, PCHK, TDO (BLAST#, BREQ#—See Note 1)	O	ED1	NA
82495DX	BGT#, BRDY#, CFG3, CLK, CNA#, CRDY#, DRCTM#, FLUSH#, KWEND#, MALE, MAOE#, MBALE, MBAOE#, MKEN#, MRO#, MWB/WT#, RESET, SNPCLK, SNPINV, SNPNCA, SNPSTB#, SWEND#, SYNC#, TCK, TDI, TMS, WRMRST	I	NA	ER2
	MSET10-0, MTAG11-0, MCFA6-0 for MALDRV = 1 for MALDRV = 0	 I/O I/O	 ED2 ED3	 ER3 ER3
	BLE#, CADS#, CAHOLD, CD/C#, CLEN0-1, CM/IO#, CPLOCK#, CW/R#, CWAY#, FSIOUT#, KLOCK#, MCACHE#, PALLC#, RDYSRC, SNPADS#, SNPCYC#, TDO	O	ED4	NA
	CDTS#, MHITM#, MTHIT#, NENE#, SMLN#, SNPBSY#	O	ED5	NA
82490DX	BRDY#, CLK, CRDY#, MBRDY# (MISTB), MCLK, MDOE#, MEOC#, MFRZ#, MOCLK (MOSTB), MSEL#, MZBT#, RESET, TCK, TDI, TMS	I	NA	ER4
	MDATA7-0 for MDLDRV = 1 for MDLDRV = 0	 I/O I/O	 ED6 ED7	 ER5 ER5
	TDO	O	ED6	NA

NOTE:
1. The Intel486™ DX CPU-Cache Chip Set does not use these signals.

Table 4.24. Input Buffer Model Parameters (External Interface)

Buffer Type	Component	Pin Type	Cp (pF)		Lp (nH)		Cin (pF)	
			Min	Max	Min	Max	Min	Max
ER1	Intel486 DX	Input Only	4.9	11.7	8.7	25.3	1.5	3.1
ER2	82495DX	Input Only	4.9	8.9	7.2	15.2	1.4	6.2
ER3	82495DX	I/O	5.2	12.1	7.2	21.6	5.9	7.3
ER4	82490DX	Input Only	0.9	1.1	7.3	10.6	1.5	3.7
ER5	82490DX	I/O	0.9	1.1	7.7	10.0	5.9	7.3

Table 4.25. Output Buffer Model Parameters (External Interface)

Buffer Type	Component	Driver Size	dV/dt (V/ns)		Ro (Ω)		Co (pF)		Lp (nH)		Cp (pF)	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
ED1	Intel486 DX	Small	2.8	5	25.5	85	5.3	12.1	10.2	22.4	3.0	6.7
ED2	82495DX	Small	2.8	5	25.5	85	5.2	12.1	7.2	21.6	5.9	7.3
ED3	82495DX	Large	3.8	7.1	14	44	5.2	12.1	7.2	21.6	5.9	7.3
ED4	82495DX	Small	2.8	5	25.5	85	4.8	8.9	7.3	14.0	4.8	8.9
ED5	82495DX	Large	3.8	7.1	14	44	5.0	9.4	7.4	10.8	0.9	9.4
ED6	82490DX	Small	2.8	5	25.5	85	0.9	1.1	7.7	10.0	5.9	7.3
ED7	82490DX	Large	3.8	7.1	14	44	0.9	1.1	7.7	10.0	5.9	7.3

Table 4.26. 82495DX and 82490DX External Interface Signals Which Have Selectable Driver Sizes

Device	Signals	Type	Driver Buffer Type	Receiver Buffer Type
82495DX	MSET10–0, MTAG11–0, MCFA6–0	I/O		
	for MALDRV = 1		ED2	ER3
	for MALDRV = 0		ED3	ER3
82490DX	MDATA7–0	I/O		
	for MDLDRV = 1		ED6	ER5
	for MDLDRV = 0		ED7	ER5

Table 4.27. Specifications for Signal Quality (External Interface)

Parameter	Description	Specification
Maximum Signal Overshoot (Undershoot)	Maximum absolute voltage signal extends above V_{CC} or below V_{SS} (without diodes present)	1.6V
Maximum Settling Time	The total time required for a signal at the receiver, to stabilize within 10% of it's final voltage (above 4.5V or below 0.5V for $V_{CC} = 5V$, $V_{SS} = 0V$). It is referenced to the time the unloaded driver pin crosses the 50% V_{CC} threshold.	Signal should be stable before next transition.
Maximum Signal Ringback	The maximum absolute value, in volts, allowed for a signal at the receiving pin, below V_{CC} or above V_{SS}, following an overshoot or undershoot event respectively.	0.8V

PRINTED CIRCUIT BOARD CHARACTERISTICS

Printed circuit board characteristics play a significant role in determining the Flight Time and quality of a signal. Table 4.28 lists the parameters a system designer needs to completely describe the board's characteristics.

SIMULATION REQUIREMENTS

When simulating the Optimize Interface for either Flight Time or Signal Quality, it is critical to use the appropriate minimum or maximum specification value for each element in the simulation. Table 4.29 shows the correct extreme value for each specification that should be used in the Flight Time and Signal Quality simulations.

Table 4.28. The Parameters Used to Specify Printed Circuit Board Characteristics

Parameters		Description
Surface Traces	Zo (Ω)	Minimum and maximum impedance for signal traces on the two outside layers of the board.
	S (ns/ft)	Minimum and maximum propagation delay for all signal traces on the two outside layers of the board.
Inner Traces	Zo (Ω)	Minimum and maximum impedance for all signal traces on the two layers of the board.
	S (ns/ft)	Minimum and maximum propagation delay for all signal traces on the inner layers of the board.
Via Capacitance	Cvia	Minimum and maximum capacitance of a via, which allows a signal to pass from one layer to another.

Table 4.29. Specifications to be Used for Simulation of Flight Time and Signal Quality

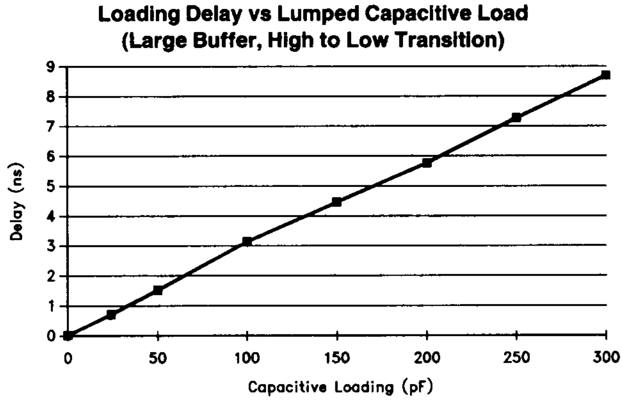
Simulation Element	Specification	Flight Time	Signal Quality
Input Buffer	Cp	Max	Min
	Lp	Max	Min
	Cin	Max	Min
Output Buffer	dV/dt	Min	Max
	Ro	Max	Min
	Co	Max	Min
	Lp	Max	Min
	Cp	Max	Min
Printed Circuit Board	Zo	Min	Max
	S	Max	Min
	Cvia	Max	Min
Other	Temperature	Max	Min
	V_{CC}	Min	Max

4.6 Capacitive Derating

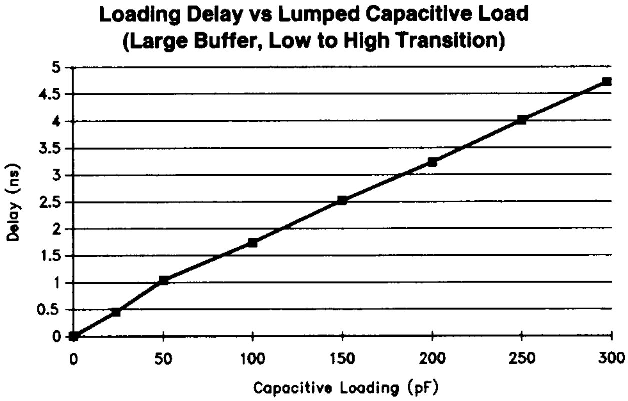
The Intel486™ DX CPU-Cache chip set AC Timing Specifications are all given at a 0 pF capacitive load. For this reason, each output must be derated according to the load being driven. Capacitive derating is not a precise method of determining a signal's delay, and must only be applied to signals that interface to the Memory Bus (t_{32} to t_{130}). A more accurate determination of delay and signal quality may be made by modeling the buffer using the technique described in the previous section.

The following graphs represent the lumped-load capacitive derating curves for the 82495DX and 82490DX buffers used to drive the memory bus. The large buffers are used for the signals CDTS#, NENE#, SMLN#, MTHIT#, MHITM#, and SNPBSY#, and when MALDRV and MDLDRV are configured low for the signals MCFA, MSET, MTAG and MDATA. The small (normal) buffers are used with all other buffers and with MCFA, MSET, MTAG, and MDATA when MALDRV and MDLDRV are configured high. Note that for both buffers, the capacitive derating for a low-to-high transition is different from a high-to-low transition.

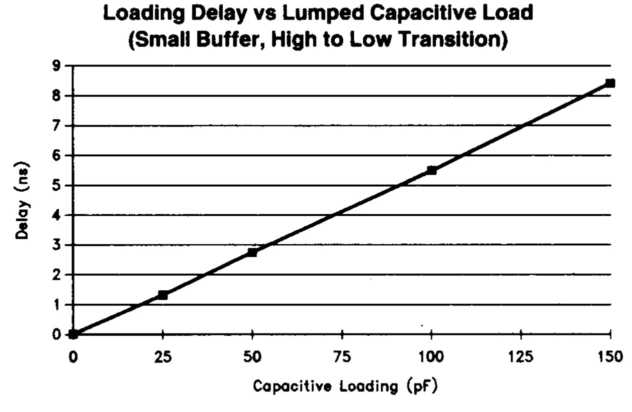
Small buffers provide the best signal quality for capacitive loads of about 50 pF or less. Large buffers provide the best quality for loads between 100 pF and 150 pF. The Intel486 DX CPU/82495DX/82490DX chip set component buffer model provides detailed information about buffer performance in specific environments.



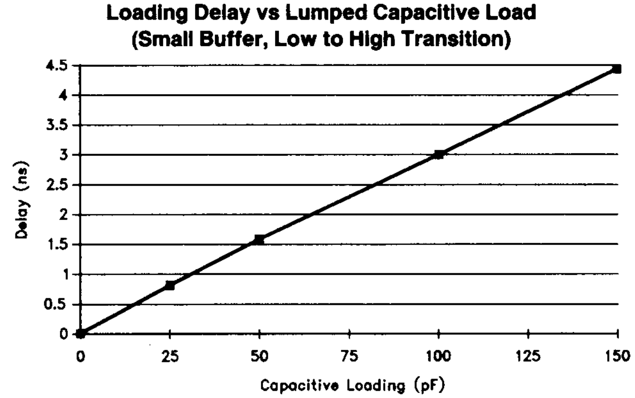
241084-22



241084-23



241084-24



241084-25

5.0 THERMAL DATA

The 82495DX and 82490DX are specified for operation when T_C (case temperature) are within the range of 0°C–75°C. T_C may be measured in any environment to determine whether the components are within the specified operating range. The case temperature should be measured at the center of the top surface, opposite the pins.

The ambient temperature (T_A) is guaranteed as long as T_C is not violated. The ambient temperature can be calculated from θ_{JC} and θ_{JA} using the following equations:

$$T_J = T_C + P \bullet \theta_{JC}$$

$$T_A = T_J + P \bullet \theta_{JA}$$

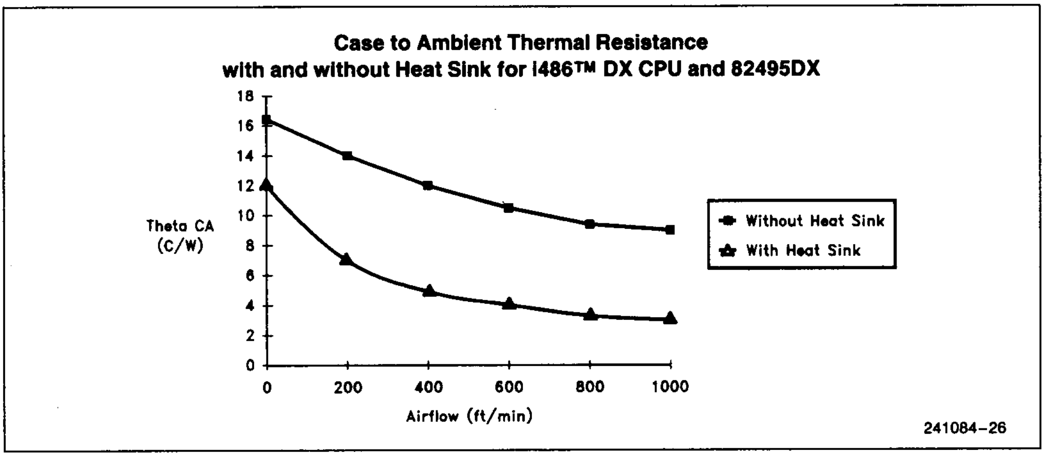
$$T_C = T_A + P \bullet (\theta_{JA} - \theta_{JC})$$

This is true where T_J, T_A and T_C = junction, ambient and case temperature, respectively, and where θ_{JC} and θ_{JA} = junction-to-case and junction-to-ambient thermal resistance, respectively. P = maximum power consumption.

The Intel486 DX CPU and 82495DX have similar package characteristics and thus similar thermal characteristics. The heat sink referenced for all parts is a unidirectional heat sink, 0.350″ high, 40 MIL fin width, and 155 MIL center-to-center fin spacing.

i486™ DX CPU and 82495DX

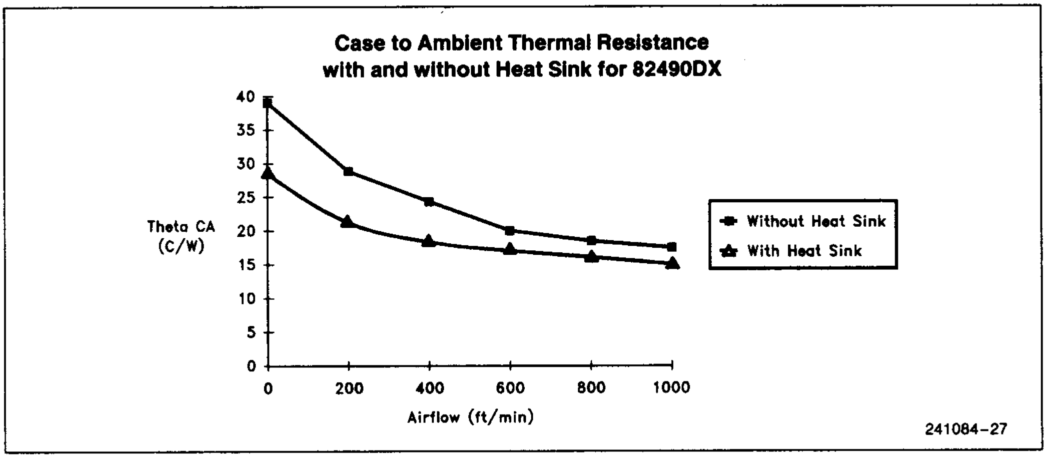
θ_{JC} (C/W) = 2.0 without heat sink
2.5 with heat sink



241084-26

82490DX

θ_{JC} (C/W) = 7.5 without heat sink
8.0 with heat sink



241084-27

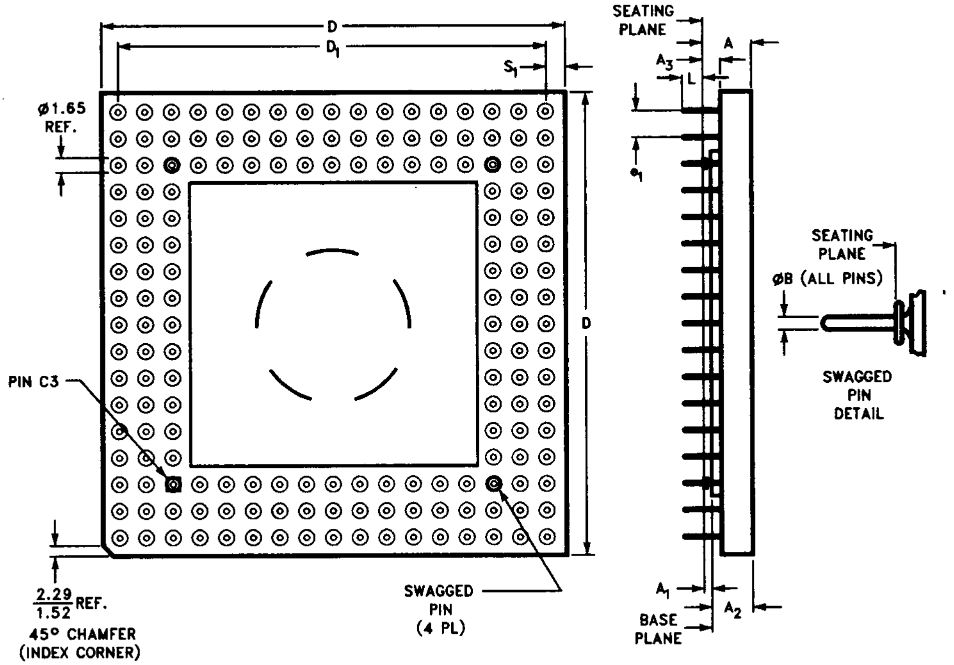
6.0 MECHANICAL DATA

Letter or Symbol	Description of Dimensions
A	Distance from seating plane to highest point of body
A_1	Distance between seating plane and base plane (lid)
A_2	Distance from base plane to highest point of body
A_3	Distance from seating plane to bottom of body
B	Diameter of terminal lead pin
D	Largest overall package dimension of length
D_1	A body length dimension, outer lead center to outer lead center
e_1	Linear spacing between true lead position centerlines
L	Distance from seating plane to end of lead
S_1	Other body dimension, outer lead center to edge of body

NOTES:

1. Controlling dimension: millimeter.
2. Dimension "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by P.C. board hole size: 0.0415 inch–0.0430 inch.
4. Dimensions "B", "B_1" and "C" are nominal.
5. Details of Pin 1 identifier are optional.

Intel486™ DX Microprocessor


D
D1
S1
SEATING PLANE
A3
L
A
ø1.65 REF.
e1
D
PIN C3
SEATING PLANE
øB (ALL PINS)
SWAGGED PIN DETAIL
2.29/1.52 REF.
45° CHAMFER (INDEX CORNER)
SWAGGED PIN (4 PL)
A1
A2
BASE PLANE

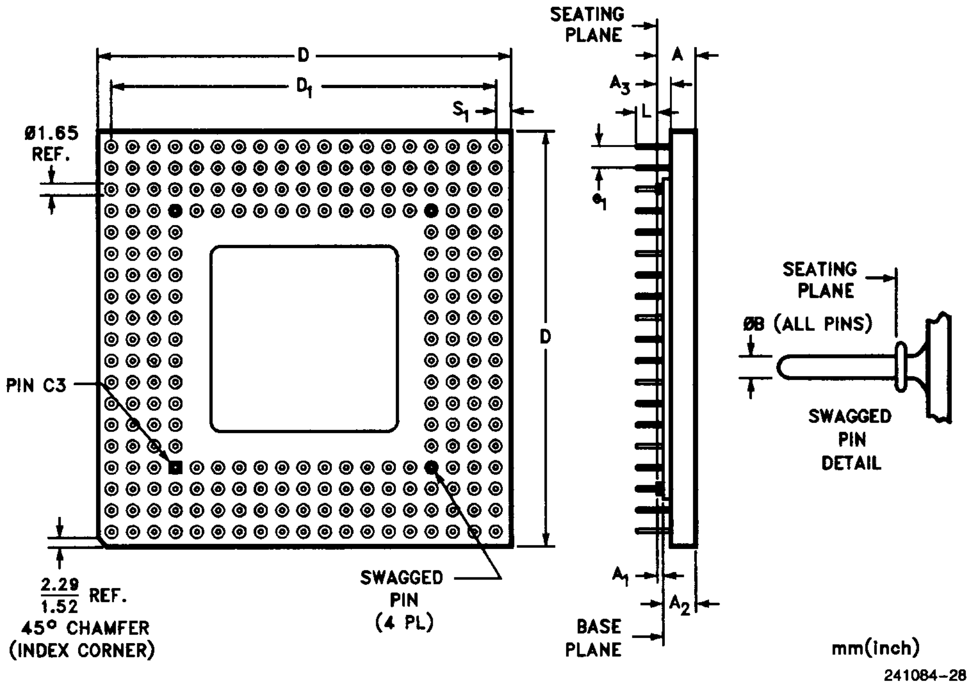
241084-38

Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A_1	0.64	1.14	Solid Lid	0.025	0.045	Solid Lid
A_2	2.8	3.5	Solid Lid	0.110	0.140	Solid Lid
A_3	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	44.07	44.83		1.735	1.765	
D_1	40.51	40.77		1.595	1.605	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	168			168		
S_1	1.52	2.54		0.060	0.100	
ISSUE	IWS Rev X 7/15/88					

Figure 6-1. Intel486™ DX CPU Mechanical Specifications

82495DX

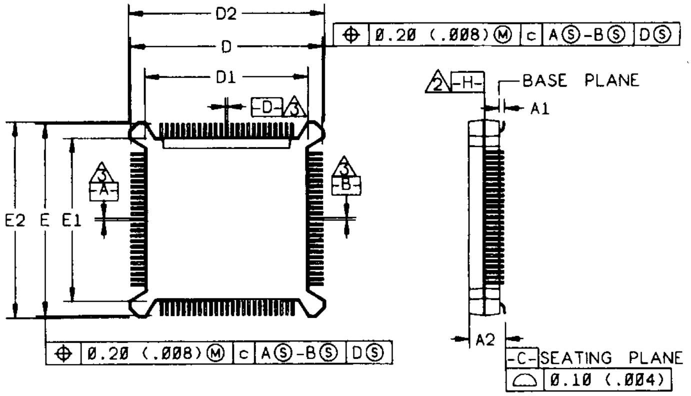
1.95″ Sq Ceramic Pin Grid Array Package


SEATING PLANE
A
A3
D
D1
S1
L
Ø1.65 REF.
e1
SEATING PLANE
ØB (ALL PINS)
SWAGGED PIN DETAIL
D
PIN C3
2.29
1.52 REF.
45° CHAMFER (INDEX CORNER)
SWAGGED PIN (4 PL)
A1
A2
BASE PLANE
mm(inch)
241084-28

Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A_1	0.64	1.14	Solid Lid	0.025	0.045	Solid Lid
A_2	0.23	0.30	Solid Lid	0.110	0.140	Solid Lid
A_3	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	49.53	50.17		1.950	1.975	
D_1	45.59	45.85		1.795	1.805	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	240	280		240	280	
S_1	1.52	2.54		0.060	0.100	
ISSUE	IWS 9/90					

Figure 6-2. 82495DX Mechanical Specifications

82490DX


D2
D
D1
⌖ Ø.20 (.008) Ⓜ c A Ⓢ - B Ⓢ D Ⓢ
-D- 3
2 -H-
BASE PLANE
A1
3 -A-
3 -B-
E2
E
E1
⌖ Ø.20 (.008) Ⓜ c A Ⓢ - B Ⓢ D Ⓢ
A2
-C- SEATING PLANE
Ø.10 (.004)

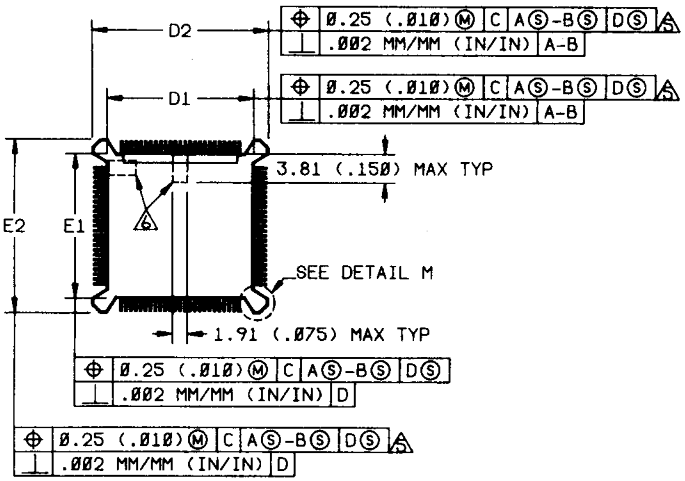
mm (inch)

241084-29

Plastic Quad Flatpack (PQFP) 0.025 In. (0.635 mm) Pitch					
Symbol	**Description**	**Min (mm)**	**Max (mm)**	**Min (in.)**	**Max (in.)**
N	Leadcount	84		84	
A	Package Height	4.06	4.57	0.160	0.180
A1	Standoff	0.51	1.02	0.020	0.040
D, E	Terminal Dimension	19.56	20.07	0.770	0.790
D1, E1	Package Body	16.43	16.59	0.647	0.653
D2, E2	Bumper Distance	20.24	20.39	0.797	0.803
D3, E3	Lead Dimension	12.70 REF		0.500 REF	
D4, E4	Foot Radius Location	18.36	18.71	0.723	0.737
L1	Foot Length	0.51	0.76	0.020	0.030
Issue					

Figure 6-3. 82490DX Mechanical Specifications

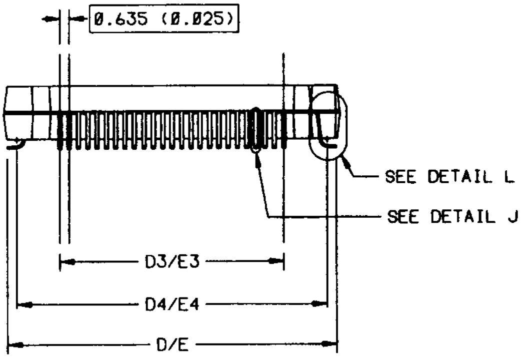
Molded Details


D2
D1
Ø.25 (.010) Ⓜ C A Ⓢ -B Ⓢ D Ⓢ
.002 MM/MM (IN/IN) A-B
3.81 (.150) MAX TYP
E2
E1
6
SEE DETAIL M
1.91 (.075) MAX TYP
Ø.25 (.010) Ⓜ C A Ⓢ -B Ⓢ D Ⓢ
.002 MM/MM (IN/IN) D
5

mm (inch)

241084-30

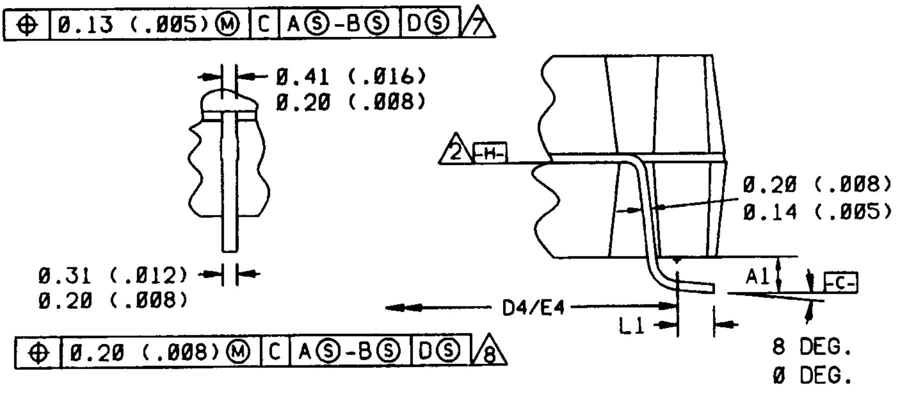
Terminal Details


0.635 (0.025)
SEE DETAIL L
SEE DETAIL J
D3/E3
D4/E4
D/E

mm (inch)

241084-31

Typical Lead

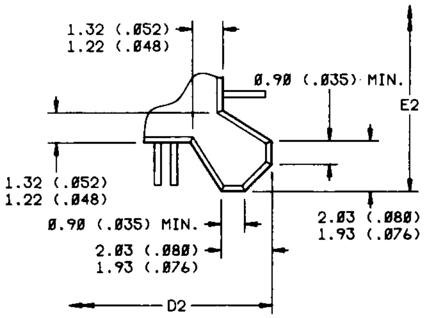

⌖ 0.13 (.005) Ⓜ C A Ⓢ -B Ⓢ D Ⓢ 7
0.41 (.016)
0.20 (.008)
0.31 (.012)
0.20 (.008)
⌖ 0.20 (.008) Ⓜ C A Ⓢ -B Ⓢ D Ⓢ 8
2 -H-
0.20 (.008)
0.14 (.005)
A1
-C-
D4/E4
L1
8 DEG.
0 DEG.

mm (inch)

241084-32

Detail J **Detail L**

Detail M


1.32 (.052)
1.22 (.048)
0.90 (.035) MIN.
E2
1.32 (.052)
1.22 (.048)
0.90 (.035) MIN.
2.03 (.080)
1.93 (.076)
2.03 (.080)
1.93 (.076)
D2

241084-33

mm (inch)