Errata in Intel386™ EX Embedded Microprocessor User's Manual

This document contains all known errata in the *Intel386™ EX Embedded Microprocessor User's Manual* (Order Number 272485-001). It contains a chapter-by-chapter description of each item. Appended to the document are the corrected pages.

HOW TO OBTAIN EMBEDDED MICROPROCESSOR ERRATA

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ERRATA SUMMARY

Thursday, June 1, 1995 - Revision 1.1

Chapter 4 - System Register Organization

Table 4-2 in the previous errata contained one error. Line 9 in the example was incorrect:

WAS: `OUT 23H, AX`

IS `OUT 22H, AX`

Thursday, April 06, 1995 - Revision 1.0

Chapter 3 Core Overview

In section 3.1.7 on page 3-9 the table's description for address 03FEFC was incorrect:

WAS: 03FEFC — SMM revision identifier (01000H)

IS: 03FEFC — SMM revision identifier (10000H)

Chapter 4 - System Register Organization

In section 4.1, Overview (page 4-2) sub-bullet contains typo error - "8257A" should be "8237A":

WAS: — DMA unit registers (8257A-compatible and enhanced function registers)

IS: — DMA unit registers (8237A-compatible and enhanced function registers)

Figure 4-4, Programming the ESE Bit (page 4-10) had several modifications; see attachment page.

In Table 4-2, Peripheral Register Addresses (page 4-18) the Reset Value for Expanded Address F092H was incorrectly shown as 00H. The correct reset value is 0EH.

Chapter 5 - Device Configuration

Figure 5-13, Port 92 Configuration Register (page 5-19) contains two errors:

Reset State is incorrectly shown as 00H. The correct value is 0EH.

Bit 1 in the register is shown as A20. The correct value is A20G. (was shown correctly in the bit description table).

Chapter 7 - Bus Interface Unit

Some figures in this chapter that contain bus cycle waveforms are incorrect. Refer to the latest *Intel386 EX™ Embedded Microprocessor* Datasheet (#272420) and the datasheet's errata document for accurate timing diagrams and bus cycle waveforms.

The 'Processor Clock' used in this chapter is the 'PH2' clock (Phase 2) described in the datasheet and other documents.

Figures 7-4 (page 7-11) and 7-5 (page 7-13) depict non-pipelined bus cycles and **not** pipelined cycles.

In Section 7.3.7, BS8 Cycle (page 7-27) the second and third bullets incorrectly referenced "phase two of T2"; these have been changed to "...at the end of the last T2 (when READY# is sampled active)".

Chapter 8 - Interrupt Control Unit

External Cascading of 8259 Interrupt Controllers requires an external state-machine to satisfy the timing requirements of the 8259, particularly the INTA signal. This state-machine needs to monitor the control signals of the processor to generate the INTA signal.

In Section 8.4.2, Interrupt Detection (page 8-27) text contains three references to T_{IRLH}; these now correctly refer to T_{JLJH}.

Chapter 9 - Timer/Counter Unit

Nine pages missing from the end of the chapter: pages 9-26 through 9-35.

Chapter 10 - Watchdog Timer Unit

In Figure 10-2, WDT Counter Value Registers (WDTCNTH and WDTCNTL) (page 10-5) the WDTCNTH Reset State is shown as 0000H, which is correct for the A-step part. The correct value for later steppings is FFFFH.

In the WDTCNTL Bit Description table, the Function field contains a typo: WDTDNTL should be WDTCNTL.

Chapter 14 - Chip-Select Unit

In Figure 14-7, Chip-select Low Address Register (page 14-14) the Reset State for UCSADL was shown incorrectly as FFEFH; now correctly shows FF6FH.

Figures 14-6, 14-7, 14-8, 14-9 (pages 14-13 to 14-16) read write status changed from "write only" to "read/write."

Chapter 16 - DMA Controller

In Section 16.2.7.2, Block Data-transfer Mode (page 16-13) the first paragraph, third sentence should read:

> "The block mode, unlike the single mode, does not give up bus control during a buffer transfer. "

It now correctly states:

> "The block mode, unlike the single mode, only gives up control of the bus for DRAM refresh cycles."

The second paragraph, third sentence incorrectly stated:

> "This is impossible with block data-transfer mode, because the channel does not relinquish bus control at any time during the buffer transfer."

It now correctly states:

> "This is impossible with block data-transfer mode, because the channel will only relinquish control of the bus for DRAM refresh cycles during the buffer transfer."

Appendix A - Signal Descriptions

In Table A-2 on page A-2, BS8# Type incorrectly shown as "O"; now correctly shows "I".

On page A-5, READY# Type incorrectly shown as "I"; now correctly shows "I/O". SMI# Type incorrectly shown as "I"; now correctly shown as "ST".

On page A-6, TRST# Type incorrectly shown as "I"; now correctly shown as "ST".

In the TCK description, the second sentence is removed. WAS:

> Test Clock Input: Provides the clock input for the test-logic unit. An external signal must provide a maximum input frequency of one-half the CLK2 input frequency. TCK is driven by the test-logic unit's control circuitry.

It now correctly states:

> Test Clock Input: Provides the clock input for the test-logic unit. TCK is driven by the test-logic unit's control circuitry.

In Table A-2, WR# pin description (page A-7) added as the last table entry of table A-2, as follows:

WR#	O	Write Enable: Indicates that the current bus cycle is a write cycle.	—

In table A-4, Pin States After Reset and During Idle, Powerdown and Hold (page A-8) the pin state during Hold for the following pins should be changed as follows:

Pin	State During Hold WAS:	State During Hold IS:
CS6#/REFRESH#	Q	1
DACK0#/CS5#	1/Q	Q/1
RD#	Z	1
SMIACT#	X	1
UCS#	Q	1
WR#	Z	1
P2.4:0/CS4:0#	X	Q/1

Hex Address	Name	Description
03FFFC	CR0	Control flags that affect the processor state
03FFF8	CR3	Page directory base register
03FFF4	EFLGS	General condition and control flags
03FFF0	EIP	Instruction pointer
03FFEC	EDI	Destination index
03FFE8	ESI	Source index
03FFE4	EBP	Base pointer
03FFE0	ESP	Stack pointer
03FFDC	EBX	General register
03FFC8	EDX	General register
03FFD4	ECX	General register
03FFD0	EAX	General register
03FFCC	DR6	Debug register; contains status at exception
03FFC8	DR7	Debug register; controls breakpoints
03FFC4	TR	Task register; used to access current task descriptor
03FFC0	LDTR	Local descriptor table pointer
03FFBC	GS	General-purpose segment register
03FFB8	FS	General-purpose segment register
03FFB4	DS	Data segment register
03FFB0	SS	Stack segment register
03FFAC	CS	Code segment register
03FFA8	ES	General-purpose segment register
03FFA7–03FF04	—	Reserved
03FF02	—	Halt restart slot
03FF00	—	I/O trap restart slot
03FEFC	—	SMM revision identifier (10000H)
03FEFB–03FE00	—	Reserved

The programmer should not modify the contents of this area in SMRAM space directly. SMRAM space is reserved for CPU access only and is intended to be used only when the processor is in SMM.

ERRATA (3/28/95)
In the table entry for HEX Address 03FEFC, the description incorrectly showed 01000H; it now correctly shows 10000H.

4.1 OVERVIEW

The Intel386 EX processor has register resources in the following categories:

- Intel386 processor core architecture registers
  - — general purpose registers
  - — segment registers
  - — instruction pointer and flags
  - — control registers
  - — system address registers (protected mode)
  - — debug registers
  - — test registers
- Intel386 EX processor peripheral registers
  - — configuration space control registers
  - — interrupt control unit registers
  - — timer/counter unit registers
  - — DMA unit registers (8237A-compatible and enhanced function registers)
  - — asynchronous serial I/O (SIO) registers
  - — clock generation selector registers
  - — power management control registers
  - — chip-select unit control registers
  - — refresh control unit registers
  - — watchdog timer control registers
  - — synchronous serial I/O control registers
  - — parallel I/O port control registers

ERRATA (3/28/95)
Sub-bullet for DMA unit registers incorrectly stated “8257A-compatible” ; now correctly states “8237A-compatible”.

4.1.1 Intel386™ Processor Core Architecture Registers

These registers are a superset of the 8086 and 80286 processor registers. All 16-bit 8086 and 80286 registers are contained within the 32-bit Intel386 processor core registers. A detailed description of the Intel386 architecture base registers can be found in the *Intel386™ SX Microprocessor Programmer's Reference Manual.*

ERRATA (3/28/95)
Figure 4-4, Programming the ESE Bit, has been substantially rewritten.

```
;;disable interrupts
     CLI
; Enable expanded I/O space of Intel386(tm) EX processor
; for peripheral initialization.
     MOV AX, 08000H      ; Enable expanded I/O space
     OUT 23H, AL         ; and unlock the re-map bits
     XCHG AL, AH
     OUT 22H, AL
     OUT 22H, AX
;; at this point PC/AT peripherals can be mapped out or in
;; other peripherals can be accessed and manipulated
;; For example,
;; Map out the on-chip DMA channels from the DOS I/O space (slot 0)
     MOV AL, 04H
     OUT 22H, AL
; Disables expanded I/O space
     MOV AL, 00H
     OUT 23H, AL
;; Re-enable Interrupts
     STI
```

ERRATA (6/1/95)
Previous errata incorrectly showed
OUT 23H, AX
Now correctly shows
OUT 22H, AX

Figure 4-4. Setting the ESE Bit

The REMAPCFG register is write-protected until the expanded I/O space is enabled. When the enabling write sequence is executed, it sets the ESE bit. A program can check this bit to see whether it has access to the expanded I/O space registers. Clearing the ESE bit disables the expanded I/O space. This again locks the REMAPCFG register and makes it read-only.

4.6 ADDRESSING MODES

Combinations of the value of the ESE bit and the individual remap bits in the REMAPCFG register yield four different peripheral addressing modes as far as I/O address decoding is concerned.

4.6.1 DOS-compatible Mode

DOS-compatible mode is achieved by clearing ESE and all the peripheral remap bits. In this mode, all PC/AT-compatible peripherals are mapped into the DOS I/O space. Only address lines A9–A0 are decoded for internal peripherals. Accesses to PC/AT-compatible peripherals are valid, while all other internal peripherals are inaccessible (see Figure 4-5).

This mode is useful for accessing the internal timer, interrupt controller, serial I/O ports, or DMA controller in a DOS-compatible environment.

ERRATA (3/28/95)
In the table entry for address F092H , the reset value incorrectly showed 00H; it now correctly shows 0EH.

Table 4-2. Peripheral Register Addresses (Sheet 3 of 6)

Expanded Address	PC/AT Address	High Byte	Low Byte	Reset Value
F08CH			Reserved	
F08DH			Reserved	
F08EH			Reserved	
F08FH			Reserved	
F098H			DMA0BYC2	00H
F099H			DMA1BYC2	00H
F09AH			Reserved	
F09BH			Reserved	
A20GATE and Fast CPU Reset				
F092H	0092H		PORT92	0EH
Slave Interrupt Controller				
F0A0H	00A0H		ICW1s/IRRs/ISRs/ OCW2s/OCW3s	XX
F0A1H	00A1H		ICW2s/ICW3s/ OCW1s/POLLs	XX
Chip-select Unit				
F400H		CS0SADL_HI	CS0ADL_LO	0000H
F402H		CS0SADH_HI	CS0ADH_LO	0000H
F404H		CS0MSKL_HI	CS0MSKL_LO	0000H
F406H		CS0MSKH_HI	CS0MSKH_LO	0000H
F408H		CS1SADL_HI	CS1ADL_LO	0000H
F40AH		CS1SADH_HI	CS1ADH_LO	0000H
F40CH		CS1MSKL_HI	CS1MSKL_LO	0000H
F40EH		CS1MSKH_HI	CS1MSKH_LO	0000H
F410H		CS2ADL_HI	CS2ADL_LO	0000H
F412H		CS2ADH_HI	CS2ADH_LO	0000H
F414H		CS2MSKL_HI	CS2MSKL_LO	0000H
F416H		CS2MSKH_HI	CS2MSKH_LO	0000H
F418H		CS3ADL_HI	CS3ADL_LO	0000H
F41AH		CS3ADH_HI	CS3ADH_LO	0000H
F41CH		CS3MSKL_HI	CS3MSKL_LO	0000H
F41EH		CS3MSKH_HI	CS3MSKH_LO	0000H
F420H		CS4ADL_HI	CS4ADL_LO	0000H

NOTE: Registers with the “High Byte” column shaded (darker shade) are byte-addressable only. LIghter shade indicates reserved areas.

Clearing bit 1 in the PORT92 register forces address line 20 to 0. This bit affects only addresses generated by the core. Addresses generated by the DMA and the refresh control unit are not affected by this bit.

Port 92 Configuration
PORT92
(read/write)

Expanded Addr: F092H
PC/AT Addr: 0092H
Reset State: 0EH

7							0
—	—	—	—	—	—	A20G	CPURST

Bit Number	Bit Mnemonic	Function
7–2	—	Reserved. These bits are undefined; for compatibility with future devices, do not modify these bits.
1	A20G	A20 Grounded: Setting this bit leaves core-generated addresses unmodified. Clearing this bit forces address line A20 to 0. This bit affects addresses generated only by the core. Addresses generated by the DMA and the Refresh Unit are not affected by this bit.
0	CPURST	CPU Reset: Setting this bit resets the core without resetting the peripherals. Clearing this bit has no effect.

Figure 5-13. Port 92 Configuration Register

ERRATA (3/28/95)
Figure 5-13 incorrectly showed Reset State as 00H; now correctly shows 0EH.
Register bit 1 incorrectly shown as A20, now correctly shows A20G.

7.3.7 BS8 Cycle

The BS8 cycle allows external logic to dynamically switch between an 8-bit data bus size and a 16-bit data bus size by using the BS8# pin. Figure 7-12 shows a word access to an 8-bit peripheral. Depending upon the current bus access width and address and the state of the BS8# pin, the processor will perform the following actions:

- If the current bus cycle is a byte write with BHE# active and BLE# inactive, the processor copies the upper eight bits of the data bus (D8–D15) to the lower eight bits of the data bus (D0–D7).
- If the current bus cycle is a word write with both BHE# and BLE# active and the processor samples the BS8# pin active at the end of the last T2 (when READY# is sampled active), the processor waits for the current bus to complete and then executes another write cycle with the upper eight bits of the data bus (D8–D15) copied to the lower eight bits of the data bus (D0–D7). The processor deactivates BLE# on the second cycle.
- If the current bus cycle is a word read with both BHE# and BLE# active and the processor samples the BS8# pin active at the end of the last T2 (when READY# is sampled active), the processor waits for the current bus cycle to complete and then executes another read cycle, with BLE# inactive, diverting the lower eight bits of the data bus (D0–D7) onto the upper eight bits of the data bus (D8–D15).
- If the current bus cycle is any byte access with BHE# inactive and BLE# active, the processor ignores the state of the BS8# pin.

The BS8 cycle generates additional bus cycles for read and write cycles only. For interrupt and halt/shutdown cycles, the accesses are byte wide and the BS8# pin is ignored. For a refresh cycle, the byte enables are both disabled and the BS8# pin is ignored.

NOTE

If a BS8 cycle requires an additional bus cycle, the processor retains the current address for the second cycle. Address pipelining **cannot** be used with BS8 cycles because address pipelining requires that the next address be generated on the bus before the end of the current bus cycle.

To utilize the dynamic 8-bit bus sizing, an external memory or I/O should connect to the lower eight bits of the data bus (D0–D7), use the BLE# as the zero address bit, and assert BS8# in T2 when the access is to the memory or I/O. The BS8# pin can also be controlled by the internal chip-select unit.

ERRATA (4/5/95)
In Section 7.3.7, BS8 Cycle (page 7-27) the second and third bullets incorrectly referenced "...phase two of T2"; these have been changed to "...at the end of the last T2 (when READY# is sampled active)".

SLAVE_IR7 = CAS2 • CAS1 • CAS0

EXTERNAL_REQUEST = SLAVE_IR1 + SLAVE_IR5 + SLAVE_IR6 + SLAVE_IR7

The state machine should generate an external INTA# signal when the INTA_BUS_CYCLE and the EXTERNAL_REQUEST conditions are met. Refer to the *82C59A CHMOS Programmable Interrupt Controller* data sheet (order number 231201) for the INTA# timing specifications.

EXT_INTA = INTA_BUS_CYCLE • EXTERNAL_REQUEST • $\overline{A2}$

8.4.2 Interrupt Detection

The processing of an interrupt begins with the assertion of an interrupt request on one of the IR signals. During system initialization, you can program the IR signals, as a group, to be either edge triggered or level sensitive.

Edge triggering means that the 82C59A will recognize a rising edge transition on an IR signal as an interrupt request. A device requesting service must maintain a high state on an IR signal until after the falling edge of the first INTA# pulse. You can reset the edge-detection circuit during initialization of the 82C59A or by deasserting the IR signal. To reset the edge-detection circuit properly, the interrupt source must hold the IR line low for a minimum time (T_{JLJH}). Unless it meets the T_{JLJH} specification, further interrupts will not be recognized from the interrupt source. Refer to the *82C59A CHMOS Programmable Interrupt Controller* data sheet (order number 231201) for the T_{JLJH} specification.

Level sensitive means that the 82C59A will recognize a high value on an IR line as an interrupt request. A device must maintain the high value until after the falling edge of the first INTA# pulse. Unlike an edge-triggered IR signal, a level-sensitive IR signal will continue to generate interrupts as long as it is asserted. To avoid continuous interrupts from the same source, a device must deassert a level-sensitive IR signal before the interrupt handler issues an end-of-interrupt command.

All of the internal peripherals interface with the 82C59As in edge-triggered mode. This is compatible with the PC/AT bus specification. Each source signal initiates an interrupt by making a low-to-high transition.

ERRATA (3/28/95)
In Section 8.4.2, text contains three references to T_{IRLH}; these now correctly refer to T_{JLJH}.

Timer Control (Control Word Format)
TMRCON

Expanded Addr: F043H
PC/AT Addr: 0043H
Reset State: 00H

7							0
SC1	SC0	RW1	RW0	M2	M1	M0	CNTFMT

Bit Number	Bit Mnemonic	Function
7–6	SC1:0	Select Counter: Use these bits to specify a particular counter. The selections you make for bits 5–0 define this counter's operation. 00 = counter 0 01 = counter 1 10 = counter 2 11 is not an option for TMRCON's control word format. Selecting 11 accesses TMRCON's read-back format, which is shown in Figure 9-30.
5–4	RW1:0	Read/Write Select: These bits select a read/write option for the counter specified by bits 7–6. 01 = read/write least-significant byte only 10 = read/write most-significant byte only 11 = read/write least-significant byte first, then most-significant byte 00 is not an option for TMRCON's control word format. Selecting 00 accesses TMRCON's counter-latch format, which is shown in Figure 9-28.
3–1	M2:0	Mode Select: These bits select an operating mode for the counter specified by bits 7–6. 000 = mode 0 001 = mode 1 X10 = mode 2 X11 = mode 3 100 = mode 4 101 = mode 5 X is a don't care.
0	CNTFMT	Count Format: This bit selects the count format for the counter specified by bits 7–6. 0 = binary (16 bits) 1 = binary coded decimal (4 decades)

NOTE: The read-back command has precedence over the counter-latch command. See TMRCON's read-back format (Figure 9-30) for the read-back function of bits 5–0.

Figure 9-26. Timer Control Register (Control Word Format)

9.3.3 Writing the Counters

Use the write format of a counter's timer *n* register (TMR*n*) to specify a counter's count. The count must conform to the write selection specified in the control word (least-significant byte only, most-significant byte only, or least-significant byte followed by the most-significant byte). You can write a new count to a counter without affecting the counter's programmed operating mode. New counts must also conform to the specified write selection.

Timer *n* (Write Format)
TMR*n* (*n* = 0–2)

Expanded Addr: F040H, F041H F042H
PC/AT Addr: 0040H, 0041H 0042H
Reset State: XX

7							0
CV7	CV6	CV5	CV4	CV3	CV2	CV1	CV0

Bit Number	Bit Mnemonic	Function
7–0	CV7:0	Count Value: Write a count value for the counter to these bits. When writing the counter's count value, follow the write selection specified in the counter's control word.

Figure 9-27. Timer *n* Register (Write Format)

Table 9-4 lists the minimum and maximum initial counts for each mode.

Table 9-4. Minimum and Maximum Initial Counts

Mode	Minimum Count	Maximum Count
0–1	1	0
2–3	2	0
4–5	1	0

NOTE: 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

9.3.4 Reading the Counter

To read the counter you can perform a simple read operation or send a latch command to the counter. TMRCON contains two formats that allow you to send latch commands to individual counters: the counter-latch and read-back format. The counter-latch command latches the count of a specific counter. The read-back command latches the count and/or status of one or more specified counters.

9.3.4.1 Simple Read

To perform a simple read operation, suspend the counter's operation (using the counter's GATE*n* signal), then read the counter's timer *n* register. You must disable the counter so that the count is not in the process of changing when it is read, giving an undefined result.

9.3.4.2 Counter-latch Command

Use the counter-latch format of TMRCON (Figure 9-28) to latch the count of a specific counter. A counter continues to run even after the count is latched. This allows reading the count without disturbing the count in progress.

Timer Control (Counter-latch Format)
TMRCON

Expanded Addr: F043H
PC/AT Addr: 0043H
Reset State: 00H

7							0
SC1	SC0	0	0	—	—	—	—

Bit Number	Bit Mnemonic	Function
7–6	SC1:0	Select Counter: These bits specify the counter that will be issued the counter-latch command. 00 = counter 0 01 = counter 1 10 = counter 2 11 is not an option for TMRCON's counter-latch format. Selecting 11 accesses TMRCON's read-back format, which is shown in Figure 9-30.
5–4	—	Write zeros to these bits to issue a counter-latch command to the counter specified by bits 7–6. 01, 10, and 11 are not valid options for TMRCON's counter-latch format.
3–0	—	Reserved; for compatibility with future devices, write zeros to these bits.

NOTE: Bits 5–0 serve another function when you select the read-back command (SC1:0 = 11). See Figure 9-30 for the read-back bit functions.

Figure 9-28. Timer Control Register (Counter-latch Format)

When a counter receives a counter-latch command, it latches the count. This count remains latched until you either read the count or reconfigure the counter. If you send multiple counter-latch commands without reading the counter, only the first counter-latch command latches the count.

After issuing a counter-latch command, you can read the counter's TMR*n* register. When reading the counter's TMR*n* register you must follow the counter's programmed read selection (least-significant byte only, most-significant byte only, or least-significant byte followed by the most-significant byte). If the counter is programmed for two-byte counts, you must read two bytes.You need not read the two bytes consecutively; you may insert read, write, or programming operations between the byte reads.

You can interleave reads and writes of the same counter; for example, if the counter is programmed for the two-byte read/write selection, the following sequence is valid.

1. Read least-significant byte.
2. Write new least-significant byte.
3. Read most-significant byte.
4. Write new most-significant byte.

Timer *n* (Read Format)
TMR*n* (*n* = 0–2)

Expanded Addr:	F040H, F041H F042H
PC/AT Addr:	0040H, 0041H 0042H
Reset State:	XX

7							0
CV7	CV6	CV5	CV4	CV3	CV2	CV1	CV0

Bit Number	Bit Mnemonic	Function
7–0	CV7:0	Count Value: These bits contain the counter's count value. When reading the counter's count value, follow the read selection specified in the counter's control word.

Figure 9-29. Timer *n* Register (Read Format)

9.3.4.3 Read-back Command

Use the read-back format of TMRCON (Figure 9-30) to latch the count and/or status of one or more counters. Latch a counter's status to check its programmed operating mode, count format, and read/write selection and to determine whether the latest count written to it has been loaded.

Timer Control (Read-back Format)
TMRCON

Expanded Addr: F043H
PC/AT Addr: 0043H
Reset State: 00H

7							0
1	1	COUNT#	STAT#	CNT2	CNT1	CNT0	—

Bit Number	Bit Mnemonic	Function
7–6	—	Write ones to these bits to select the read-back command. 00, 01, and 10 are not valid options for TMRCON's read-back format.
5	COUNT#	Count Latch: Clearing this bit latches the count of each selected counter. Use bits 3–1 to select one or more of the counters.
4	STAT#	Status Latch: Clearing this bit latches the status of each selected counter. Use bits 3–1 to select one or more of the counters.
3	CNT2	Counter 2 Select: When this bit is set, the actions specified by bits 5 and 4 affect counter 2. Otherwise, the actions do not affect counter 2.
2	CNT1	Counter 1 Select: When this bit is set, the actions specified by bits 5 and 4 affect counter 1. Otherwise, the actions do not affect counter 1.
1	CNT0	Counter 0 Select: When this bit is set, the actions specified by bits 5 and 4 affect counter 0. Otherwise, the actions do not affect counter 0.
0	—	Reserved. This bit is undefined.

Figure 9-30. Timer Control Register (Read-back Format)

The read-back command can latch the count and status of multiple counters. This single command is functionally equivalent to several counter-latch commands, one for each counter latched. Each counter's latched count and status is held until it is read or until you reconfigure the counter. A counter's latched count or status is automatically unlatched when read, but other counters' latched values remain latched until they are read.

After latching a counter's status and count with a read-back command, reading TMR*n* accesses its status format (Figure 9-31). Reading TMR*n* again accesses its read format. If both the count and status of a counter are latched, the first read of TMR*n* indicates the counter's status and the next one or two reads (depending on the counter's read selection) indicate the counter's count. If only the count of a counter is latched, then the first one or two reads of TMR*n* indicate the counter's count. If the counter is programmed for the two-byte read selection, you must read two bytes.

Timer *n* (Status Format)
TMR*n* (*n* = 0–2)

Expanded Addr: F040H, F041H F042H
PC/AT Addr: 0040H, 0041H 0042H
Reset State: XX

7							0
OUTPUT	NULCNT	RW1	RW0	M2	M1	M0	CNTFMT

Bit Number	Bit Mnemonic	Function
7	OUTPUT	Output Status: This bit indicates the current state of the counter's output signal. 1 = OUT*n* is high 0 = OUT*n* is low
6	NULCNT	Count Status: This bit indicates whether the latest count written to the counter has been loaded. Some modes require a gate-trigger before the counter loads new count values. 1 = a count has been written to the counter but has not yet been loaded 0 = the latest count written to the counter has been loaded
5	RW1:0	Read/Write Select Status: These bits indicate the counter's programmed read/write selection. 01 = read/write least-significant byte only 10 = read/write most-significant byte only 11 = read/write least-significant byte first, then most-significant byte
4	M2:0	Mode Status: These bits indicate the counter's programmed operating mode. 000 = mode 0 001 = mode 1 X10 = mode 2 X11 = mode 3 100 = mode 4 101 = mode 5 X is a don't care.
0	CNTFMT	Counter Format Status: This bit indicates the counter's programmed count format. 0 = binary (16 bits) 1 = binary coded decimal (4 decades)

Figure 9-31. Timer *n* Register (Status Format)

With the read-back command, you can simultaneously latch both the count and status of one or more counters. This is functionally the same as issuing two separate read-back commands. In this case, the first read operation of that counter returns the latched status, regardless of which was latched first. The next one or two reads (depending on the counter's read selection) returns the latched count. Subsequent reads return unlatched count.

When a counter receives multiple read-back commands, it ignores all but the first command; the count/status that the CPU reads is the count/status latched from the first read-back command (see Table 9-5).

Table 9-5. Results of Multiple Read-back Commands Without Reads

Command Sequence	Read-back Command	Command Result
1	Latch counter 0's count and status.	Counter 0's count and status latched.
2	Latch counter 1's status.	Counter 1's status latched.
3	Latch counter 2 and 1's status.	Counter 2's status latched; counter 1's status command ignored because command 2 already latched its status.
4	Latch counter 2's count.	Counter 2's count latched.
5	Latch counter 1's count and status.	Counter 1's count latched; counter 1's status command ignored because command 2 already latched its status.
6	Latch counter 0's count.	Counter 0's count command ignored because command 1 already latched its count.

9.3.5 Programming Considerations

Consider the following when programming the TCU.

- The 16-bit counters are read and written a byte at a time. The control word format of TMRCON selects whether you read or write the least-significant byte only, most-significant byte only, or least-significant byte then most-significant byte (this is called the counter's read/write selection). You must read and write the counters according to their programmed read/write selections.
- When you program a counter for the two-byte read or write selection, you must read or write both bytes. If you're using more than one subroutine to read or write a counter, make sure that each subroutine reads or writes both bytes before transferring control.
- You can program the counters for either an internal or external clock source. The internal source is a prescaled value of the processor's clock and is affected by the processor's powerdown and idle modes. Because an external source is provided off-chip, it is not affected by the processor's powerdown and idle modes. "Controlling Power Management Modes" on page 6-8 describes the processor's powerdown and idle modes.

10.2 PROGRAMMING THE WDT

Each WDT operating mode requires different programming, but the modes use common registers. In all operating modes, software can read the count registers, WDTCNTH and WDTCNTL (Figure 10-2), to determine the current down-counter value and can read the status register, WDTSTATUS (Figure 10-3), to determine the WDT mode. Bus monitor mode requires a write to WDTSTATUS. All operating modes use the reload registers, WDTRLDH and WDTRLDL (Figure 10-4). This section describes the registers, then explains how to enable and use each mode.

WDT Counter Value (High)
WDTCNTH
(read only)

Expanded Addr: F4C4H
ISA Addr: —
Reset State: 0000H (A-step only)
FFFFH (all others)

15							8
WC31	WC30	WC29	WC28	WC27	WC26	WC25	WC24
7							**0**
WC23	WC22	WC21	WC20	WC19	WC18	WC17	WC16

WDT Counter Value (Low)
WDTCNTL
(read only)

Expanded Addr: F4C6H
ISA Addr: —
Reset State: FFFFH

15							8
WC15	WC14	WC13	WC12	WC11	WC10	WC9	WC8
7							**0**
WC7	WC6	WC5	WC4	WC3	WC2	WC1	WC0

Bit Number	Bit Mnemonic	Function
High 15–0	WC31:16	WDT Counter Value High Word and Low Word: Read the high word of the counter value from WDTCNTH and the low word from WDTCNTL.
Low 15–0	WC15:0	

Figure 10-2. WDT Counter Value Registers (WDTCNTH and WDTCNTL)

ERRATA (3/28/95)
In Figure 10-2, The Reset State 0000H is for A-step devices only.
Now includes FFFFH, which is the reset state for all later steppings.
In the WDTCNTL “Function” description, WDTCNTL was incorrectly shown as WDTDNTL.

14.3.3 Chip-select Address Registers

Write a channel's 15-bit address to the chip-select address registers. These bits are masked by the channel's 15-bit mask. During bus cycles, the CSU compares the channel's address to the upper 15 memory or I/O address bits. A match indicates that the processor is accessing the channel's address block. Whether the CSU activates the channel depends on the values of the channel's SMM address and mask bits. These bits determine whether or not the channel is activated when the processor is operating in SMM.

Chip-select High Address
CS*n*ADH (*n* = 0–6), **UCSADH**
(read/write)

Expanded Addr: F402H, F40AH
F412H, F41AH
F422H, F42AH
F432H, F43AH
PC/AT Addr: —
Reset State: 0000H (CS*n*ADH)
FFFFH (UCSADH)

15							8
—	—	—	—	—	—	CA15	CA14
7							**0**
CA13	CA12	CA11	CA10	CA9	CA8	CA7	CA6

Bit Number	Bit Mnemonic	Function
15–10	—	Reserved; for compatibility with future devices, write zeros to these bits.
9–0	CA15:6	Chip-select Channel Address Upper Bits: Defines the upper 10 bits of the channel's 15-bit address. The address bits CA15:6 and the mask bits CM15:6 form a masked address that is compared to memory address bits A25:16 or I/O address bits A15:6.

Figure 14-6. Chip-select High Address Register (CS*n*ADH, UCSADH)

ERRATA (3/28/95)
In Chapter 14, Figures 14-6, 14-7, 14-8, 14-9 read write status changed from "write only" to "read/write."

ERRATA (3/28/95)
In Figure 14-7, the Reset State for UCSADL was shown incorrectly as FFEFH; now correctly shows FF6FH.

Chip-select Low Address
CS*n*ADL (*n* = 0–6), **UCSADL**
(read/write)

Expanded Addr: F400H, F408H
F410H, F418H
F420H, F428H
F430H, F438H
PC/AT Addr: —
Reset State: 0000H (CS*n*ADL)
FF6FH (UCSADL)

15							8
CA5	CA4	CA3	CA2	CA1	CASMM	BS16	MEM
7							**0**
RDY	—	—	WS4	WS3	WS2	WS1	WS0

Bit Number	Bit Mnemonic	Function
15–11	CA5:1	Chip-select Address Value Lower Bits: Defines the lower 5 bits of the channel's 15-bit address. The address bits CA5:1 and the mask bits CM5:1 form a masked address that is compared to memory address bits A15:11 or I/O address bits A5:1.
10	CASMM	SMM Address Bit: If this bit is set (and unmasked), the CSU activates the chip-select channel only while the processor is in SMM. Otherwise, the CSU activates the channel only when processor is operating in a mode other than SMM. Setting the SMM mask bit in the channel's mask low register masks this bit. When this bit is masked, an address match activates the chip-select, regardless of whether the processor is in SMM.
9	BS16	Bus Size 16-bit: When this bit is clear, all bus cycles to the channel's address block are byte-wide. When this bit is set, bus cycles are 16 bits unless the bus size control pin (BS8#) is asserted.
8	MEM	Bus Cycle Type: Setting this bit configures the channel for memory addresses. Clearing this bit configures the channel for an I/O addresses.
7	RDY	Bus Ready Enable: Setting this bit requires that bus READY be active to complete a bus cycle. Bus READY is ignored when this bit is cleared. This bit must be set to extend wait states beyond the number determined by WS4:0.
6–5	—	Reserved; for compatibility with future devices, write zeros to these bits.
4–0	WS4:0	Wait State Value: WS4:0 defines the minimum number of wait states inserted into the bus cycle. A zero value means no wait states.

Figure 14-7. Chip-select Low Address Register (CS*n*ADL, UCSADL)

ERRATA (3/28/95)
In Chapter 14, Figures 14-6, 14-7, 14-8, 14-9 read write status changed from "write only" to "read/write."

14.3.4 Chip-select Mask Registers

Write a channel's 15-bit mask to the chip-select mask registers. Use the chip-select low mask register to enable the channel and to mask the channel's SMM address bit. When the channel's SMM address bit is masked, the CSU activates the channel regardless of whether the channel is operating in SMM.

Chip-select High Mask
CS*n*MSKH (*n* = 0–6), **UCSMSKH**
(read/write)

Expanded Addr: F406H, F40EH
F416H, F41EH
F426H, F42EH
F436H, F43EH
PC/AT Addr: —
Reset State: 0000H (CS*n*MSKH)
FFFFH (UCSMSKH)

15						8	
—	—	—	—	—	—	CM15	CM14
7							**0**
CM13	CM12	CM11	CM10	CM9	CM8	CM7	CM6

Bit Number	Bit Mnemonic	Function
15–10	—	Reserved; for compatibility with future devices, write zeros to these bits.
9–0	CM15:6	Mask Value Upper Bits: Defines the upper 10 bits of the channel's 15-bit mask. The mask bits CM15:6 and the address bits CA15:6 form a masked address that is compared to memory address bits A25:16 or I/O address bits A15:6.

Figure 14-8. Chip-select High Mask Registers (CS*n*MSKH, UCSMSKH)

ERRATA (3/28/95)
In Chapter 14, Figures 14-6, 14-7, 14-8, 14-9 read write status changed from "write only" to "read/write."

ERRATA (3/28/95)
In Chapter 14, Figures 14-6, 14-7, 14-8, 14-9 read write status changed from “write only” to “read/write.”

Chip-select Low Mask
CS*n*MSKL (*n* = 0–6), **UCSMSKL**
(read/write)

Expanded Addr: F404H, F40CH
F414H, F41CH
F424H, F42CH
F434H, F43CH
PC/AT Addr: —
Reset State: 0000H (CS*n*MSKL)
FFFFH (UCSMSKL)

15							8
CM5	CM4	CM3	CM2	CM1	CMSMM	—	—
7							**0**
—	—	—	—	—	—	—	CSEN

Bit Number	Bit Mnemonic	Function
15–11	CM5:1	Chip-select Mask Value Lower Bits: Defines the lower 5 bits of the channel’s 15-bit mask. The mask bits CM5:1 and the address bits CA5:1 form a masked address that is compared to memory address bits A15:11 or I/O address bits A5:1.
10	CMSMM	SMM Mask Bit: Setting this bit masks the SMM address bit in the channel’s chip-select address low register. When the SMM address bit is masked, an address match activates the chip-select, regardless of whether the processor is in SMM.
9–1	—	Reserved; for compatibility with future devices, write zeros to these bits.
0	CSEN	Chip-select Enable: Setting this bit enables the chip-select channel. Clearing this bit disables the chip-select channel.

Figure 14-9. Chip-select Low Mask Registers (CS*n*MSKL, UCSMSKL)

14.3.5 Programming Considerations

When programming the CSU, consider the following.

- A chip-select channel is enabled by setting bit 0 of its chip-select low mask register and connecting its output signal to the package pin by clearing the appropriate pin or port 2 configuration register bit. The pin and port 2 configuration registers are shown in Figures 14-4 and 14-5.
- The minimum address block for memory address-configured channels is 2 Kbytes and for I/O address-configured channels is 2 bytes. The size of these address blocks can be increased by multiples of 2 Kbytes for memory addresses and by multiples of 2 bytes for I/O addresses.
- A channel’s address block of size *n* will always start on an *n* address boundary.

16.2.7.2 Block Data-transfer Mode

In block data-transfer mode, a channel request initiates a buffer transfer. The channel gains bus control, then transfers the entire buffer of data. The block mode, unlike the single mode, only gives up control of the bus for DRAM refresh cycles. As with single mode, the channel's buffer-transfer mode determines whether the channel becomes idle or is reprogrammed after the buffer transfer completes or is terminated.

The block data-transfer mode is compatible with the single and autoinitialize buffer-transfer modes, but not with the chaining buffer-transfer mode. The chaining buffer-transfer mode requires that the transfer information for the next buffer transfer be written to the channel before the current buffer transfer completes. This is impossible with block data-transfer mode, because the channel will only relinquish control of the bus for DRAM refresh cycles during the buffer transfer. The following flowcharts show the transfer process flow for a channel programmed for the block data-transfer mode with the single (Figure 16-9) and autoinitialize (Figure 16-10) buffer-transfer modes.

ERRATA (3/28/95)
In the first paragraph in Section 16.2.7.2, the third sentence incorrectly stated:
The block mode, unlike the single mode, does not give up bus control during a buffer transfer.
It now correctly states:
The block mode, unlike the single mode, only gives up control of the bus for DRAM refresh cycles.

The second paragraph, third sentence incorrectly stated:
This is impossible with block data-transfer mode, because the channel does not relinquish bus control at any time during the buffer transfer.
It now correctly states:
This is impossible with block data-transfer mode, because the channel will only relinquish control of the bus for DRAM refresh cycles during the buffer transfer.

ERRATA (4/4/95)
In Table A-2 (page A-2) BS8# Type incorrectly shown as “O”; now correctly shows “I”.

Table A-2 is an alphabetical list of the device signals. The *Multiplexed with* column lists other signals that share a pin with the signal listed in the *Signal* column.

Table A-2. Signal Descriptions (Sheet 1 of 6)

Signal	Type	Name and Description	Multiplexed with
A25:19 A18:16 A15:1	O	Address Bus: Outputs physical memory or port I/O addresses. These signals are valid when ADS# is active and remain valid until the next T1, T2P, or Ti.	— CAS2:0 —
ADS#	O	Address Status: Indicates that the processor is driving a valid bus-cycle definition and address (W/R#, D/C#, M/IO#, A25:1, BHE#, BLE#) onto its pins.	—
BHE#	O	Byte High Enable: Indicates that the processor is transferring a high data byte.	—
BLE#	O	Byte Low Enable: Indicates that the processor is transferring a low data byte.	—
BS8#	I	Bus Size: Indicates that an 8-bit device is currently being addressed.	—
BUSY#	I	Busy: Indicates that the math coprocessor is busy. If BUSY# is sampled low at the falling edge of RESET, the processor performs an internal self test.	TMRGATE2
CAS2:0	O	Cascade Address: Carries the slave address information from the master 8259A interrupt module during interrupt acknowledge bus cycles.	A18:16
CLK2	ST	Input Clock: Connect an external clock to this pin to provide the fundamental timing for the microprocessor. The internal processor clock frequency is half the CLK2 frequency.	—
COMCLK	I	SIO Baud Clock: An external source connected to this pin can clock the SIO*n* baud-rate generator.	P3.7
CS6# CS5# CS4# CS3# CS2# CS1# CS0#	O	Chip-selects (lower): Asserted when the address of a memory of I/O bus cycle is within the programmed address region.	REFRESH# DACK0# P2.4 P2.3 P2.2 P2.1 P2.0
CTS1# CTS0#	I	Clear to Send: Indicates that the modem or data set is ready to exchange data with the SIO channel.	EOP# P2.7

ERRATA (4/4/95) In Table A-2 (page A-5) READY# Type incorrectly shown as “I”; now correctly shows “I/O”. SMI# Type incorrectly shown as “I”; now correctly shown as “ST”.

Table A-2. Signal Descriptions (Sheet 4 of 6)

Signal	Type	Name and Description	Multiplexed with
P3.7 P3.6 P3.5 P3.4 P3.3 P3.2 P3.1 P3.0	I/O	Port 3: General-purpose, bidirectional I/O port.	COMCLK PWRDOWN INT3 INT2 INT1 INT0 TMROUT1 TMROUT0
PWRDOWN	O	Powerdown Output: Indicates that the device is in powerdown mode.	P3.6
RD#	O	Read Enable: Indicates that the current bus cycle is a read cycle and the data bus is able to accept data.	
READY#	I/O	Ready: Indicates that the current bus cycle has completed. The processor drives READY# when LBA# is active; otherwise, the processor samples READY# on the falling edge of phase 2 of T2, T2P or T2i.	—
REFRESH#	O	Refresh: Indicates that a refresh bus cycle is in progress and that the refresh address is on the bus for the DRAM controller.	CS6#
RESET	ST	System Reset Input: Suspends any operation in progress and places the processor into a known reset state.	—
RI1# RI0#	I	Ring Indicator: Indicates that the modem or data set has received a telephone ringing signal.	SSIORX P1.4
RTS1# RTS0#	O	Request to Send: Indicates that the SIO channel is ready to exchange data with the modem or data set.	SSIOTX P1.1
RXD1 RXD0	I	Receive Data: Accepts data from the modem or data set to the SIO channel.	DRQ1 P2.5
SMI#	ST	System Management Interrupt: Causes the device to enter System Management Mode. SMI# is the highest priority external interrupt.	—
SMIACT#	O	System Management Interrupt Active: Indicates that the processor is in System Management Mode.	—
SRXCLK	I/O	SSIO Receive Clock: In master mode, the baud-rate generator’s output appears on SRXCLK and can be used to clock a slave transmitter. In slave mode, SRXCLK functions as an input clock for the receiver.	DTR1#
SSIORX	I	SSIO Receive Serial Data: Accepts serial data (most-significant bit first) into the SSIO.	RI1#

ERRATA (3/28/95)
TCK description, second sentence removed. TRST# Type incorrectly shown as “I”; now correctly shown as “ST”.

Table A-2. Signal Descriptions (Sheet 5 of 6)

Signal	Type	Name and Description	Multiplexed with
SSIOTX	O	SSIO Transmit Serial Data: Sends serial data (most-significant bit first) from the SSIO.	RTS1#
STXCLK	I/O	SSIO Transmit Clock: In master mode, the baud-rate generator’s output appears on STXCLK and can be used to clock a slave receiver. In slave mode, STXCLK functions as an input clock for the transmitter.	DSR1
TCK	I	Test Clock Input: Provides the clock input for the test-logic unit. An external signal must provide a maximum input frequency of one-half the CLK2 input frequency. TCK is driven by the test-logic unit’s control circuitry.	—
TDI	I	Test Data Input: Serial input for test instructions and data. Sampled on the rising edge of TCK; valid only when either the instruction register or a data register is being serially loaded.	—
TDO	O	Test Data Output: Serial output for test instructions and data. TDO shifts out the contents of the instruction register or the selected data register (LSB first) on the falling edge of TCK. If serial shifting is not taking place, TDO floats.	—
TMRCLK2 TMRCLK1 TMRCLK0	I	Timer/Counter Clock Input: An external clock source connected to the TMRCLK*n* pin can drive the corresponding timer/counter. Alternatively, the internal prescaled clock can drive the timer/counter.	PEREQ INT6 INT4
TMRGATE2 TMRGATE1 TMRGATE0	I	Timer/Counter Gate Input: Can control the counter’s operation (enable, disable, or trigger, depending on the programmed mode).	BUSY# INT7 INT5
TMROUT2 TMROUT1 TMROUT0	O	Timer/Counter Output: Can provide the timer/counter’s output. The form of the output depends on the programmed mode.	ERROR# P3.1 P3.0
TMS	I	Test Mode Select: Controls the sequence of the test-logic unit’s TAP controller states. Sampled on the rising edge of TCK.	—
TRST#	ST	Test Reset: Resets the test-logic unit’s TAP controller at power-up. Asynchronously clears the data registers and initializes the instruction register to 0010 (the IDCODE instruction opcode).	—
TXD1 TXD0	O	Transmit Data: Transmits serial data from the corresponding SIO channel.	DACK1# P2.6
UCS#	O	Upper Chip-select: Asserted when the address of a memory or I/O bus cycle is within the programmed address region.	—

Table A-2. Signal Descriptions (Sheet 6 of 6)

Signal	Type	Name and Description	Multiplexed with
V_{CC}	P	System Power: Provides the nominal DC supply input. Connected externally to a V_{CC} board plane.	—
V_{SS}	G	System Ground: Provides the 0 volt connection from which all inputs and outputs are measured. Connected externally to a ground board plane.	—
WDTOUT	O	Watchdog Timer Output: Indicates that the watchdog timer has expired.	—
W/R#	O	Write/Read: Indicates whether the current bus cycle is a write cycle or a read cycle.	—
WR#	O	Write Enable: Indicates that the current bus cycle is a write cycle.	—

Table A-3 defines the abbreviations used in Table A-4 to describe the pin states.

Table A-3. Pin State Abbreviations

Abbreviation	Description
1	Output driven to V_{CC}
0	Output driven to V_{SS}
Z	Output floats
Q	Output remains active
X	Output retains current state
WH	Pin has permanent weak pull-up
WL	Pin has permanent weak pull-down

ERRATA (3/28/95)
WR# pin description added to table

Table A-4 lists the states of output and bidirectional pins after reset and during idle, powerdown, and hold. It also lists input pins that have permanent weak pull-ups and pull-downs.

Table A-4. Pin States After Reset and During Idle, Powerdown, and Hold

Symbol	Type	Pin State			
		Reset	Idle	Powerdown	Hold
A15:0	O	1	1	1	Z
A18:16 or CAS2:0	O	1	1	1	Z
A25:19	O	1	1	1	Z
ADS#	O	1	1	1	Z
BHE#	O	1	0/1	0/1	Z
BLE#	O	1	0/1	0/1	Z
CS6#/REFRESH#	O	1	Q	X	1
DACK0#/CS5#	O	1	Q	X	Q/1
DACK1#/TXD1	O	1	Q	X	1/X
D/C#	O	1	0	0	Z
LBA#	O	1	Q	X	1
M/IO#	O	1	1	1	Z
RD#	O	1	1	1	1
RTS1#/SSIOTX	O	WL	Q	X	Q
SMIACT#	O	1	X	X	1
TDO	O	—	—	—	—
UCS#	O	1	Q	X	1
W/R#	O	1	1	1	Z
WDTOUT	O	0	Q	X	Q
WR#	O	1	1	1	1
DTR1#/SRXCLK	I or I/O	WH	Q	X	Q
ERROR#/TMROUT2	I or O	WH	Q	X or Q *	Q
D15:0	I/O	—	—	—	Z
READY#	I/O	input	Z	Z	Z
P1.1/RTS0#	I/O or O	WH	X/Q	X	X
P1.2/DTR0#	I/O or O	WH	X	X	X
P1.5/LOCK#	I/O or O	WH	X	X	X/Z
P1.7/HLDA	I/O or O	WL	X/Q	X	X/Q
P2.4:0/CS4:0#	I/O or O	WH	X/Q	X	Q/1
P2.6/TXD0	I/O or O	WL	X/Q	X/X or Q *	X

* X if clock source is internal; Q if clock source is external.

ERRATA (3/28/95)
Pin State During Hold changed for the following pins: