ADVANCE INFORMATION

Intel386™ CXSA EMBEDDED MICROPROCESSOR

SmartDie Product Specification

- **Static Intel386™ CPU Core**
  - **Low Power Consumption**
  - **Operating Power Supply 4.5V to 5.5V**
  - **Operating Frequency 33 MHz**
- **Transparent Power-Management System Architecture**
  - **Intel System Management Mode (SMM) Architecture Extension for Truly Compatible Systems**
  - **Power Management Transparent to Operating System and Application Programs**
  - **Programmable Power Management Modes**
- **Clock Freeze Mode Allows Clock Stopping at Any Time**
- **Full 32-Bit Internal Architecture**
  - **8-, 16-, 32-Bit Data Types**
  - **8 General-Purpose 32-Bit Registers**
- **Runs Intel386 Architecture Software in a Cost Effective 16-Bit Hardware Environment**
  - **Runs Same Applications and Operating Systems as the Intel386 SX and Intel386 DX Processors**
  - **Object Code Compatible with 8086, 80186, 80286 and Intel386 Processors**
- **High Performance 16-Bit Data Bus**
  - **33 MHz Clock**
  - **Two-Clock Bus Cycles**
  - **Address Pipelining Allows Use of Slower, Inexpensive Memories**
- **Virtual 8086 Mode Allows Execution of 8086 Software in a Protected and Paged System**
- **Large Uniform Address Space**
  - **64 Megabyte Physical**
  - **64 Terabyte Virtual**
  - **4 Gigabyte Maximum Segment Size**
- **On-Chip Debugging Support Including Breakpoint Registers**
- **Complete System Development Support**
- **High-Speed CHMOS Technology**
- **Integrated Memory Management Unit (MMU)**
  - **Virtual Memory Support**
  - **Optional On-Chip Paging**
  - **Four Levels of Hardware-Enforced Protection**
  - **MMU fully compatible with those of the 80286 and Intel386 DX Processors**
- **Intel SmartDie Product**
  - **Full AC/DC Testing at Die Level**
  - **+25°C–80°C (Junction) Temperature Range**

NOTICE: This document contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest SmartDie Product Specification before finalizing a design.

REFERENCE INFORMATION: The information in this document is provided as a supplement to the Standard Package Data Sheet on a specific product. Please reference the Standard Package Data Sheet (Order No. 272418) for additional product information and specifications not found in this document.

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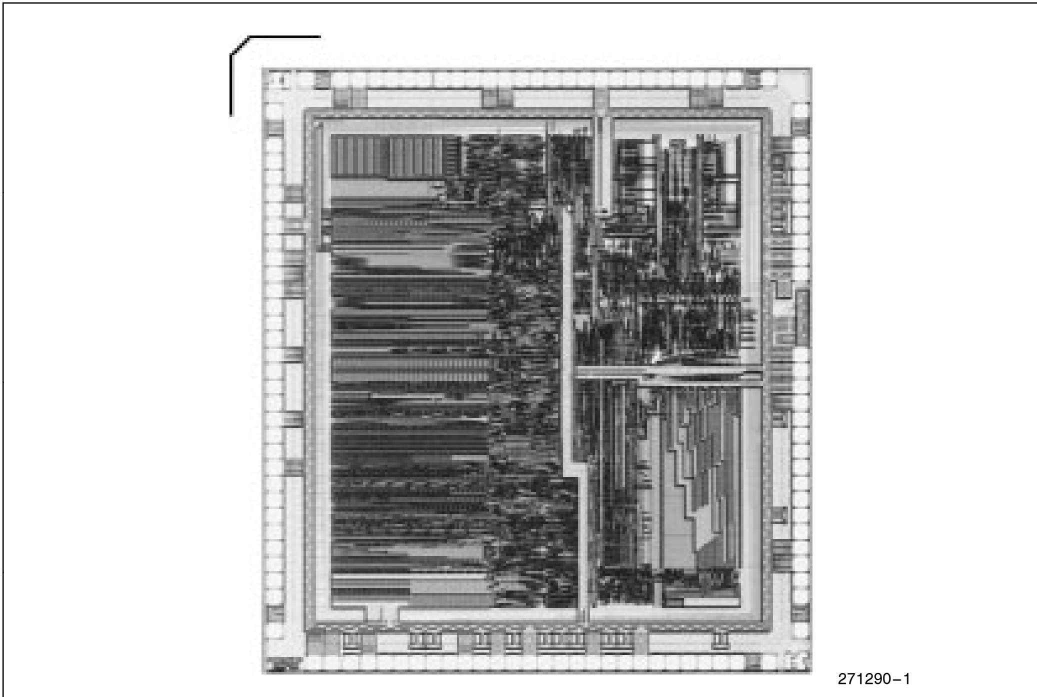
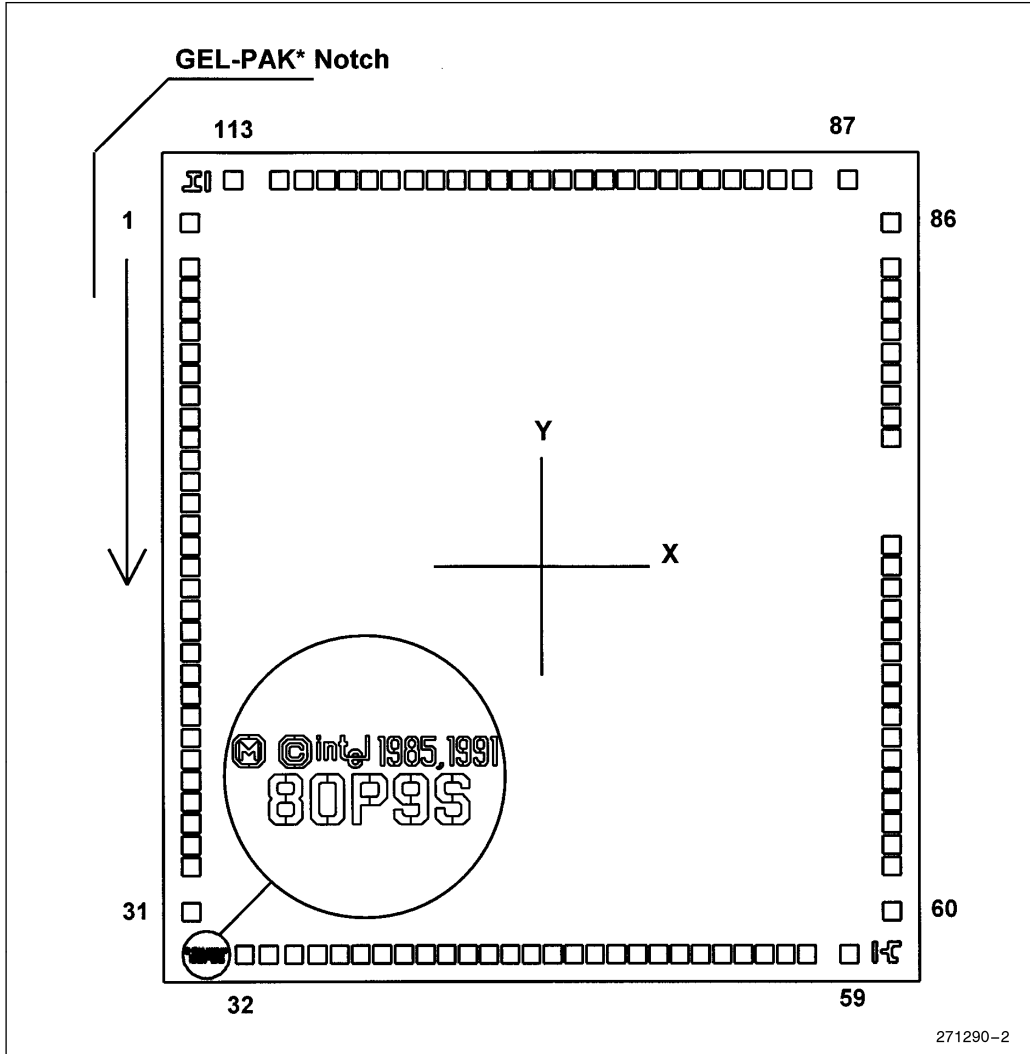


Intel386™ CXSA Microprocessor Die Photo

1.0 DIE SPECIFICATIONS



NOTE: The die photo on the opposite page indicates actual orientation of the die in the GEL-PAK* (shipping container). The 45° notch shown on the plot indicates the location of the 45° notch on the GEL-PAK. Intel uses an internal logo '80P9S' on X80386CXSA die.

Figure 1. Intel386™ CXSA Embedded Microprocessor Die/Bond Pad Layout

1.1 Pad Description

Table 1. Intel386™ CXSA Embedded Microprocessor Bond Pad Center Data

Pad	Signal	Pad Center			
		(Mils = 0.001 in.)		(Microns)	
		X	Y	X	Y
001	A20	−97.4	95.1	−2474	2415
002	A19	−97.4	82.7	−2474	2100
003	A18	−97.4	76.8	−2474	1950
004	A17	−97.4	70.9	−2474	1800
005	V_{CC}	−97.4	65.0	−2474	1650
006	A16	−97.4	59.1	−2474	1500
007	V_{CC}	−97.4	53.1	−2474	1350
008	N.C.	−97.4	47.2	−2474	1200
009	V_{SS}	−97.4	41.3	−2474	1050
010	V_{SS}	−97.4	35.4	−2474	900
011	N.C.	−97.4	29.5	−2474	750
012	A15	−97.4	23.6	−2474	600
013	A14	−97.4	17.7	−2474	450
014	A13	−97.4	11.8	−2474	300
015	V_{SS}	−97.4	5.9	−2474	150
016	A12	−97.4	0.0	−2474	0
017	A11	−97.4	−5.9	−2474	−150
018	A10	−97.4	−11.8	−2474	−300
019	N.C.	−97.4	−17.7	−2474	−450
020	A9	−97.4	−23.6	−2474	−600
021	A8	−97.4	−29.5	−2474	−750
022	V_{CC}	−97.4	−35.4	−2474	−900
023	N.C.	−97.4	−41.3	−2474	−1050
024	N.C.	−97.4	−47.2	−2474	−1200
025	N.C.	−97.4	−53.1	−2474	−1350
026	A7	−97.4	−59.1	−2474	−1500
027	A6	−97.4	−65.0	−2474	−1650
028	A5	−97.4	−70.9	−2474	−1800
029	A4	−97.4	−76.8	−2474	−1950
030	A3	−97.4	−82.7	−2474	−2100
031	A2	−97.4	−95.1	−2474	−2415
032	V_{SS}	−82.7	−107.0	−2102	−2718
033	V_{SS}	−76.0	−107.0	−1932	−2718
034	V_{CC}	−69.0	−107.0	−1754	−2718
035	V_{CC}	−62.6	−107.0	−1589	−2718
036	A25	−56.5	−107.0	−1434	−2718

Table 1. Intel386™ CXSA Embedded Microprocessor Bond Pad Center Data (Continued)

Pad	Signal	Pad Center			
		(Mils = 0.001 in.)		(Microns)	
		X	Y	X	Y
037	A24	−50.6	−107.0	−1284	−2718
038	A20M#	−44.6	−107.0	−1134	−2718
039	SMI#	−38.5	−107.0	−979	−2718
040	SMIACT#	−32.6	−107.0	−828	−2718
041	V_{CC}	−26.7	−107.0	−679	−2718
042	V_{SS}	−20.8	−107.0	−529	−2718
043	V_{SS}	−14.9	−107.0	−378	−2718
044	INTR	−9.0	−107.0	−229	−2718
045	V_{CC}	−3.1	−107.0	−78	−2718
046	NMI	2.8	−107.0	71	−2718
047	PEREQ	8.7	−107.0	221	−2718
048	ERROR#	14.6	−107.0	372	−2718
049	V_{SS}	20.5	−107.0	522	−2718
050	BUSY#	26.4	−107.0	671	−2718
051	RESET	32.3	−107.0	821	−2718
052	V_{CC}	38.2	−107.0	972	−2718
053	N.C.	44.2	−107.0	1122	−2718
054	N.C.	50.1	−107.0	1271	−2718
055	N.C.	56.0	−107.0	1421	−2718
056	N.C.	61.9	−107.0	1571	−2718
057	FLT#	67.8	−107.0	1722	−2718
058	N.C.	73.7	−107.0	1871	−2718
059	LOCK#	85.5	−107.0	2172	−2718
060	W/R#	97.4	−95.1	2474	−2415
061	D/C#	97.4	−82.7	2474	−2100
062	M/IO#	97.4	−76.8	2474	−1950
063	V_{SS}	97.4	−70.9	2474	−1800
064	V_{CC}	97.4	−65.0	2474	−1650
065	N.C.	97.4	−59.1	2474	−1500
066	N.C.	97.4	−53.1	2474	−1350
067	BHE#	97.4	−47.2	2474	−1200
068	A1	97.4	−41.3	2474	−1050
069	BLE#	97.4	−35.4	2474	−900
070	ADS#	97.4	−29.5	2474	−750
071	N.C.	97.4	−23.6	2474	−600
072	CLK2	97.4	−17.7	2474	−450
073	V_{SS}	97.4	−11.8	2474	−300
074	V_{SS}	97.4	−5.9	2474	−150

Table 1. Intel386™ CXSA Embedded Microprocessor Bond Pad Center Data (Continued)

Pad	Signal	Pad Center (Mils = 0.001 in.)		Pad Center (Microns)	
		X	Y	X	Y
075	V_{SS}	97.4	0.0	2474	0
076	V_{SS}	97.4	5.9	2474	150
077	V_{CC}	97.4	35.4	2474	900
078	V_{CC}	97.4	41.3	2474	1050
079	V_{CC}	97.4	47.2	2474	1200
080	READY#	97.4	53.1	2474	1350
081	NA#	97.4	59.1	2474	1500
082	V_{SS}	97.4	65.0	2474	1650
083	HOLD	97.4	70.9	2474	1800
084	HLDA	97.4	76.8	2474	1950
085	V_{SS}	97.4	82.7	2474	2100
086	D0	97.4	95.1	2474	2415
087	D1	85.5	107.0	2172	2718
088	D2	72.7	107.0	1846	2718
089	V_{SS}	65.8	107.0	1672	2718
090	V_{CC}	59.1	107.0	1501	2718
091	D3	53.2	107.0	1351	2718
092	D4	47.3	107.0	1202	2718
093	D5	41.4	107.0	1052	2718
094	D6	35.5	107.0	902	2718
095	D7	29.6	107.0	751	2718
096	V_{CC}	23.7	107.0	601	2718
097	D8	17.8	107.0	452	2718
098	D9	11.9	107.0	301	2718
099	D10	6.0	107.0	152	2718
100	D11	0.1	107.0	2	2718
101	D12	−5.8	107.0	−149	2718
102	V_{SS}	−11.8	107.0	−299	2718
103	V_{CC}	−17.7	107.0	−449	2718
104	D13	−23.6	107.0	−599	2718
105	D14	−29.5	107.0	−748	2718
106	D15	−35.4	107.0	−898	2718
107	N.C.	−42.0	107.0	−1067	2718
108	N.C.	−47.9	107.0	−1216	2718
109	A23	−53.8	107.0	−1366	2718
110	A22	−59.7	107.0	−1517	2718
111	V_{SS}	−66.0	107.0	−1677	2718

Table 1. Intel386™ CXSA Embedded Microprocessor Bond Pad Center Data (Continued)

Pad	Signal	Pad Center (Mils = 0.001 in.)		Pad Center (Microns)	
		X	Y	X	Y
112	V_{SS}	−72.7	107.0	−1846	2718
113	A21	−85.5	107.0	−2172	2718

Notes:
1. X-Y pad coordinates represent bond pad centers and are relative to center of die.
2. The symbol "#" is used at the end of a signal name to denote an active low signal.
3. N.C. signifies no connect. These pads must not be connected.

2.0 INTEL DIE PRODUCTS PROCESSING

TEST PROCEDURE

Intel has instituted full-speed functional testing at the die level for all SmartDie products. This level of testing is ordinarily performed only after assembly into a package. Each die is tested to the same electrical limits as the equivalent packaged unit.

WAFER PROBE

Wafer probing is performed on every wafer produced in an Intel Fab. The process consists of specific electrical tests and device-specific functionality tests.

At the wafer level, built-in test structures are probed to verify that device electrical characteristics are in control and meet specifications. Measurements are made of transistor threshold voltages and current characteristics; poly and contact resistance; gate oxide and junction integrity; and specific parameters critical to the particular technology and device type. Wafer-to-wafer, across-the-wafer run-to-run variation and conformance to spec limits are checked.

The actual devices on each wafer are then probed for both functionality and performance to specifications. Additional reliability tests are also included in the probe steps.

WAFER SAW

Probed wafers are transferred to Intel's assembly sites to be sawed. The saw cuts completely through the wafer.

DIE INSPECTION

Upon completion of the wafer saw, the die are moved to pick and place equipment that removes reject die. The remaining die are submitted to the same visual inspection as standard packaged product. The compliant die are then transferred to GEL-PAK's for shipment.

PACKING PROCEDURE

Intel will ship all Intel die products in GEL-PAKs*. GEL-PAKs eliminate the die edge damage usually associated with die cavity plates or chip trays.

The backside of each die adheres to the gel membrane in the GEL-PAK, eliminating the risk of damage to the active die surface. A simple vacuum release mechanism allows for pick and place removal at the customer's site.

Only die from the same wafer lot are packaged together in a GEL-PAK, and all die are placed in the GEL-PAKs with a consistent orientation. The GEL-PAKs are then sealed and labeled with the following information:

- Intel Die Products
- Intel Part Number
- Spec
- Customer Part Number (if applicable)
- Fab Lot Number
- Quantity
- Assembly Lot Traveler Number
- Seal Date
- ROM Code (if applicable)

NOTE:
GEL-PAKs require a Vacuum Release Station. Contact Vichem Corporation for more information.

INSPECTION STEPS

Multiple inspection steps are performed during the die fabrication and packing flow. These steps are performed according to the same specifications and criteria established for Intel's standard packaged product. Specific inspection steps include a wafer saw visual as well as a final die visual just before die are sealed in moisture barrier bags.

STORAGE REQUIREMENTS

Intel die products will be shipped in GEL-PAKs and sealed in a moisture-barrier anti-static bag with a desiccant. No special storage procedures are required while the bag is still unopened. Once opened, the GEL-PAK should be stored in a dry, inert atmosphere to prevent corrosion of the bond pads.

ESD

Components are ESD sensitive.

3.0 SPECIFICATIONS

Specifications within this document are specific to a particular die revision and are subject to change without notice. Verify with your local Intel Sales Office that you have the latest data before finalizing a design.

3.1 Physical Specifications

Substrate Bias Condition: V_{SS}

Post-Saw Die Dimensions:
Mils: X = 209 ± 0.5, Y = 228 ± 0.5

See associated Die/Bond Pad Layout for X,Y orientation.

Die Backside Material: (outer most layer first)
1500 (±) 500 Angstroms Gold, 200 (±) 100 Angstroms Chrome

Pad Passivation Opening Size:
Mils: 4.9 x 4.9 (single pads)
Microns: 125 x 125 (single pads)

Die Thickness: 17 ±1 mils

Minimum Pad Pitch:
Pads may not be evenly pitched. Minimum pitch is 150 microns (5.9 mils).

Bond Pad Metalization (outer most layer first):
1 Micron Aluminum (0.5% Copper), 0.1 Micron Titanium

Die Revision: A-2

Pads per Die: 113

Intel Fabrication Process: CHMOS V (min. feature size 0.8 microns)

Passivation: (outer most layer first)
5 Microns Polyimide, 0.6 Microns Nitride

NOTE:
Avoid exposing this device to light sources. Exposure to light will increase the leakage current of the device significantly and may result in temporary functional failure. Future planned revisions of this die may affect bond pad layout and, thus, substrate design.

3.2 DC Specifications

ABSOLUTE MAXIMUM RATINGS*

GEL-PAK Storage Temperature ....0°C to +70°C
Junction Temperature Under Bias ...... −65°C to +110°C
Supply Voltage with Respect to V_{SS} ...... −0.5V to +6.5V
Voltage on Other Pads .... −0.5V to V_{CC} + 0.5V

OPERATING CONDITIONS*

V_{CC} (Digital Supply Voltage) ....5.0V ± 0.5V
T_J (Junction Temperature Under Bias) ....25°C to 80°C
Operating Frequency.........................0–33 MHz

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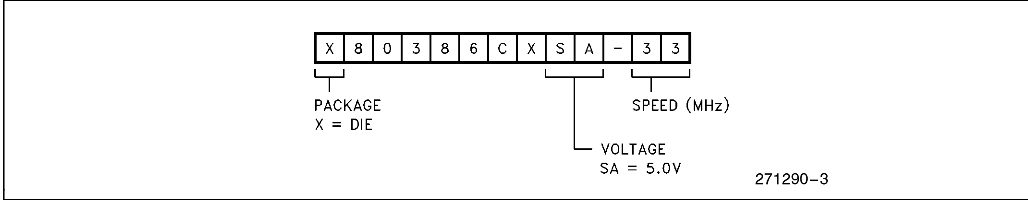
*****WARNING:*** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.0 DEVICE NOMENCLATURE



5.0 REFERENCE INFORMATION

Title	Order No.
Intel386™ CXSA Embedded Microprocessor Datasheet	272418
Intel386™ EX and CX CPU Development Tools Fact Sheet	272423
iRMX__EMB O.S. for the CX and EX Fact Sheet	272424
Intel386™ CX Processor Reference Manual	TBD

6.0 REVISION HISTORY

Rev	Date	Description
001	6/94	Initial release.