# IDT-C6™ Processor

## from Centaur Technology Inc.

*"The Value Processor"*

# Centaur Technology Inc.

- x86 processor design
- Started 4/95 by Glenn Henry
- Subsidiary of Integrated Device Technology
  - Manufacturing & sales partner
- Substantial processor & x86 expertise
  - IBM, Somerset, Motorola, DEC, AMD, TI, Dell
- Unique culture & management approach
  - Yields very high productivity & responsiveness

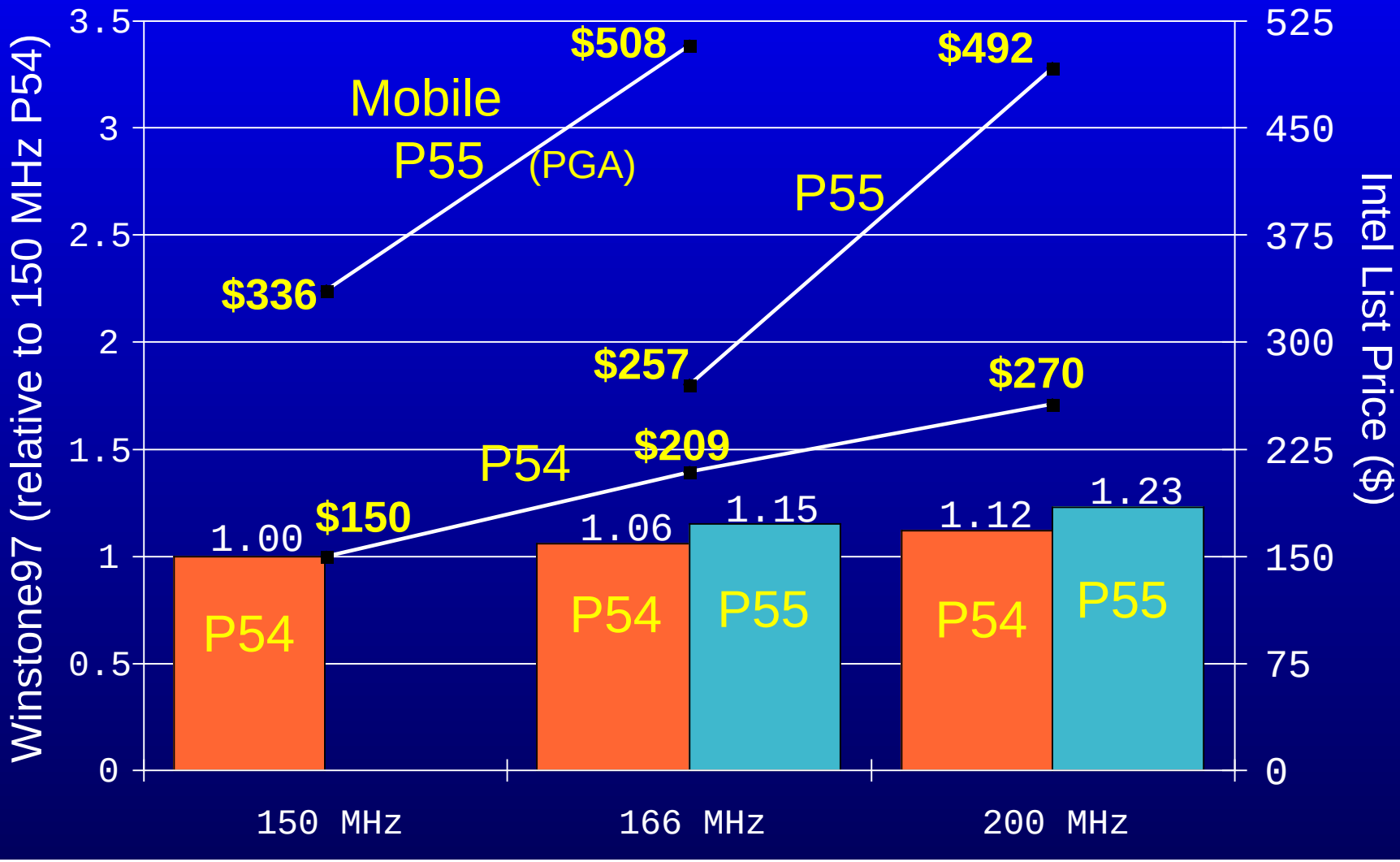
# Target Market

## *Who Did We Design For?*

- Low-cost desktops & mobile systems
  - Substantially less than $1500 total system
  - Currently with 120-150 MHz P54-class CPU
- Price-conscious consumers
  - Looking for best value
  - Focusing on total system price & performance
- Running primarily business applications
  - Word, spreadsheet, database, drawing
- Represents 40-50% of market volume

# Observations

*Low-end commodity desktop (VX, 256 KB, 32-MB EDO, Trident 1MB)*



# IDT-C6 Strategy


*Target Markets*

*< $1500 Desktops*

*&*

*Mobile Systems*

*Unique Design Approach*

*Best Value*

*(WS/$ & WS/Watt)*

# IDT-C6 Processor

- Plug-compatible with P55 (Socket 7)
  - Includes MMX™-compatible instructions
- Competitive performance
  - On targeted applications/environments
- Very low cost ➨ aggressive pricing
  - 88-mm$^2$ die
  - Low-cost technology
- Lowest power
  - Less than mobile P55 (which is less than all else)

*"Back to the future" design approach*

MMX is a trademark of Intel Corporation

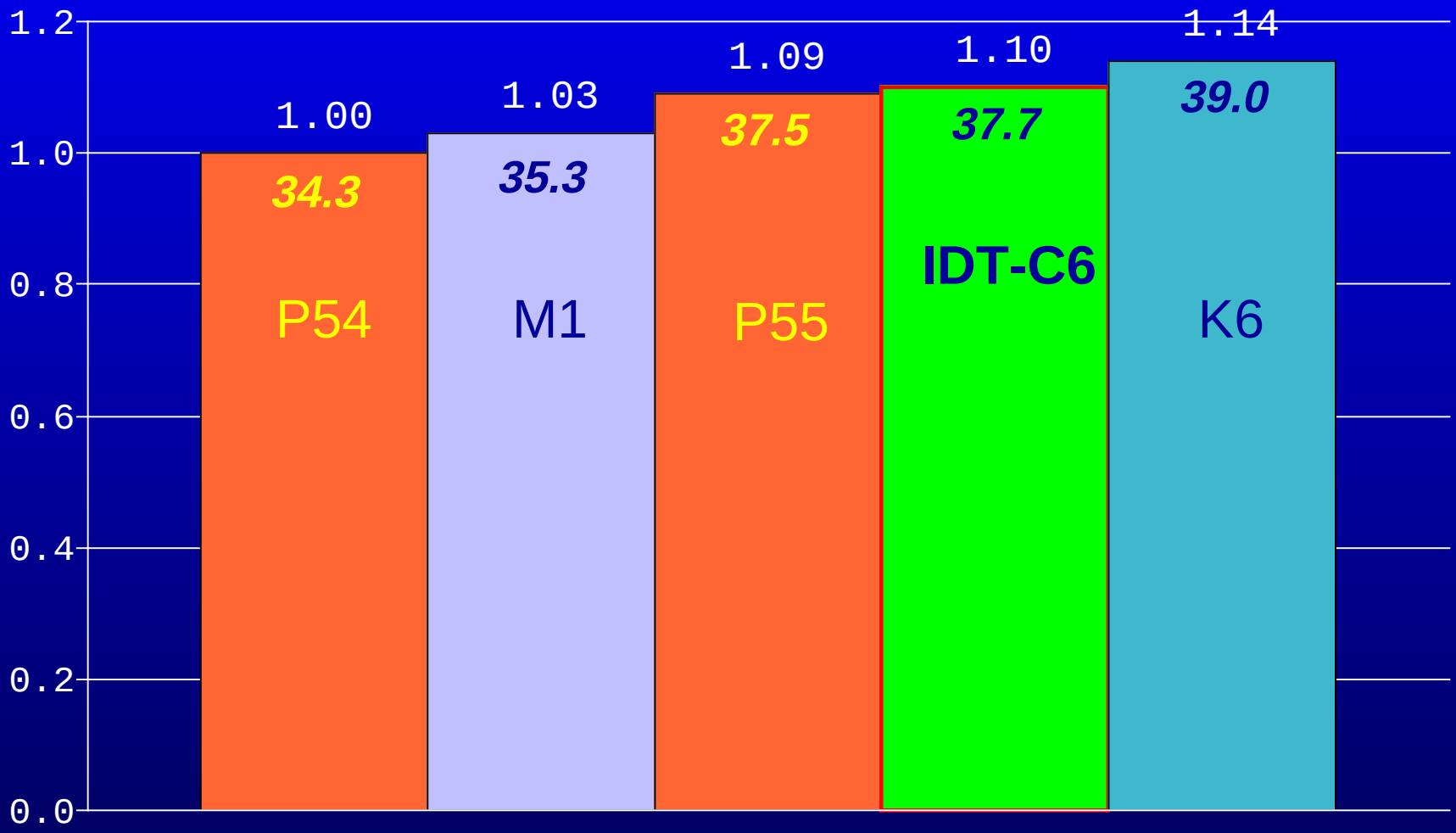
# IDT-C6 Product Offerings

- Separate desktop & mobile versions
  - More dynamic power management in mobile
  - All with MMX-compatible instructions
- 296-pin CPGA packages
- Single voltage (3.3V/3.52V)

| Desktop | Mobile | |
|---|---|---|
| 200 MHz | 200 MHz | 66 MHz Bus |
| 180 MHz | 180 MHz | 60 MHz Bus |
| 150 MHz | 150 MHz | 75 MHz Bus |
| | | 50 MHz Bus |

# Performance (200 MHz, WS97-B-95)

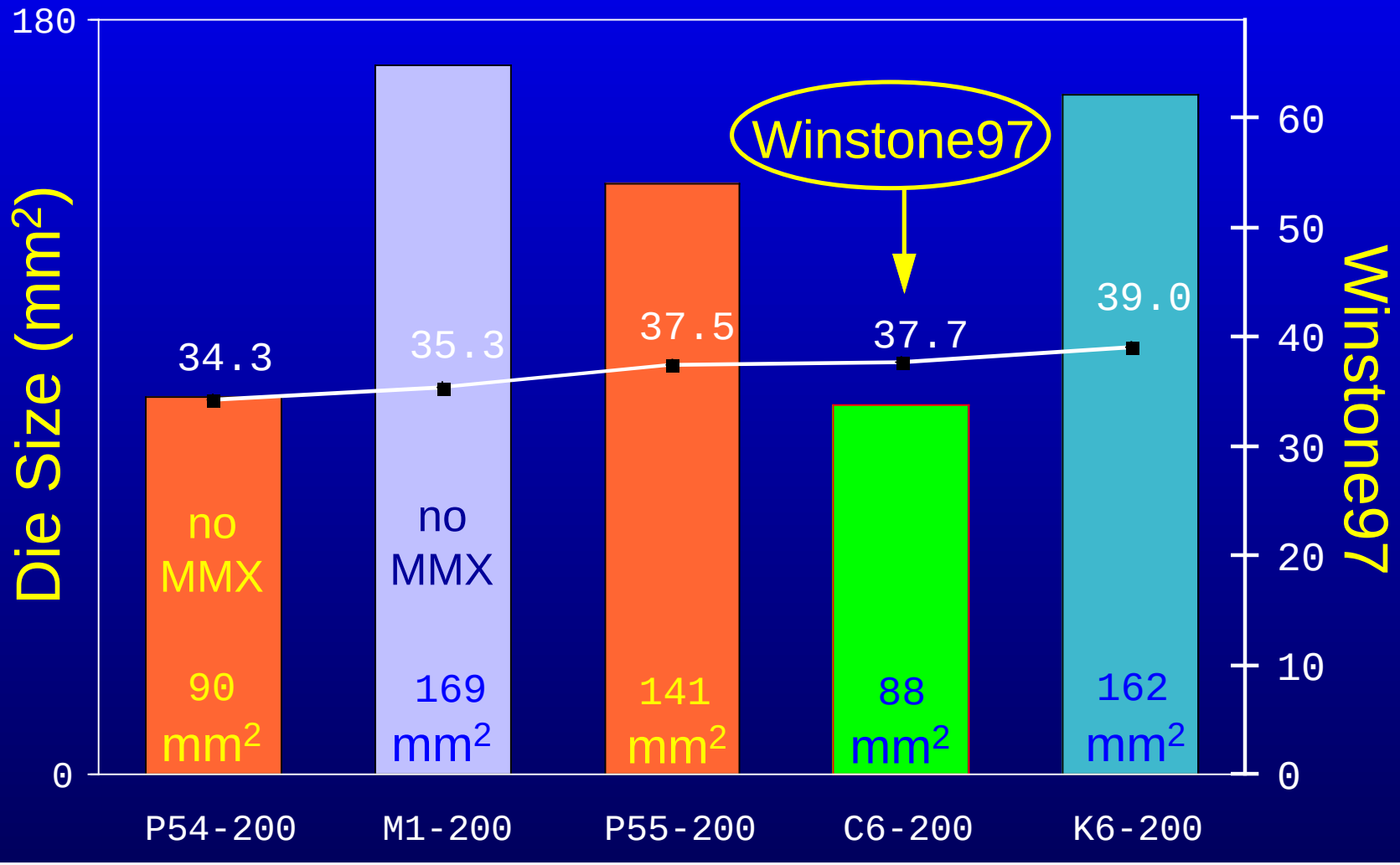
*Low-end commodity desktop (VX, 256 KB, 32-MB EDO, Trident 1MB)*




*Winstone97 (Business) for Windows 95*

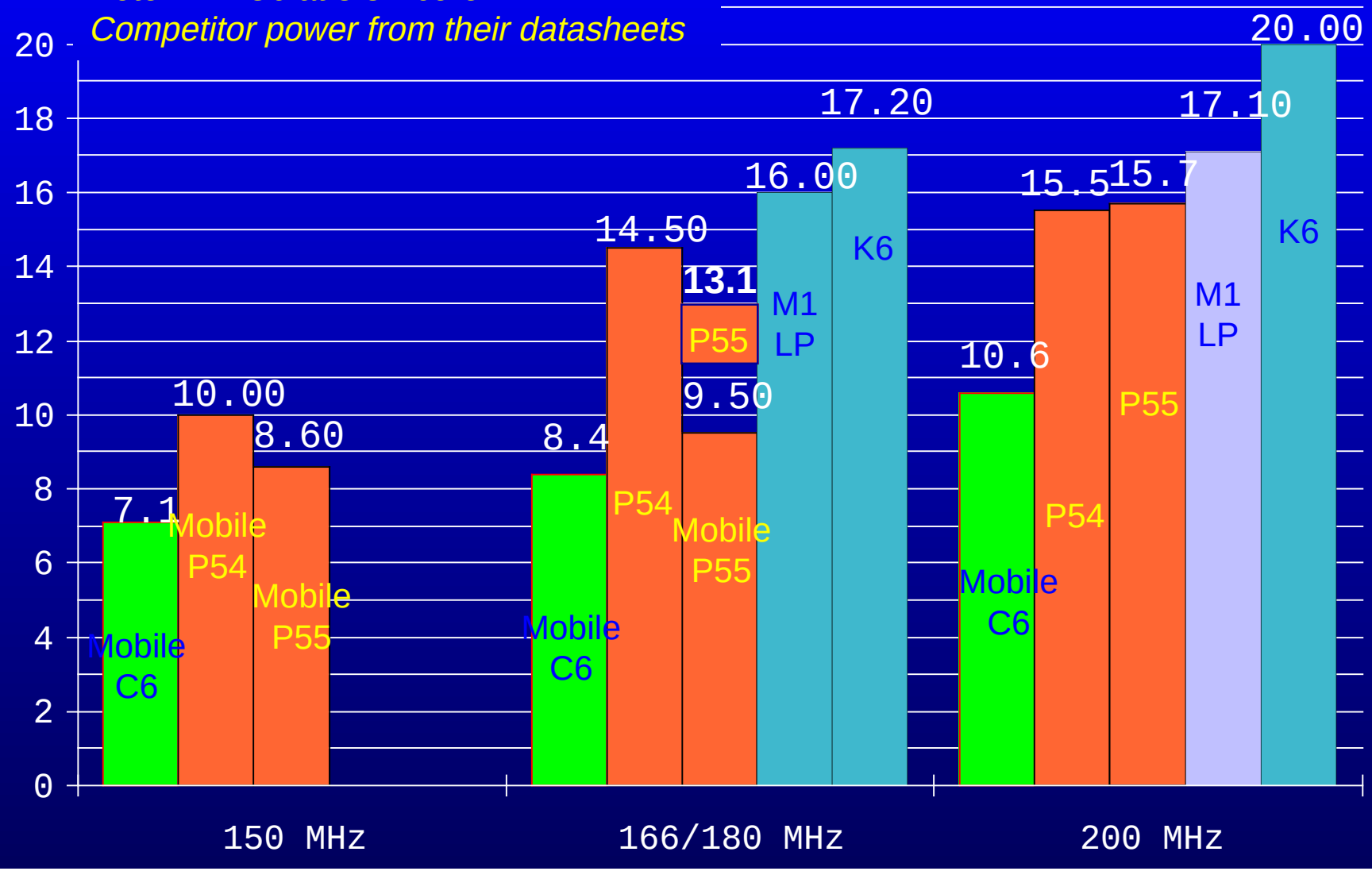
# Performance / Size (Cost)

*Low-end commodity desktop*



# Power Dissipation (Max W)

*Note: IDT-C6 at 3.3V core*
*Competitor power from their datasheets*

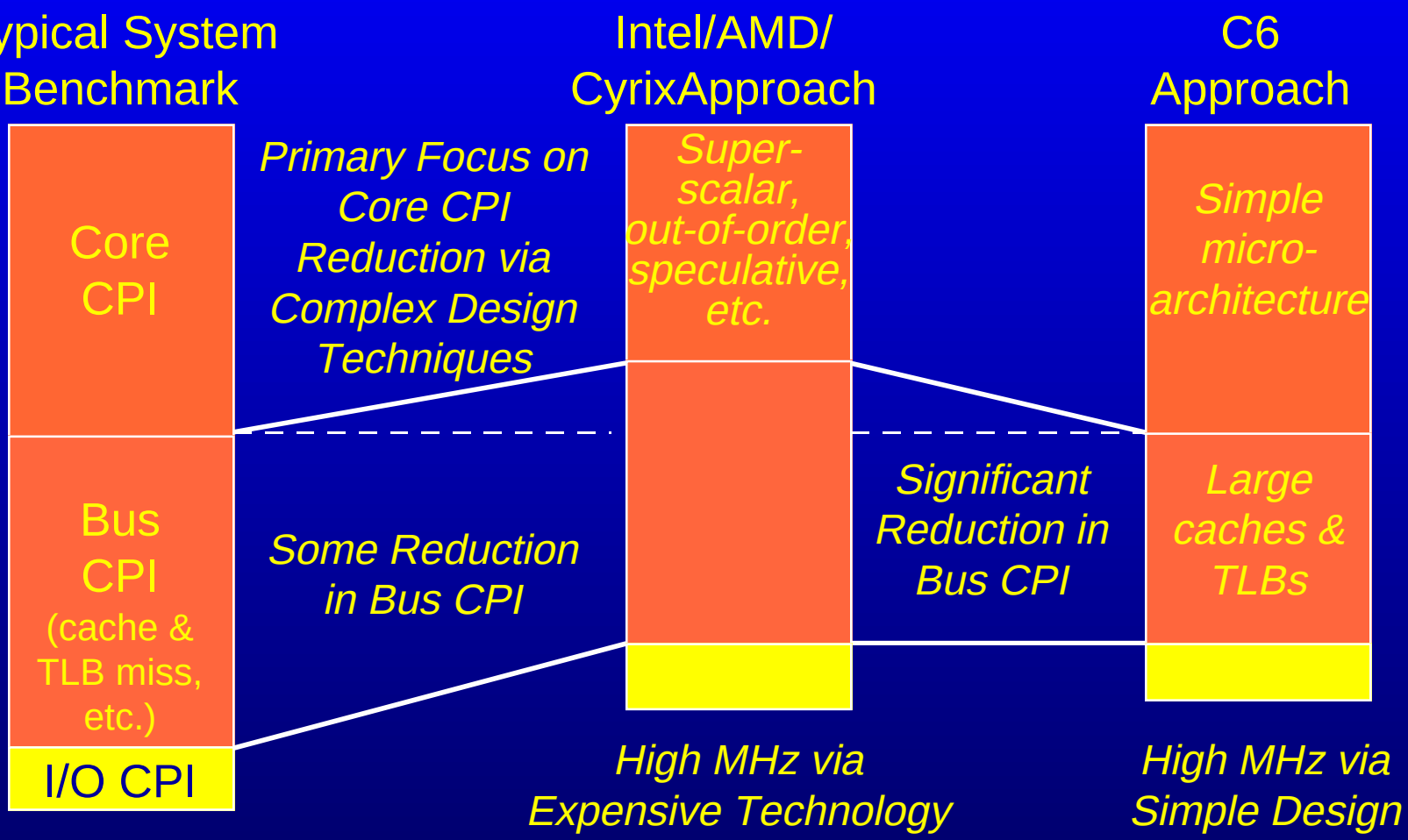


# How'd We Do It?

*Back To The Future!*

- Re-applied original RISC principles
  - Simple microarchitecture
  - Large caches (KB) & TLBs
  - Highly tuned for actual usage
- "Value-justification" of hardware
- vs. current trend of complexity & large size
  - Techno mumbo jumbo for its own sake
- Patents pending

# IDT-C6 Design Concept

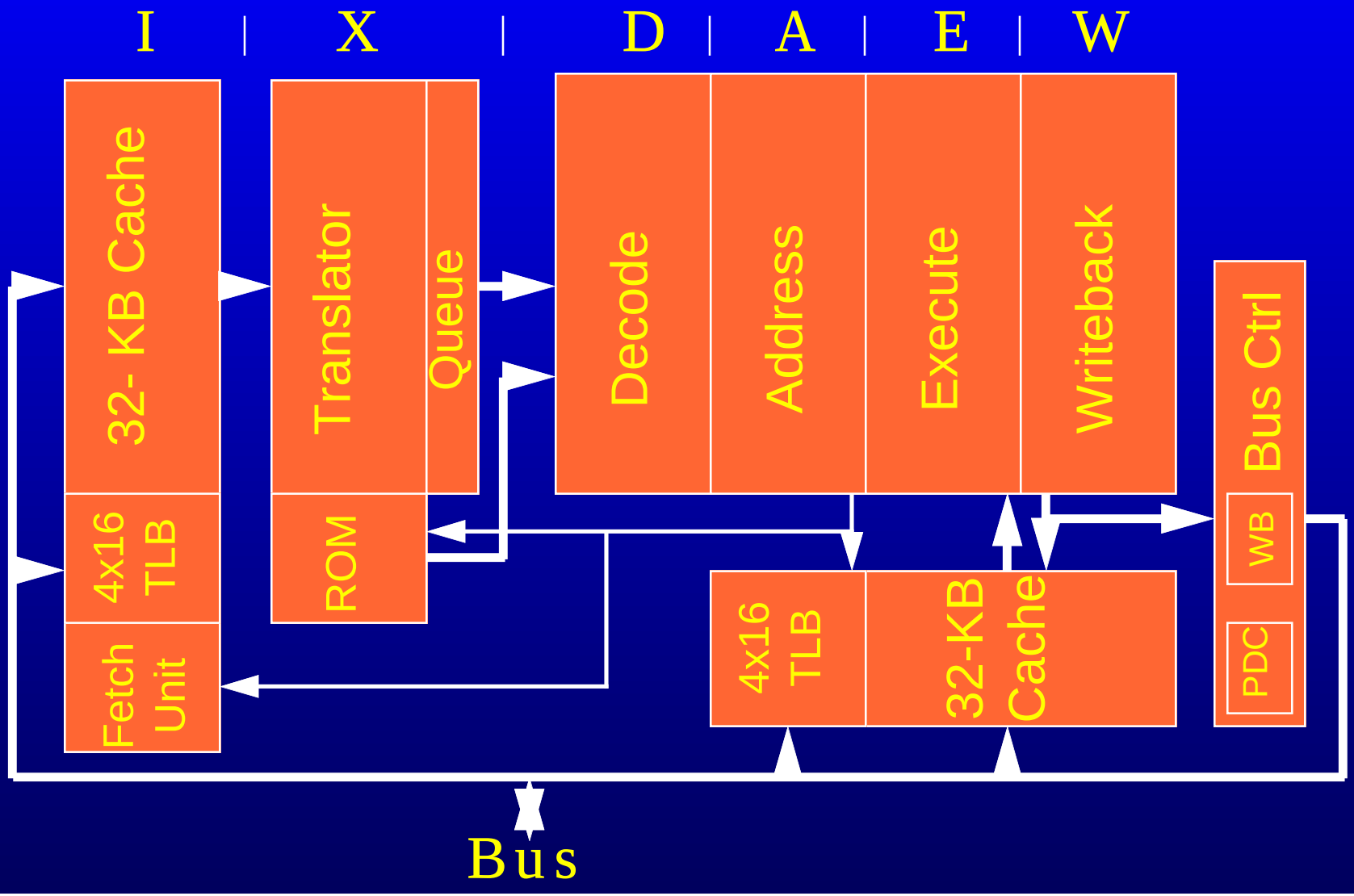


# Benefits of IDT-C6 Approach

- Small size
  - High efficiency of cache & arrays
  - Minimal control logic
- No bleeding-edge technology needed
- Low power dissipation
  - Few logic transistors
  - Easy to dynamically manage caches
- Fast design cycle ➨ market responsive
- Easy to verify (compatibility)
  - vs. out-of-order, super-scalar, etc.

*Low Cost*

# IDT-C6 Architecture



# Transistors

Transistors

3.99 M SRAM

0.32 ROM

0.37 Full Custom

0.51 Datapath

0.21 Control logic

*5.40 M Total C6*

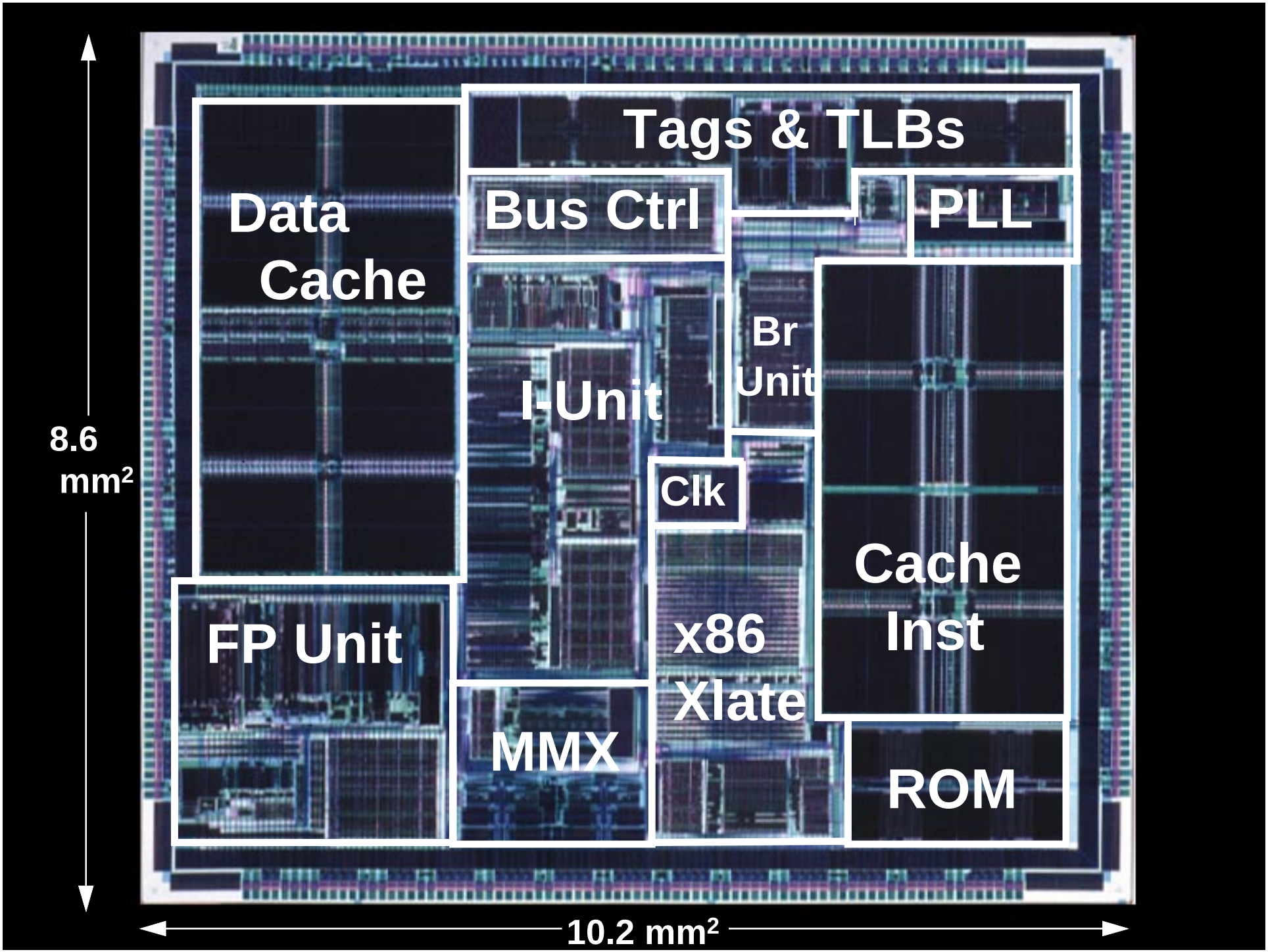
*88 mm²*

vs. *4.50 M Total P55*

*141 mm²*

# Technology

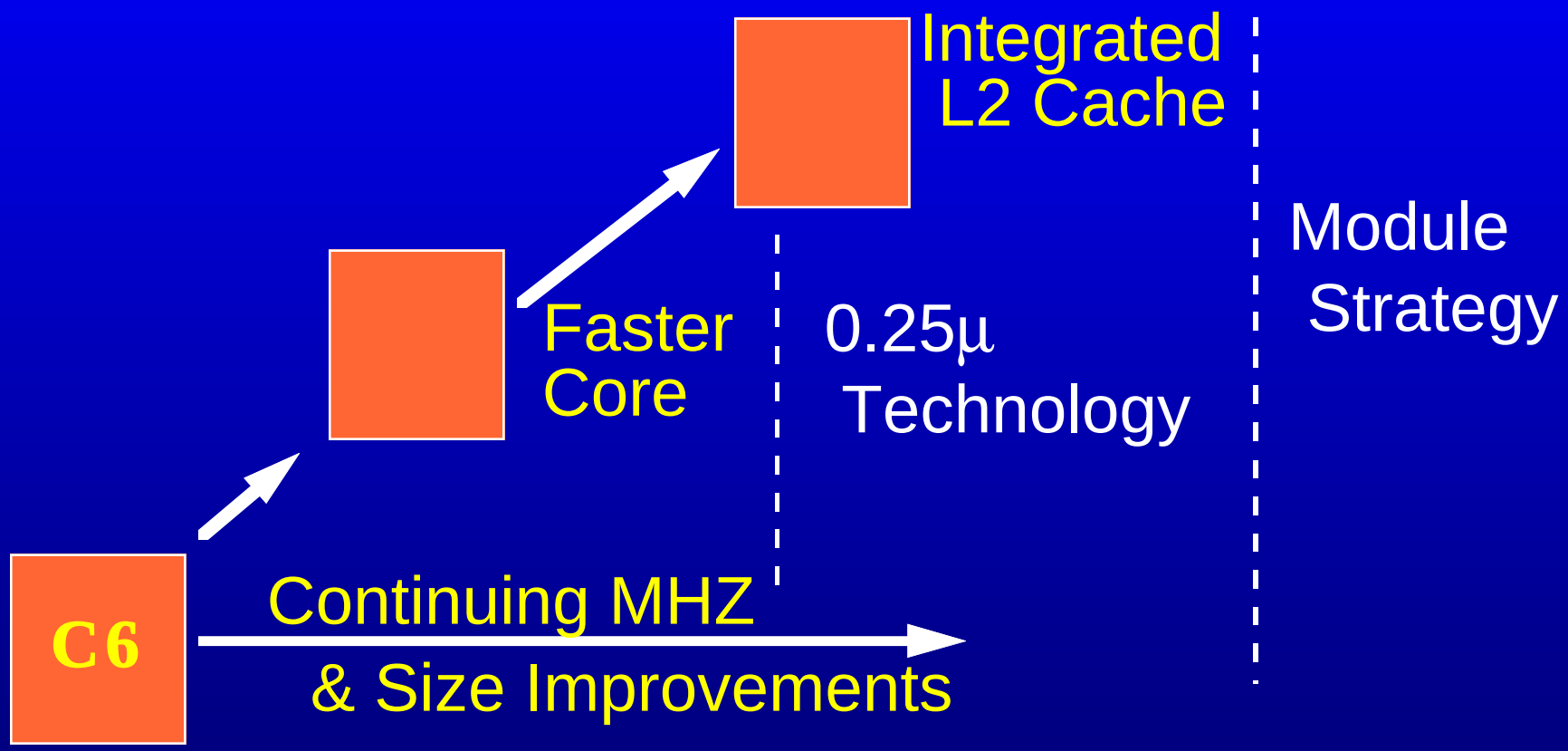
- 0.35µ CMOS (IDT “CMOS 9.5”)
- 0.28µ gate length (drawn)
- 4-level metal, stacked vias
- 6T SRAM cell
- Low cost technology
  - No local interconnect, no trench isolation, etc.
- To be manufactured in 2 IDT Fabs
  - Including new 8” Fab 4 (Oregon)


Tags & TLBs
Data Cache
Bus Ctrl
PLL
I-Unit
Br Unit
Clk
Cache Inst
FP Unit
x86 Xlate
MMX
ROM
8.6 mm²
10.2 mm²

# Current Status

- Working silicon available for 11 months
  - First silicon booted Windows
- Compatible now
  - Extensive board, OS & application testing
  - No significant errata
  - Ready for formal outside testing
- Engineering samples available now
  - To Beta customers
- Production shipments 3rd quarter

# Roadmap


Integrated
L2 Cache
Module
Strategy
Faster
Core
0.25µ
Technology
C6
Continuing MHZ
& Size Improvements