Linear Burst Performance with the IBM 6x86 and 6x86L Microprocessor

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Application Note

Revision Summary: This revision has added information about using a COASt (Cache On A Stick) module to implement L2 cache.

Performance Advantage

The default burst mode of the IBM 6x86 and 6x86L processor[1] is '1 + 4', which requires an additional single memory transfer. Linear burst mode permits all burst cycles to complete using just four cycles. When linear burst is used, system performance is increased because data is received by the processor more quickly and the available bus bandwidth is effectively increased.

IBM 6x86 and 6x86L Linear Burst and L2 Synchronous Burst SRAM

Each part of the memory subsystem must support the same burst sequence. Lower performance L2 caches are implemented with asynchronous SRAM. An address is presented for each access to the asynchronous SRAM. The burst mode isn't relevant for asynchronous L2 cache.

Synchronous SRAM was introduced to reduce the number of wait states needed to complete a burst cycle. The first access to synchronous SRAM is the same as for ascyhronous. Since the burst sequence is known, the synchronous SRAM only needs to increment a counter to provide the next piece of data in the burst sequence. The data for the second and subsequent parts of the burst cycle are held in a buffer after the first access. An increment signal to the SRAM causes the next data to appear on its output. Thus the wait states needed for the first access can be reduced for the subsequent parts of the burst.

Many burst SRAMs support both interleaved and linear burst modes. On the commonly available 32K x 32 SRAMs in a 100-pin TQPF package, pin 31 controls the burst mode. If the pin is tied high or left floating, interleaved burst mode is selected. Tying the pin low selects linear burst mode.

Using COASt to Implement L2 Cache

If L2 cache is to be implemented using a COASt (Cache On A Stick) module, we recommend that only modules compliant with Intel's** COASt specification Revision 1.4 or later should be used. Modules built to earlier specification may suffer from 'ringing' on the data lines depending on whether or not the drivers on the SRAM memory devices fall into the 'strong' category. Ringing on the data lines, especially during the CPU Set-Up period, can cause the CPU to lock up or to act in unpredictable ways. Revision 1.4 of the specification details the use of damping resistors in series with the data lines to attenuate the magnitude of the ringing to acceptable levels.

[1] The IBM 6x86 and 6x86L microprocessor is designed by Cyrix Corp., and manufactured by IBM Microelectronics.

Checklist for enabling Linear Burst

The following items need to be verified for a motherboard to support linear burst.

___ BIOS is updated to support linear burst

___ Chipset supports Linear Burst

___ Synchronous burst SRAMs support Linear Burst

___ Motherboard or COAST module provides a jumper to select linear burst mode

References

- 1995 Static RAMs Data Book, Document N. 60318, NEC Electronics Inc.
- COASt 1.4: Flexible Cache Solution for the Intel 430FX PCIset Rev 1.4, Intel, January 1996