



# AMD-K6™ E

## High-Performance, AMD-K6 Embedded Processor

### DISTINCTIVE CHARACTERISTICS

- **Advanced 6-Issue RISC86® Superscalar Microarchitecture**
  - Seven parallel specialized execution units
  - Multiple sophisticated x86-to-RISC86® instruction decoders
  - Advanced two-level branch prediction
  - Speculative execution
  - Out-of-order execution
  - Register renaming and data forwarding
  - Issues up to six RISC86 instructions per clock
- **High-Performance IEEE 754-Compatible and 854-Compatible Floating-Point Unit**
- **High-Performance Industry-Standard MMX™ Instructions**
- **Large On-Chip Split 64-Kbyte Level-One (L1) Cache**
  - 32-Kbyte instruction cache with additional predecode cache
  - 32-Kbyte writeback dual-ported data cache
  - MESI protocol support
- **321-Pin Ceramic PGA (Socket 7 Compatible) Package**
- **Industry-Standard System Management Mode (SMM)**
- **IEEE 1149.1 Boundary Scan**
- **x86 Binary Software Compatibility**
- **0.25-Micron Process Technology**

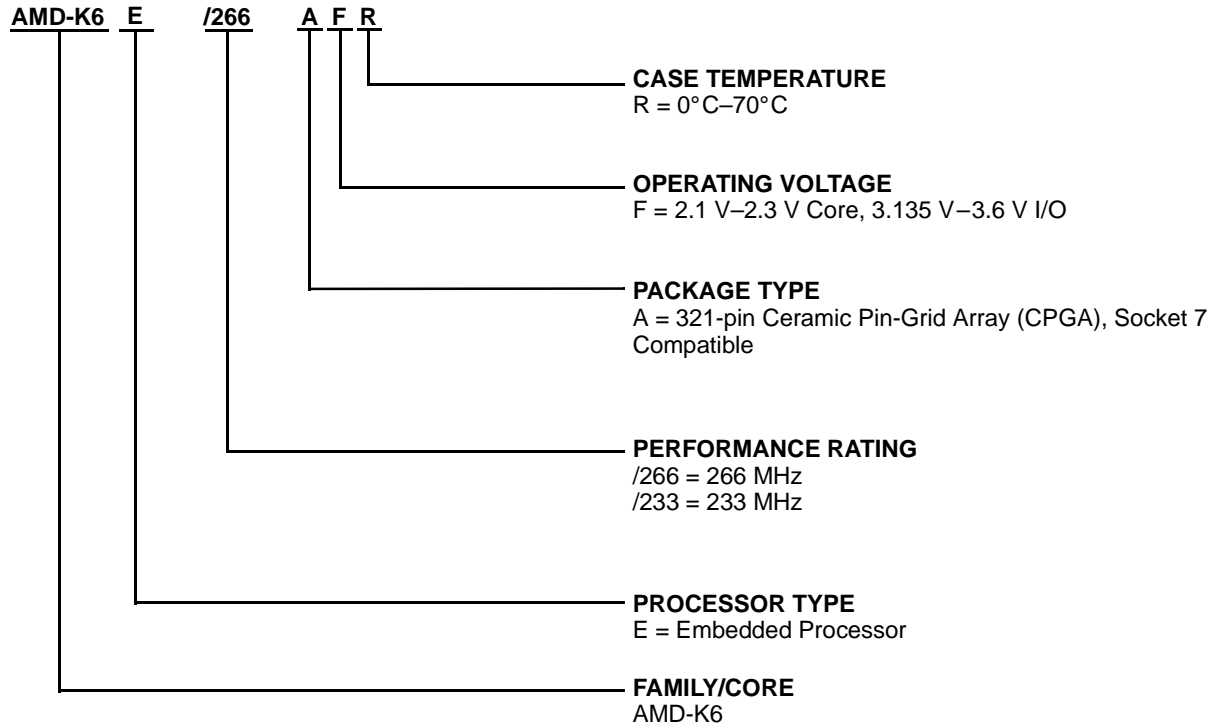
### GENERAL DESCRIPTION

**Note:** This data sheet provides information specific to the AMD-K6E processor. For more information about the AMD-K6E processor, see the Model 7 section of the AMD-K6 Processor Data Sheet, order #20695.

With the AMD-K6E embedded processor, AMD continues to deliver leading-edge processor solutions. Based on the highly successful AMD-K6 processor with 0.25-micron process technology, the AMD-K6E processor delivers high performance with a low core voltage and low power dissipation. This new, embedded version of the AMD-K6 processor continues to leverage today's cost-effective infrastructure to deliver a superior price/performance solution.

As a member of AMD's E86™ family of embedded x86-based processors, the AMD-K6E processor extends the range of software-compatible performance allowing existing x86 designs and software to be used in high-performance products. In addition to a wide selection of inexpensive development tools, compilers, debuggers, chip sets, and PC operating systems, the AMD-K6E processor is also supported by a number of real-time operating systems (RTOS) such as QNX, pSOS, RTXC, and Windows® CE. This compatibility and support result in decreased development costs and improved time to market.

**ORDERING INFORMATION**

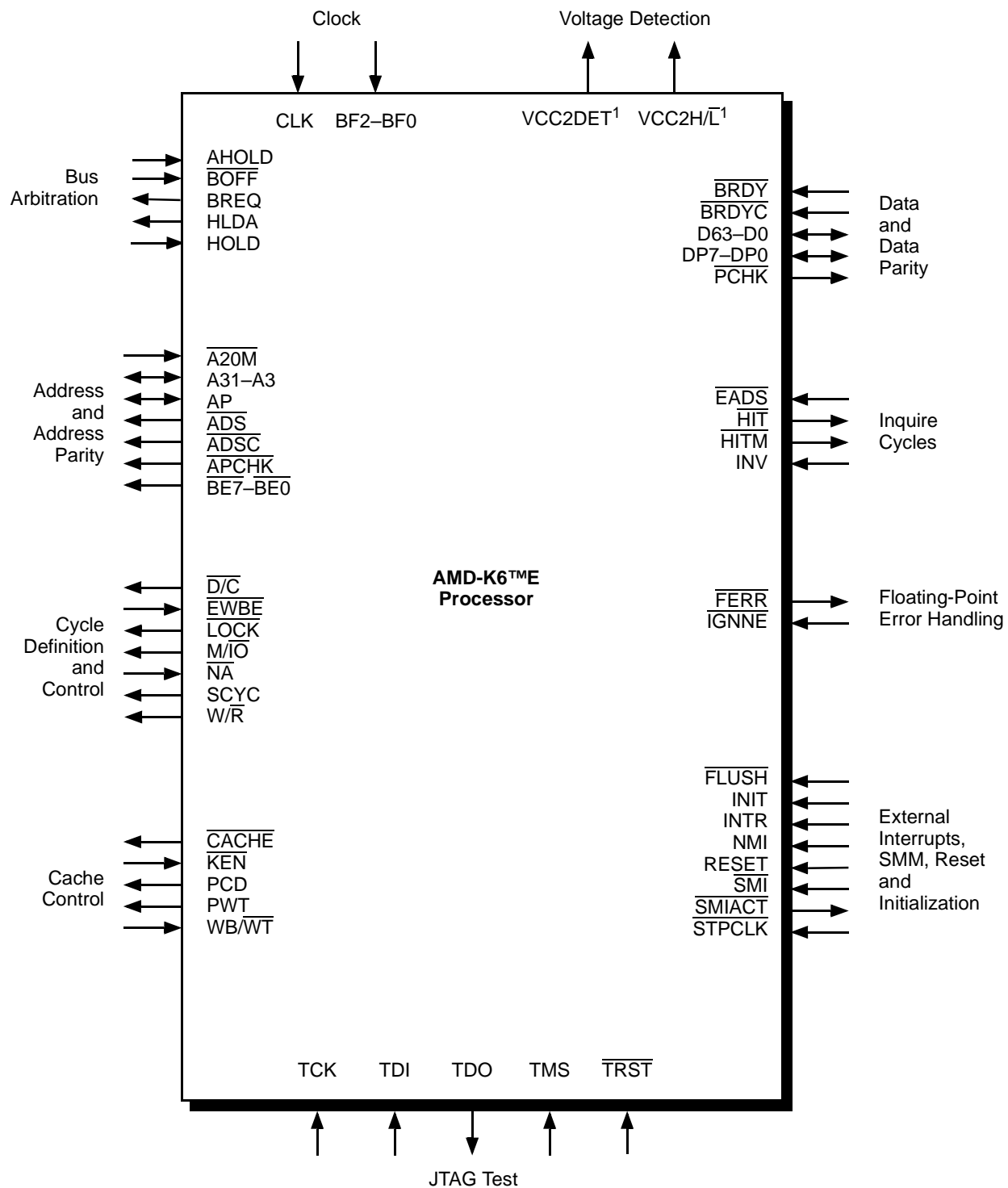


Valid Combinations	
AMD-K6E/266 AMD-K6E/233	AFR

**Valid Combinations**

Valid combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

# LOGIC DIAGRAM BY INTERFACE



**Notes:**

1. For information about the VCC2DET and VCC2H/L pins, see Chapter 26, "Signal Descriptions," in the AMD-K6 Processor Data Sheet, order #20695.

## ARCHITECTURAL OVERVIEW

Figure 1 shows the block diagram for the AMD-K6E embedded processor. The sections that follow describe the features of the part.

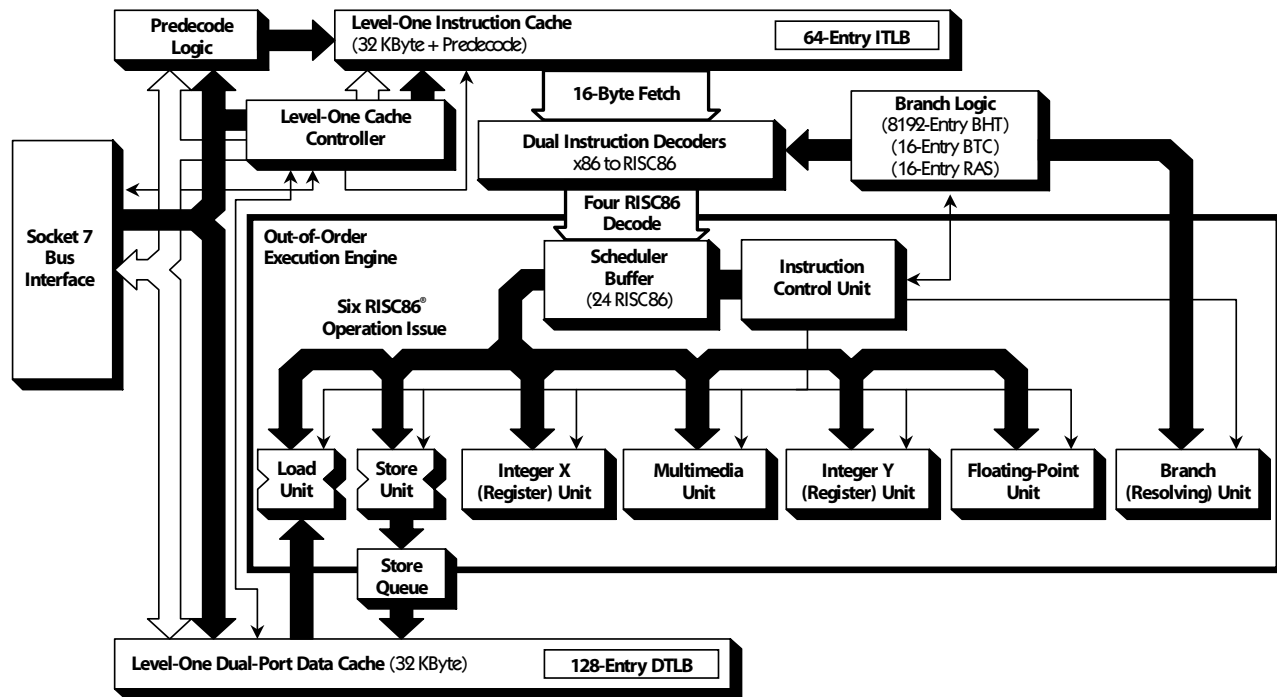


Figure 1. AMD-K6™E Embedded Processor Block Diagram

### The AMD-K6™E Processor

The AMD-K6E embedded processor is function- and pin-compatible with the industry-leading AMD-K6 processor (Model 7). It is an excellent choice for embedded applications that require a high-performance x86-compatible processor such as central office switches, network routers, point-of-sale terminals, information appliances, and Socket 7/ Windows based single-board computers.

### The AMD-K6™ Processor Core

The AMD-K6E embedded processor is based on the AMD-K6 processor (Model 7), and it maintains pin, function, and software compatibility.

To provide industry-leading performance, the AMD-K6 processor core incorporates the innovative and efficient RISC86 microarchitecture, a large 64-Kbyte level-one cache (32-Kbyte dual-ported data cache, 32-Kbyte instruction cache with predecode data), a powerful IEEE 754-compatible and 854-compatible floating-point execution unit, and a high-performance multimedia execution unit for executing industry-standard MMX™ instructions. These features have been combined to deliver industry leadership in

16-bit and 32-bit performance.

The AMD-K6 processor's RISC86 microarchitecture is a decoupled decode/execution superscalar design that implements state-of-the-art design techniques to achieve leading-edge performance. Advanced design techniques implemented in the AMD-K6 include multiple x86 instruction decode, single-clock internal RISC operations, seven execution units that support superscalar operation, out-of-order execution, data forwarding, speculative execution, and register renaming. In addition, the processor supports state-of-the-art advanced branch prediction logic by implementing an 8192-entry branch history table (the industry's only branch target cache) and a return address stack, which combine to deliver an extremely high prediction rate. These design techniques enable the AMD-K6 processor to issue, execute, and retire multiple x86 instructions per clock, resulting in excellent scalable performance.

Designed to run both 16-bit and 32-bit software, the AMD-K6 processor is x86 binary-code compatible. AMD's extensive experience through four generations of x86 processors has been carefully integrated into the AMD-K6 to provide complete compatibility with

Windows 3.x, Windows CE, Windows 95, Windows 98, Windows NT®, DOS, OS/2, UNIX, Solaris, NetWare®, Vines, and other leading x86 operating systems and applications. The AMD-K6 processor is Socket 7 compatible, allowing the processor to be quickly and easily integrated into a mature and cost-effective industry-standard infrastructure of motherboards, chip sets, power supplies, and thermal solutions.

AMD has designed, manufactured, and delivered over 50 million Microsoft Windows compatible processors. The AMD-K6 processor is one in a long line of processors.

With its combination of state-of-the-art features, industry-leading performance, high-performance multimedia engine, full x86 compatibility, and low-cost

infrastructure, the AMD-K6E embedded processor is an excellent choice for high-performance embedded applications and fast time to market.

### Maximum Frequency

Table 1 shows the maximum CPU and maximum bus frequencies for the AMD-K6E processor.

**Table 1. Maximum Frequency**

Processor	CPU Clock Max. Frequency	Bus Input Clock Max. Frequency
AMD-K6™E/266	266 MHz	66 MHz
AMD-K6E/233	233 MHz	66 MHz

## OPERATING RANGES

The functional operation of the AMD-K6E processor is designed to work within the voltage and temperature parameters defined in Table 2.

**Table 2. AMD-K6™E Operating Ranges**

Parameter	Minimum	Typical	Maximum
$V_{CC2}^{1,2}$	2.1 V	2.2 V	2.3 V
$V_{CC3}^1$	3.135 V	3.3 V	3.6 V
$T_{CASE}$	0°C	—	70°C

**Notes:**

- $V_{CC2}$  and  $V_{CC3}$  are referenced from  $V_{SS}$ .
- $V_{CC2}$  specification for 2.2 V components.

## ABSOLUTE RATINGS

Exposure to conditions outside the operating ranges listed in Table 2 for extended periods of time can affect long-term reliability. Permanent damage can occur if the absolute ratings listed in Table 3 are exceeded.

**Table 3. AMD-K6™E Absolute Ratings**

Parameter	Minimum	Maximum
$V_{CC2}$	-0.5 V	2.5 V
$V_{CC3}$	-0.5 V	3.6 V
$V_{PIN}^1$	-0.5 V	$V_{CC3} + 0.5 V$ and $\leq 4.0 V$
$T_{CASE}$ (under bias)	-65°C	+110°C
$T_{STORAGE}$	-65°C	+150°C

**Notes:**

- $V_{PIN}$  (the voltage on any I/O pin) must not be greater than 0.5 V above the voltage being applied to  $V_{CC3}$ . In addition, the  $V_{PIN}$  voltage must never exceed 4.0 V.

## POWER DISSIPATION

Table 4 contains the typical and maximum power dissipation of the AMD-K6E processor during normal and reduced power states.

**Table 4. AMD-K6™E Typical and Maximum Power Dissipation**

<b>Clock Control State</b>	<b>233 MHz</b>	<b>266 MHz</b>
Normal (Maximum Thermal Power) <sup>1</sup>	13.50 W	14.55 W
Normal (Typical Thermal Power) <sup>2</sup>	8.10 W	8.75 W
Stop Grant / Halt (Maximum) <sup>3</sup>	2.46 W	2.48 W
Stop Clock (Maximum) <sup>4</sup>	2.25 W	2.25 W

**Notes:**

1. The maximum power dissipated in the normal clock control state must be taken into account when designing a solution for thermal dissipation for the AMD-K6E processor. Maximum power is determined for the worst-case instruction sequence or function for the listed clock control states with  $V_{CC2} = 2.2$  V and  $V_{CC3} = 3.3$  V.
2. Typical power is determined for the typical instruction sequences or functions associated with normal system operation with  $V_{CC2} = 2.2$  V and  $V_{CC3} = 3.3$  V.
3. The CLK signal and the internal PLL are still running but most internal clocking has stopped.
4. The CLK signal, the internal PLL, and all internal clocking has stopped.

## THERMAL SPECIFICATIONS

The AMD-K6E processor operating specifications call for the case temperature ( $T_C$ ) to be in the range of 0°C to 70°C for the CPGA package.

The ambient temperature ( $T_A$ ) is not specified as long as the case temperature is not violated. The case temperature must be measured on the top center of the package.

Table 5 shows the thermal specifications derated,

based on operating the CPU at frequencies lower than the maximum rated frequency.

For more information about the AMD-K6E thermal specifications, see Chapter 38, “Thermal Design” in the *AMD-K6 Processor Data Sheet*, order #20695. For information about thermal solutions, see the *AMD-K6 Processor Thermal Solution Design Application Note*, order #21085.

**Table 5. AMD-K6™E Thermal Power Derating Based On Lower CPU Frequencies**

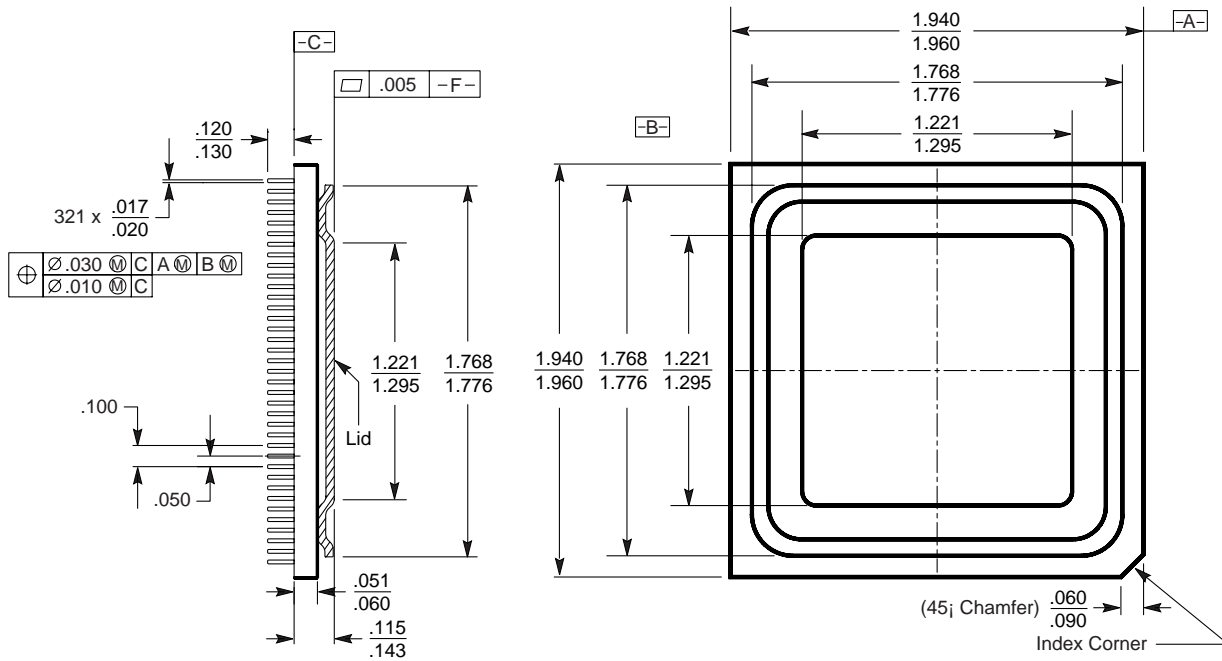
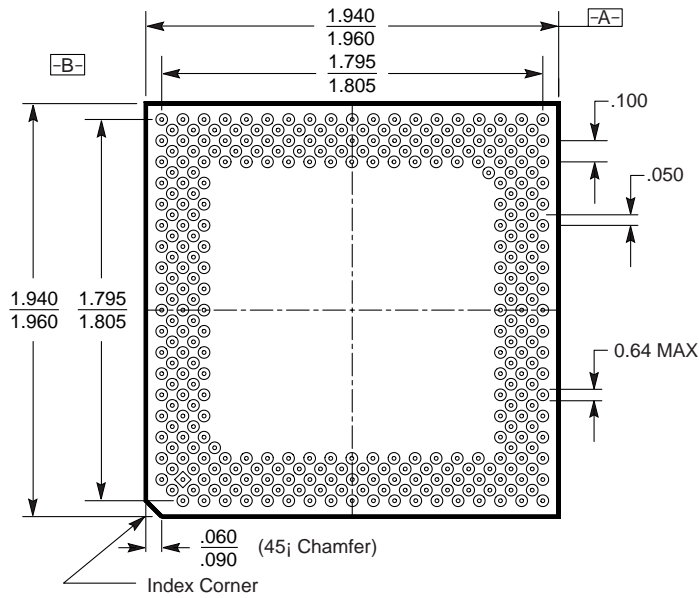
Frequency	Max. $I_{CC2}$ (core) $V_{CC2} = 2.2\text{ V} \pm 100\text{ mV}^1$	Max. $I_{CC3}$ (I/O) $V_{CC3} = 3.3\text{ V} + 300\text{ mV}, -165\text{ mV}^2$	Max. Thermal Power <sup>3</sup>	Typical Thermal Power <sup>4</sup>	Clock Multiple	BF2–BF0
133 MHz	3.95 A	0.46 A	8.60 W	5.20 W	2.0X	110b
166 MHz	4.95 A	0.48 A	10.50 W	6.30 W	2.5X	100b
200 MHz	5.95 A	0.50 A	12.45 W	7.50 W	3.0X	101b
233 MHz	6.50 A	0.52 A	13.50 W	8.10 W	3.5X	111b
266 MHz	7.05 A	0.54 A	14.55 W	8.75 W	4.0X	010b

**Notes:**

1. Max.  $I_{CC2}$  specification is taken at  $V_{CC2} = 2.3\text{ V}$ . (The maximum power supply current must be taken into account when designing a power supply.)
2. Max.  $I_{CC3}$  specification is taken at  $V_{CC3} = 3.6\text{ V}$ . (The maximum power supply current must be taken into account when designing a power supply.)
3. The maximum power dissipated in the normal clock control state must be taken into account when designing a solution for thermal dissipation for the AMD-K6E processor. Maximum power is determined for the worst-case instruction sequence or function for the listed clock control states with  $V_{CC2} = 2.2\text{ V}$  and  $V_{CC3} = 3.3\text{ V}$ .
4. Typical power is determined for the typical instruction sequences or functions associated with normal system operation with  $V_{CC2} = 2.2\text{ V}$  and  $V_{CC3} = 3.3\text{ V}$ .



**PHYSICAL DIMENSIONS**  
**CGF 321, Ceramic Pin-Grid Array (CPGA)**



SIDE VIEW OF CGF PGA

16-038-CP-5\_AC  
CGF321  
EU160  
1.13.99 Iv

**Note:** All dimensions are in inches.

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