PRELIMINARY

Am486™DX2

High-Performance, Clock-Doubled, 32-Bit Microprocessor

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Binary Compatible with Large Software Base**
  - — MS-DOS, OS/2, Windows
  - — UNIX, Windows NT
- **High Integration On-Chip**
  - — 8-Kbyte code and data cache
  - — Paged, virtual memory management
- **Easy To Use**
  - — Built-in self test
  - — Hardware debugging support
  - — Extensive third-party software support
- **Standard 168-Pin PGA Package**
- **IEEE 1149.1 Boundary Scan Compatibility on all versions**
- **High-performance Design**
  - — Frequent instructions execute in one clock
  - — 50-MHz clock frequencies
  - — 80-Million bytes/second burst bus at 25 MHz
  - — 0.7-micron CMOS process technology
  - — Dynamic bus sizing for 8-, 16-, and 32-bit buses
- **Complete 32-bit Architecture**
  - — All registers
  - — 8-, 16-, and 32-bit data types
- **Multiprocessor Support**
  - — Multiprocessor instructions
  - — Cache consistency
  - — Support for second-level cache
- **Pin-for-Pin Replacement of the i486DX**

GENERAL DESCRIPTION

The Am486DX2 CPU offers the highest performance for DOS, OS/2, Windows, and UNIX applications. It is 100% binary compatible with the 386 architecture. One million plus transistors integrate cache memory, and memory management on-chip while retaining binary compatibility with previous members of the x86 architectural family. Frequently used instructions execute in one cycle, resulting in RISC performance levels. An 8-Kbyte unified code and data cache combine with an 80-Million bytes/second burst bus at 25 MHz to ensure high system throughput.

New features enhance multiprocessing systems. New instructions speed manipulation of memory-based semaphores. On-chip hardware ensures cache consistency and provides hooks for multilevel caches.

The Am486DX2 microprocessor features boundary scan test signals. This provides additional testability features compatible with the IEEE Standard Test Access Port and Boundary Scan Architecture (IEEE Standard 1149.1 JTAG).

The built-in self test extensively tests on-chip logic, cache memory, and the on-chip paging translation cache. Debug features include breakpoint traps on code execution and data accesses.

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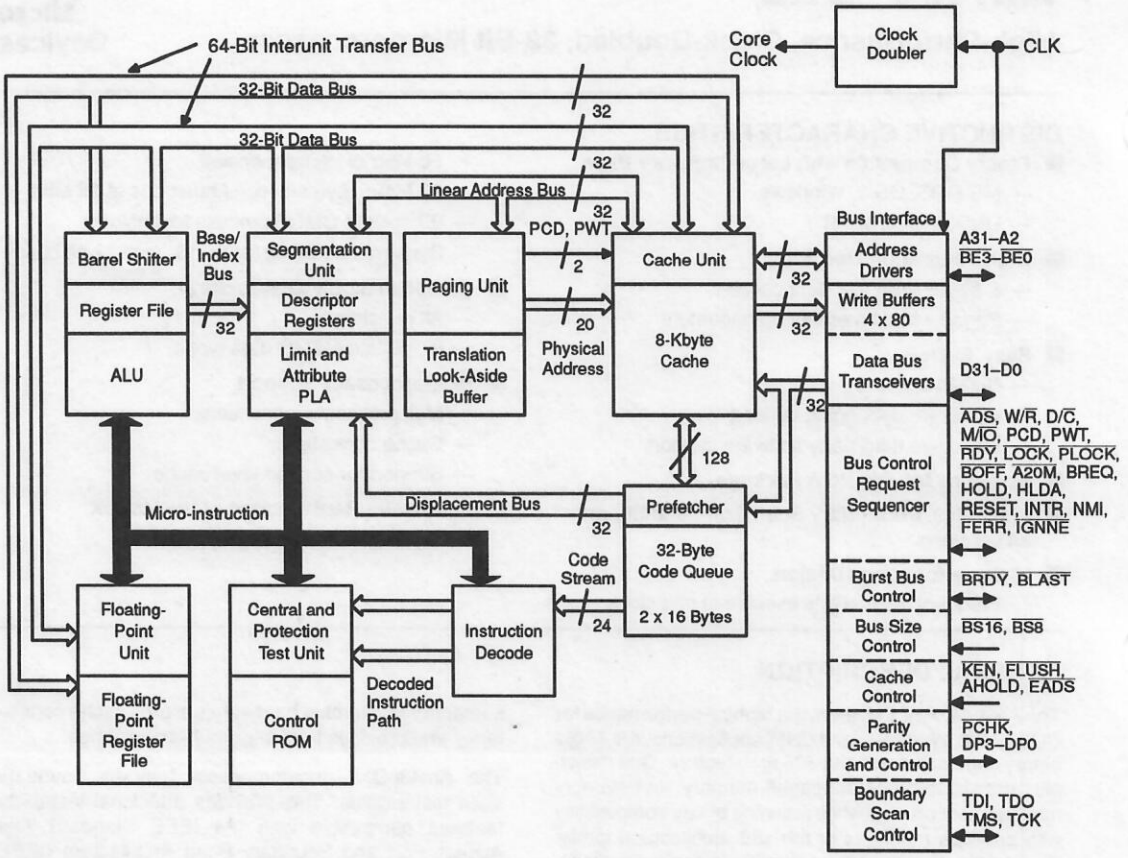
Am486 CPU PIPELINED 32-BIT MICROARCHITECTURE BLOCK DIAGRAM



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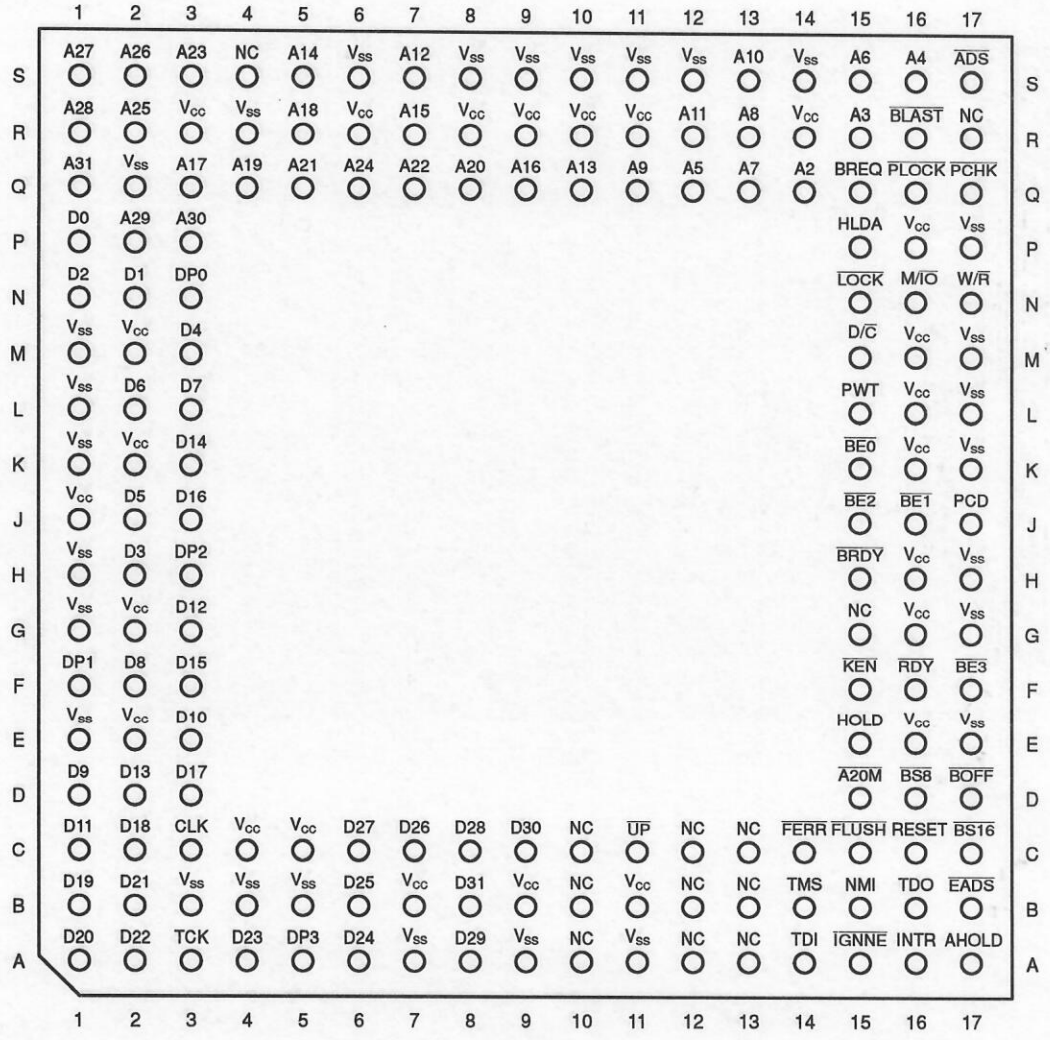
CONNECTION DIAGRAMS
Am486 CPU Pin Side View

168-Pin PGA (Pin Grid Array) Package



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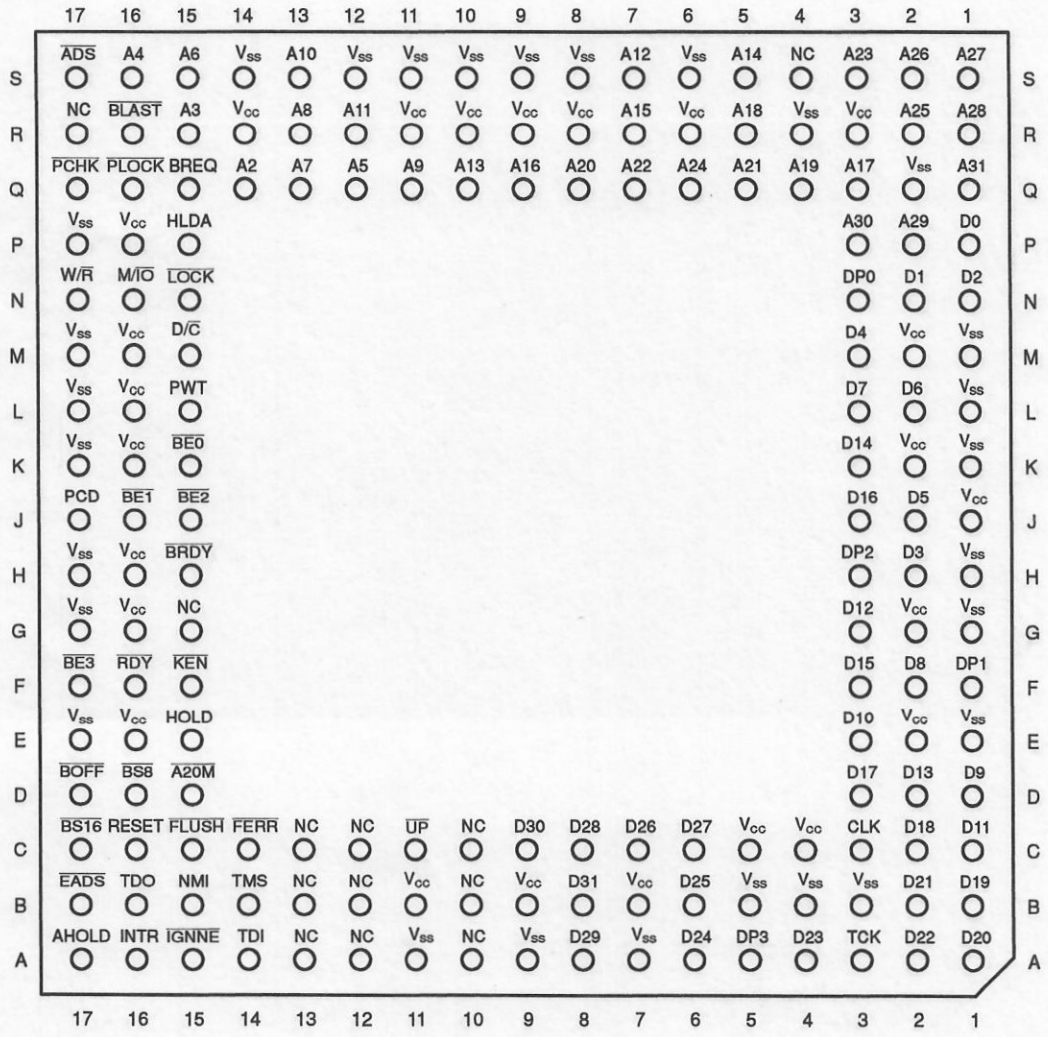
Notes:

NC = Not connected. To guarantee functionality with future revisions, these pins must not be connected.

CONNECTION DIAGRAMS
Am486 CPU Top Side View

168-Pin PGA (Pin Grid Array) Package



17852A–003

Notes:

NC = Not connected. To guarantee functionality with future revisions, these pins must not be connected.

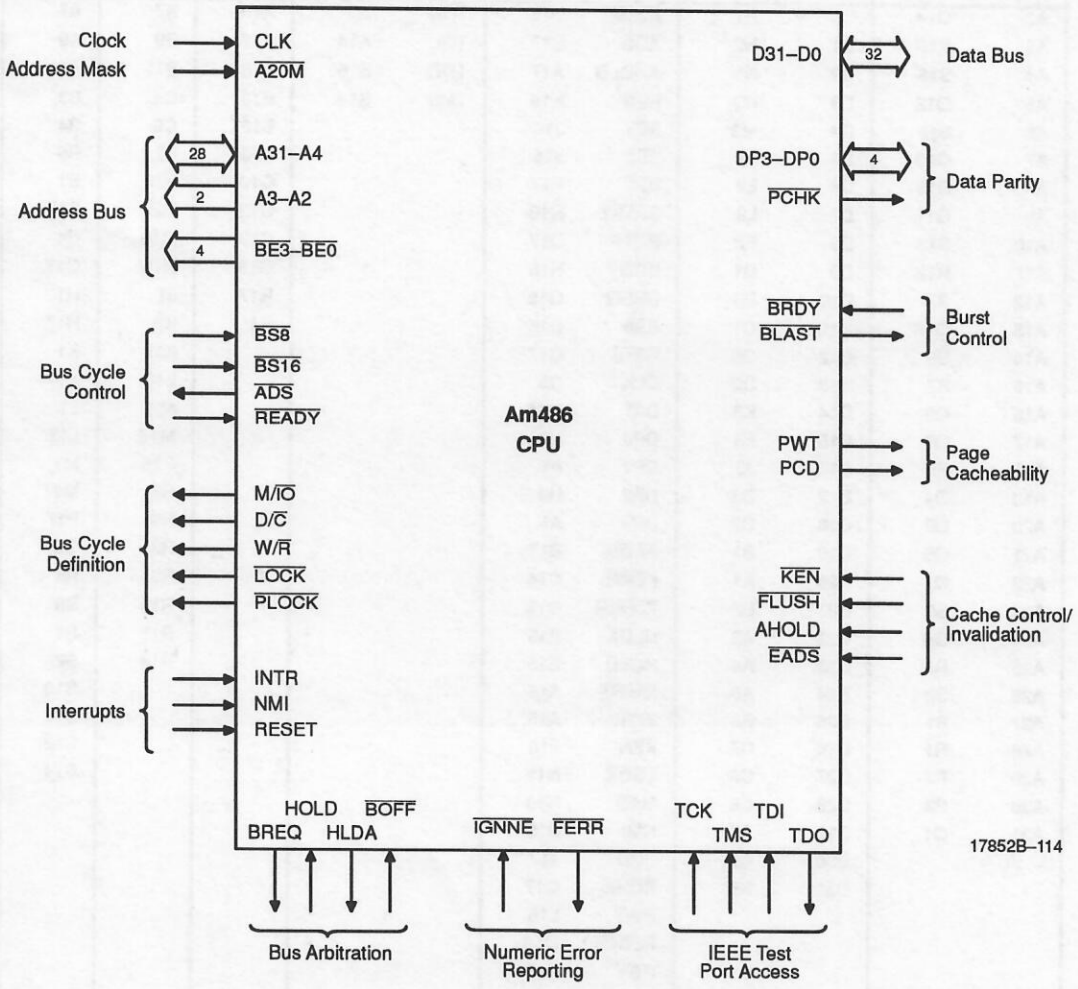
Am486DX2 CPU PIN DESIGNATIONS (FUNCTIONAL GROUPING)

Address		Data		Control		Test		NC	V_{cc}	V_{ss}
Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin No.	Pin No.	Pin No.
A2	Q14	D0	P1	$\overline{A20M}$	D15	TCK	A3	A10	B7	A7
A3	R15	D1	N2	$\overline{ADS}$	S17	TDI	A14	A12	B9	A9
A4	S16	D2	N1	AHOLD	A17	TDO	B16	A13	B11	A11
A5	Q12	D3	H2	$\overline{BE0}$	K15	TMS	B14	B10	C4	B3
A6	S15	D4	M3	$\overline{BE1}$	J16			B12	C5	B4
A7	Q13	D5	J2	$\overline{BE2}$	J15			B13	E2	B5
A8	R13	D6	L2	$\overline{BE3}$	F17			C10	E16	E1
A9	Q11	D7	L3	$\overline{BLAST}$	R16			C12	G2	E17
A10	S13	D8	F2	$\overline{BOFF}$	D17			C13	G16	G1
A11	R12	D9	D1	$\overline{BRDY}$	H15			G15	H16	G17
A12	S7	D10	E3	BREQ	Q15			R17	J1	H1
A13	Q10	D11	C1	$\overline{BS8}$	D16			S4	K2	H17
A14	S5	D12	G3	$\overline{BS16}$	C17				K16	K1
A15	R7	D13	D2	CLK	C3				L16	K17
A16	Q9	D14	K3	D/$\overline{C}$	M15				M2	L1
A17	Q3	D15	F3	DP0	N3				M16	L17
A18	R5	D16	J3	DP1	F1				P16	M1
A19	Q4	D17	D3	DP2	H3				R3	M17
A20	Q8	D18	C2	DP3	A5				R6	P17
A21	Q5	D19	B1	$\overline{EADS}$	B17				R8	Q2
A22	Q7	D20	A1	$\overline{FERR}$	C14				R9	R4
A23	S3	D21	B2	$\overline{FLUSH}$	C15				R10	S6
A24	Q6	D22	A2	HLDA	P15				R11	S8
A25	R2	D23	A4	HOLD	E15				R14	S9
A26	S2	D24	A6	$\overline{IGNNE}$	A15					S10
A27	S1	D25	B6	INTR	A16					S11
A28	R1	D26	C7	$\overline{KEN}$	F15					S12
A29	P2	D27	C6	$\overline{LOCK}$	N15					S14
A30	P3	D28	C8	M/$\overline{IO}$	N16					
A31	Q1	D29	A8	NMI	B15					
		D30	C9	PCD	J17					
		D31	B8	$\overline{PCHK}$	Q17					
				PWT	L15					
				$\overline{PLOCK}$	Q16					
				$\overline{RDY}$	F16					
				RESET	C16					
				$\overline{UP}$(1)	C11					
				W/$\overline{R}$	N17					

Note:

1. *This pin was No-Connect on the Am486DX microprocessor. For compatibility with old designs it can still be left unconnected.*

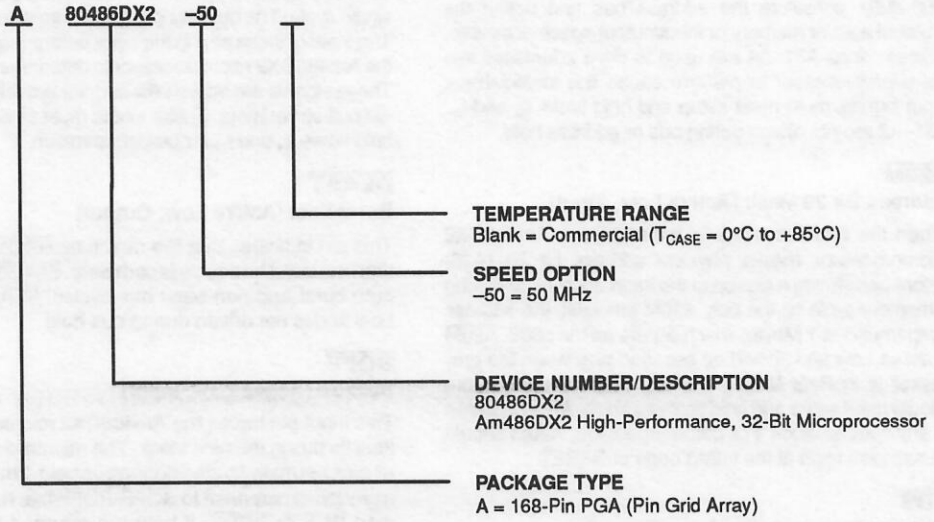
LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
A	80486DX2	–50

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTIONS

The following paragraphs define the pins (signals) of the Am486DX2 microprocessor.

A31–A4/A3–2

Address Lines (Inputs/Outputs)/(Outputs)

Pins A31–A2, together with the byte enable pins $\overline{BE3}$–$\overline{BE0}$, constitute the address bus and define the physical area of memory or input/output space accessed. Address lines A31–A4 are used to drive addresses into the microprocessor to perform cache line invalidations. Input signals must meet setup and hold times t_{22} and t_{23}. A31–A2 are not driven during bus or address hold.

$\overline{A20M}$

Address Bit 20 Mask (Active Low; Input)

When the address mask is asserted, the Am486DX2 microprocessor masks physical address bit 20 (A20) before performing a lookup to the internal cache or driving a memory cycle on the bus. $\overline{A20M}$ emulates the address wraparound at 1 Mbyte, which occurs on the 8086. $\overline{A20M}$ is active Low and should be asserted only when the processor is in Real Mode. This pin is asynchronous but should meet setup and hold times t_{20} and t_{21} for recognition in any specific clock. For proper operation, $\overline{A20M}$ should be sampled High at the falling edge of RESET.

$\overline{ADS}$

Address Status (Active Low; Output)

This pin is used to indicate that a valid bus cycle definition and address are available on the cycle definition lines and address bus. $\overline{ADS}$ is driven active in the same clock as the addresses are driven. $\overline{ADS}$ is active Low and is not driven during bus hold.

AHOLD

Address Hold (Active High; Input)

An address hold request allows another bus master access to the Am486DX2 microprocessor's address bus for a cache invalidation cycle. The Am486DX2 microprocessor stops driving its address bus in the clock following AHOLD going active. Only the address bus is floated during address hold; the remainder of the bus remains active. AHOLD is active High and is provided with a small internal pull-down resistor. For proper operation, AHOLD must meet setup and hold times t_{18} and t_{19}.

$\overline{BE3}$–$\overline{BE0}$

Byte Enables (Active Low; Outputs)

The address bus byte-enable pins indicate active bytes during read and write cycles. During the first cycle of a cache fill, the external system should assume that all byte enables are active. $\overline{BE3}$ applies to D31–D24, $\overline{BE2}$ applies to D23–D16, $\overline{BE1}$ applies to D15–D8, and $\overline{BE0}$ applies to D7–D0. $\overline{BE3}$–$\overline{BE0}$ are active Low and are not driven during bus hold.

$\overline{BS8}$/$\overline{BS16}$

Bus Size 8 (Active Low; Input)/Bus Size 16 (Active Low; Input)

The bus sizing pins cause the Am486DX2 microprocessor to run multiple bus cycles to complete a request from devices that cannot provide or accept 32 bits of data in a single cycle. The bus sizing pins are sampled every clock. The state of these pins in the clock before ready is used by the Am486DX2 microprocessor to determine the bus size. These signals are active Low and are provided with internal pull-up resistors. These inputs must satisfy setup and hold times t_{14} and t_{15} for proper operation.

$\overline{BLAST}$

Burst Last (Active Low; Output)

This pin indicates that the next time $\overline{BRDY}$ is returned then the burst bus cycle is complete. $\overline{BLAST}$ is active for both burst and non-burst bus cycles. $\overline{BLAST}$ is active Low and is not driven during bus hold.

$\overline{BOFF}$

Backoff (Active Low; Input)

This input pin forces the Am486DX2 microprocessor to float its bus in the next clock. The microprocessor floats all pins normally floated during bus hold, but HLDA is not asserted in response to $\overline{BOFF}$. $\overline{BOFF}$ has higher priority than $\overline{RDY}$ or $\overline{BRDY}$; if both are returned in the same clock, $\overline{BOFF}$ takes effect. The microprocessor remains in bus hold until $\overline{BOFF}$ is negated. If a bus cycle is in progress when $\overline{BOFF}$ is asserted, the cycle is restarted. $\overline{BOFF}$ is active Low and must meet setup and hold times t_{18} and t_{19} for proper operation.

$\overline{BRDY}$

Burst Ready Input (Active Low; Input)

The $\overline{BRDY}$ signal performs the same cycle during a burst cycle that $\overline{RDY}$ performs during a non-burst cycle. $\overline{BRDY}$ indicates that the external system has presented valid data in response to a read, or that the external system has accepted data in response to write. $\overline{BRDY}$ is ignored when the bus is idle and at the end of the first clock in a bus cycle.

$\overline{BRDY}$ is sampled in the second and subsequent clocks of a burst cycle. The data presented on the data bus is strobed into the microprocessor when $\overline{BRDY}$ is sampled active. If $\overline{RDY}$ is returned simultaneously with $\overline{BRDY}$, $\overline{BRDY}$ is ignored and the burst cycle is prematurely aborted.

$\overline{BRDY}$ is active Low and is provided with a small pull-up resistor. $\overline{BRDY}$ must satisfy the setup and hold times t_{16} and t_{17}.

BREQ

Internal Cycle Pending (Output)

BREQ indicates that the Am486DX2 microprocessor has internally generated a bus request. BREQ is generated whether or not the Am486DX2 microprocessor is

driving the bus. BREQ is active High and is never floated, except during three-state test mode (see $\overline{\text{FLUSH}}$).

CLK
Clock (Input)

The CLK input provides the fundamental timing and the internal operating frequency for the Am486DX2 microprocessor. All external timing parameters are specified with respect to the rising edge of CLK.

D31–D0
Data Lines (Inputs/Outputs)

Lines D7–D0 define the least significant byte of the bus while lines D31–D24 define the most significant byte of the data bus. These signals must meet setup and hold times t_{22} and t_{23} for proper operation on reads. These pins are driven during the second and subsequent clocks of write cycles.

D/$\overline{\text{C}}$
Data/Control (Output)

This bus cycle definition pin distinguishes data cycles, either memory or I/O, from control cycles. These control cycles are: interrupt acknowledge, halt, and instruction fetching.

DP3–DP0
Data Parity (Inputs/Outputs)

Data parity is generated on all write data cycles with the same timing as the data driven by the Am486DX2 microprocessor. Even parity information must be driven back into the microprocessor on the data parity pins with the same timing as read information; this ensures that the correct parity check status is indicated by the Am486DX2 microprocessor. The signals read on these pins do not affect program execution.

Input signals must meet setup and hold times t_{22} and t_{23}. DP3–DP0 should be connected to V_{CC} through a pull-up resistor in systems not using parity. DP3–DP0 are active High and are driven during the second and subsequent clocks of write cycles.

$\overline{\text{EADS}}$
Valid External Address (Active Low; Input)

This address indicates a valid external address has been driven onto the Am486DX2 microprocessor address pins. This address is used to perform an internal cache invalidation cycle. $\overline{\text{EADS}}$ is active Low and is provided with an internal pull-up resistor. $\overline{\text{EADS}}$ must satisfy setup and hold times t_{12} and t_{13} for proper operation.

$\overline{\text{FERR}}$
Floating-Point Error (Active Low; Output)

Driven active when a floating-point error occurs, $\overline{\text{FERR}}$ is similar to the $\overline{\text{ERROR}}$ pin on a 387 math coprocessor. $\overline{\text{FERR}}$ is included for compatibility with systems using DOS-type floating-point error reporting. $\overline{\text{FERR}}$ is active Low and is not floated during bus hold, except during three-state test mode (see $\overline{\text{FLUSH}}$).

$\overline{\text{FLUSH}}$
Cache Flush (Active Low; Input)

$\overline{\text{FLUSH}}$ forces the Am486DX2 microprocessor to flush its entire internal cache. This input pin is active Low and need only be asserted for one clock. $\overline{\text{FLUSH}}$ is asynchronous but setup and hold times t_{20} and t_{21} must be met for recognition in any specific clock. $\overline{\text{FLUSH}}$ being sampled Low in the clock before the falling edge of RESET causes the Am486DX2 microprocessor to enter the three-state test mode.

HLDA
Hold Acknowledge (Output)

The HLDA signal is activated in response to a hold request presented on the HOLD pin. HLDA indicates that the Am486DX2 microprocessor has given the bus to another local bus master. HLDA is driven active in the same clock in which the Am486DX2 microprocessor floats its bus. HLDA is driven inactive when leaving bus hold. HLDA is active High and remains driven during bus hold. HLDA is never floated except during three-state test mode (see $\overline{\text{FLUSH}}$).

HOLD
Bus Hold Request (Input)

HOLD gives another bus master control of the Am486DX2 microprocessor bus. In response to HOLD going active, the Am486DX2 microprocessor floats most of its output and input/output pins. HLDA is asserted after completing the current bus cycle, burst cycle, or sequence of locked cycles. The Am486DX2 microprocessor remains in this state until HOLD is deasserted. HOLD is active High and is not provided with an internal pull-down resistor. HOLD must satisfy setup and hold times t_{18} and t_{19} for proper operation.

$\overline{\text{IGNNE}}$
Ignore Numeric Error (Active Low; Input)

When this pin is asserted, the Am486DX2 microprocessor ignores a numeric error and continues executing non-control floating-point instructions. When $\overline{\text{IGNNE}}$ is deasserted, the Am486DX2 microprocessor freezes on a non-control floating-point instruction if a previous floating-point instruction caused an error. $\overline{\text{IGNNE}}$ has no effect when the NE bit in Control Register 0 is set. $\overline{\text{IGNNE}}$ is active Low and is provided with a small internal pull-up resistor. $\overline{\text{IGNNE}}$ is asynchronous but setup and hold times t_{20} and t_{21} must be met to insure recognition on any specific clock.

INTR
Maskable Interrupt (Input)

When asserted, this signal indicates that an external interrupt has been generated. If the internal interrupt

flag is set in EFLAGS, active interrupt processing is initiated. The Am486DX2 microprocessor generates two locked interrupt acknowledge bus cycles in response to the INTR pin going active. INTR must remain active until the interrupt acknowledges have been performed to ensure that the interrupt is recognized. INTR is active High and is not provided with an internal pull-down resistor. INTR is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

$\overline{KEN}$

Cache Enable (Active Low; Input)

$\overline{KEN}$ is used to determine whether the current cycle is cacheable. When the Am486DX2 microprocessor generates a cacheable cycle and $\overline{KEN}$ is active one clock before $\overline{RDY}$ or $\overline{BRDY}$ during the first transfer of the cycle, the cycle becomes a cache line fill cycle. Returning $\overline{KEN}$ active one clock before $\overline{RDY}$ during the last read in the cache line fill causes the line to be placed in the on-chip cache. $\overline{KEN}$ is active Low and is provided with a small internal pull-up resistor. $\overline{KEN}$ must satisfy setup and hold times t_{14} and t_{15} for proper operation.

$\overline{LOCK}$

Bus Lock (Active Low; Output)

This pin indicates that the current bus cycle is locked. The Am486DX2 microprocessor does not allow a bus hold when $\overline{LOCK}$ is asserted (but address holds are allowed). $\overline{LOCK}$ goes active in the first clock of the first locked bus cycle and goes inactive after the last clock of the last locked bus cycle. The last locked cycle ends when ready is returned. $\overline{LOCK}$ is active Low and is not driven during bus hold. Locked read cycles will not be transformed into cache fill cycles if $\overline{KEN}$ is returned active.

M/$\overline{IO}$

Memory (Input/Output) (Output)

This bus cycle definition pin distinguishes memory cycles from input/output cycles.

NMI

Non-maskable Interrupt (Input)

The NMI request signal indicates that an external non-maskable interrupt has been generated. NMI is rising edge sensitive. NMI must be held Low for at least four CLK periods before this rising edge. NMI is not provided with an internal pull-down resistor. NMI is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

PCD/PWT

Page Cache Disable/Page Write-Through (Outputs)

These pins reflect the state of the page attribute bits, PWT and PCD, in the page table entry or page directory entry. If paging is disabled or for unpaged cycles, PWT and PCD reflect the state of the PWT and PCD bits in Control Register 3. PWT and PCD have the same timing as the cycle definition pins (M/$\overline{IO}$, D/$\overline{C}$, and W/$\overline{R}$). PWT and PCD are active High and are not driven during bus hold. PCD is masked by the Cache Disable Bit (CD) in Control Register 0.

$\overline{PCHK}$

Parity Status (Active Low; Output)

Parity status is driven on the $\overline{PCHK}$ pin the clock after ready for read operations. The parity status is for data sampled at the end of the previous clock. A parity error is indicated by $\overline{PCHK}$ being Low. Parity status is only checked for enabled bytes as indicated by the byte enable and bus size signals. $\overline{PCHK}$ is valid only in the clock immediately after read data is returned to the microprocessor; at all other times $\overline{PCHK}$ is inactive High. $\overline{PCHK}$ is never floated, except during three-state test mode (see $\overline{FLUSH}$).

$\overline{PLOCK}$

Pseudo-Lock (Active Low; Output)

$\overline{PLOCK}$ indicates that the current bus transaction requires more than one bus cycle to complete. Examples of such operations are segment table descriptor reads (64 bits) and cache line fills (128 bits). The Am486DX2 microprocessor drives $\overline{PLOCK}$ active until the addresses for the last bus cycle of the transaction have been driven, regardless of whether $\overline{RDY}$ or $\overline{BRDY}$ have been returned.

$\overline{PLOCK}$ is a function of the $\overline{BS8}$, $\overline{BS16}$, and $\overline{KEN}$ inputs. $\overline{PLOCK}$ should be sampled on if the clock ready is returned. $\overline{PLOCK}$ is active Low and is not driven during bus hold.

RESET

Reset (Active High; Input)

RESET forces the Am486DX2 microprocessor to begin execution at a known state. The microprocessor cannot begin execution of instructions until at least 1 ms after V_{CC} and CLK have reached their proper DC and AC specifications. The RESET pin should remain active during this time to ensure proper microprocessor operation. RESET is active High. RESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in specific clock.

$\overline{RDY}$

Non-Burst Ready (Active Low; Input)

This pin indicates that the current bus cycle is complete. $\overline{RDY}$ indicates that the external system has presented valid data on the data pins in response to a read, or that the external system has accepted data from the Am486DX2 microprocessor in response to a write. $\overline{RDY}$ is ignored when the bus is idle and at the end of the bus cycle's first clock.

$\overline{RDY}$ is active during address hold. Data can be returned to the processor while AHOLD is active.

$\overline{RDY}$ is active Low and is not provided with an internal pull-up resistor. $\overline{RDY}$ must satisfy setup and hold times t_{16} and t_{17} for proper chip operation.

TCK
Test Clock (Input)

Test Clock is an input to the Am486 CPU and provides the clocking function required by the JTAG boundary scan feature. TCK is used to clock state information and data into and out of the component. State select information and data are clocked into the component on the rising edge of TCK on TMS and TDI, respectively. Data is clocked out of the component on the falling edge of TCK on TDO.

TDI
Test Data Input (Input)

TDI is the serial input used to shift JTAG instructions and data into the component. TDI is sampled on the rising edge of TCK during the SHIFT-IR and the SHIFT-DR TAP (Tap Access Port) controller states. During all other tap controller states, TDI is a "don't care."

TDO
Test Data Output (Output)

TDO is the serial output used to shift JTAG instructions and data out of the component. TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR TAP controller states. At all other times, TDO is driven to the high impedance state.

TMS
Test Mode Select (Input)

TMS is decoded by the JTAG TAP to select the operation of the test logic. TMS is sampled on the rising edge of TCK. To guarantee deterministic behavior of the TAP controller, TMS is provided with an internal pull-up resistor.

W/$\overline{R}$
Write/Read (Output)

A bus cycle definition pin, W/$\overline{R}$ distinguishes write cycles from read cycles.

$\overline{UP}$
Write/Read (Input) (PQFP package only)

The upgrade Present pin forces the Am486DX2 CPU to three-state all its outputs and enter the power-down mode. When the Upgrade Present pin is sampled asserted by the CPU in the clock before the falling edge of RESET, the power-down mode is enabled. $\overline{UP}$ has no effect on the power-down status expect during this edge. The CPU is also forced to three-state all of its outputs immediately in response to this signal. The $\overline{UP}$ signal must remain asserted in order to keep the pins three-stated. $\overline{UP}$ is active Low and is provided with an internal pull-up resistor.

Table 1 Output Pins

Name	Active Level	Floated At
BREQ	High	
HLDA	High	
$\overline{BE3}$–$\overline{BE0}$	Low	Bus Hold
PCD/PWT	High	Bus Hold
W/$\overline{R}$, D/$\overline{C}$, M/$\overline{IO}$	High	Bus Hold
$\overline{LOCK}$	Low	Bus Hold
$\overline{PLOCK}$	Low	Bus Hold
$\overline{ADS}$	Low	Bus Hold
$\overline{BLAST}$	Low	Bus Hold
$\overline{PCHK}$	Low	
$\overline{FERR}$	Low	
A3–A2	High	Bus, Address Hold

Table 2 Input Pins

Name	Active Level	Synchronous/ Asynchronous
CLK		
RESET	High	Asynchronous
HOLD	High	Synchronous
AHOLD	High	Synchronous
$\overline{EADS}$	Low	Synchronous
$\overline{BOFF}$	Low	Synchronous
$\overline{FLUSH}$	Low	Asynchronous
$\overline{A20M}$	Low	Asynchronous
$\overline{BS16}$, $\overline{BS8}$	Low	Synchronous
$\overline{KEN}$	Low	Synchronous
$\overline{RDY}$	Low	Synchronous
$\overline{BRDY}$	Low	Synchronous
INTR	High	Asynchronous
NMI	High	Asynchronous
$\overline{IGNNE}$	Low	Asynchronous

Table 3 Input/Output Pins

Name	Active Level	Floated At
D31–D0	High	Bus Hold
DP3–DP0	High	Bus Hold
A31–A4	High	Bus, Address Hold

Table 4 Bus Cycle Definition

M/$\overline{IO}$	D/$\overline{C}$	W/$\overline{R}$	Bus Cycle Initiated
0	0	0	Interrupt Acknowledge
0	0	1	Halt/Special Cycle
0	1	0	I/O Read
0	1	1	I/O Write
1	0	0	Code Read
1	0	1	Reserved
1	1	0	Memory Read
1	1	1	Memory Write

Table 5 Test Pins

Name	Input or Output	Sampled/Driven On
TCK	Input	N/A
TDI	Input	Rising Edge of TCK
TDO	Output	Falling Edge of TCK
TMS	Input	Rising Edge of TCK

Am486DX2 CPU REGISTERS

Architectural Overview

The Am486DX2 microprocessor is a 32-bit architecture with on-chip memory management and cache memory units.

The Am486DX2 microprocessor contains all the features of the 386 microprocessor with enhancements to increase performance. The instruction set includes the complete 386 microprocessor instruction set along with extensions to serve new applications. The on-chip Memory Management Unit (MMU) is completely compatible with the 386 MMU. All software written for the 386 microprocessor and previous members of the x86 architectural family can run on the Am486DX2 microprocessor without any modifications.

Several enhancements have been added to the Am486DX2 microprocessor to increase performance. On-chip cache memory allows frequently used data and code to be stored on-chip, thereby reducing accesses to the external bus. RISC design techniques have been used to reduce instruction cycle times. A burst bus feature enables fast cache fills. All of these features combined lead to performance greater than twice that of a 386 microprocessor.

The Am486 microprocessor MMU consists of a segmentation unit and a paging unit. Segmentation allows management of the logical address space by providing easy data and code relocatibility and efficient sharing of global resources. The paging mechanism operates beneath segmentation and is transparent to the segmentation process. Paging is optional and can be disabled by system software. Each segment can be divided into one or more 4-Kbyte segments. To implement a virtual memory system, the Am486DX2 microprocessor supports full restartability for all page and segment faults.

Memory is organized into one or more variable length segments, each up to 4 Gbytes (2^{32} bytes) in size. A segment can have attributes associated with it. These attributes include its location, size, type (i.e., stack, code, or data), and protection characteristics. Each task on an Am486DX2 microprocessor can have a maximum of 16,381 segments, each up to 4 Gbytes in size. Thus, each task has a maximum of 64 Tbyte (terabytes) of virtual memory.

The segmentation unit provides four levels of protection for isolating and protecting applications and the operating system from each other. The hardware enforced protection allows high integrity system designs.

The Am486DX2 microprocessor has two modes of operation: Real Address Mode (Real Mode) and Virtual Address Mode (Protected Mode). In Real Mode, the Am486DX2 microprocessor operates as a very fast 8086. Real Mode is required primarily to set up the processor for Protected Mode operation. Protected Mode provides access to the sophisticated memory management paging and privilege capabilities of the processor.

Within Protected Mode, software can perform a task switch to enter into tasks designated as Virtual 8086 Mode tasks. Each Virtual 8086 task behaves with 8086 semantics, allowing 8086 software (an application program or an entire operating system) to execute.

The on-chip floating-point unit (FPU) operates in parallel with the arithmetic and logic unit and provides arithmetic instructions for a variety of numeric data types. The FPU executes numerous built-in transcendental functions (e.g., tangent, sine, cosine, and log functions) and conforms to the ANSI/IEEE standard 754-1985 for floating-point arithmetic.

The on-chip cache is 8 Kbytes. It is four-way set associative and follows a write-through policy. The on-chip cache includes features that provide flexibility in external memory system design. Individual pages can be designated as cacheable or non-cacheable by software or hardware. The cache can also be enabled and disabled by software or hardware.

Finally, the Am486DX2 microprocessor has features that facilitate high-performance hardware designs. The 1X clock eases high frequency board level designs, while the 2X clock doubler improves execution performance without increasing the board design complexity. This 2X clock doubler enhances all operations operating out of the cache and/or not blocked by external bus assesses. The burst bus feature enables fast cache fills.

DIFFERENCES BETWEEN THE Am486DX2 MICROPROCESSOR AND THE 386 MICROPROCESSOR, PLUS THE 387 MATH COPROCESSOR EXTENSION

The differences between the Am486DX2 microprocessor and the 386 microprocessor are due to performance enhancements. The differences between the microprocessors are listed below.

1. Instruction clock counts have been reduced to achieve higher performance.
2. The Am486DX2 microprocessor bus is significantly faster than the 386 microprocessor bus. Differences include a 1X clock, parity support, burst cycles, cacheable cycles, cache invalidate cycles, and 8-bit bus support.
3. To support the on-chip cache, new bits have been added to control register 0 (CD and NW), new pins have been added to the bus, and new bus cycle types have been added. The on-chip cache needs to be enabled after reset by clearing the CD and NW bit in CR0.
4. The complete 387 math coprocessor instruction set and register set have been added. No I/O cycles are performed during floating-point instructions. The instruction and data pointers are set to 0 after FINIT/FSAVE. Interrupt 9 can no longer occur, interrupt 13 occurs instead.
5. The Am486DX2 microprocessor supports new floating-point error reporting modes to guarantee DOS compatibility. These new modes require a new bit in control register 0 (NE) and new pins ($\overline{\text{FERR}}$ and $\overline{\text{IGNNE}}$).
6. In some cases $\overline{\text{FERR}}$ is asserted when the next floating-point instruction is encountered; and in other cases, it is asserted before the next floating-point instruction is encountered, depending upon the execution state the instruction causing exception. For both of these cases, the 387 math coprocessor asserts $\overline{\text{ERROR}}$ when the error occurs and does not wait for the next floating-point instruction to be encountered.
7. Six new instructions have been added:
   - Byte Swap (BSWAP)
   - Exchange-and-Add (XADD)
   - Compare and Exchange (CMPXCHG)
   - Invalidate Data Cache (INVD)
   - Write-back and Invalidate Data Cache (WBINVD)
   - Invalidate TLB Entry (INVLPG)
8. There are two new bits defined in control register 3, the page table entries and page directory entries (PCD and PWT).
9. A new page protection feature has been added. This feature requires a new bit in control register 0 (WP).
10. A new Alignment Check feature has been added. This feature requires a new bit in the flags register (AC) and a new bit in control register 0 (AM).
11. The replacement algorithm for the TLB has been changed from a random algorithm to a pseudo least recently used algorithm, like that used by the on-chip cache.
12. Three new testability registers, TR3, TR4, and TR5, have been added for testing the on-chip cache. TLB testability has been enhanced.
13. The prefetch queue has been increased from 16 bytes to 32 bytes. A jump always needs to execute after modifying code to guarantee correct execution of the new instruction.
14. After reset, the ID in the upper byte of the DX register is 04. The contents of the base registers, including the floating-point registers, can be different after reset.

ELECTRICAL DATA

The following sections describe recommended electrical connections for the Am486DX2 microprocessor and its electrical specifications.

Power and Grounding

Power Connections

The Am486DX2 microprocessor is implemented in CS14 technology and has modest power requirements. However, its high clock frequency output buffers can cause power surges as multiple output buffers drive new signal levels simultaneously. For clean, on-chip power distribution at high frequency, 24-V_{CC} and 28-V_{SS} pins feed the Am486DX2 microprocessor.

Power and ground connections must be made to all external V_{CC} and GND pins of the Am486DX2 microprocessor. On the circuit board, all V_{CC} pins must be connected on a V_{CC} plane. All V_{SS} pins must likewise be connected on a GND plane.

Power Decoupling Recommendations

Liberal decoupling capacitance should be placed near the Am486DX2 microprocessor. The Am486DX2 microprocessor, driving its 32-bit parallel address and data buses at high frequencies, can cause transient power surges, particularly when driving large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high-frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the Am486DX2 microprocessor, and decoupling capacitors as much as possible. Capacitors specifically for PGA packages are also commercially available.

Other Connection Recommendations

NC pins should always remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Active Low inputs should be connected to V_{CC} through a pull up resistor. Pull-ups in the range of 20 KΩ are recommended. Active High inputs should be connected to GND.

ABSOLUTE MAXIMUM RATINGS

Case Temperature under Bias .... −65°C to +110°C
Storage Temperature ..... −65°C to +150°C
Voltage on any pin
with respect to ground ..... −0.5 V to V_{CC} + 0.5 V
Supply voltage with
respect to V_{SS} ..... −0.5 V to +6.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

T_{CASE} ..... 0°C to +85°C
V_{CC} ..... 5V ± 5%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

V_{CC} = 5 V ± 5%; T_{CASE} = 0°C to + 85°C

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	−0.3	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage		0.45	V	Note 1
V_{OH}	Output High Voltage	2.4		V	Note 2
I_{CC}	Power Supply Current (50 MHz)		900	mA	Note 3
I_{CCF}	Power Supply Current in Power Down Mode		50	mA	Note 8
I_{LI}	Input Leakage Current		±15	mA	Note 4
I_{IH}	Input Leakage Current		200	mA	Note 5
I_{IL}	Input Leakage Current		−400	mA	Note 6
I_{LO}	Output Leakage Current		±15	mA	
C_{IN}	Input Capacitance (50 MHz)		13	pF	F_C = 1 MHz (Note 7)
C_O	I/O or Output Capacitance (50 MHz)		17	pF	F_C = 1 MHz (Note 7)
C_{CLK}	CLK Capacitance (50 MHz)		15	pF	F_C = 1 MHz (Note 7)

Notes:

1. *This parameter is measured at:*
   Address, Data, $\overline{BE}$n 4.0 mA
   Definition, Control 5.0 mA
2. *This parameter is measured at:*
   Address, Data, $\overline{BE}$n −1.0 mA
   Definition, Control −0.9 mA
3. *Typical supply current*
   775 mA @ 50 MHz
4. *This parameter is for inputs without internal pull-ups or pull-downs and $0 \le V_{IN} \le V_{CC}$.*
5. *This parameter is for inputs with internal pull-downs and V_{IH} = 2.4 V.*
6. *This parameter is for inputs with internal pull-ups and V_{IL} = 0.45 V.*
7. *Not 100% tested.*
8. *The I_{CCF} specification is a target value. It has not been tested.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

The AC specifications, provided in the AC characteristics table, consists of output delays, input setup requirements, and input hold requirements. All AC specifications are relative to the rising edge of the CLK signal.

AC specifications measurement is defined by Figure 1. All timings are referenced to 1.5 V unless otherwise specified. Inputs must be driven to the voltage levels indicated by Figure 1 when AC specifications are measured. Am486DX2 microprocessor output delays are specified with minimum and maximum limits, measured as shown. The minimum Am486DX2 microprocessor delay times are hold times provided to external circuitry. Am486DX2 microprocessor input setup and hold times are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct Am486DX2 microprocessor operation.

Switching Characteristics at 50 MHz

V_{CC} = 5 V ±5%; T_{CASE} = 0°C to + 85°C; C_L = see Note 2

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	8	25	MHz		1X Clock to Am486 CPU
t_1	CLK Period	40	125	ns	Figure 1	
t_{1a}	CLK Period Stability		0.1%	Δ		Adjacent Clocks
t_2	CLK High Time	14		ns	Figure 1	at 2V (Note 1)
t_3	CLK Low Time	14		ns	Figure 1	at 0.8V (Note 1)
t_4	CLK Fall Time		4	ns	Figure 1	(2.0 V–0.8 V) (Note 1)
t_5	CLK Rise Time		4	ns	Figure 1	(0.8 V–2.0 V) (Note 1)
t_6	A31–A2, PWT, PCD, $\overline{BE3}$–$\overline{BE0}$, M/$\overline{IO}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$, $\overline{LOCK}$, $\overline{FERR}$, BREQ, HLDA Valid Delay	3	19	ns	Figure 5	
t_7	A31–A2, PWT, PCD, $\overline{BE3}$–$\overline{BE0}$, M/$\overline{IO}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$, $\overline{LOCK}$, $\overline{FERR}$, BREQ Float Delay		28	ns	Figure 6	Note 1
t_8	$\overline{PCHK}$ Valid Delay	3	24	ns	Figure 5	Note 3
t_{8a}	$\overline{BLAST}$, $\overline{PLOCK}$ Valid Delay	3	24	ns	Figure 5	Note 3
t_9	$\overline{BLAST}$, $\overline{PLOCK}$ Float Delay		28	ns	Figure 6	Note 1
t_{10}	D31–D0, DP3–DP0 Write Data Valid Delay	3	20	ns	Figure 5	Note 3
t_{11}	D31–D0, DP3–DP0 Write Data Float Delay		28	ns	Figure 6	Note 1
t_{12}	$\overline{EADS}$ Setup Time	8		ns	Figure 2	
t_{13}	$\overline{EADS}$ Hold Time	3		ns	Figure 2	
t_{14}	$\overline{KEN}$, $\overline{BS16}$, $\overline{BS8}$ Setup Time	8		ns	Figure 2	
t_{15}	$\overline{KEN}$, $\overline{BS16}$, $\overline{BS8}$ Hold Time	3		ns	Figure 2	
t_{16}	$\overline{RDY}$, $\overline{BRDY}$ Setup Time	8		ns	Figure 3	
t_{17}	$\overline{RDY}$, $\overline{BRDY}$ Hold Time	3		ns	Figure 3	
t_{18}	$\overline{HOLD}$, $\overline{AHOLD}$, $\overline{BOFF}$ Setup Time	8		ns	Figure 2	
t_{19}	HOLD, AHOLD, $\overline{BOFF}$ Hold Time	3		ns	Figure 2	
t_{20}	RESET, $\overline{FLUSH}$, $\overline{A20M}$, NMI, INTR, $\overline{IGNNE}$ Setup Time	8		ns	Figure 2	Note 4
t_{21}	RESET, $\overline{FLUSH}$, $\overline{A20M}$, NMI, INTR, $\overline{IGNNE}$ Hold Time	3		ns	Figure 2	Note 4
t_{22}	D31–D0, DP3–DP0, A31–A4 Read Data Setup Time	5		ns	Figure 2 Figure 3	
t_{23}	D31–D0, DP3–DP0, A31–A4 Read Data Hold Time	3		ns	Figure 2 Figure 3	

Notes: *1. Not 100% tested. Guaranteed by design characterization.*

2. Specifications assume C_L = 50 pF. I/O Buffer model must be used to determine delays due to loading (trace and component). First Order I/O buffer models for the Am486 CPU are available.

3. The minimum Am486DX2 CPU output valid delays are hold times provided to external circuitry.

4. A reset pulse width of 15 CLK cycles is required for warm resets. Power up resets require RESET to be asserted for at least 1 ms after V_{CC} and CLK are stable.

50-MHz Am486 Microprocessor AC Characteristics for Boundary Scan Test Signals

V_{CC} = 5 V ±5%; T_{CASE} = 0°C to +85°C, C_L = 50 pF unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{24}	TCK Frequency		25	MHz		1X Clock
t_{25}	TCK Period	40		ns		Note 2
t_{26}	TCK High Time	10		ns		@ 2.0 V
t_{27}	TCK Low Time	10		ns		@ 0.8 V
t_{28}	TCK Rise Time		4	ns		Note 1
t_{29}	TCK Fall Time		4	ns		Note 1
t_{30}	TDI, TMS Setup Time	8		ns	Figure 7	Note 3
t_{31}	TDI, TMS Hold Time	7		ns	Figure 7	Note 3
t_{32}	TDO Valid Delay	3	25	ns	Figure 7	Note 3
t_{33}	TDO Float Delay		TBD			
t_{34}	All Outputs (Non-Test) Valid Delay	3	25	ns	Figure 7	Note 3
t_{35}	All Outputs (Non-Test) Float Delay		36	ns	Figure 7	Note 3
t_{36}	All Inputs (Non-Test) Setup Time	8		ns	Figure 7	Note 3
t_{37}	All Inputs (Non-Test) Hold Time	7		ns	Figure 7	Note 3

Notes: *1. Rise/Fall times are measured between 0.8 V and 2.0 V. Rise/Fall times can be relaxed by 1 ns per 10-ns increase in TCK period.*

2. TCK period ≥ CLK period.

3. Parameter measured from TCK.

4. Boundary Scan AC Specifications in the above table are target values. They have not been characterized. Therefore, they are subject to change.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

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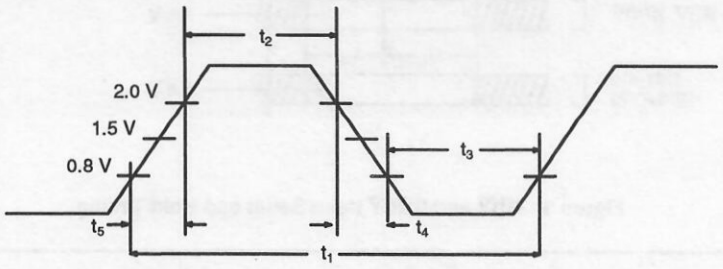

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Figure 1 CLK Waveforms

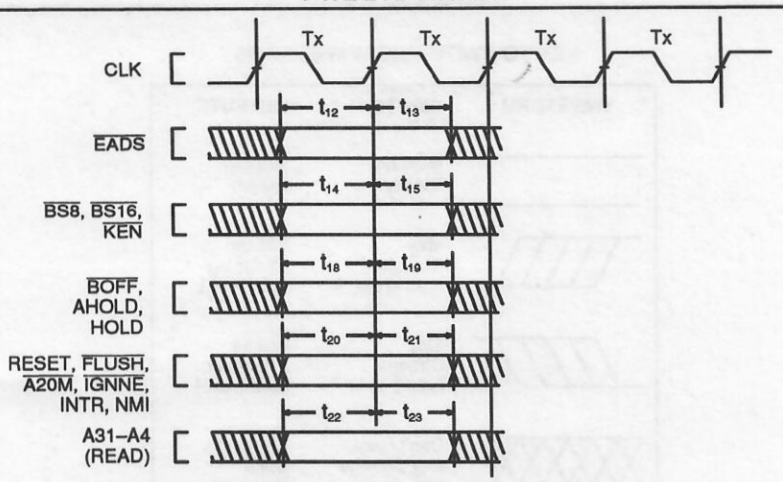

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Figure 2 Input Setup and Hold Timing

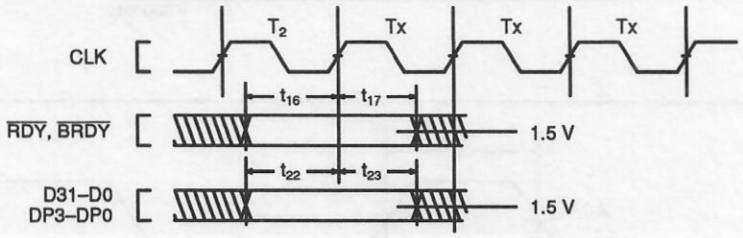

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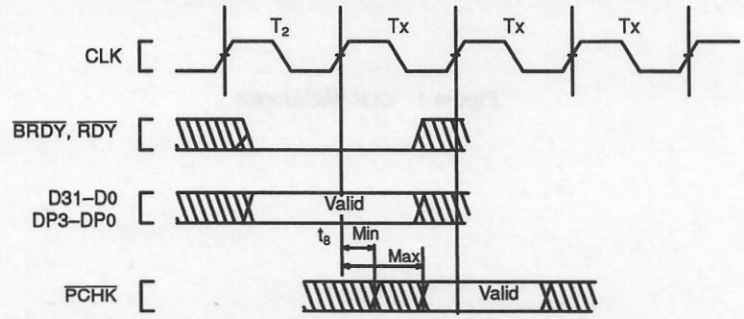
Figure 3 RDY and BRDY Input Setup and Hold Timing



17852A–101

Figure 4 PCHK Valid Delay Timing

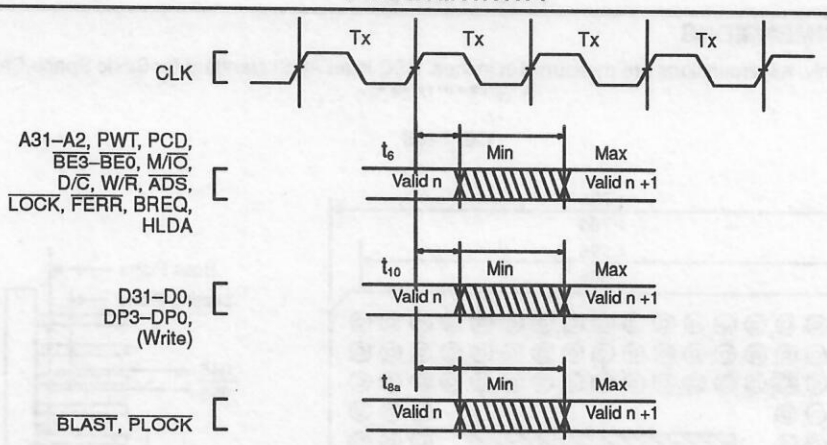


Figure 5 Output Valid Delay Timing

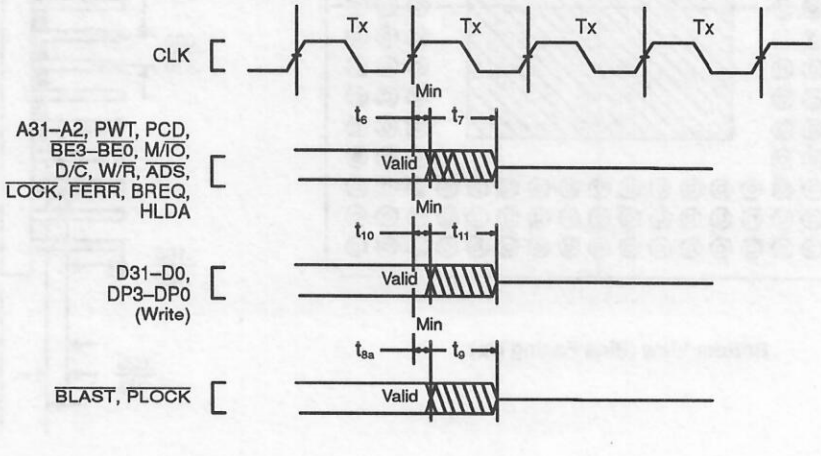


Figure 6 Maximum Float Delay Timing

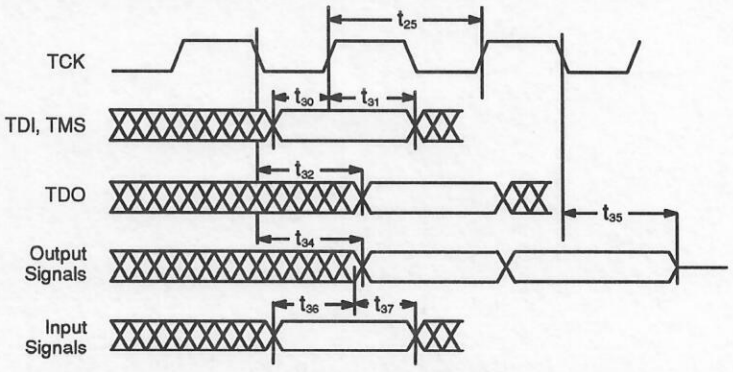
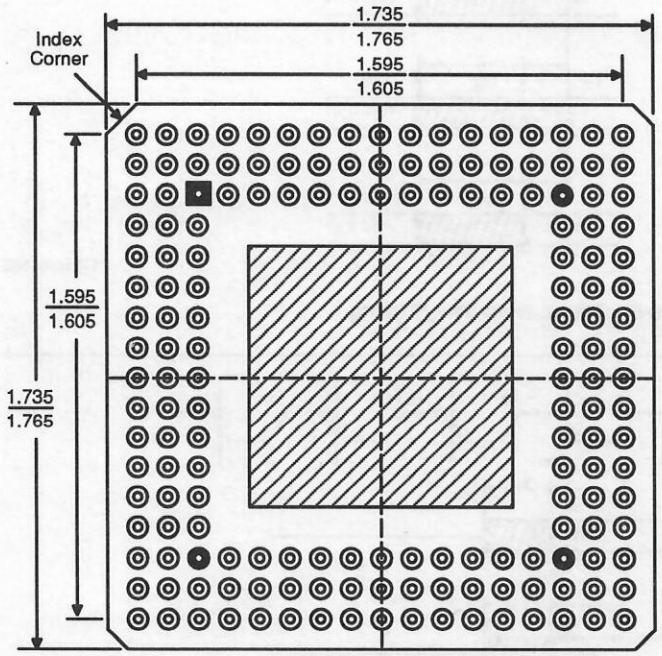


Figure 7 Test Signal Timing Diagram

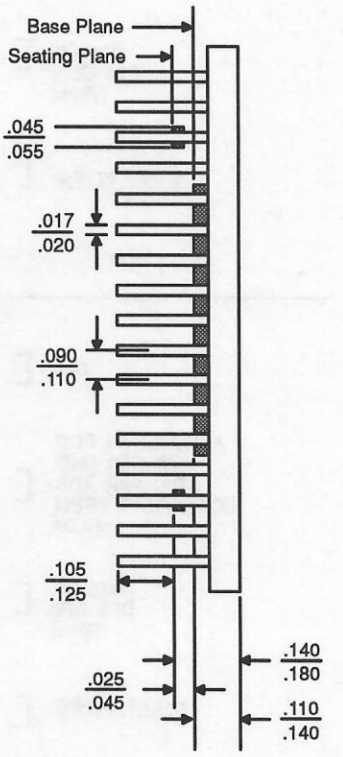
PHYSICAL DIMENSIONS

For reference only. All dimensions are measured in inches. BSC is an ANSI standard for Basic Space Centering.

CGM 168



Bottom View (Pins Facing Up)



Side View

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Package Thermal Specifications

The Am486DX2 microprocessor is specified for operation when T_c (the case temperature) is within the range of 0°C to 85°C. T_c can be measured in any environment to determine whether the Am486DX2 microprocessor is within specified operating range. The case temperature should be measured at the center of the top surface opposite the pins.

The ambient temperature (T_A) is guaranteed as long as T_C is not violated. The ambient temperature can be calculated from θ_{JC} and θ_{JA} and from the following equations.

$T_J = T_C + P * {}_{JC}$

$T_A = T_J - P * {}_{JA}$

$T_C = T_A + P * [\theta_{JA} - {}_{JC}]$

where:

T_J, T_A, T_C = Junction, Ambient, and Case Temperature.

θJ_C, θ_{JA} = Junction-to-Case and Junction-to-Ambient Thermal Resistance, respectively.

P = Maximum Power Consumption

The values for θ_{JA} and θ_{JC} are given in Table 6 for the 1.75 sq. in., 168-pin, ceramic PGA.

Table 7 shows the T_A allowable (without exceeding Tc) at various airflows and operating frequencies (f_{CLK}). Note that T_A is greatly improved by attaching "fins" or a "heat sink" to the package. Heat sink dimensions are shown in Figure 8. P (the maximum power consumption) is calculated by using the maximum 1_{CC} at 5 V as tabulated in the *DC Characteristics*.

Table 6 Thermal Resistance (°C/W) θ_{JC} and θ_{JA} 50-MHz Am486DX2 CPU

	θ_{JA} vs. Airflow–ft/min. (m/sec)						
	θ_{JC}	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
Without Heat Sink	1.5	16.5	14.0	12.0	10.5	9.5	9.0
With Heat Sink*	2.0	12.0	7.0	5.0	4.0	3.5	3.25

**0.350" high unidirectional heat sink (Al alloy 6063, 40 mil fin width, 155 mil center-to-center fin spacing).*

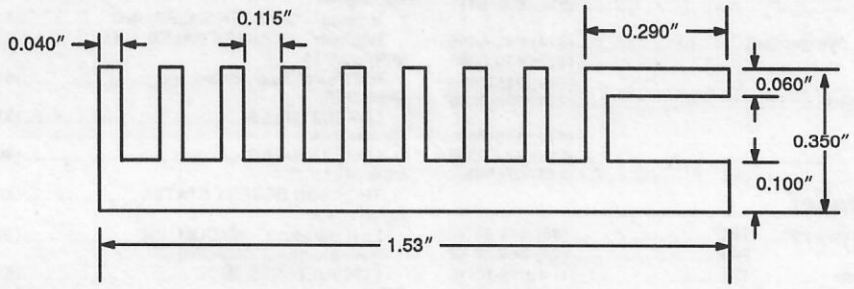

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Figure 8 Heat Sink Dimensions

Table 7 Maximum T_A at Various Airflows in °C

	Airflow–ft/min. (m/sec)						
	f_{CLK} (MHz)	0 (0)	200 (1.01)	400 (2.03)	500 (3.04)	800 (4.06)	1000 (5.07)
T_A with Heat Sink	50	35	60	70	75	77.5	78.75
T_A without Heat Sink	50	10	22.5	32.5	40	45	47.5

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