PRELIMINARY

Am486™DXLV

High-Performance, Low-Voltage, 32-Bit Microprocessor

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Operating voltage range 3.0 V to 3.6 V—The best microprocessor for portable PC applications**
  - — 33-MHz operating frequencies
  - — Over 50% longer battery life over conventional 486 notebooks
  - — Wide range of chipsets and support available through the AMD® FusionPC℠ Program
  - — Fully static design
- **High Integration On-Chip**
  - — 8-Kbyte code and data cache
  - — Floating-point unit
  - — Paged, virtual memory management
- **High-performance Design**
  - — Frequent instructions execute in one clock
  - — 106-Mb/s burst bus at 33 MHz
  - — 0.7-micron CMOS process technology
  - — Dynamic bus sizing for 8-, 16-, and 32-bit buses
- **Complete 32-bit Architecture**
  - — Address and data buses
  - — All Registers
  - — 8-, 16-, and 32-bit data types
- **Multiprocessor Support**
  - — Multiprocessor instructions
  - — Cache consistency protocols
  - — Support for second-level cache
- **System Management Mode (SMM) for system and power management**
  - — System Management Interrupt (SMI) for power management independent of processor operating mode and operating system.
  - — SMI is a non-maskable interrupt that has higher priority than NMI
  - — Automatic save and restore of microprocessor state
  - — Wide range of chipsets supporting SMM available to allow product differentiation
- **Lower heat dissipation and increased reliability**
- **Standard 196-Pin PQFP Package**
- **AMD advanced 0.7-micron, three-layer CMOS technology**

GENERAL DESCRIPTION

The Am486DXLV microprocessor is a low-voltage, true static implementation of the 486DX. The operating voltage range is from 3.0 V–3.6 V. The low-voltage operation of the Am486DXLV microprocessor enables longer battery life in notebook computers. The price/performance of the full 32-bit processor and floating-point unit provides the best value for designing high-volume, mainstream 486 notebooks. At 33 MHz, this device has 56% lower operating power than the Am486DX microprocessor. Lowering the typical operating voltage from 5.0 V to 3.3 V doubles the battery life.

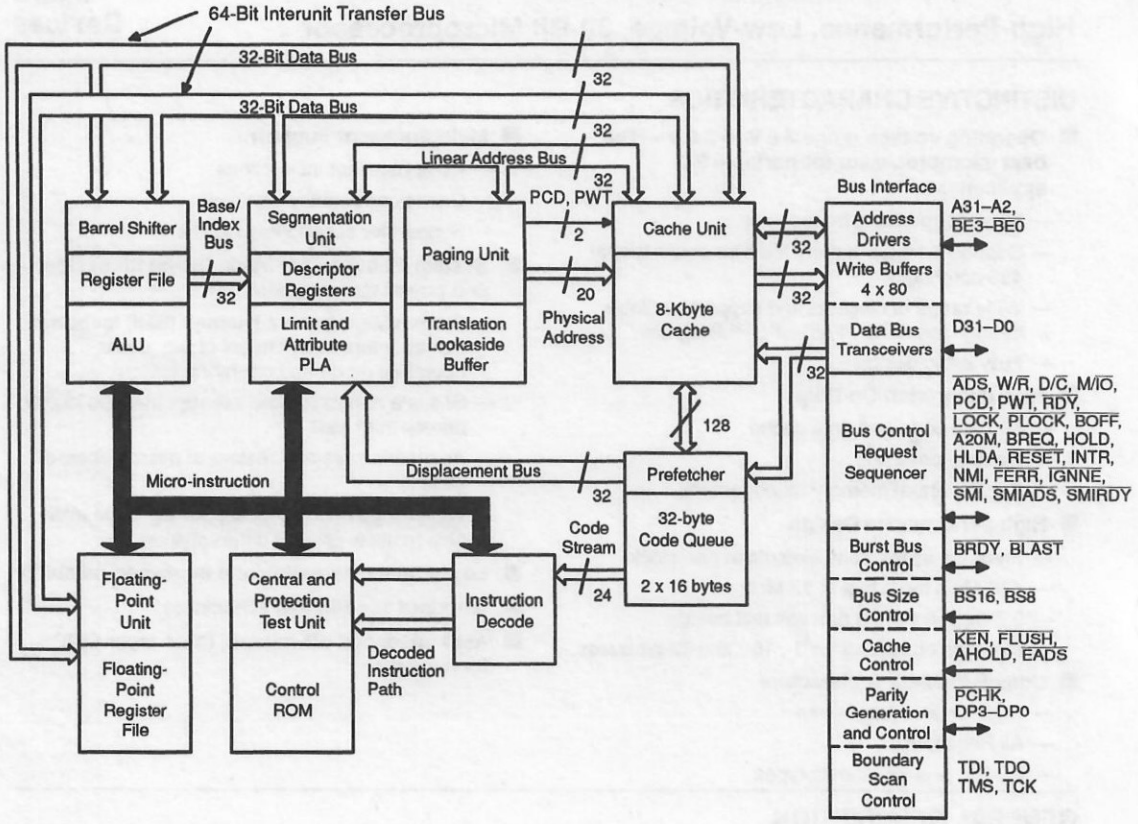
The Am486DXLV microprocessor features a static design that allows the clock to go to 0 MHz (DC) and retain full register contents. The full static mode is achieved by operating the Am486DXLV microprocessor with a 2X clock input. The input frequency can be varied dynamically from maximum to full stop, or vice versa. The frequency change does not affect contents of the register and data integrity is maintained.

SMM is provided as a mechanism to interrupt the microprocessor operation and resume the interrupted operation transparent to the operating system or application running on the system. The Am486DXLV microprocessor supports Microsoft's Advanced Power Management specification for new "power managed" applications.

Publication #: 17381 Rev. A Amendment: /0
Issue Date: May 1993

BLOCK DIAGRAM

Am486DXLV Microprocessor Pipelined 32-bit Microarchitecture

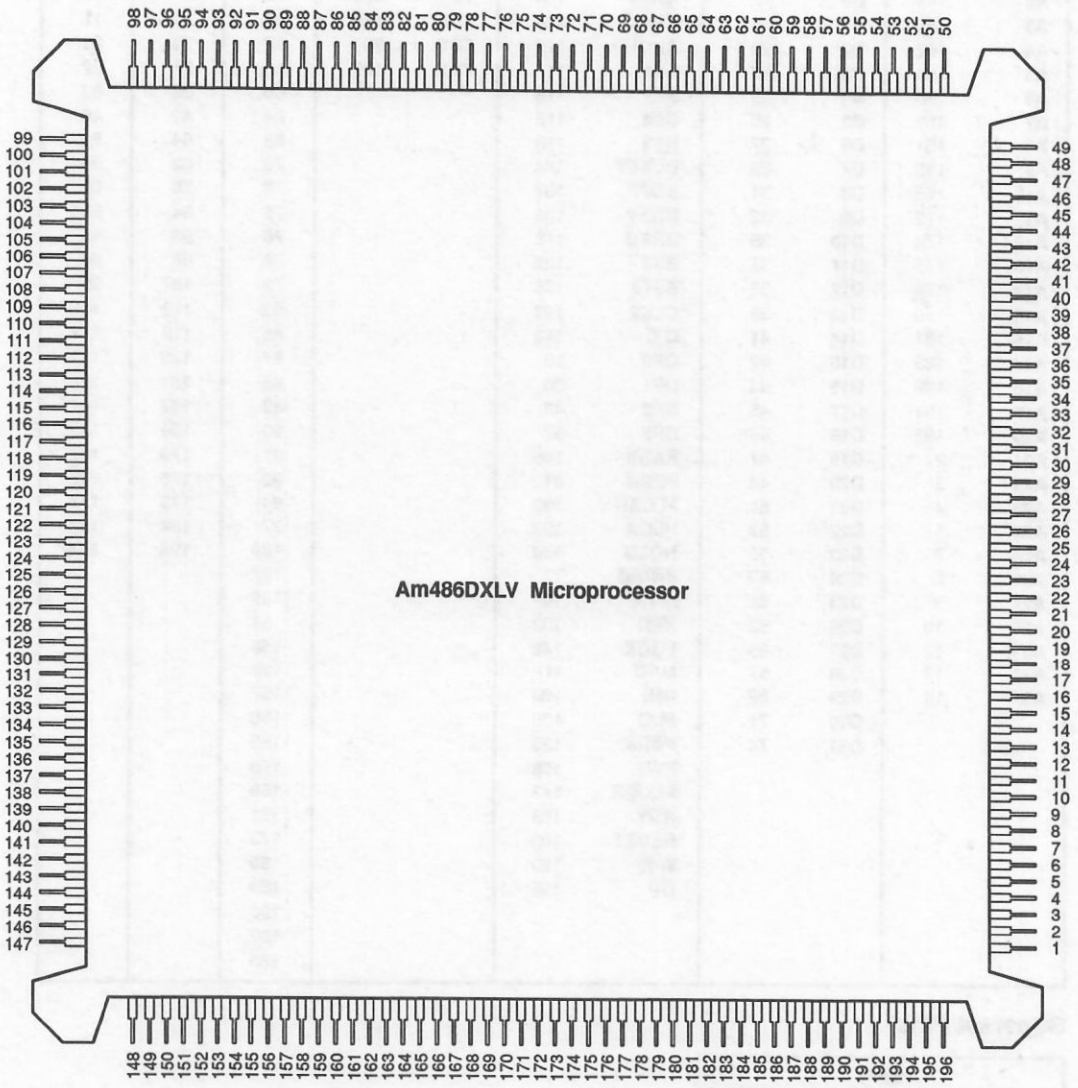


10344D–001

CONNECTION DIAGRAM

Top Side View

196-Pin PQFP (Plastic Quad Flat Pack) Package



PQFP Pin Designations (Functional Grouping)

Address		Data		Control		Test		NC	V_{CC}	V_{SS}
Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin No.	Pin No.	Pin No.
A2	146	D0	17	$\overline{A20M}$	104	TCK	128	15	6	1
A3	150	D1	18	$\overline{ADS}$	145	TDI	185	34	19	11
A4	152	D2	20	AHOLD	129	TDO	80	52	24	21
A5	154	D3	23	$\overline{BE0}$	117	TMS	187	56	28	22
A6	158	D4	25	$\overline{BE1}$	116			60	36	33
A7	159	D5	26	$\overline{BE2}$	115			64	49	40
A8	161	D6	27	$\overline{BE3}$	113			68	54	50
A9	163	D7	29	$\overline{BLAST}$	144			72	62	58
A10	165	D8	31	$\overline{BOFF}$	137			73	70	66
A11	172	D9	32	$\overline{BRDY}$	138			75	84	86
A12	174	D10	35	BREQ	118			76	93	95
A13	176	D11	37	$\overline{BS8}$	135			78	98	96
A14	178	D12	38	$\overline{BS16}$	136			79	107	99
A15	180	D13	39	CLK2	123			83	112	109
A16	181	D14	41	D/$\overline{C}$	110			85	119	114
A17	183	D15	42	DP0	16			87	125	121
A18	189	D16	44	DP1	30			88	131	126
A19	191	D17	45	DP2	43			89	147	141
A20	193	D18	46	DP3	57			90	164	148
A21	2	D19	47	$\overline{EADS}$	105			91	170	167
A22	3	D20	48	$\overline{FERR}$	81			92	175	168
A23	4	D21	51	$\overline{FLUSH}$	102			94	179	177
A24	5	D22	53	HLDA	122			97	184	182
A25	7	D23	55	HOLD	130			124	196	194
A26	8	D24	59	$\overline{IGNNE}$	77			127		
A27	9	D25	61	INTR	101			149		
A28	10	D26	63	$\overline{KEN}$	132			151		
A29	12	D27	65	$\overline{LOCK}$	142			153		
A30	13	D28	67	M/$\overline{IO}$	111			155		
A31	14	D29	69	NMI	100			157		
		D30	71	PCD	106			160		
		D31	74	$\overline{PCHK}$	139			162		
				PWT	108			166		
				$\overline{PLOCK}$	143			169		
				$\overline{RDY}$	133			171		
				RESET	103			173		
				W/$\overline{R}$	120			186		
				$\overline{UP}$	156			188		
								190		
								192		
								195		

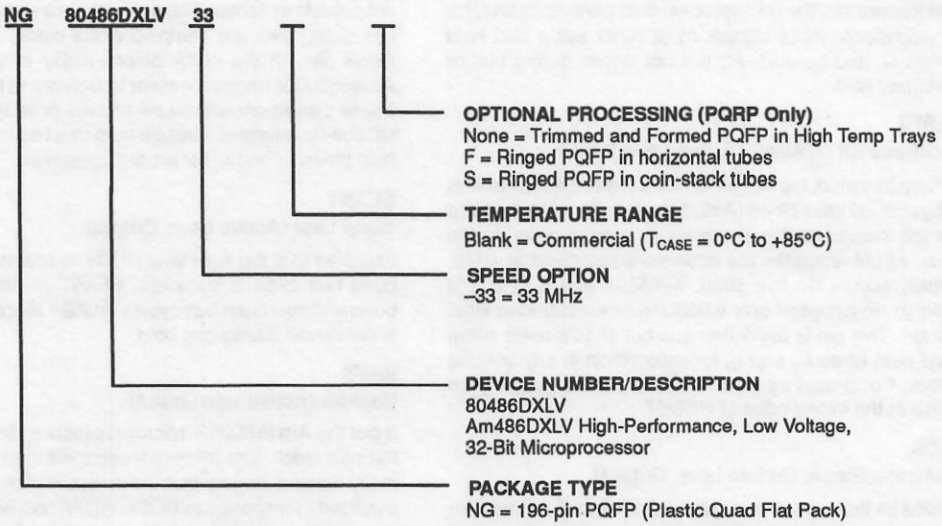
Superset Pins

SMM	
Pin Name	Pin No.
$\overline{SMI}$	82
$\overline{SMIADS}$	140
$\overline{SMIRDY}$	134

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations			
NG	80486DXLV	–33	F
		–33	S

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTIONS

A31–A4/A3–A2
Address Lines (Inputs/Outputs)/(Outputs)

A31–A2, together with the byte enables $\overline{BE3}$–$\overline{BE0}$, define the physical area of memory or input/output space accessed. Address lines A31–A4 are used to drive addresses into the microprocessor to perform cache line invalidations. Input signals must meet setup and hold times t_{22} and t_{23}. A31–A2 are not driven during bus or address hold.

$\overline{A20M}$
Address Bit 20 Mask (Active Low; Input)

When asserted, the Am486DXLV microprocessor masks physical address bit 20 (A20) before performing a lookup to the internal cache or driving a memory cycle on the bus. $\overline{A20M}$ emulates the address wraparound at 1 Mb, which occurs on the 8086. $\overline{A20M}$ is active Low and should be asserted only when the processor is in Real Mode. This pin is asynchronous but should meet setup and hold times t_{20} and t_{21} for recognition in any specific clock. For proper operation, $\overline{A20M}$ should be sampled High at the falling edge of RESET.

$\overline{ADS}$
Address Status (Active Low; Output)

Indicates that a valid bus cycle definition and address are available on the cycle definition lines and address bus. $\overline{ADS}$ is driven active in the same clock as the addresses are driven. $\overline{ADS}$ is active Low and is not driven during bus hold.

AHOLD
Address Hold (Input)

Request allows another bus master access to the Am486DXLV microprocessor's address bus for a cache invalidation cycle. The Am486DXLV microprocessor will stop driving its address bus in the clock following AHOLD going active. Only the address bus will be floated during address hold; the remainder of the bus will remain active. AHOLD is active High and is provided with a small internal pull-down resistor. For proper operation, AHOLD must meet setup and hold times t_{18} and t_{19}.

$\overline{BE3}$–$\overline{BE0}$
Byte Enables (Active Low; Outputs)

Indicate active bytes during read and write cycles. During the first cycle of a cache fill, the external system should assume that all byte enables are active. $\overline{BE3}$ applies to D31–D24, $\overline{BE2}$ applies to D23–D16, $\overline{BE1}$ applies to D15–D8, and $\overline{BE0}$ applies to D7–D0. $\overline{BE3}$–$\overline{BE0}$ are active Low and are not driven during bus hold.

$\overline{BS8}$/$\overline{BS16}$
Bus Size 8 (Active Low; Input)/
Bus Size 16 (Active Low; Input)

Cause the Am486DXLV microprocessor to run multiple bus cycles to complete a request from devices that cannot provide or accept 32 bits of data in a single cycle. The bus sizing pins are sampled every clock. The state of these pins in the clock before ready is used by the Am486DXLV microprocessor to determine the bus size. These signals are active Low and are provided with internal pull-up resistors. These inputs must satisfy setup and hold times t_{14} and t_{15} for proper operation.

$\overline{BLAST}$
Burst Last (Active Low; Output)

Indicates that the next time $\overline{BRDY}$ is returned, then the burst bus cycle is complete. $\overline{BLAST}$ is active for both burst and non-burst bus cycles. $\overline{BLAST}$ is active Low and is not driven during bus hold.

$\overline{BOFF}$
Backoff (Active Low; Input)

Input the Am486DXLV microprocessor to float its bus in the next clock. The microprocessor will float all pins normally floated during bus hold, but HLDA will not be asserted in response to $\overline{BOFF}$. $\overline{BOFF}$ has higher priority than $\overline{RDY}$ or $\overline{BRDY}$; if both are returned in the same clock, $\overline{BOFF}$ takes effect. The microprocessor remains in bus hold until $\overline{BOFF}$ is negated. If a bus cycle was in progress when $\overline{BOFF}$ was asserted, the cycle will be restarted. $\overline{BOFF}$ is active Low and must meet setup and hold times t_{18} and t_{19} for proper operation.

$\overline{BRDY}$
Burst Ready Input (Active Low; Input)

Performs the same cycle during a burst cycle that $\overline{RDY}$ performs during a non-burst cycle. $\overline{BRDY}$ indicates that the external system has presented valid data in response to a read or that the external system has accepted data in response to write. $\overline{BRDY}$ is ignored when the bus is idle and at the end of the first clock in a bus cycle.

$\overline{BRDY}$ is sampled in the second and subsequent clocks of a burst cycle. The data presented on the data bus will be strobed into the microprocessor when $\overline{BRDY}$ is sampled active. If $\overline{RDY}$ is returned simultaneously with $\overline{BRDY}$, $\overline{BRDY}$ is ignored and the burst cycle is prematurely aborted.

$\overline{BRDY}$ is active Low and is provided with a small pull-up resistor. $\overline{BRDY}$ must satisfy the setup and hold times t_{16} and t_{17}.

BREQ
Internal Cycle Pending (Output)

Indicates that the Am486DXLV microprocessor has internally generated a bus request. BREQ is generated whether or not the Am486DXLV microprocessor is driving the bus. BREQ is active High and is never floated, except during three-state test mode (see $\overline{\text{FLUSH}}$).

CLK2
Clock (Input)

CLK2 provides the fundamental timing for the Am486DXLV microprocessor. It is divided by 2 internally to generate the internal processor clock used for instruction execution. The internal clock is comprised of two phases, phase one and phase two. Each CLK2 period is a phase of the internal clock. Figure 1 illustrates this relationship. The phase of the internal processor clock can be synchronized to a known phase by ensuring the RESET signal falling edge meets it applicable setup and hold times, t_{20} and t_{21} (see Figure 2). All setup, hold, float delay, and valid delay timings are references to phase one of the clock as shown in Figure 4. All I/O signals get sampled on the rising edge of the internal clock signal (i.e., the rising edge of phase one). Thus, it is important to synchronize the external circuitry with phase one of CLK2.

D31–D0
Data Lines (Inputs/Outputs)

Lines D7–D0 define the least significant byte of the bus while lines D31–D24 define the most significant byte of the data bus. These signals must meet setup and hold times t_{22} and t_{23} for proper operation on reads. These pins are driven during the second and subsequent clocks of write cycles.

D/$\overline{\text{C}}$
Data/Control (Output)

A bus cycle definition pin that distinguishes data cycles, either memory or I/O, from control cycles. These control cycles are: interrupt acknowledge, halt, and instruction fetching.

DP3–DP0
Data Parity (Inputs/Outputs)

Data parity is generated on all write data cycles with the same timing as the data driven by the Am486DXLV microprocessor. Even parity information must be driven back into the microprocessor on the data parity pins with the same timing as read information to insure that the correct parity check status is indicated by the Am486DXLV microprocessor. The signals read on these pins do not affect program execution.

Input signals must meet setup and hold times t_{22} and t_{23}. DP3–DP0 should be connected to V_{CC} through a pull-up resistor in systems not using parity. DP3–DP0 are active High and are driven during the second and subsequent clocks of write cycles.

$\overline{\text{EADS}}$
Valid External Address (Active Low; Input)

Indicates a valid external address has been driven onto the Am486DXLV microprocessor address pins. This address will be used to perform an internal cache invalidation cycle. $\overline{\text{EADS}}$ is active Low and is provided with an internal pull-up resistor. $\overline{\text{EADS}}$ must satisfy setup and hold time t_{12} and t_{13} for proper operation.

$\overline{\text{FERR}}$
Floating-Point Error (Active Low; Output)

Driven active when a floating-point error occurs. $\overline{\text{FERR}}$ is similar to the $\overline{\text{ERROR}}$ pin on a 387 math coprocessor. $\overline{\text{FERR}}$ is included for compatibility with systems using DOS type floating-point error reporting. $\overline{\text{FERR}}$ is active Low, and is not floated during bus hold, except during three-state test mode (see $\overline{\text{FLUSH}}$).

$\overline{\text{FLUSH}}$
Cache Flush (Active Low; Input)

Forces the Am486DXLV microprocessor to flush its entire internal cache. $\overline{\text{FLUSH}}$ is active Low and need only be asserted for one clock. $\overline{\text{FLUSH}}$ is asynchronous but setup and hold times t_{20} and t_{21} must be met for recognition in any specific clock. $\overline{\text{FLUSH}}$ being sampled Low in the clock before the falling edge of RESET causes the Am486DXLV microprocessor to enter the three-state test mode.

HLDA
Hold Acknowledge (Output)

Goes active in response to a hold request presented on the HOLD pin. HLDA indicates that the Am486DXLV microprocessor has given the bus to another local bus master. HLDA is driven active in the same clock that the Am486DXLV microprocessor floats its bus. HLDA is driven inactive when leaving bus hold. HLDA is active High and remains driven during bus hold. HLDA is never floated except during three-state test mode (see $\overline{\text{FLUSH}}$).

HOLD
Bus Hold Request (Input)

Allows another bus master complete control of the Am486DXLV microprocessor bus. In response to HOLD going active, the Am486DXLV microprocessor will float most of its output and input/output pins. HLDA will be asserted after completing the current bus cycle, burst cycle, or sequence of locked cycles. The Am486DXLV microprocessor will remain in this state until HOLD is deasserted. HOLD is active High and is not provided with an internal pull-down resistor. HOLD must satisfy setup and hold times t_{18} and t_{19} for proper operation.

$\overline{\text{IGNNE}}$
Ignore Numeric Error (Active Low; Input)

When this pin is asserted, the Am486DXLV microprocessor will ignore a numeric error and continue executing non-control floating-point instructions. When $\overline{\text{IGNNE}}$ is

deasserted, the Am486DXLV microprocessor will freeze on a non-control floating-point instruction if a previous floating-point instruction caused an error. $\overline{IGNNE}$ has no effect when the NE bit in Control Register 0 is set. $\overline{IGNNE}$ is active Low and is provided with a small internal pull-up resistor. $\overline{IGNNE}$ is asynchronous but setup and hold times t_{20} and t_{21} must be met to insure recognition on any specific clock.

INTR
Maskable Interrupt (Input)

Indicates an external interrupt has been generated. If the internal interrupt flag is set in EFLAGS, active interrupt processing will be initiated. The Am486DXLV microprocessor will generate two locked interrupt acknowledge bus cycles in response to the INTR pin going active. INTR must remain active until the interrupt acknowledges have been performed to assure that the interrupt is recognized. INTR is active High and is not provided with an internal pull-down resistor. INTR is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

$\overline{KEN}$
Cache Enable (Active Low; Input)

Used to determine whether the current cycle is cacheable. When the Am486DXLV microprocessor generates a cacheable cycle and $\overline{KEN}$ is active, the cycle will become a cache line fill cycle. Returning $\overline{KEN}$ active one clock before ready during the last read in the cache line fill will cause the line to be placed in the on-chip cache. $\overline{KEN}$ is active Low and is provided with a small internal pull-up resistor. $\overline{KEN}$ must satisfy setup and hold times t_{14} and t_{15} for proper operation.

$\overline{LOCK}$
Bus Lock (Active Low; Output)

Indicates the current bus cycle is locked. The Am486DXLV microprocessor will not allow a bus hold when $\overline{LOCK}$ is asserted (but address holds are allowed). $\overline{LOCK}$ goes active in the first clock of the first locked bus cycle and goes inactive after the last clock of the last locked bus cycle. The last locked cycle ends when ready is returned. $\overline{LOCK}$ is active Low and is not driven during bus hold. Locked read cycles will not be transformed into cache fill cycles if $\overline{KEN}$ is returned active.

M/$\overline{IO}$
Memory/Input_Output (Output)

A bus cycle definition pin that distinguishes memory cycles from input/output cycles.

NMI
Non-maskable Interrupt (Input)

Request signal indicates that an external non-maskable interrupt has been generated. NMI is rising edge sensitive. NMI must be held Low for at least four CLK2 periods before this rising edge. NMI is not provided with an internal pull-down resistor. NMI is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

PCD/PWT
Page Cache Disable/Page Write-Through (Outputs)

Reflect the state of the page attribute bits, PWT and PCD, in the page table entry or page directory entry. If paging is disabled or for unpaged cycles, PWT and PCD reflect the state of the PWT and PCD bits in Control Register 3. PWT and PCD have the same timing as the cycle definition pins (M/$\overline{IO}$, D/$\overline{C}$, and W/$\overline{R}$). PWT and PCD are active High and are not driven during bus hold. PCD is masked by the Cache Disable Bit (CD) in Control Register 0.

$\overline{PCHK}$
Parity Status (Active Low; Output)

Parity status is driven on the $\overline{PCHK}$ pin the clock after ready for read operations. The parity status is for data sampled at the end of the previous clock. A parity error is indicated by $\overline{PCHK}$ being Low. Parity status is only checked for enabled bytes as indicated by the byte enable and bus size signals. $\overline{PCHK}$ is valid only in the clock immediately after read data is returned to the microprocessor. At all other times $\overline{PCHK}$ is inactive High. $\overline{PCHK}$ is never floated, except during three-state test mode (see $\overline{FLUSH}$).

$\overline{PLOCK}$
Pseudo-lock (Active Low; Output)

Indicates that the current bus transaction requires more than one bus cycle to complete. Examples of such operations are floating-point long reads and writes (64 bits), segment table descriptor reads (64 bits), and cache line fills (128 bits). The Am486DXLV microprocessor will drive $\overline{PLOCK}$ active until the addresses for the last bus cycle of the transaction have been driven, regardless of whether $\overline{RDY}$ or $\overline{BRDY}$ have been returned.

Normally $\overline{PLOCK}$ and $\overline{BLAST}$ are inverse of each other. However, during the first bus cycle of a 64-bit floating-point write, both $\overline{PLOCK}$ and $\overline{BLAST}$ will be asserted. $\overline{PLOCK}$ is a function of the $\overline{BS8}$, $\overline{BS16}$, and $\overline{KEN}$ inputs. $\overline{PLOCK}$ should be sampled only in the clock ready is returned. $\overline{PLOCK}$ is active Low and is not driven during bus hold.

RESET
Reset (Input)

Forces the Am486DXLV microprocessor to begin execution at a known state. The microprocessor cannot begin execution of instructions until at least 1 ms after V_{CC} and CLK2 have reached their proper DC and AC specifications. The RESET pin should remain active during this time to insure proper microprocessor operation. RESET is active High. RESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.

$\overline{RDY}$
Non-burst Ready (Active Low; Input)

Indicates that the current bus cycle is complete. $\overline{RDY}$ indicates that the external system has presented valid data on the data pins in response to a read, or that the external system has accepted data from the Am486DXLV microprocessor in response to a write. $\overline{RDY}$ is ignored when the bus is idle and at the end of the bus cycle's first clock.

$\overline{RDY}$ is active during address hold. Data can be returned to the processor while AHOLD is active.

$\overline{RDY}$ is active Low and is not provided with an internal pull-up resistor. $\overline{RDY}$ must satisfy setup and hold times t_{16} and t_{17} for proper chip operation.

$\overline{SMI}$
System Management Interrupt (Active Low; Synchronous Input/Output)

This pin is the highest level, non-maskable interrupt to the Am486 CPU that is driven by the system logic of the Am486 CPU. The system logic must assert $\overline{SMI}$ synchronously to CLK2. When this signal is activated by the system logic, the Am486 microprocessor will suspend normal execution and enter SMM. When the CPU recognizes the interrupt (with an active $\overline{SMIADS}$ pulse), the CPU will drive $\overline{SMI}$ active Low. The CPU will continue to drive $\overline{SMI}$ Low until it exits SMM via a RESET or RES4 instruction (when the system asserts RESET, it must also release $\overline{SMI}$ to prevent buffer contention). When exiting SMM, the CPU will drive $\overline{SMI}$ High for two clocks and then release $\overline{SMI}$ to a weak internal pull-up resistor. The $\overline{SMI}$ pull-up is active during RESET and whenever the CPU is not driving $\overline{SMI}$ active Low. The CPU disables the pull-up when it drives $\overline{SMI}$ active to minimize CPU power consumption. $\overline{SMI}$ is not three-stated during HLDA bus cycles. **Note: $\overline{SMI}$ should not be used to qualify SMM accesses.**

$\overline{SMIADS}$
SMI Address Status (Active Low; Three-State; Output)

The Am486 CPU activates this pin to initiate a valid bus cycle to the separate SMM memory space. The function of $\overline{SMIADS}$ is analogous to $\overline{ADS}$. This signal validates the address and control lines for SMM memory, just as $\overline{ADS}$ validates address and control for non-SMM memory cycles. The system must terminate $\overline{SMIADS}$ initiated bus cycles with $\overline{SMIRDY}$. The Am486 CPU ignores both $\overline{RDY}$ and $\overline{BRDY}$ on $\overline{SMIADS}$ initiated cycles. This three-state output is floated during HLDA bus cycles.

$\overline{SMIRDY}$
SMI Ready (Active Low; Synchronous Input)

This input terminates the current bus cycle that $\overline{SMIADS}$ initiated in the same manner as $\overline{RDY}$ terminates $\overline{ADS}$ initiated bus cycles. The system must assert and deassert $\overline{SMIRDY}$ synchronously to CLK2. The Am486 CPU ignores $\overline{SMIRDY}$ on $\overline{ADS}$ initiated cycles. $\overline{SMIRDY}$ has an internal pull-down resistor. This is different from the Am386® CPU $\overline{SMIRDY}$ which has an internal pull-up resistor. $\overline{SMIRDY}$ should not be physically connected to $\overline{RDY}$.

TCK
Test Clock (Input)

Test Clock is an input to the Am486 CPU and provides the clocking function required by the JTAG boundary scan feature. TCK is used to clock state information and data into and out of the component. State select information and data are clocked into the component on the rising edge of TCK on TMS and TDI, respectively. Data is clocked out of the component on the falling edge of TCK on TDO.

TDI
Test Data Input (Input)

TDI is the serial input used to shift JTAG instructions and data into the component. TDI is sampled on the rising edge of TCK, during the SHIFT-IR and the SHIFT-DR TAP controller states. During all other tap controller states, TDI is a "don't care."

TDO
Test Data Output (Output)

TDO is the serial output used to shift JTAG instructions and data out of the component. TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR TAP controller states. At all other times, TDO is driven to the high impedance state.

TMS
Test Mode Select (Input)

TMS is decoded by the JTAG TAP (Tap Access Port) to select the operation of the test logic. TMS is sampled on the rising edge of TCK. To guarantee deterministic behavior of the TAP controller, TMS is provided with an internal pull-up resistor.

$\overline{UP}$
Write/Read (Input) (PQFP package only)

The upgrade Present pin forces the Am486DXLV CPU to three-state all its outputs and enter the power-down mode. When the Upgrade Present pin is sampled asserted by the CPU in the clock before the falling edge of RESET, the power-down mode is enabled. $\overline{UP}$ has no effect on the power-down status expect during this edge. The CPU is also forced to three-state all of its outputs immediately in response to this signal. The $\overline{UP}$ signal must remain asserted in order to keep the pins three-stated. $\overline{UP}$ is active Low and is provided with an internal pull-up resistor.

W/$\overline{R}$
Write/Read (Output)

A bus definition pin that distinguishes write cycles from read cycles.

ABSOLUTE MAXIMUM RATINGS

Case Temperature under Bias .... −65°C to +110°C
Storage Temperature ..... −65°C to +150°C
Voltage on any pin
with respect to ground ..... −0.5 V to V_{CC} +0.5 V
Supply voltage with
respect to V_{SS} ..... −0.5 V to +6.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

T_{CASE} ..... 0°C to +85°C
V_{CC} ..... 3.3 V ± 0.3 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges

V_{CC} = 3.3 V ± 0.3 V ; T_{CASE} = 0°C to +85°C

Symbol	Parameter Description	Notes	Preliminary		Unit
			Min	Max	
V_{IL}	Input Low Voltage		−0.3	+0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = (Note 1) I_{OL} = 0.1 mA		0.45 0.2	V
V_{OH}	Output High Voltage	I_{OH} = (Note 2) I_{OH} = −0.1 mA	2.4 V_{CC} −0.2		V
I_{CC}	Power Supply Current — 33 MHz	V_{CC} = 3.6 V (Note 3)		425	mA
I_{LI}	Input Leakage Current	(Note 4)		±15	µA
I_{IH}	Input Leakage Current	(Note 5)		200	µA
I_{IL}	Input Leakage Current	(Note 6)		−400	µA
I_{LO}	Output Leakage Current			±15	µA
C_{IN}	Input Capacitance (33 MHz)	F_C = 1 MHz (Note 7)		13	pF
C_O	I/O or Output Capacitance (33 MHz)	F_C = 1 MHz (Note 7)		17	pF
C_{CLK}	CLK2 Capacitance (33 MHz)	F_C = 1 MHz (Note 7)		15	pF

Notes: *1. This parameter is measured at: Address, Data, $\overline{BE3}$–$\overline{BE0}$ 4.0 mA; Definition, Control 5.0 mA*

2. This parameter is measured at: Address, Data, $\overline{BE3}$–$\overline{BE0}$ −1.0 mA; Definition, Control −0.9 mA

3. Typical supply current (V_{CC} = 3.3 V): 375 mA @ 33 MHz

4. This parameter is for inputs without pull-ups or pull-downs and $0 \le V_{IN} \le V_{CC}$.

5. This parameter is for inputs with pull-downs and V_{IH} = 2.4 V.

6. This parameter is for inputs with pull-ups and V_{IL} = 0.45 V.

7. Not 100% tested.

SWITCHING CHARACTERISTICS

The switching characteristics consist of output delays, input set-up requirements, and input hold requirements. All switching characteristics are relative to the rising edge of the CLK2 signal.

Switching characteristics measurement is defined by Figures 3–5. Inputs must be driven to the voltage levels indicated by Figure 5 when switching characteristics are measured. Am486DXLV microprocessor output delays are specified with minimum and maximum limits, measured as shown. The minimum Am486DXLV microprocessor delay times are hold times provided to external circuitry. Am486DXLV microprocessor input setup and hold times are specified as minimums, defining the smallest acceptable sampling windows. Within the sampling windows, a synchronous input signal must be stable for correct Am486DXLV microprocessor operation.

Switching Characteristics over COMMERCIAL operating ranges

Switching Characteristics at 33 MHz: 3.3 V ±0.3 V; T_{CASE} = 0°C to +85°C; C_L = 50 pF unless otherwise specified.

Symbol	Parameter Description	Notes	Figure	Preliminary		Unit
				Min	Max	
	Operating Frequency	Half CLK2 Frequency		0	33.3	MHz
t_1	CLK2 Period		3	15		ns
t_2	CLK2 High Time	@ 2.0 V	3	5		ns
t_3	CLK2 Low Time	@ 0.8 V	3	5		ns
t_4	CLK2 Fall Time		3		5	ns
t_5	CLK2 Rise Time		3		5	ns
t_6	A31–A2, PWT, PCD, M/$\overline{IO}$, $\overline{BE3}$–$\overline{BE0}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$, $\overline{LOCK}$, $\overline{FERR}$, BREQ, HLDA Valid Delay		4	3	19	ns
t_{6s}	$\overline{SMIADS}$ Valid Delay	C_L = 50 pF	4	3	19	ns
t_7	A31–A2, PWT, PCD, M/$\overline{IO}$, $\overline{BE3}$–$\overline{BE0}$, D/$\overline{C}$, W/$\overline{R}$, $\overline{ADS}$, $\overline{LOCK}$ Float Delay	(Note 1)	4		20	ns
t_{7s}	$\overline{SMIADS}$ Float Delay	(Note 1)	4		20	ns
t_8	$\overline{PCHK}$ Valid Delay		4	3	22	ns
t_{8a}	$\overline{BLAST}$, $\overline{PLOCK}$ Valid Delay		4	3	20	ns
t_9	$\overline{BLAST}$, $\overline{PLOCK}$ Float Delay	(Note 1)	4		20	ns
t_{10}	D31–D0, DP3–DP0 Write Data Valid Delay		4	3	18	ns
t_{11}	D31–D0, DP3–DP0 Write Data Float Delay	(Note 1)	4		20	ns
t_{12}	$\overline{EADS}$ Setup Time		5	5		ns
t_{13}	$\overline{EADS}$ Hold Time		5	4		ns
t_{14}	$\overline{KEN}$, $\overline{BS16}$, $\overline{BS8}$ Setup Time		5	5		ns
t_{15}	$\overline{KEN}$, $\overline{BS16}$, $\overline{BS8}$ Hold Time		5	4		ns
t_{16}	$\overline{RDY}$, $\overline{BRDY}$ Setup Time		5	5		ns
t_{16s}	$\overline{SMIRDY}$ Setup Time		5	5		ns
t_{17}	$\overline{RDY}$, $\overline{BRDY}$ Hold Time		5	4		ns
t_{17s}	$\overline{SMIRDY}$ Hold Time		5	4		ns
t_{18}	HOLD, AHOLD Setup Time		5	6		ns
t_{18a}	$\overline{BOFF}$ Setup Time		5	8		ns
t_{19}	HOLD, AHOLD, $\overline{BOFF}$ Hold Time		5	4		ns
t_{20}	RESET, $\overline{FLUSH}$, $\overline{A20M}$, NMI, INTR, $\overline{IGNNE}$ Setup Time		2, 5	5		ns
t_{20s}	$\overline{SMI}$ Setup Time		2, 5	5		ns
t_{21}	RESET, $\overline{FLUSH}$, $\overline{A20M}$, NMI, INTR, $\overline{IGNNE}$ Hold Time		2, 5	4		ns
t_{21s}	$\overline{SMI}$ Hold Time		2, 5	4		ns
t_{22}	D31–D0, DP3–DP0, A31–A4 Read Setup Time		5	5		ns
t_{23}	D31–D0, DP3–DP0, A31–A4 Read Hold Time		5	6		ns

Note: 1. Not 100% tested. Guaranteed by design characterization.

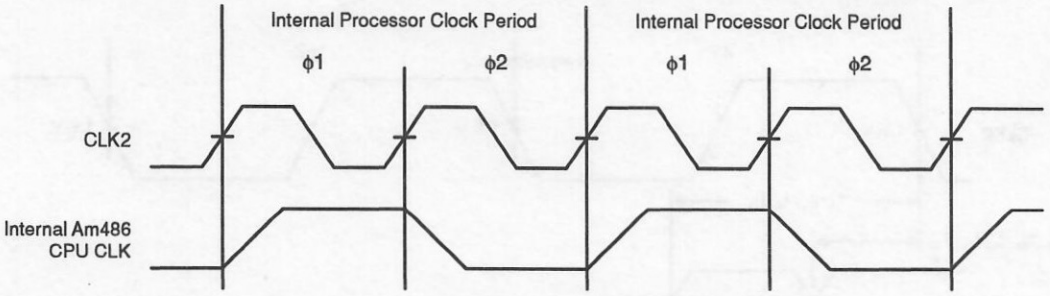
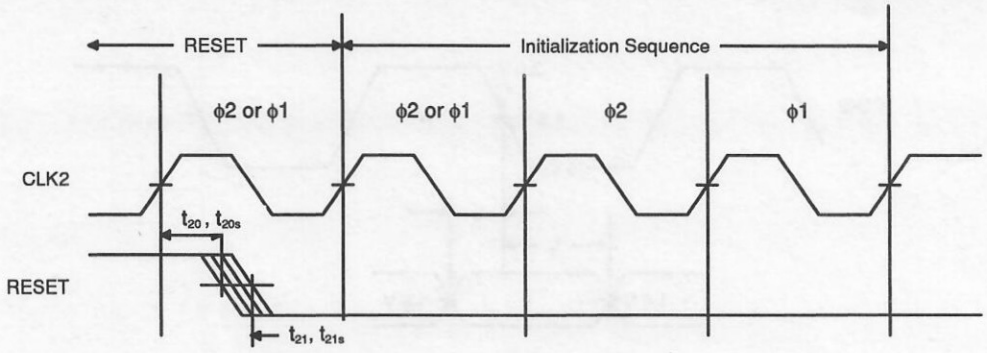


Figure 1. CLK2 Signal and Internal Processor Clock



Note: *The second internal processor phase following RESET High-to-Low transition (provided t_{20} and t_{21} are met) is φ2.*

Figure 2. RESET Setup and Hold Timing, and Internal Phase

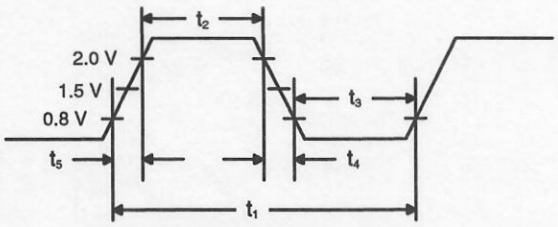


Figure 3. CLK2 Waveforms

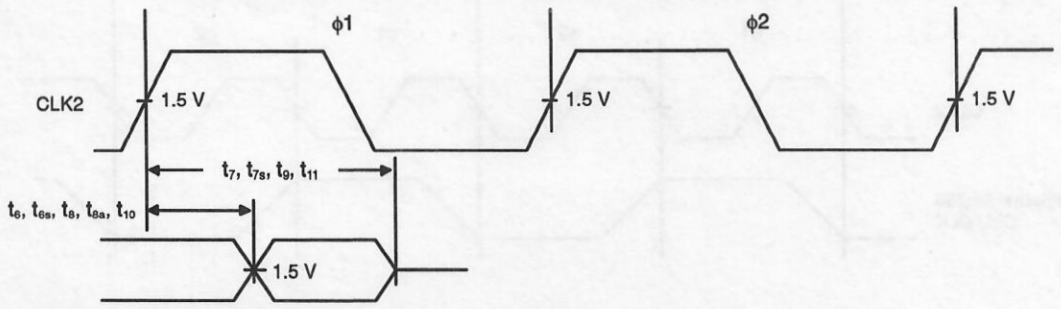
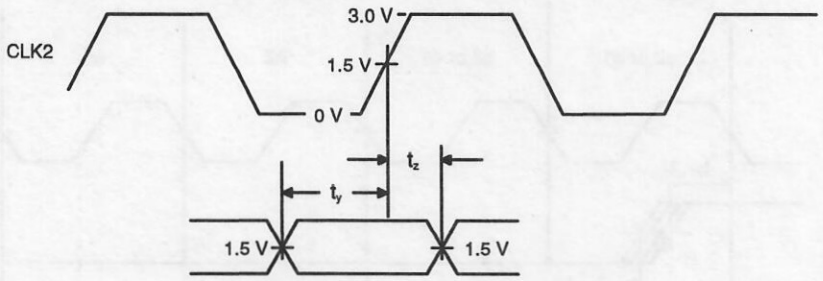


Figure 4. Output Waveforms



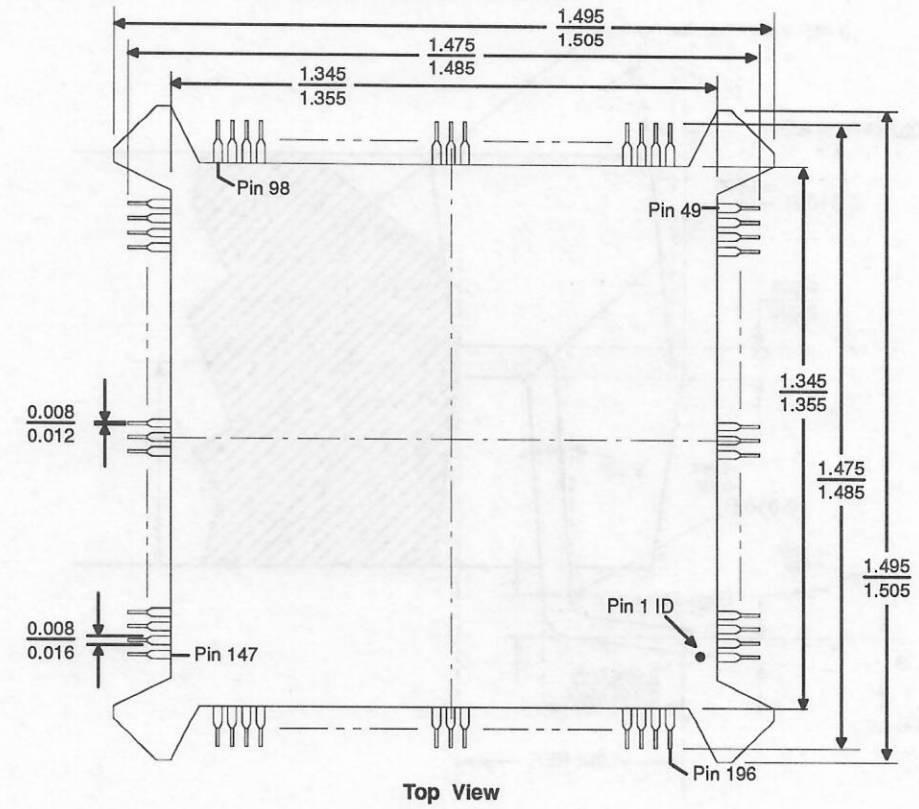
$t_y = t_{12}, t_{14}, t_{16}, t_{16s}, t_{18}, t_{18a}, t_{20}, t_{20s}, t_{22}$
$t_z = t_{13}, t_{15}, t_{17}, t_{17s}, t_{19}, t_{21}, t_{21s}, t_{23}$

Figure 5. Input Waveforms

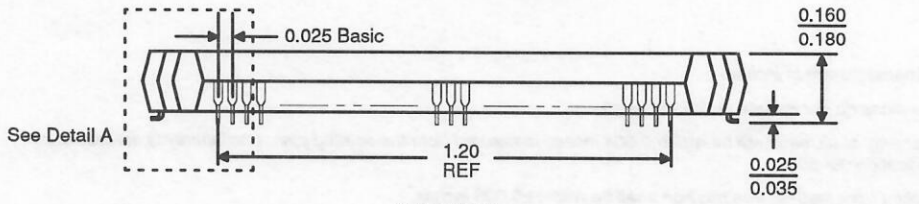
PHYSICAL DIMENSIONS

PQB 196

Plastic Quad Flat Pack; Trimmed and Formed (Measured in inches)



Top View



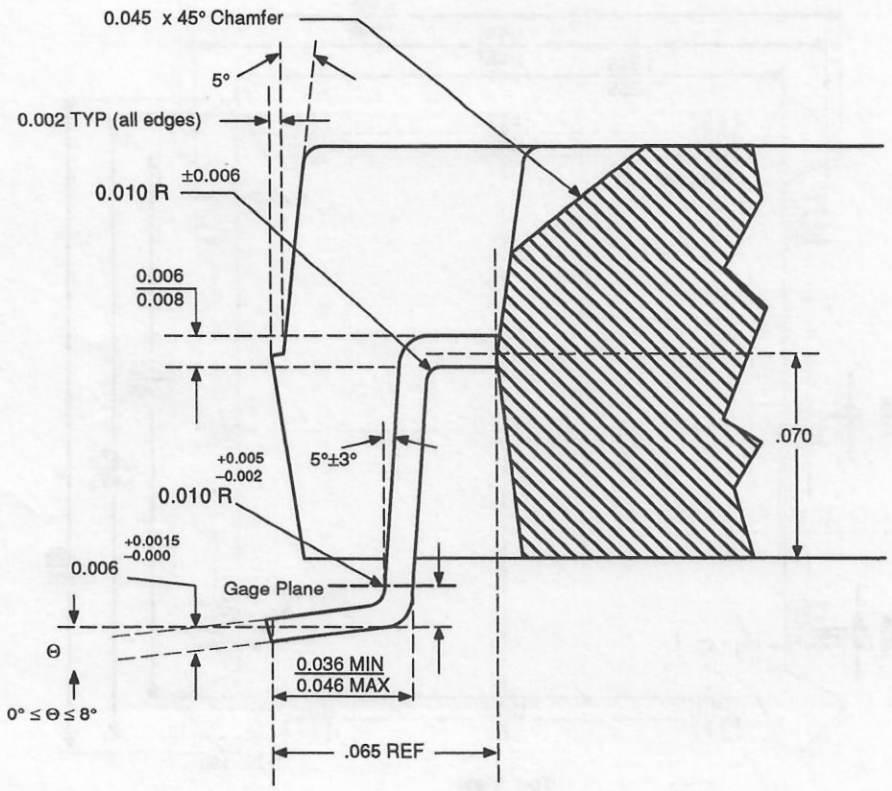
Side View

20012A
CL85
04/9/93 MB

Notes: *For reference only. BSC is an ANSI standard for Basic Space Centering.*

PHYSICAL DIMENSIONS (continued)

PQB 196—Plastic Quad Flat Pack; Trimmed and Formed (continued)



Detail A

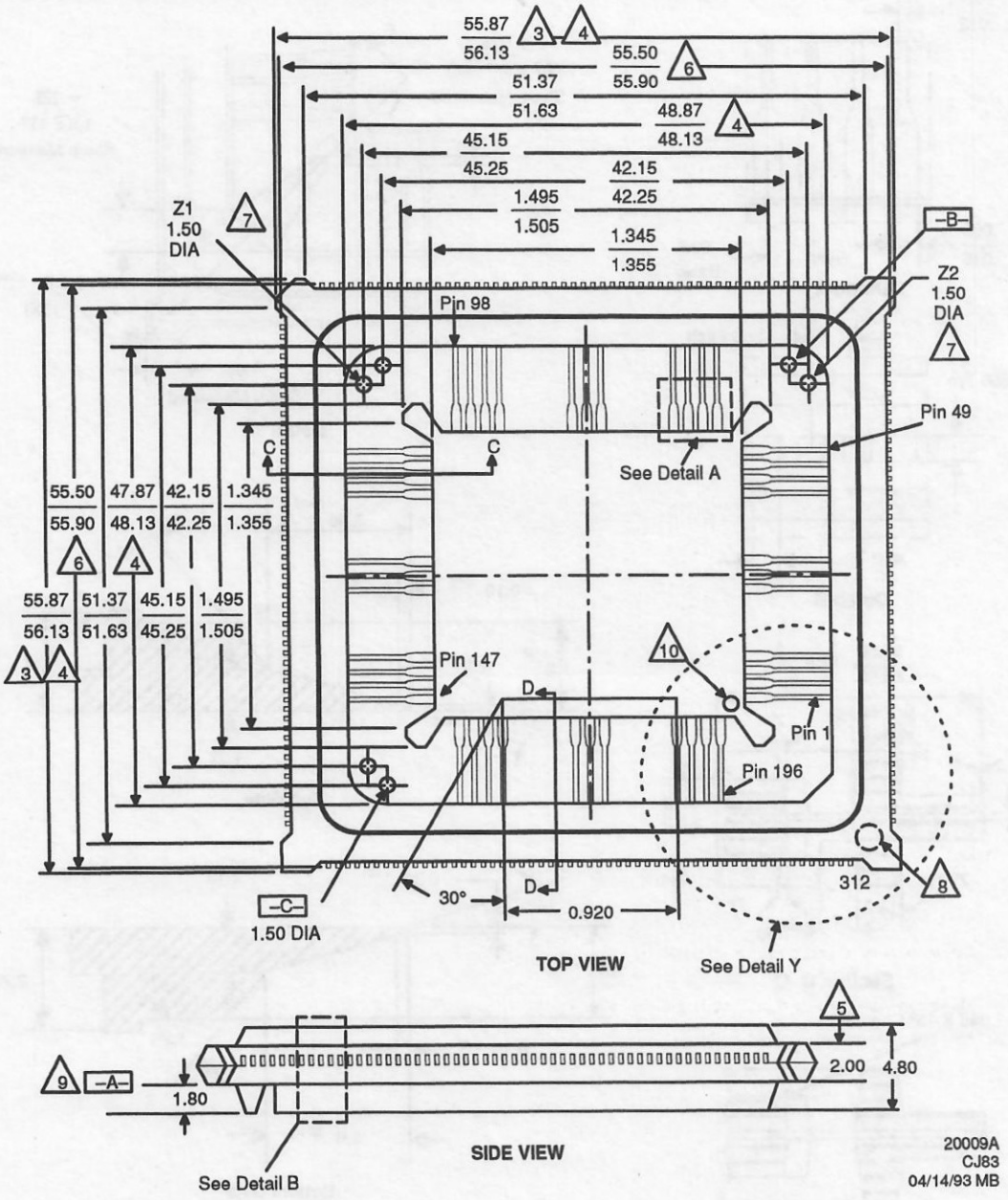
Notes:

1. *All dimensions are in inches.*
2. *Dimensions do not include mold protrusion.*
3. *Coplanarity of all leads will be within 0.004 inches measured from the seating plan. Coplanarity is measured per specification 06–500.*
4. *Deviation from lead-tip true position shall be within ±0.003 inches.*
5. *Half span (center of package to lead-tip) shall be within ±0.0085 inches.*

PHYSICAL DIMENSIONS (continued)

PQB 196

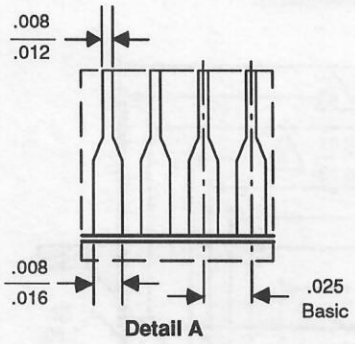
Plastic Quad Flat Pack; Molded Carrier Ring (outer ring measured in millimeters)



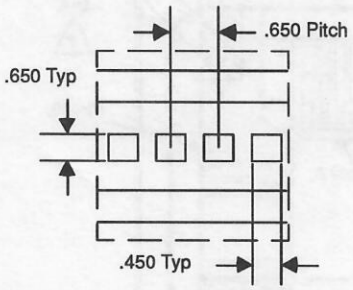
Notes: *For reference only.*

PHYSICAL DIMENSIONS (continued)

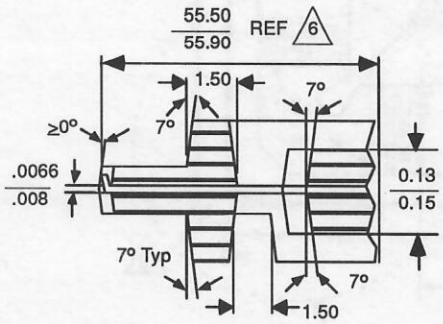
PQB 196—Plastic Quad Flat Pack with Molded Carrier Ring (continued)



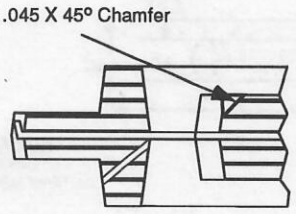
Detail A



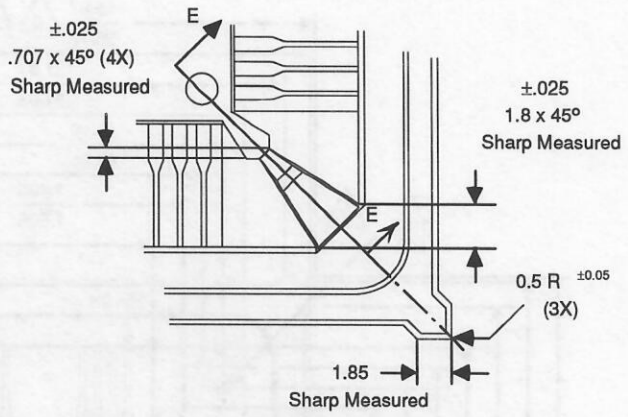
Detail B



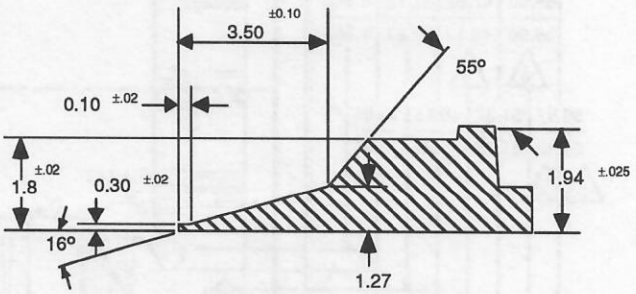
Section C–C



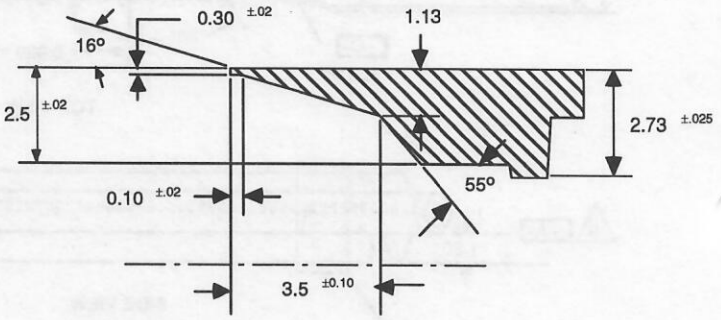
Section D–D



Detail Y



Top Gate



Bottom Gate

Section E–E

PHYSICAL DIMENSIONS (continued)

PQB 196—Plastic Quad Flat Pack with Molded Carrier Ring (continued)

Notes:

1. *All dimensions and tolerances conform to ANSI Y14.5M–1982.*
2. *Controlling dimensions: package is measured in inches and ring is measured in millimeters.*
3. *These dimensions do not include mold protrusion. Allowable mold protrusion is 0.2 mm per side.*
4. *These dimensions include mold mismatch and are measured at the parting line.*
5. *Dimensions are centered about centerline of lead material.*
6. *These dimensions are from the outside edge to the outside edge of the test points.*
7. *There are six locating holes in the ring. –B– and –C– datum holes are used for trim form and excise of the molded package only. Holes Z1 and Z2 are used for electrical testing only.*
8. *This area is reserved for vacuum pickup on each of the four corners of the ring and must be flat within 0.025 mm. No ejector pins in this area.*
9. *Datum –A– surface for seating in socket applications.*
10. *Pin one orientation with respect to carrier ring as indicated.*

Sales Offices

North American

ALABAMA		(205) 882-9122
ARIZONA		(602) 242-4400
CALIFORNIA,		
Culver City		(310) 645-1524
Newport Beach		(714) 752-6262
Sacramento(Roseville)		(916) 786-6700
San Diego		(619) 560-7030
San Jose		(408) 452-0500
Woodland Hills		(818) 992-4155
CANADA, Ontario,		
Kanata		(613) 592-0060
Willowdale		(416) 222-7800
COLORADO		(303) 741-2900
CONNECTICUT		(203) 264-7800
FLORIDA,		
Clearwater		(813) 530-9971
Boca Raton		(407) 361-0050
Orlando (Longwood)		(407) 862-9292
GEORGIA		(404) 449-7920
IDAHO		(208) 377-0393
ILLINOIS,		
Chicago (Itasca)		(708) 773-4422
Naperville		(708) 505-9517
MARYLAND		(301) 381-3790
MASSACHUSETTS		(617) 273-3970
MINNESOTA		(612) 938-0001
NEW JERSEY,		
Cherry Hill		(609) 662-2900
Parsippany		(201) 299-0002
NEW YORK,		
Brewster		(914) 279-8323
Rochester		(716) 425-8050
NORTH CAROLINA		
Charlotte		(704) 875- 3091
Raleigh		(919) 878- 8111
OHIO,		
Columbus (Westerville)		(614) 891-6455
Dayton		(513) 439-0268
OREGON		(503) 245-0080
PENNSYLVANIA		(215) 398-8006
TEXAS,		
Austin		(512) 346-7830
Dallas		(214) 934-9099
Houston		(713) 376-8084

International

BELGIUM, Antwerpen	TEL	(03) 248 43 00
	FAX	(03) 248 46 42
FRANCE, Paris	TEL	(1) 49-75-10-10
	FAX	(1) 49-75-10-13
GERMANY,		
Bad Homburg	TEL	(06172)-24061
	FAX	(06172)-23195
München	TEL	(089) 45053-0
	FAX	(089) 406490
HONG KONG,	TEL	(852) 865-4525
Wanchai	FAX	(852) 865-4335
ITALY, Milano	TEL	(02) 3390541
	FAX	(02) 38103458
JAPAN,		
Atsugi	TEL	(0462) 29-8460
	FAX	(0462) 29-8458
Kanagawa	TEL	(0462) 47-2911
	FAX	(0462) 47-1729
Tokyo	TEL	(03) 3346-7550
	FAX	(03) 3342-5196

International (Continued)

Osaka	TEL	(06) 243-3250
	FAX	(06) 243-3253
KOREA, Seoul	TEL	(82) 2-784-0030
	FAX	(82) 2-784-8014
LATIN AMERICA,		
Ft. Lauderdale	TEL	(305) 484-8600
	FAX	(305) 485-9736
SINGAPORE	TEL	(65) 3481188
	FAX	(65) 3480161
SWEDEN,		
Stockholm area	TEL	(08) 98 61 80
(Bromma)	FAX	(08) 98 09 06
TAIWAN, Taipei	TEL	(886) 2-7153536
	FAX	(886) 2-7122183
UNITED KINGDOM,		
Manchester area	TEL	(0925) 830380
(Warrington)	FAX	(0925) 830204
London area	TEL	(0483) 740440
(Woking)	FAX	(0483) 756196

North American Representatives

CANADA	
Burnaby, B.C. – DAVETEK MARKETING	(604) 430-3680
Kanata, Ontario – VITEL ELECTRONICS	(613) 592-0060
Mississauga, Ontario – VITEL ELECTRONICS	(416) 564-9720
Lachine, Quebec – VITEL ELECTRONICS	(514) 636-5951
ILLINOIS	
Skokie – INDUSTRIAL REPRESENTATIVES,INC	(708) 967-8430
IOWA	
LORENZ SALES	(319) 377-4666
KANSAS	
Merriam – LORENZ SALES	(913) 469-1312
Wichita – LORENZ SALES	(316) 721-0500
MICHIGAN	
Holland – COM-TEK SALES, INC	(616) 335-8418
Brighton – COM-TEK SALES, INC	(313) 227-0007
MINNESOTA	
Mel Foster Tech. Sales, Inc.	(612) 941-9790
MISSOURI	
LORENZ SALES	(314) 997-4558
NEBRASKA	
LORENZ SALES	(402) 475-4660
NEW MEXICO	
THORSON DESERT STATES	(505) 883-4343
NEW YORK	
East Syracuse – NYCOM, INC	(315) 437-8343
Hauppauge – COMPONENT CONSULTANTS, INC	(516) 273-5050
OHIO	
Centerville – DOLFUSS ROOT & CO	(513) 433-6776
Columbus – DOLFUSS ROOT & CO	(614) 885-4844
Westlake – DOLFUSS ROOT & CO	(216) 899-9370
OREGON	
ELECTRA TECHNICAL SALES, INC	(503) 643-5074
PENNSYLVANIA	
RUSSELL F. CLARK CO.,INC.	(412) 242-9500
PUERTO RICO	
COMP REP ASSOC, INC	(809) 746-6550
UTAH	
Front Range Marketing	(801) 288-2500
WASHINGTON	
ELECTRA TECHNICAL SALES	(206) 821-7442
WISCONSIN	
Brookfield – INDUSTRIAL REPRESENTATIVES,INC	(414) 574-9393

Advanced Micro Devices, Inc. 901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088, USA
Tel: (408) 732-2400 • TWX: 910-339-9280 • TELEX: 34-6306 • TOLL FREE: (800) 538-8450
APPLICATIONS HOTLINE & LITERATURE ORDERING • TOLL FREE: (800) 222-9323 • (408) 749-5703

17381A 4/15/93
Con-16M-5/93-0 Printed in USA