



MITSUBISHI LSiS

M5M5256FP-10, -12, -15, -10L, -12L, -15L

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

This M5M5256FP is a 262,144-bit CMOS static RAM organized as 32,768 words by 8 bits which is fabricated using high-performance double polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS peripherals result in a high-density and low-power static RAM. It is ideal for the memory systems which require simple interface.

The stand-by current is low enough for a battery back-up application. It is mounted in a 28 pin flat package and configured in an industrial standard 32K x 8-bit pinout.

FEATURES

Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5256FP-10	100 ns	70 mA	2 mA
M5M5256FP-12	120 ns		
M5M5256FP-15	150 ns		
M5M5256FP-10L	100 ns		100 μ A
M5M5256FP-12L	120 ns		
M5M5256FP-15L	150 ns		

- Single +5V Power Supply
- No Clocks, No Refresh
- Data-Hold on +2V Power Supply
- Directly TTL Compatible: All Inputs and Outputs
- Three-State Outputs: OR-tie Capability
- Simple Memory Expansion by \bar{S}
- \bar{OE} Prevents Data Contention in the I/O Bus
- Common Data I/O

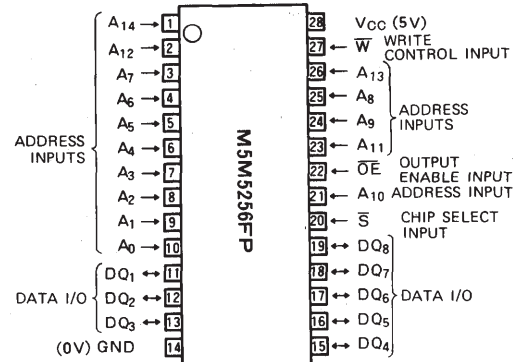
APPLICATION

Small Capacity Memory Units.

FUNCTION

The operation mode of the M5M5256FP is determined by a combination of the device control inputs \bar{S} , \bar{W} and \bar{OE} .

PIN CONFIGURATION (TOP VIEW)



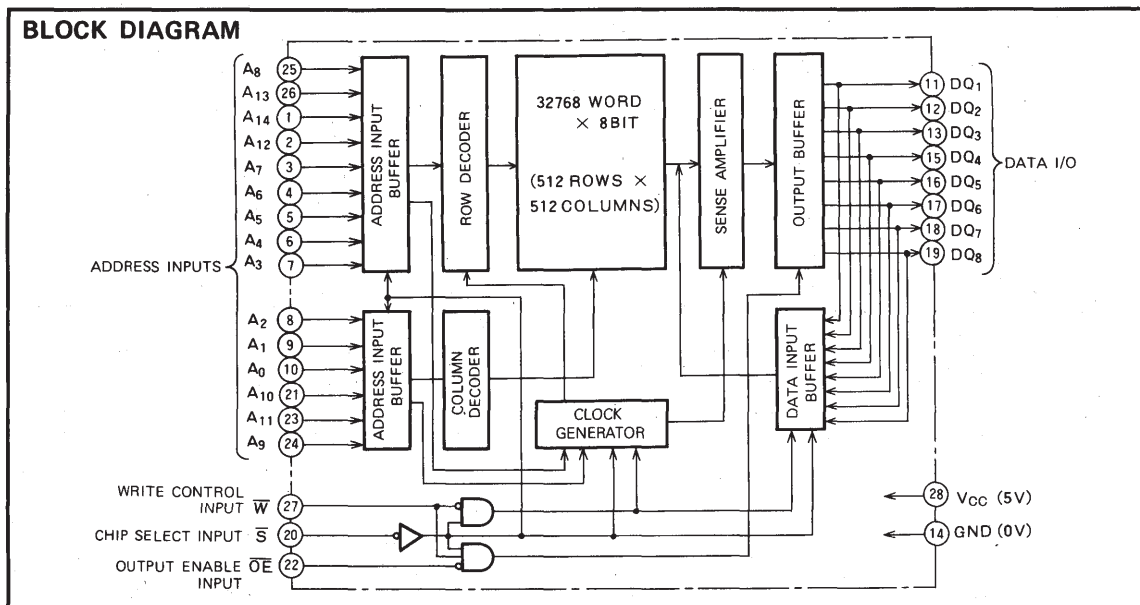
Outline 28P2W

Each mode is summarized in the function table. (see next page)

A write cycle is executed whenever the low level \bar{W} overlaps with the low level \bar{S} . The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of \bar{W} , \bar{S} , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable \bar{OE} directly controls the output stage. Setting the \bar{OE} at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting \bar{W} at a high level and \bar{OE} at a low level while \bar{S} are in an active state.

BLOCK DIAGRAM



MITSUBISHI LSIs
M5M5256FP-10, -12, -15, -10L, -12L, -15L

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

When setting \bar{S} at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by \bar{S} . The power supply current is reduced as low as the stand-by current which is specified as I_{CC5} or I_{CC6} , and the memory data can be held +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

\bar{S}	\bar{W}	\bar{OE}	Mode	DQ	I_{CC}
H	X	X	Non selection	high-impedance	Standby
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	H	H		high-impedance	Active

RECOMMENDED OPERATING CONDITIONS ($T_a = 0 \sim 70^\circ\text{C}$, unless otherwise noted).

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
GND	Supply voltage		0		V
V_{IL}	low input voltage	-0.3		0.8	V
V_{IH}	high input voltage	2.2		$V_{CC}+0.3$	V

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	-0.3 ~ 7	V
V_I	Input voltage		-0.3 ~ $V_{CC}+0.3$	V
V_O	Output voltage		0 ~ V_{CC}	V
P_d	Power dissipation	$T_a = 25^\circ\text{C}$	700	mW
T_{opr}	Operating temperature		0 ~ 70	$^\circ\text{C}$
T_{stg}	Storage temperature		-65 ~ 150	$^\circ\text{C}$

ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High input voltage		2.2		$V_{CC}+0.3$	V
V_{IL}	Low input voltage		-0.3		0.8	V
V_{OH}	High output voltage	$I_{OH} = -1\text{mA}$	2.4			V
V_{OL}	Low output voltage	$I_{OL} = 2\text{mA}$			0.4	V
I_I	Input current	$V_I = 0 \sim V_{CC}$			± 1	μA
I_{OZH}	High level output current in off-state	$\bar{S} = V_{IH}$ or $\bar{OE} = V_{IH}$			1	μA
I_{OZL}	Low level output current in off-state	$V_I/O = 0 \sim V_{CC}$			-1	μA
I_{CC1}	Active supply current (AC, MOS level)	$\bar{S} < 0.2, \bar{W} > V_{CC}-0.3$ output open other input < 0.2 or $> V_{CC}-0.3$ toycle = $1\mu\text{s}$		3	10	mA
I_{CC2}	Active supply current (AC, MOS level)	$\bar{S} < 0.2, \bar{W} > V_{CC}-0.3$ output open other input < 0.2 or $> V_{CC}-0.3$ Min. cycle		30	65	mA
I_{CC3}	Active supply current (AC, TTL level)	$\bar{S} = V_{IL}, \bar{W} = V_{IH}$ output open other input = V_{IL} or V_{IH} toycle = $1\mu\text{s}$		7	15	mA
I_{CC4}	Active supply current (AC, TTL level)	$\bar{S} = V_{IL}, \bar{W} = V_{IH}$ output open other input = V_{IL} or V_{IH} Min. cycle		35	70	mA
I_{CC5}	Stand-by supply current	$\bar{S} \geq V_{CC}-0.2\text{V}$ Other inputs = $0 \sim V_{CC}$			2(P)	mA
					100(P-L)	μA
I_{CC6}	Stand-by supply current	$\bar{S} = V_{IH}$, Other inputs = $0 \sim V_{CC}$			3	mA
C_i	Input capacitance ($T_a = 25^\circ\text{C}$)	$V_I = \text{GND}, V_i = 25\text{mV}_{rms}, f = 1\text{MHz}$			6	pF
C_o	Outout capacitance ($T_a = 25^\circ\text{C}$)	$V_O = \text{GND}, V_O = 25\text{mV}_{rms}, f = 1\text{MHz}$			8	pF

Note 1 Direction for current flowing into IC is indicated as positive (no mark)

2 Typical value is $V_{CC} = 5V, T_a = 25^\circ\text{C}$



MITSUBISHI LSIs
M5M5256FP-10, -12, -15, -10L, -12L, -15L

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

SWITCHING CHARACTERISTICS ($T_a=0\sim 70^\circ\text{C}$, $V_{CC}=5V\pm 10\%$, unless otherwise noted)

Read cycle

Symbol	Parameter	Limits									Unit
		M5M5256FP-10 M5M5256FP-10L			M5M5256FP-12 M5M5256FP-12L			M5M5256FP-15 M5M5256FP-15L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{cR}	Read cycle time	100			120			150			ns
$t_a(A)$	Address access time			100			120			150	ns
$t_a(S)$	Chip select access time			100			120			150	ns
$t_a(OE)$	Output enable access time			50			60			75	ns
$t_{dis}(S)$	Output disable time after \bar{S} high			35			40			45	ns
$t_{dis}(OE)$	Output disable time after \overline{OE} high			35			40			45	ns
$t_{en}(S)$	Output enable time after \bar{S} low	10			10			10			ns
$t_{en}(OE)$	Output enable time after \overline{OE} low	10			10			10			ns
$t_v(A)$	Data valid time after address change	20			20			20			ns

TIMING REQUIREMENTS ($T_a=0\sim 70^\circ\text{C}$, $V_{CC}=5V\pm 10\%$, unless otherwise noted)

Write cycle

Symbol	Parameter	Limits									Unit
		M5M5256FP-10 M5M5256FP-10L			M5M5256FP-12 M5M5256FP-12L			M5M5256FP-15 M5M5256FP-15L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{cW}	Write cycle time	100			120			150			ns
$t_w(W)$	Write pulse width	60			70			80			ns
$t_{su}(A)$	Address set up time	0			0			0			ns
$t_{su}(A-\bar{W}H)$	Address set up time with respect to \bar{W} high	80			85			90			ns
$t_{su}(S)$	Chip select set up time	80			85			90			ns
$t_{su}(D)$	Data set up time	35			40			50			ns
$t_h(D)$	Data hold time	0			0			0			ns
$t_{rec}(W)$	Write recovery time	0			0			0			ns
$t_{dis}(W)$	Output disable time after \bar{W} low			35			40			45	ns
$t_{dis}(OE)$	Output disable time after \overline{OE} high			35			40			45	ns
$t_{en}(W)$	Output enable time after \bar{W} high	10			10			10			ns
$t_{en}(OE)$	Output enable time after \overline{OE} low	10			10			10			ns

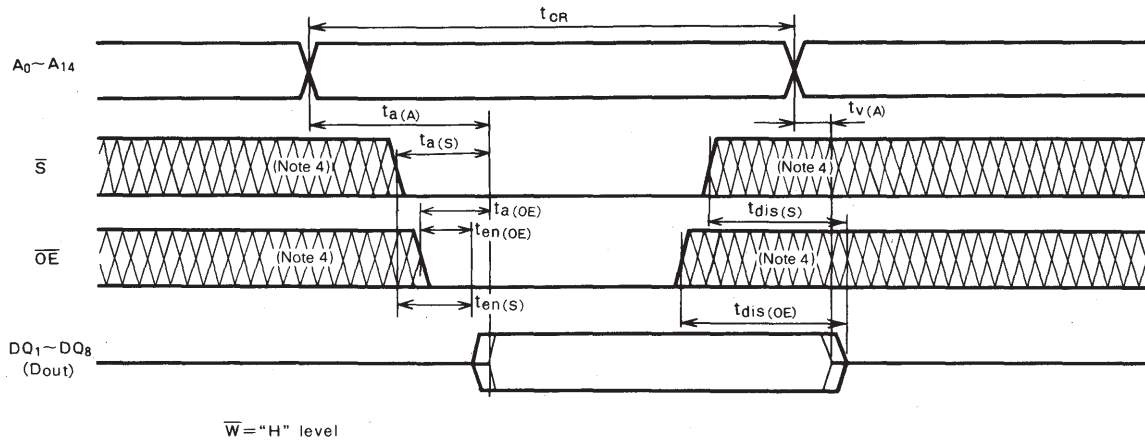
MITSUBISHI LSIs

M5M5256FP-10, -12, -15, -10L, -12L, -15L

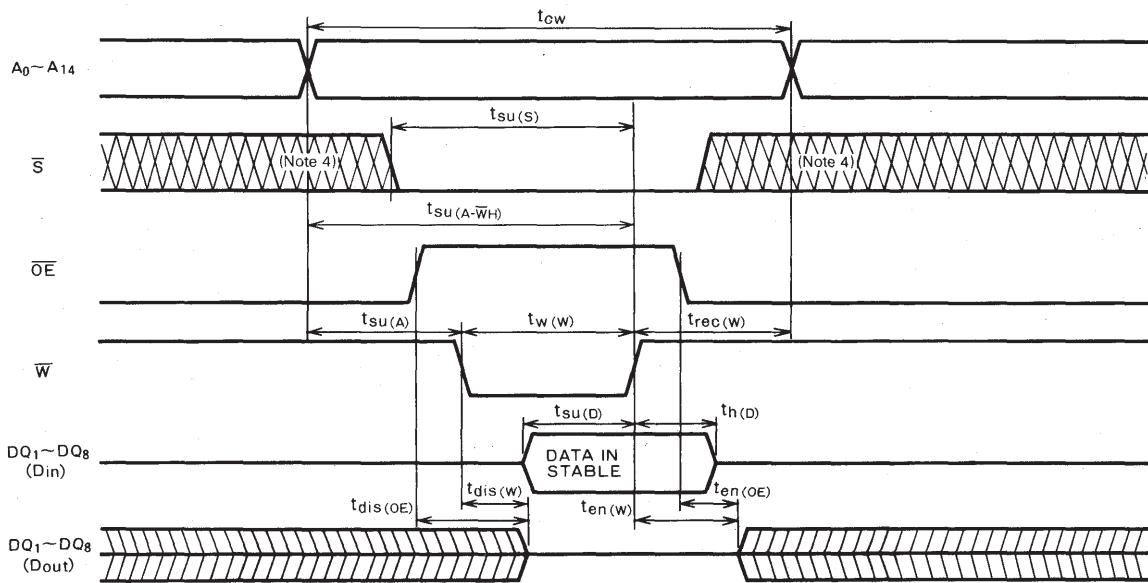
262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

TIMING DIAGRAM

Read cycle



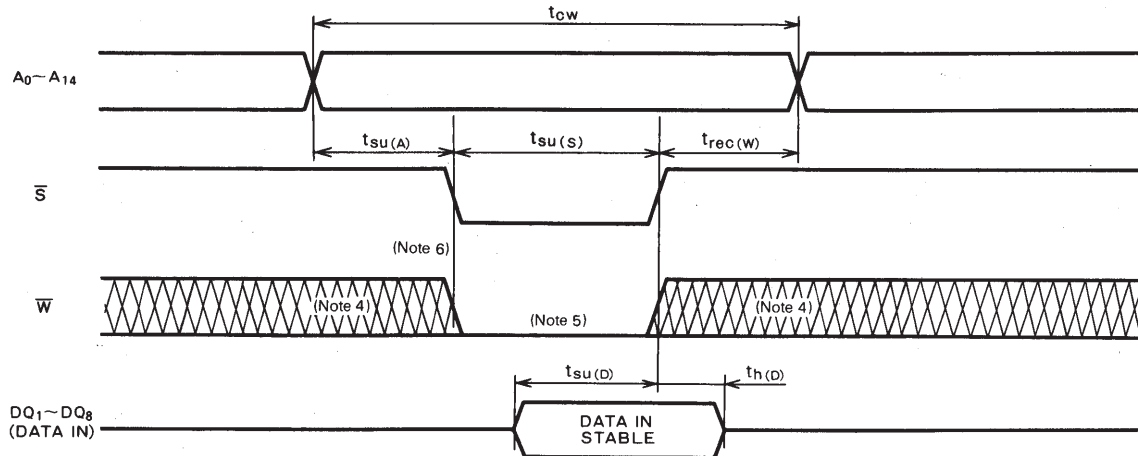
Write cycle (WE control)



M5M5256FP-10, -12, -15, -10L, -12L, -15L

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

Write cycle (\bar{S} control)



Note 3: Test condition

Input pulse level: 0.6~2.4V
 Input pulse rise, fall time: 10ns
 Load: 1 TTL, $C_L = 100\text{pF}$
 Conditions of assessment: 1.5V

4: Hatching indicates the state is don't care.

5: Writing is executed in overlap of \bar{S} and \bar{W} low.

6: If \bar{W} goes low simultaneously with or prior to \bar{S} , the output remains in the high-impedance state.

7: Don't apply inverted phase signal externally when DQ pin is in output mode.

POWER DOWN CHARACTERISTICS

ELECTRICAL CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage		2			V
$V_I(\bar{S})$	Chip select input \bar{S}	$2.2\text{V} \leq V_{CC(PD)}$	2.2			V
		$2\text{V} \leq V_{CC(PD)} \leq 2.2\text{V}$		$V_{CC(PD)}$		
$I_{CC(PD)}$	Power down supply current	$V_{CC} = 3\text{V}$, Other inputs = 3V			2 (P)	mA
					50 (P-L)	μA

TIMING REQUIREMENTS ($T_a = 0 \sim 70^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{SU(PD)}$	Power down setup time		0			ns
$t_{REC(PD)}$	Power down recovery time		t_{CR}			ns

POWER DOWN CHARACTERISTICS

