National Semiconductor

LM1524/LM2524/LM3524
Regulating Pulse Width Modulator

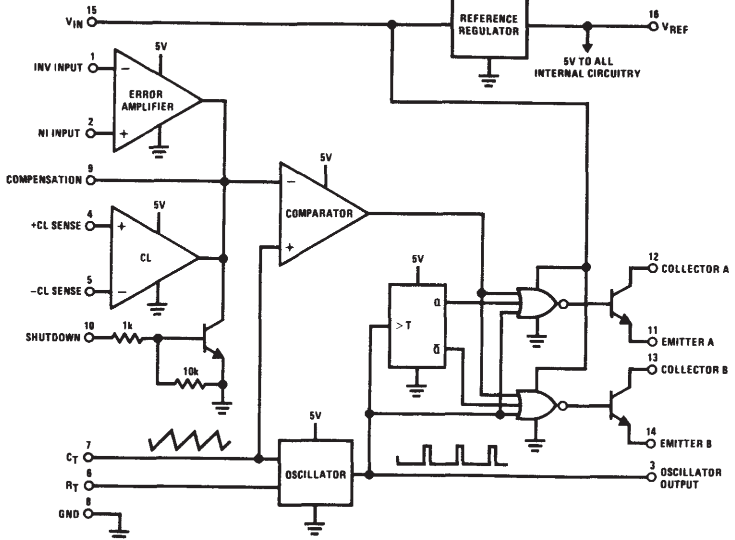
General Description

The LM1524 series of regulating pulse width modulators contains all of the control circuitry necessary to implement switching regulators of either polarity, transformer coupled DC to DC converters, transformerless polarity converters and voltage doublers, as well as other power control applications. This device includes a 5V voltage regulator capable of supplying up to 50 mA to external circuitry, a control amplifier, an oscillator, a pulse width modulator, a phase splitting flip-flop, dual alternating output switch transistors, and current limiting and shutdown circuitry. Both the regulator output transistor and each output switch are internally current limited and, to limit junction temperature, an internal thermal shutdown circuit is employed. The LM1524 is rated for operation from −55°C to +125°C and is packaged in a hermetic 16-lead DIP (J). The LM2524 and LM3524 are rated for operation from 0°C to +70°C and are packaged in either a hermetic 16-lead DIP (J) or a 16-lead molded DIP (N).

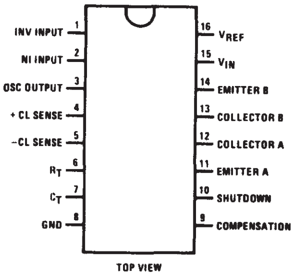
Features

- Complete PWM power control circuitry
- Frequency adjustable to greater than 100 kHz
- 2% frequency stability with temperature
- Total quiescent current less than 10 mA
- Dual alternating output switches for both push-pull or single-ended applications
- Current limit amplifier provides external component protection
- On-chip protection against excessive junction temperature and output current
- 5V, 50 mA linear regulator output available to user

Block and Connection Diagrams



Dual-In-Line Package



Order Number LM1524J, LM2524J
or LM3524J
See NS Package J16A

Order Number LM2524N
or LM3524N
See NS Package N16A

Absolute Maximum Ratings

Input Voltage	40V
Reference Voltage, Forced	6V
Reference Output Current	50 mA
Output Current (Each Output)	100 mA
Oscillator Charging Current (Pin 6 or 7)	5 mA
Internal Power Dissipation (Note 1)	1W
Operating Temperature Range	
LM1524	−55°C to +125°C
LM2524/LM3524	0°C to +70°C

Maximum Junction Temperature	
(J Package)	150°C
(N Package)	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

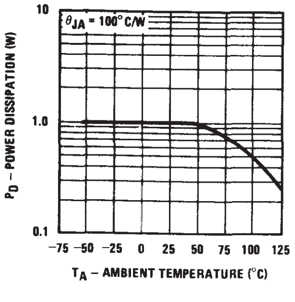
Unless otherwise stated, these specifications apply for $T_A = -55°C$ to $+125°C$ for the LM1524 and 0°C to +70°C for the LM2524 and LM3524, $V_{IN} = 20V$, and f = 20 kHz. Typical values other than temperature coefficients, are at $T_A = 25°C$.

PARAMETER	CONDITIONS	LM1524/ LM2524			LM3524			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage		4.8	5.0	5.2	4.6	5.0	5.4	V
Line Regulation	$V_{IN} = 8–40V$		10	20		10	30	mV
Load Regulation	$I_L = 0–20$ mA		20	50		20	50	mV
Ripple Rejection	f = 120 Hz, $T_A = 25°C$		66			66		dB
Short-Circuit Output Current	$V_{REF} = 0$, $T_A = 25°C$		100			100		mA
Temperature Stability	Over Operating Temperature Range		0.3	1		0.3	1	%
Long Term Stability	$T_A = 25°C$		20			20		mV/khr
Oscillator Section								
Maximum Frequency	$C_T = 0.001\ \mu F$, $R_T = 2\ k\Omega$		350			350		kHz
Initial Accuracy	R_T and C_T constant		5			5		%
Frequency Change with Voltage	$V_{IN} = 8–40V$, $T_A = 25°C$			1			1	%
Frequency Change with Temperature	Over Operating Temperature Range			2			2	%
Output Amplitude (Pin 3)	$T_A = 25°C$		3.5			3.5		V
Output Pulse Width (Pin 3)	$C_T = 0.01\ \mu F$, $T_A = 25°C$		0.5			0.5		µs
Error Amplifier Section								
Input Offset Voltage	$V_{CM} = 2.5V$		0.5	5		2	10	mV
Input Bias Current	$V_{CM} = 2.5V$		2	10		2	10	µA
Open Loop Voltage Gain		72	80		60	80		dB
Common-Mode Input Voltage Range	$T_A = 25°C$	1.8		3.4	1.8		3.4	V
Common-Mode Rejection Ratio	$T_A = 25°C$		70			70		dB
Small Signal Bandwidth	$A_V = 0$ dB, $T_A = 25°C$		3			3		MHz
Output Voltage Swing	$T_A = 25°C$	0.5		3.8	0.5		3.8	V
Comparator Section								
Maximum Duty Cycle	% Each Output ON	45			45			%
Input Threshold (Pin 9)	Zero Duty Cycle		1			1		V
Input Threshold (Pin 9)	Maximum Duty Cycle		3.5			3.5		V
Input Bias Current			−1			−1		µA
Current Limiting Section								
Sense Voltage	$V_{(Pin\ 2)} - V_{(Pin\ 1)} \geq 50$ mV, Pin 9 = 2V, $T_A = 25°C$	190	200	210	180	200	220	mV
Sense Voltage T.C.			0.2			0.2		mV/°C
Common-Mode Voltage		−0.7		1	− 0.7		1	V
Output Section (Each Output)								
Collector-Emitter Voltage		40			40			V
Collector Leakage Current	$V_{CE} = 40V$		0.1	50		0.1	50	µA
Saturation Voltage	$I_C = 50$ mA		1	2		1	2	V
Emitter Output Voltage	$V_{IN} = 20V$, $I_E = -250\ \mu A$	17	18		17	18		V
Rise Time (10% to 90%)	$R_C = 2\ k\Omega$, $T_A = 25°C$		0.2			0.2		µs
Fall Time (90% to 10%)	$R_C = 2\ k\Omega$, $T_A = 25°C$		0.1			0.1		µs
Total Standby Current	$V_{IN} = 40V$, Pins 1, 4, 7, 8, 11 and 14 are grounded, Pin 2 = 2V, All Other Inputs and Outputs Open		5	10		5	10	mA

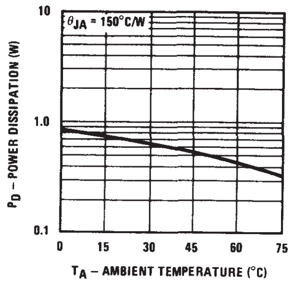
Note 1: For operation at elevated temperatures, devices in the J package must be derated based on a thermal resistance of 100°C/W, junction to ambient, and devices in the N package must be derated based on a thermal resistance of 150°C/W, junction to ambient.

Typical Performance Characteristics

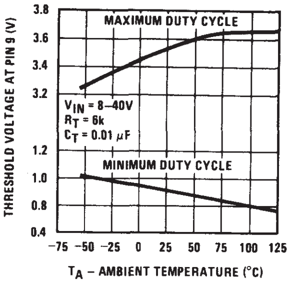
Maximum Average Power Dissipation (J Package)



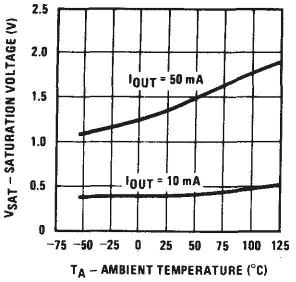
Maximum Average Power Dissipation (N Package)



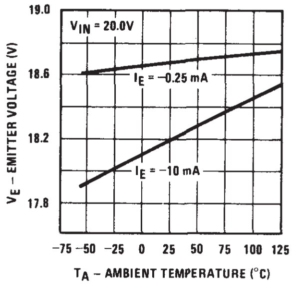
Maximum and Minimum Duty Cycle Threshold Voltage



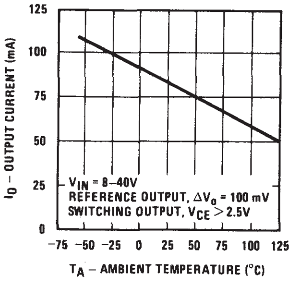
Output Transistor Saturation Voltage



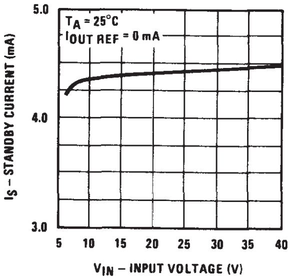
Output Transistor Emitter Voltage



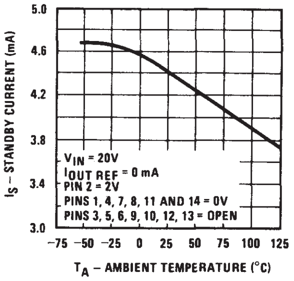
Reference and Switching Transistor Peak Output Current



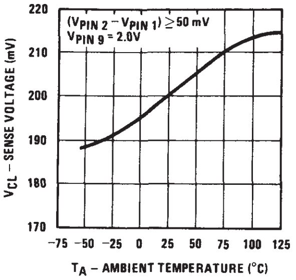
Standby Current



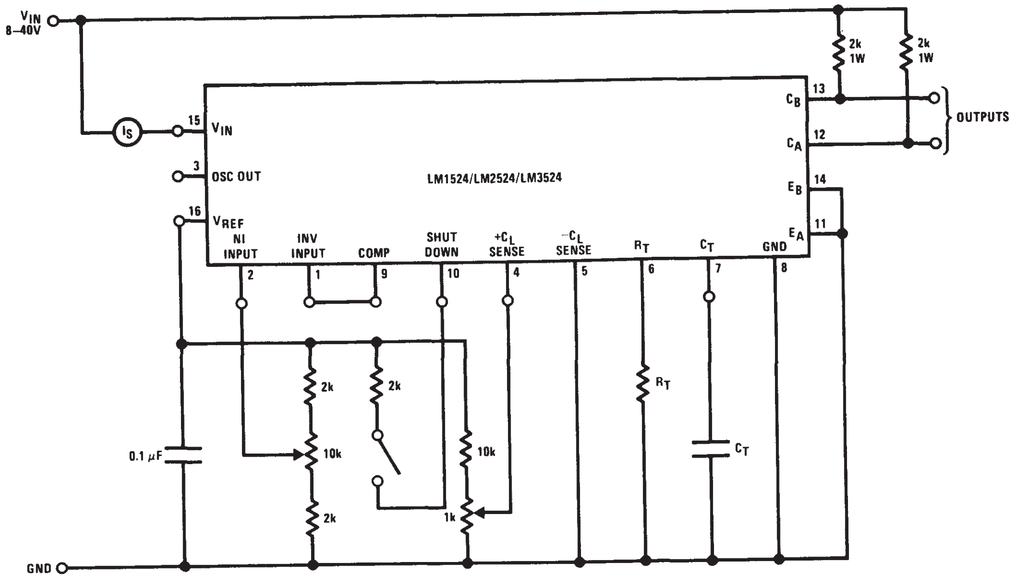
Standby Current



Current Limit Sense Voltage ($V_{Pin\ 4} - V_{Pin\ 5}$)



Test Circuit

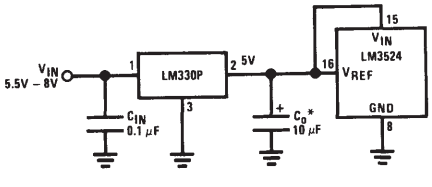


Functional Description

INTERNAL VOLTAGE REGULATOR

The LM3524 has on chip a 5V, 50 mA, short circuit protected voltage regulator. This voltage regulator provides a supply for all internal circuitry of the device and can be used as an external reference.

For input voltages of less than 8V the 5V output should be shorted to pin 15, V_{IN}, which disables the 5V regulator. With these pins shorted the input voltage must be limited to a maximum of 6V. If input voltages of 6–8V are to be used, a pre-regulator, as shown in *Figure 1*, must be added.



*Minimum C_O of 10 μF required for stability.

FIGURE 1

OSCILLATOR

The LM3524 provides a stable on-board oscillator. Its frequency is set by an external resistor, R_T and capacitor, C_T. A graph of R_T, C_T vs oscillator frequency is shown in *Figure 2*. The oscillator's output provides the signals for triggering an internal flip-flop, which directs the PWM information to the outputs, and a blanking pulse to turn off both outputs during transitions to ensure that cross conduction does not occur. The width of the blanking pulse, or dead time, is controlled by the value of C_T, as shown in *Figure 3*. The recommended values of R_T are 1.8 kΩ to 100 kΩ, and for C_T, 0.001 μF to 0.1 μF.

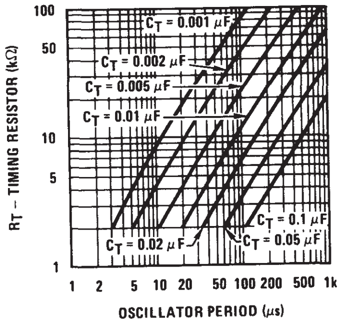


FIGURE 2

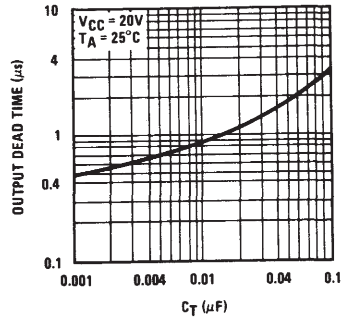


FIGURE 3

Functional Description (Continued)

ERROR AMPLIFIER

The error amplifier is a differential input, transconductance amplifier. Its gain, nominally 80 dB, is set by either feedback or output loading. This output loading can be done with either purely resistive or a combination of resistive and reactive components. A graph of the amplifier's gain vs output load resistance is shown in *Figure 4*.

The output of the amplifier, or input to the pulse width modulator, can be overridden easily as its output impedance is very high ($Z_O \simeq 5\ M\Omega$). For this reason a DC voltage can be applied to pin 9 which will override the error amplifier and force a particular duty cycle to the outputs. An example of this could be a non-regulating motor speed control where a variable voltage was applied to pin 9 to control motor speed. A graph of the output duty cycle vs the voltage on pin 9 is shown in *Figure 5*.

The amplifier's inputs have a common-mode input range of 1.8V–3.4V. The on board regulator is useful for biasing the inputs to within this range.

CURRENT LIMITING

The function of the current limit amplifier is to override the error amplifier's output and take control of the pulse width. The output duty cycle drops to about 25% when a current limit sense voltage of 200 mV is applied between the $+C_L$ and $-C_L$ terminals. Increasing the sense voltage approximately 5% results in a 0% output duty cycle. Care should be taken to ensure the −0.7V to +1.0V input common-mode range is not exceeded.

OUTPUT STAGES

The outputs of the LM3524 are NPN transistors, capable of a maximum current of 100 mA. These transistors are driven 180° out of phase and have non-committed open collectors and emitters as shown in *Figure 6*.

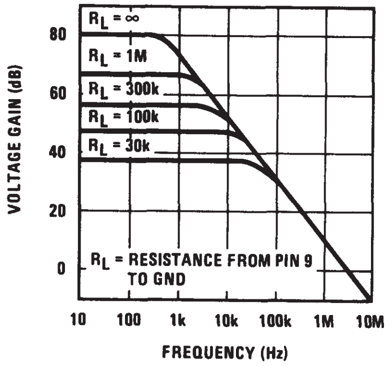


FIGURE 4

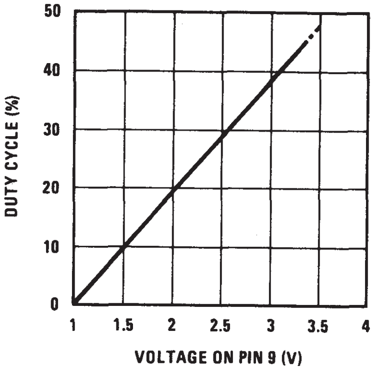


FIGURE 5

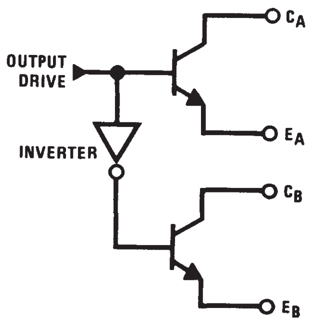
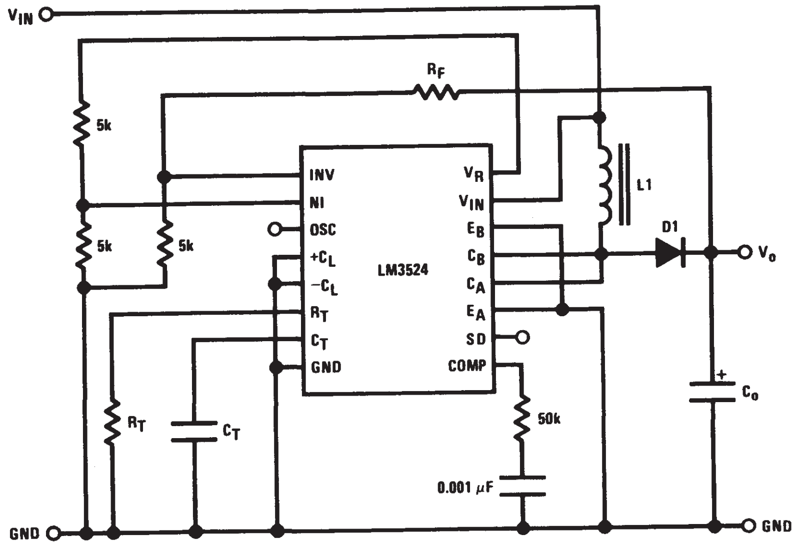


FIGURE 6

Typical Applications



DESIGN EQUATIONS

$$R_F = 5k\left(\frac{V_O}{2.5} - 1\right)$$

$$f_{OSC} \simeq \frac{1}{R_T C_T}$$

$$L1 = \frac{2.5V_{IN}^2 (V_O - V_{IN})}{f_{OSC} I_O V_O^2}$$

$$C_O = \frac{I_O (V_O - V_{IN})}{f_{OSC} \Delta V_O V_O}$$

$$I_{O(MAX)} = I_{IN} \frac{V_{IN}}{V_O}$$

FIGURE 7. Positive Regulator, Step-Up Basic Configuration ($I_{IN(MAX)}$ = 80 mA)

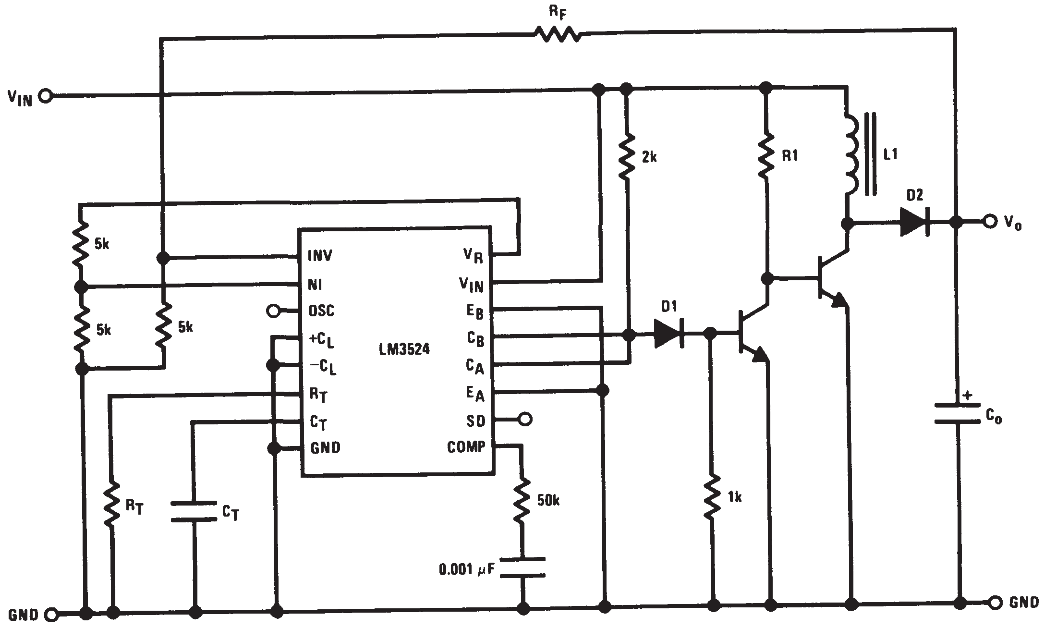
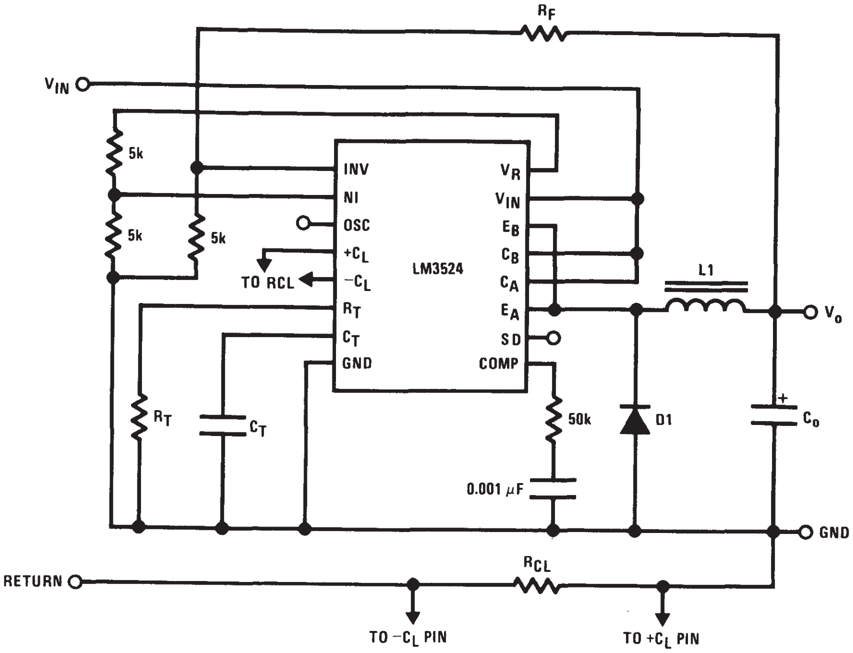


FIGURE 8. Positive Regulator, Step-Up Boosted Current Configuration

Typical Applications (Continued)



DESIGN EQUATIONS

$$R_F = 5\ \text{k}\Omega\left(\frac{V_o}{2.5} - 1\right)$$

$$R_{CL} = \frac{\text{CURRENT LIMIT SENSE VOLT}}{I_{o(MAX)}}$$

$$f_{OSC} \simeq \frac{1}{R_T C_T}$$

$$L1 = \frac{2.5V_o\ (V_{IN} - V_o)}{I_o\ V_{IN}\ f_{OSC}}$$

$$C_o = \frac{(V_{IN} - V_o)\ V_o T^2}{8\ \Delta V_o\ V_{IN} L1}$$

$$I_{o(MAX)} = I_{IN}\frac{V_{IN}}{V_o}$$

FIGURE 9. Positive Regulator, Step-Down Basic Configuration ($I_{IN(MAX)}$ = 80 mA)

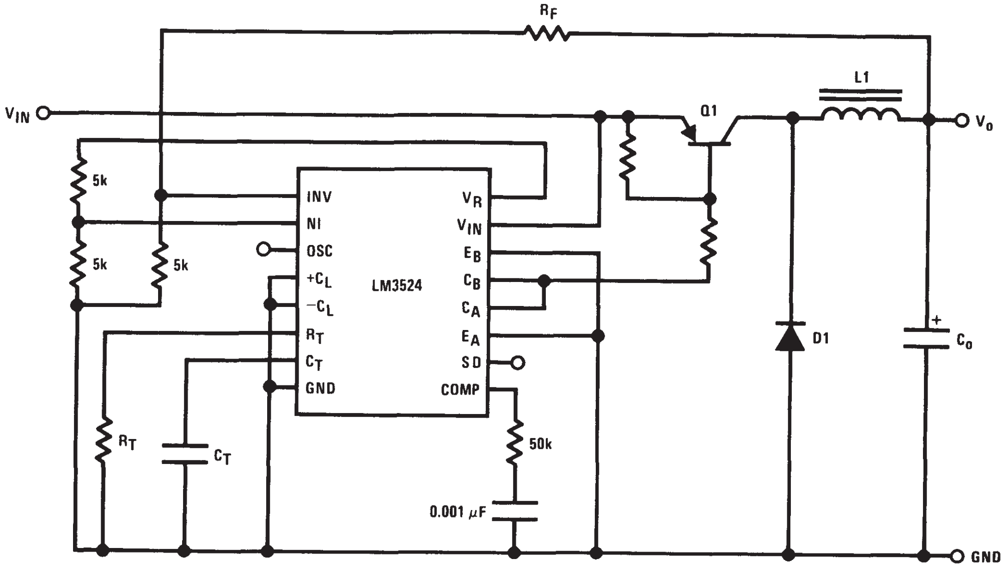
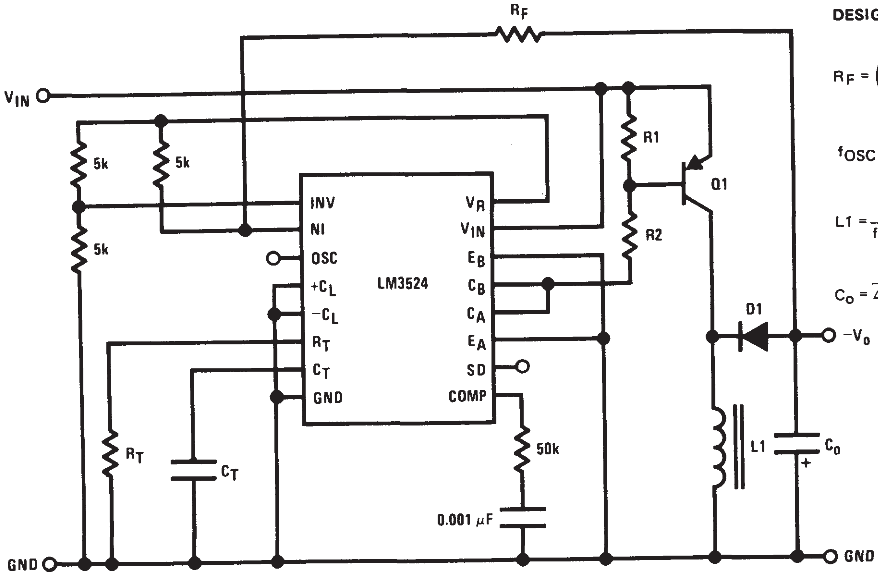


FIGURE 10. Positive Regulator, Step-Down Boosted Current Configuration

Typical Applications (Continued)



DESIGN EQUATIONS

$$R_F = \left(1 - \frac{V_o}{2.5}\right) R1$$

$$f_{OSC} \simeq \frac{1}{R_T C_T}$$

$$L1 = \frac{2.5 V_{IN} V_o}{f_{OSC} (V_o + V_{IN}) I_o}$$

$$C_o = \frac{I_o V_o}{\Delta V_o f_{OSC} (V_o + V_{IN})}$$

FIGURE 11. Boosted Current Polarity Inverter

BASIC SWITCHING REGULATOR THEORY AND APPLICATIONS

The basic circuit of a step-down switching regulator circuit is shown in *Figure 12*, along with a practical circuit design using the LM3524 in *Figure 15*.

The circuit works as follows: Q1 is used as a switch, which has ON and OFF times controlled by the pulse width modulator. When Q1 is ON, power is drawn from V_{IN} and supplied to the load through L1; V_A is at approximately V_{IN}, D1 is reverse biased, and C_o is charging. When Q1 turns OFF the inductor L1 will force V_A negative to keep the current flowing in it, D1 will start conducting and the load current will flow through D1 and L1. The voltage at V_A is smoothed by the L1, C_o filter giving a clean DC output. The current flowing through L1 is equal to the nominal DC load current plus some ΔI_L which is due to the changing voltage across it. *A good rule of thumb is to set* $\Delta I_{Lp\text{-}p} \simeq 40\% \cdot I_o$.

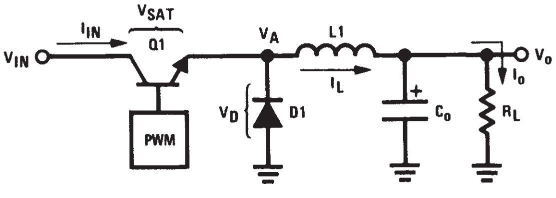


FIGURE 12. Basic Step-Down Switching Regulator

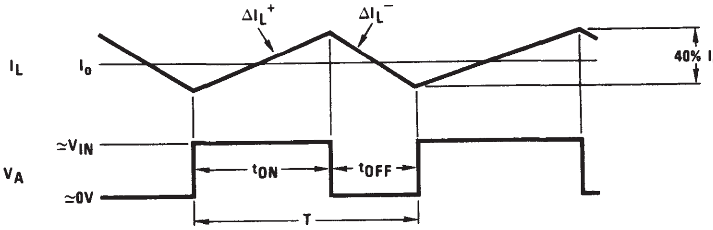


FIGURE 13

Typical Applications (Continued)

From the relation $V_L = L\frac{d_i}{d_t}$, $\Delta I_L \simeq \frac{V_L T}{L1}$

$$\Delta I_L^+ = \frac{(V_{IN} - V_o)\, t_{ON}}{L1}; \quad \Delta I_L^- = \frac{V_o\, t_{OFF}}{L1}$$

Neglecting V_{SAT}, V_D, and settling $\Delta I_L^+ = \Delta I_L^-$;

$$\boxed{V_o \simeq V_{IN}\left(\frac{t_{ON}}{t_{OFF} + t_{ON}}\right)} = V_{IN}\left(\frac{t_{ON}}{T}\right);$$

where T = Total Period

The above shows the relation between V_{IN}, V_o and duty cycle.

$$I_{IN(DC)} = I_{OUT(DC)}\left(\frac{t_{ON}}{t_{ON} + t_{OFF}}\right),$$

as Q1 only conducts during t_{ON}.

$$P_{IN} = I_{IN(DC)}V_{IN} = (I_{o(DC)})\left(\frac{t_{ON}}{t_{ON} + t_{OFF}}\right)V_{IN}$$

$$P_o = I_oV_o$$

The efficiency, η, of the circuit is:

$$\eta_{MAX} = \frac{P_o}{P_{IN}} = \frac{I_oV_o}{\frac{I_o(t_{ON})V_{IN}}{T} + \frac{(V_{SAT}\, t_{ON} + V_{D1}t_{OFF})\, I_o}{T}}$$

$$= \boxed{\frac{V_o}{V_o + 1}} \text{ for } V_{SAT} = V_{D1} = 1V.$$

η_{MAX} will be further decreased due to switching losses in Q1. For this reason Q1 should be selected to have the maximum possible f_T, which implies very fast rise and fall times.

CALCULATING INDUCTOR L1

$$t_{ON} \simeq \frac{(\Delta I_L^+) \bullet L1}{(V_{IN} - V_o)}, \quad t_{OFF} = \frac{(\Delta I_L^-) \bullet L1}{V_o}$$

$$t_{ON} + t_{OFF} = T = \frac{(\Delta I_L^+) \bullet L1}{(V_{IN} - V_o)} + \frac{(\Delta I_L^-) \bullet L1}{V_o}$$

$$= \frac{0.4I_oL1}{(V_{IN} - V_o)} + \frac{0.4I_oL1}{V_o}$$

Since $\Delta I_L^+ = \Delta I_L^- = 0.4I_o$

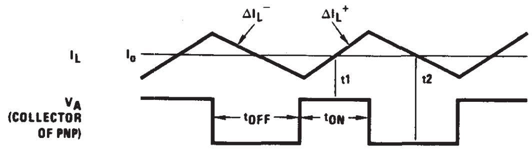


FIGURE 14

Solving the above for L1

$$\boxed{L1 = \frac{2.5\, V_o(V_{IN} - V_o)}{I_oV_{IN}\, f}}$$

where: L1 is in Henrys
f is switching frequency in Hz

CALCULATING OUTPUT FILTER CAPACITOR C_o:

Figure 14 shows L1's current with respect to Q1's t_{ON} and t_{OFF} times. This current must flow to the load and C_o. C_o's current will then be the difference between I_L, and I_o.

$$I_{C_o} = I_L - I_o$$

From *Figure 14* it can be seen that current will be flowing into C_o for the second half of t_{ON} through the first half of t_{OFF}, or a time , $t_{ON}/2 + t_{OFF}/2$. The current flowing for this time is $\Delta I_L/4$. The resulting ΔV_c or ΔV_o is described by:

$$\Delta V_{op\text{-}p} = \frac{1}{C} \bullet \frac{\Delta I_L}{4} \bullet \left(\frac{t_{ON}}{2} + \frac{t_{OFF}}{2}\right)$$

$$= \frac{\Delta I_L}{4C}\left(\frac{t_{ON} + t_{OFF}}{2}\right)$$

Since $\Delta I_L = \frac{V_o(T - t_{ON})}{L1}$ and $t_{ON} = \frac{V_oT}{V_{IN}}$

$$\Delta V_{op\text{-}p} = \frac{V_o\left(T - \frac{V_oT}{V_{IN}}\right)}{4C\ L1}\left(\frac{T}{2}\right) = \frac{(V_{IN} - V_o)\, V_oT^2}{8V_{IN}C_oL1} \quad \text{or}$$

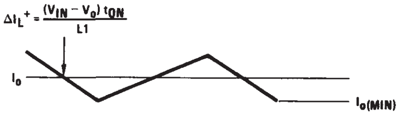
$$\boxed{C_o = \frac{(V_{IN} - V_o)V_o\, T^2}{8\Delta V_oV_{IN}L1}}$$

where: C is in farads, T is $\frac{1}{\text{switching frequency}}$,

ΔV_o is p-p output ripple

The inductor's current cannot be allowed to fall to zero, as this would cause the inductor to saturate. For this reason some minimum I_o is required as shown below:

$$I_{o(MIN)} = \frac{(V_{IN} - V_o)\, t_{ON}}{2L1} = \boxed{\frac{(V_{IN} - V_o)\, V_o}{2fV_{IN}L1}}$$



Typical Applications (Continued)

A complete step-down switching regulator schematic, using the LM3524, is illustrated in *Figure 15*. Transistors Q1 and Q2 have been added to boost the output to 1A. The 5V regulator of the LM3524 has been divided in half to bias the error amplifier's non-inverting input to within its common-mode range. Since each output transistor is on for half the period, actually 45%, they have been paralleled to allow longer possible duty cycles, up to 90%. This makes a lower possible input voltage. The output voltage is set by:

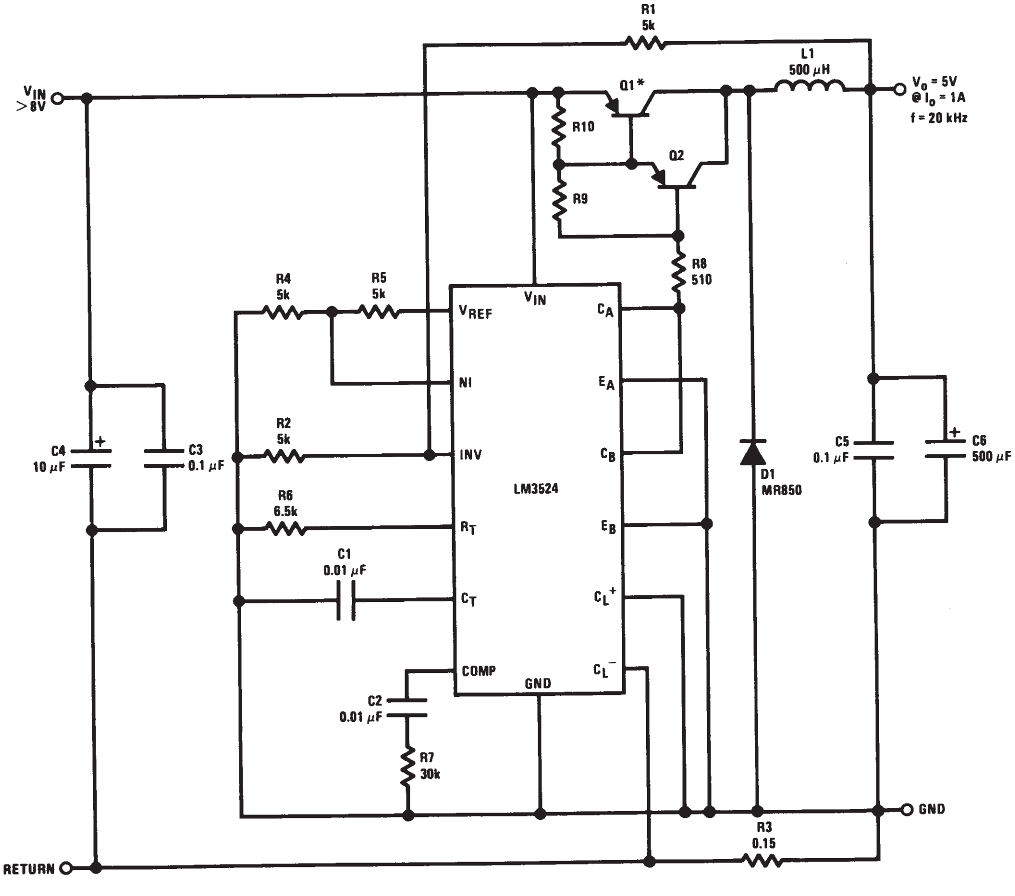
$$V_O = V_{NI}\left(1 + \frac{R1}{R2}\right),$$

where V_{NI} is the voltage at the error amplifier's non-inverting input.

Resistor R3 sets the current limit to:

$$\frac{200\text{ mV}}{R3} = \frac{200\text{ mV}}{0.15} = 1.3\text{A}.$$

Figure 16 and *17* show a PC board layout and stuffing diagram for the 5V, 1A regulator of *Figure 15*. The regulator's performance is listed in Table I.



*Mounted to Staver Heatsink No. V5-1.

Q1 = BD344

Q2 = 2N5023

L1 = > 40 turns No. 22 wire on Ferroxcube No. K300502 Torroid core.

FIGURE 15. 5V, 1 Amp Step-Down Switching Regulator

Typical Applications (Continued)

TABLE I

PARAMETER	CONDITIONS	TYPICAL CHARACTERISTICS
Output Voltage	$V_{IN} = 10V$, $I_O = 1A$	5V
Switching Frequency	$V_{IN} = 10V$, $I_O = 1A$	20 kHz
Short Circuit Current Limit	$V_{IN} = 10V$	1.3A
Load Regulation	$V_{IN} = 10V$, $I_O = 0.2 - 1A$	3 mV
Line Regulation	$\Delta V_{IN} = 10 - 20V$, $I_O = 1A$	6 mV
Efficiency	$V_{IN} = 10V$, $I_O = 1A$	80%
Output Ripple	$V_{IN} = 10V$, $I_O = 1A$	10 mVp-p

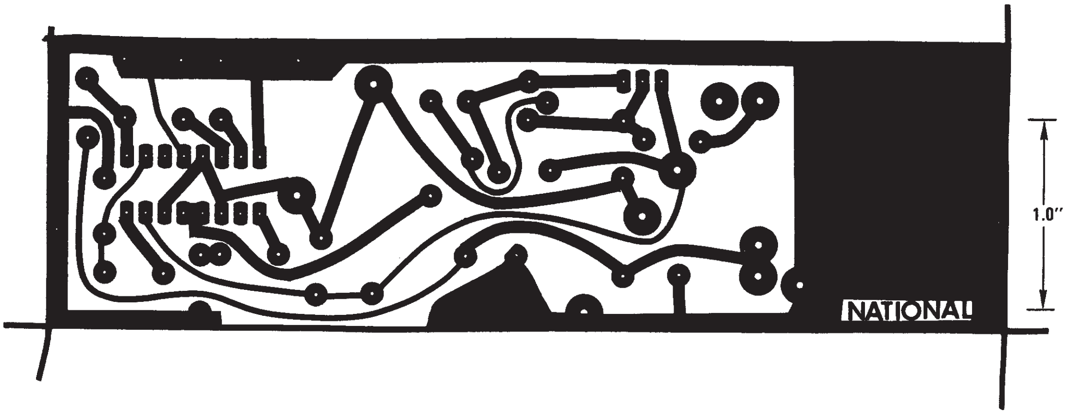


FIGURE 16. 5V, 1 Amp Switching Regulator, Foil Side

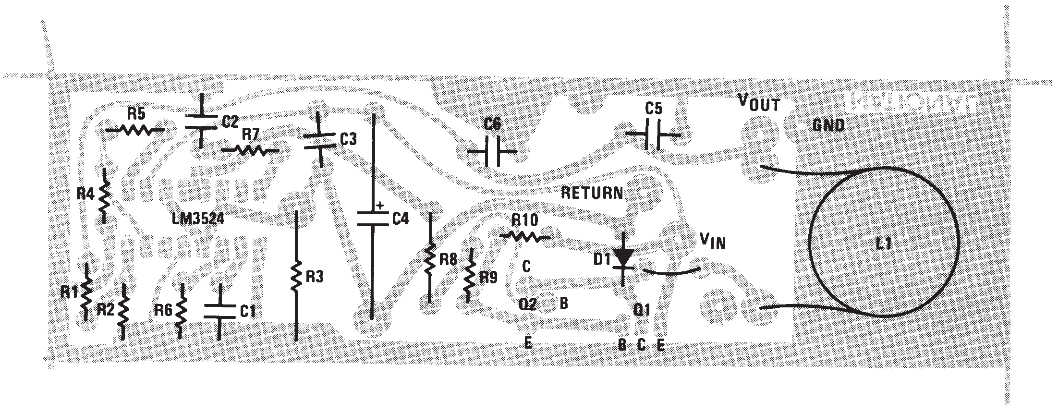


FIGURE 17. Stuffing Diagram, Component Side.

Typical Applications (Continued)

THE STEP-UP SWITCHING REGULATOR

Figure 18 shows the basic circuit for a step-up switching regulator. In this circuit Q1 is used as a switch to alternately apply V_{IN} across inductor L1. During the time, t_{ON}, Q1 is ON and energy is drawn from V_{IN} and stored in L1; D1 is reverse biased and I_o is supplied from the charge stored in C_O. When Q1 opens, t_{OFF}, voltage V1 will rise positively to the point where D1 turns ON. The output current is now supplied through L1,D1 to the load and any charge lost from C_O during t_{ON} is replenished. Here also, as in the step-down regulator, the current through L1 has a DC component plus some ΔI_L. ΔI_L is again selected to be approximately 40% of I_L. *Figure 19* shows the inductor's current in relation to Q1's ON and OFF times.

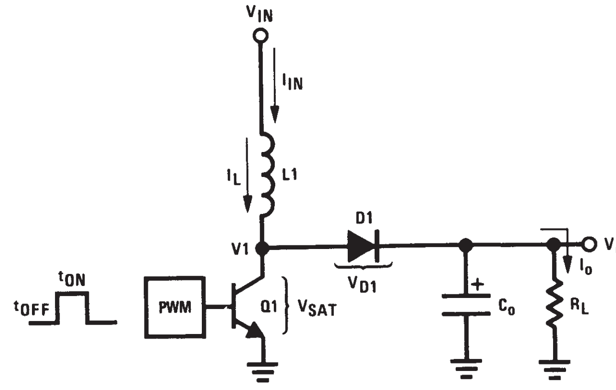


FIGURE 18. Basic Step-Up Switching Regulator

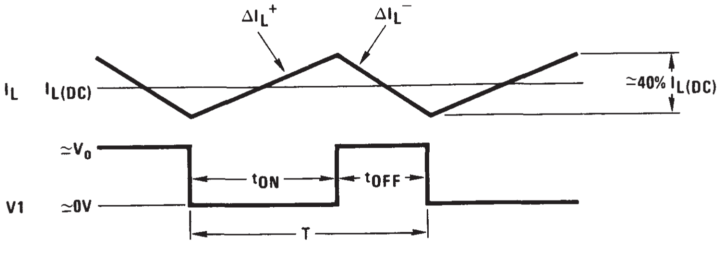


FIGURE 19

Typical Applications (Continued)

From $\Delta I_L = \frac{V_L T}{L}$, $\Delta I_L^+ \simeq \frac{V_{IN} t_{ON}}{L1}$

and $\Delta I_L^- \simeq \frac{(V_o - V_{IN}) t_{OFF}}{L1}$

Since $\Delta I_L^+ = \Delta I_L^-$, $V_{IN} t_{ON} = V_o t_{OFF} - V_{IN} t_{OFF}$,

and neglecting V_{SAT} and V_{D1}

$$\boxed{V_o \simeq V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right)}$$

The above equation shows the relationship between V_{IN}, V_o and duty cycle.

In calculating input current $I_{IN(DC)}$, which equals the inductor's DC current, assume first 100% efficiency:

$$P_{IN} = I_{IN(DC)} V_{IN}$$

$$P_{OUT} = I_o V_o = I_o \ V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right)$$

for η = 100%, $P_{OUT} = P_{IN}$

$$I_o \ V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right) = I_{IN(DC)} \ V_{IN}$$

$$I_{IN(DC)} = I_o\left(1 + \frac{t_{ON}}{t_{OFF}}\right)$$

This equation shows that the input, or inductor, current is larger than the output current by the factor $(1 + t_{ON}/t_{OFF})$. Since this factor is the same as the relation between V_o and V_{IN}, $I_{IN(DC)}$ can also be expressed as:

$$\boxed{I_{IN(DC)} = I_o\left(\frac{V_o}{V_{IN}}\right)}$$

So far it is assumed η = 100%, where the actual efficiency or η_{MAX} will be somewhat less due to the saturation voltage of Q1 and forward on voltage of D1. The internal power loss due to these voltages is the average I_L current flowing, or I_{IN}, through either V_{SAT} or V_{D1}. For $V_{SAT} = V_{D1}$ = 1V this power loss becomes $I_{IN(DC)}$ (1V). η_{MAX} is then:

$$\eta_{MAX} = \frac{P_o}{P_{IN}} = \frac{V_o I_o}{V_o I_o + I_{IN}\ (1V)} = \frac{V_o I_o}{V_o I_o + I_o\left(1 + \frac{t_{ON}}{t_{OFF}}\right)}$$

From $V_o = V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right)$,

$$\boxed{\eta_{max} = \frac{V_{IN}}{V_{IN} + 1}}$$

This equation assumes only DC losses, however η_{MAX} is further decreased because of the switching time of Q1 and D1.

In calculating the output capacitor C_o it can be seen that C_o supplies I_o during t_{ON}. The voltage change on C_o during this time will be some $\Delta V_c = \Delta V_o$ or the output ripple of the regulator. Calculation of C_o is:

$$\Delta V_o = \frac{I_o t_{ON}}{C_o} \text{ or } C_o = \frac{I_o t_{ON}}{\Delta V_o}$$

From $V_o = V_{IN}\left(\frac{T}{t_{OFF}}\right)$; $t_{OFF} = \frac{V_{IN}}{V_o} T$

where $T = t_{ON} + t_{OFF} = \frac{1}{f}$

$t_{ON} = T - \frac{V_{IN}}{V_o} T = T\left(\frac{V_o - V_{IN}}{V_o}\right)$ therefore:

$$C_o = \frac{I_o T\left(\frac{V_o - V_{IN}}{V_o}\right)}{\Delta V_o} = \boxed{\frac{I_o(V_o - V_{IN})}{f \Delta V_o V_o}}$$

where: C_o is in farads, f is the switching frequency, ΔV_o is the p-p output ripple

Calculation of inductor L1 is as follows:

$L1 = \frac{V_{IN} t_{ON}}{\Delta I_L^+}$, since during t_{ON},

V_{IN} is applied across L1

$\Delta I_{Lp\text{-}p} = 0.4 I_L = 0.4 I_{IN} = 0.4 I_o\left(\frac{V_o}{V_{IN}}\right)$, therefore:

$L1 = \frac{V_{IN} t_{ON}}{0.4 I_o\left(\frac{V_o}{V_{IN}}\right)}$ and since $t_{ON} = \frac{T(V_o - V_{IN})}{V_o}$

$$\boxed{L1 = \frac{2.5\ V_{IN}^2 (V_o - V_{IN})}{f\ I_o V_o^2}}$$

where : L1 is in henrys, f is the switching frequency in Hz

Typical Applications (Continued)

To apply the above theory, a complete step-up switching regulator is shown in *Figure 20*. Since V_{IN} is 5V, V_{REF} is tied to V_{IN}. The input voltage is divided by 2 to bias the error amplifier's inverting input. The output voltage is:

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) \cdot V_{INV} = 2.5 \cdot \left(1 + \frac{R2}{R1}\right)$$

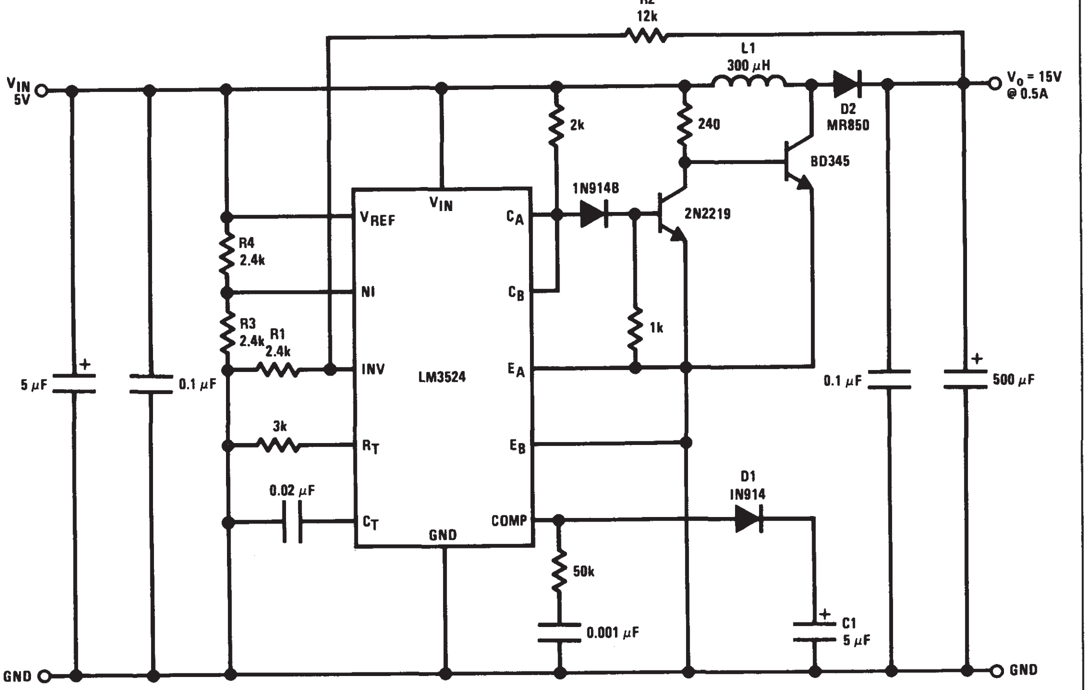
The network D1, C1 forms a slow start circuit.

This holds the output of the error amplifier initially low thus reducing the duty-cycle to a minimum. Without the slow start circuit the inductor may saturate at turn-on because it has to supply high peak currents to charge the output capacitor from 0V. It should also be noted that this circuit has no supply rejection. By adding a reference voltage at the non-inverting input to the error amplifier, see *Figure 21*, the input voltage variations are rejected.

The LM3524 can also be used in inductorless switching regulators. *Figure 22* shows a polarity inverter which if connected to *Figure 20* provides a −15V unregulated output.

MOTOR SPEED CONTROL

Figure 23 shows a regulating series DC motor speed control circuit using the LM3524 for the control and drive for the motor and the LM2907 as a speed sensor for the feedback network.



L1 = > 25 turns No. 24 wire on Ferroxcube No. K300502 Torroid core.

FIGURE 20. 15V, 0.5A Step-Up Switching Regulator

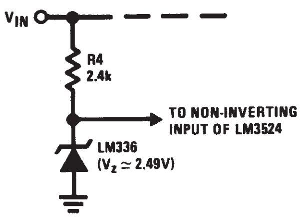


FIGURE 21

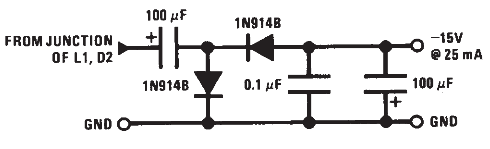


FIGURE 22

Typical Applications (Continued)

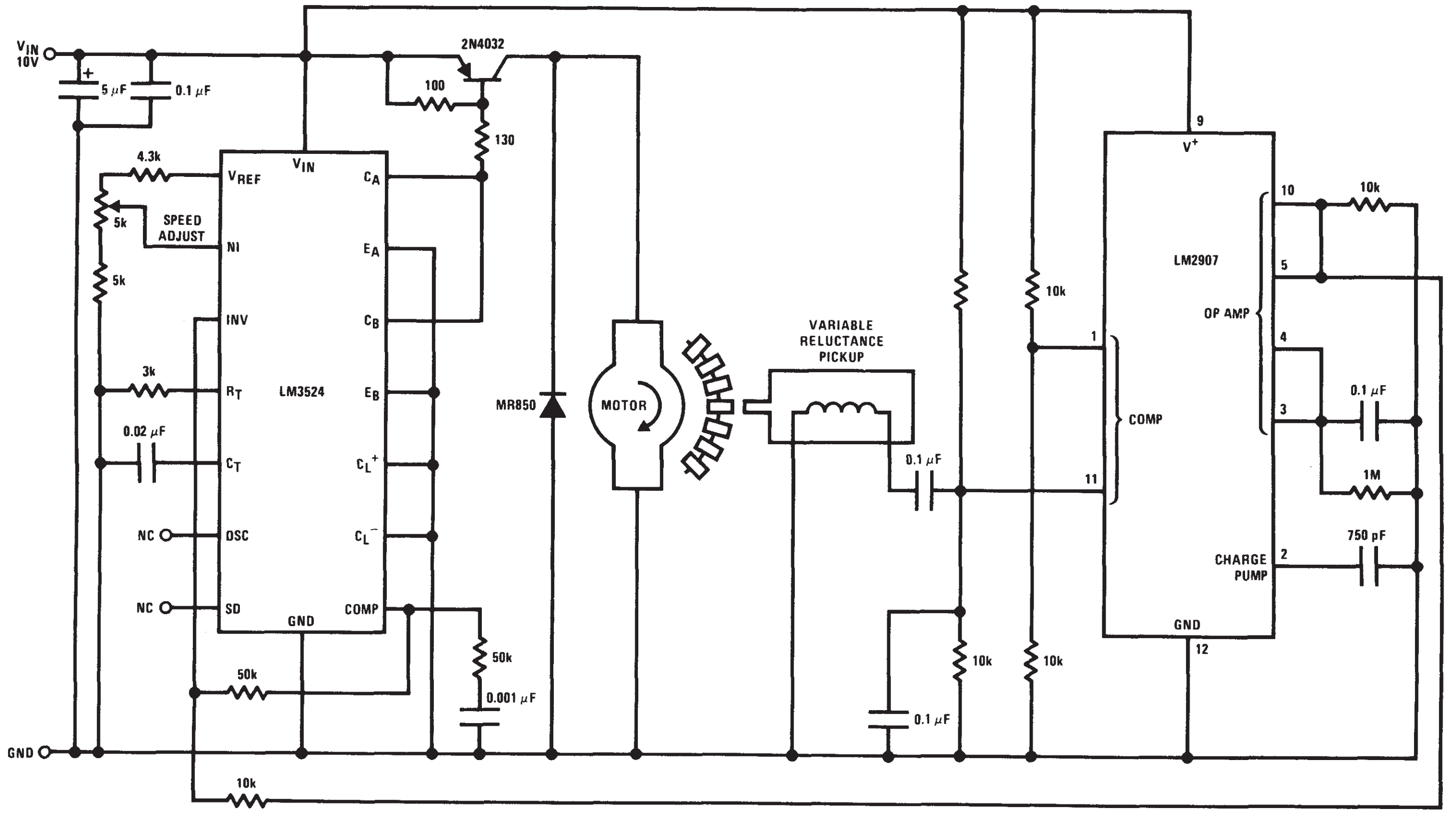


FIGURE 23. Motor Speed Control