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Headland
Technology

HT209
Graphics Chip

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HT209
Graphics Chip

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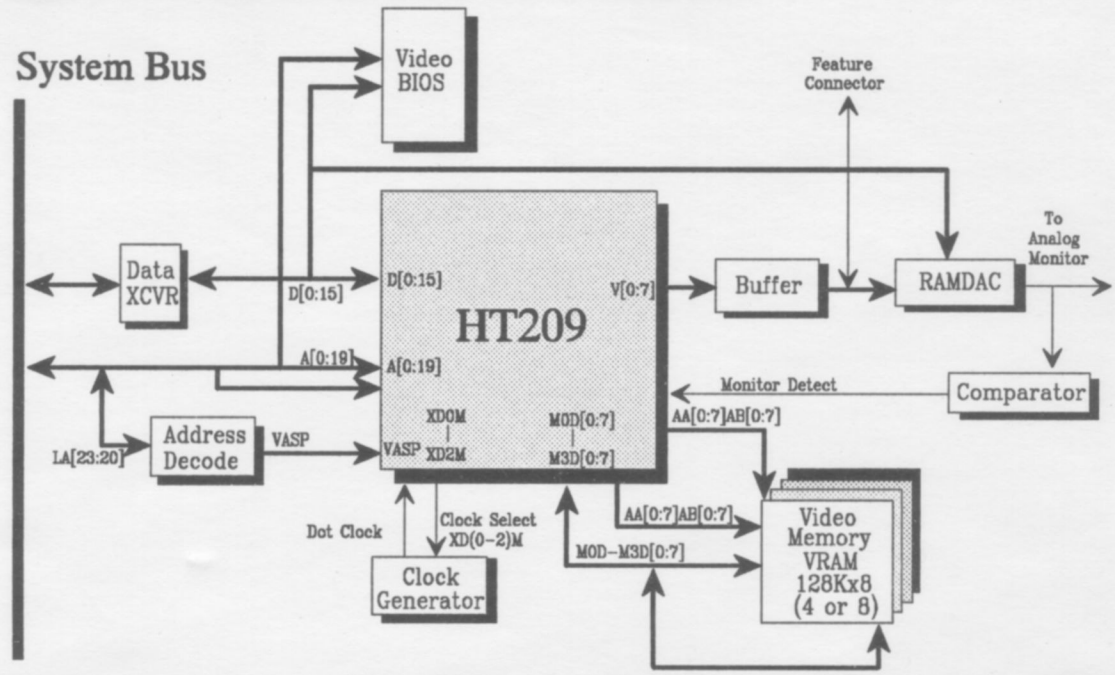
FEATURES

- Fully hardware compatible with the IBM VGA
- Hercules and CGA register compatibility; BIOS compatible with the EGA
- Fast host access to 120ns DRAM video memory: every other cycle or better for all standard VGA graphics modes plus any time during horizontal and vertical retrace; paged DRAM mode supports host access every fourth cycle up to 800x600 graphics resolutions
- Built-in support for VRAMs; provides host access every cycle for all standard linear VGA graphics modes, every second cycle up to 800x600, every fourth cycle up to 1024x768; VRAM operation transparent to existing application programs
- Software-selectable 16-bit memory and I/O interface logic eliminates 8-bit bus emulation wait states in 80286 and 80386 computers; true word access in text mode and odd/even graphics modes (including hi-res modes).
- Supports both PC/AT and PS/2 bus interfaces
- Operates with dot clocks of up to 75MHz
- Foreground/background write mode speeds bit-mapped fonts and dithered fills
- Supports 132-column text on all monitors with 120ns DRAMs (Text to 40MHz with 120ns RAMs, 50MHz with 100ns, & 65MHz with 80ns)
- Supports up to 800x600 256-color and 1024x768 256-color non-interlaced resolutions
- Interlace capability for 8514 monitor support
- Hardware graphics pointer
- 3270 compatible text mode (blink, reverse video, under/overline, color, and 8 font selections)
- Supports dual VGA boards in one system (1 color, 1 monochrome)

HT209 High Performance VGA Application



OVERVIEW

The HT209 chip is hardware and software compatible with the IBM™ VGA while providing improved performance and additional functionality. Designed to operate at dot clock rates up to 75 MHz, the HT209 supports both monochrome and color high resolution graphics and text display modes on displays such as IBM's PS/2™ analog monitors and the NEC MultiSync™ and Sony MultiScan™ monitors. The HT209 is intended to be used with an external palette, such as the IMSG176, which provides blanking and look-up of the 8 bits per pixel generated by the HT209 into a larger color set.

The HT209 implements all registers, data paths, and functionality of the IBM VGA, including features not currently used by IBM.

The HT209 can be programmed to present 16-bit display memory and I/O interfaces to the host, eliminating 8-bit bus emulation wait states in AT™, Micro Channel™, and other high-performance buses. The HT209 is designed to interface to the PC™, AT and Micro Channel buses with minimal external support circuitry.

All memory cycles not used to refresh the display or video memory can be allocated to process host memory requests. During display enable the HT209 can achieve a 1:2 interleave with 120ns DRAMs for all standard VGA graphics modes, including 640x480 modes, and a 1:4 paged mode interleave with 120ns DRAMs in 800x600 60Hz graphics modes.

Once the BIOS has initialized VRAM mode, the HT209 supports VRAMs transparently to all software without any sacrifice of VGA compatibility. No external logic is required to support VRAMs. In VRAM mode, a 1:1 interleave can be achieved for all standard VGA graphics modes, a 1:2 interleave can be achieved for 800x600 graphics modes. A 1:4 interleave can be achieved for 1024x768 graphics modes and 132-column text modes. A 1:4 interleave can also be achieved for all other graphics modes up to 65MHz and text modes up to 40MHz.

Hardware support is provided to display a 32x32 pixel pattern for use as a mouse pointer.

COMPATIBILITY

The HT209 is fully compatible with the IBM VGA at the register level. In fact, the HT209 incorporates useful registers not documented by IBM and supports modes which are not used by the current IBM VGA BIOS. These modes and registers are not described by IBM but are none the less powerful and likely to be used in the future.

The HT209 chip provides the same BIOS level compatibility with the EGA, CGA, and MDA as does the IBM VGA. In addition, it provides register level compatibility with CGA and Hercules adapters.

BUSES

With only minimal support logic, the HT209 operates directly on the Micro Channel, AT, and PC buses. Both 8 bit and 16 bit data transfers are supported for I/O, display memory, and BIOS ROM.

RAM CONFIGURATIONS

The HT209 supports multiple RAM configurations including DRAMs, VRAMs in both 256K bit (64kx4) and 1MB (256kx4) and (128kx8) configurations. If 256K bit chips are used, multiple banks are supported. It also supports 64k x 16 DRAMs.

PERFORMANCE

The HT209 is designed to be a high performance VGA chip, greatly speeding up all graphics operations in both IBM and enhanced text and graphics modes. This performance improvement is achieved by:

1. reducing wait states,
2. using masked VRAM writes,
3. providing a hardware pointer,
4. implementing special data paths to speed up dithered fills and text, and
5. supporting a 16 bit ROM interface.

In order to reduce wait states, the HT209 offers timing states that provide 3 1/2 times the display memory bandwidth of the IBM VGA in all standard VGA graphics modes with standard 120ns DRAMs. Even at 800x600 resolutions using 120ns DRAMs, the HT209 provides nearly three times the memory bandwidth of the IBM VGA at 640x480 resolution. At all VGA compatible modes, the CPU gets access every other character clock; at 800x600, a special paged mode allows the CPU access every fourth character clock. By contrast, the IBM VGA allows access every seventh character clock in its 640x480 mode. The HT209 allows CPU access as much as possible during non-display times.

Wait states are reduced even more dramatically when VRAMs are used with the HT209. VRAMs are a dual-ported memory chip, the normal row/column access constitutes one port, and the shift register the other. The ports are linked only in that a row access must be used to load the shift register which is used for refreshing the display. The addressing of the memory is arranged so that a row of the memory chip contains bits that describe adjacent pixels on a scan line. The shift register is loaded at the beginning of the scan line, and then shifted to obtain the values of subsequent pixels. Since the shift register can operate at only about 30MHz, several chips are usually operated in parallel, and a final high-speed video buffer produces values at pixel rates. If necessary, the VRAM shift register can be loaded again during a scan line to accomodate long scan lines. Only infrequently must update accesses be suspended so that a row access can reload the shift register.

HT209 VRAM allows up to seven times the memory bandwidth of the IBM VGA. At 800x600 resolutions the band width is more than five times greater than the IBM 640x480 mode. In fact, at all modes up to 720x540, including all VGA compatible modes, the CPU gets an access every character clock. At 800x600, the CPU gets an access every other character clock and at 1024x768 the CPU gets an access every fourth character clock.

Greater memory bandwidth does not by itself greatly improve display performance. True high

performance video requires that the improved memory bandwidth be available in all modes, not just the enhanced ones so that all software will run faster. In addition the display memory bandwidth must be available to the CPU. The HT209 accomplishes that.

Most video adapters are strictly 8 bit devices and consequently have a minimum of three wait states inserted during every CPU access on AT compatible buses. The HT209 supports independently selectable 16 bit interfaces to the system memory and the I/O buses, eliminating wait states when emulating the 8 bit bus. The benefit of the 16 bit bus is clear since pixels are controlled by manipulating display memory.

What is not so obvious is that the 16 bit I/O interface will also produce comparable improvement in all graphics modes since the Bit Mask, Set/Reset, Map Mask, and other indexed VGA registers are written to as often as once per pixel when drawing graphics.

The HT209 adds another feature to reduce wait states to virtually zero on CPU writes: the "FastWrite™" feature. When the CPU writes to display memory, the HT209 immediately lets the CPU continue processing rather than forcing a wait state until the write operation is completed. Therefore, the write operation continues in the background while the CPU continues processing independently. The background processing of the write allows the CPU to write as fast as it does to normal system RAM. This is a vast improvement over other display adapters which is often 14 times slower than system RAM.

This FastWrite feature is especially suitable with the 16 bit memory interface and VRAMs. Together, these features allow display memory to approach system RAM in overall performance. This is about an order of magnitude of speed improvement over the IBM display adapter in most cases and no less than 2 to 3 times in all cases.

The HT209 supports masked writes to VRAMs (write per bit writes), which allow selected bits within a display memory byte to be modified without first reading the byte. This feature cuts in half the number of display memory accesses required when drawing lines, clipping on fills and bitblts, and drawing transparent text. Additionally, it frees up the Bit Mask register for use in combining foreground and background patterns, thereby speeding up color expansion of binary data, especially opaque text.

The HT209's 32x32 hardware pointer (which works in all modes, including text modes) improves both the appearance and performance of environments which use pointers, such as Microsoft Windows™. The improvement in appearance occurs because the hardware pointer eliminates the need to erase the pointer whenever the bit-map is drawn into, thereby eliminating flicker. The improvement in performance occurs because the hardware pointer eliminates the considerable time required to save and restore the area of bit-map covered by the pointer and to draw the pointer.

In order to boost filling and text drawing performance, especially in Windows™, the HT209 provides all data paths required to draw independently-controllable foreground and background colors or dither patterns with a single CPU write; the masked write feature makes it possible to do all this with a single write to VRAMs even when the operation is not byte-aligned. By contrast, two to twelve display memory accesses are required to draw dithered text on a standard VGA. The HT209 also provides a special data path for expanding two-color font data into 16-color text on a 16-color background with a single CPU write.

The net effect of these performance enhancements is a chip, the HT209, around which an adapter can be built which is two to ten times faster than the IBM VGA, running off-the-shelf software. Specially optimized software, such as Windows™ drivers, achieves even higher performance.

RESOLUTION & COLOR

The HT209 supports much higher resolution, with more simultaneous colors, than does the IBM VGA. In addition to all standard IBM VGA modes, the HT209 supports 800x600 256-color modes with 120ns DRAMs. VRAMs support 1024x768 256-color and 720x540 256-color modes as well as all the above-mentioned modes.

As regards text modes, in addition to all IBM VGA text modes the HT209 supports 132-column text on PS/2-type fixed-frequency monitors with 120ns DRAMs, and supports 132-column text on PS/2 monitors as well with VRAMs.

VIRTUAL VGA

The HT209 provides all internal controls and external pins required to support up to four virtual VGA sessions in 1MB of memory. (This requires 256K DRAMs/VRAMs.) This feature dramatically increases video speed when switching tasks for multitasking environments such as 80386 virtual 8086 operating systems.

3270-COMPATIBLE TEXT MODE SUPPORT

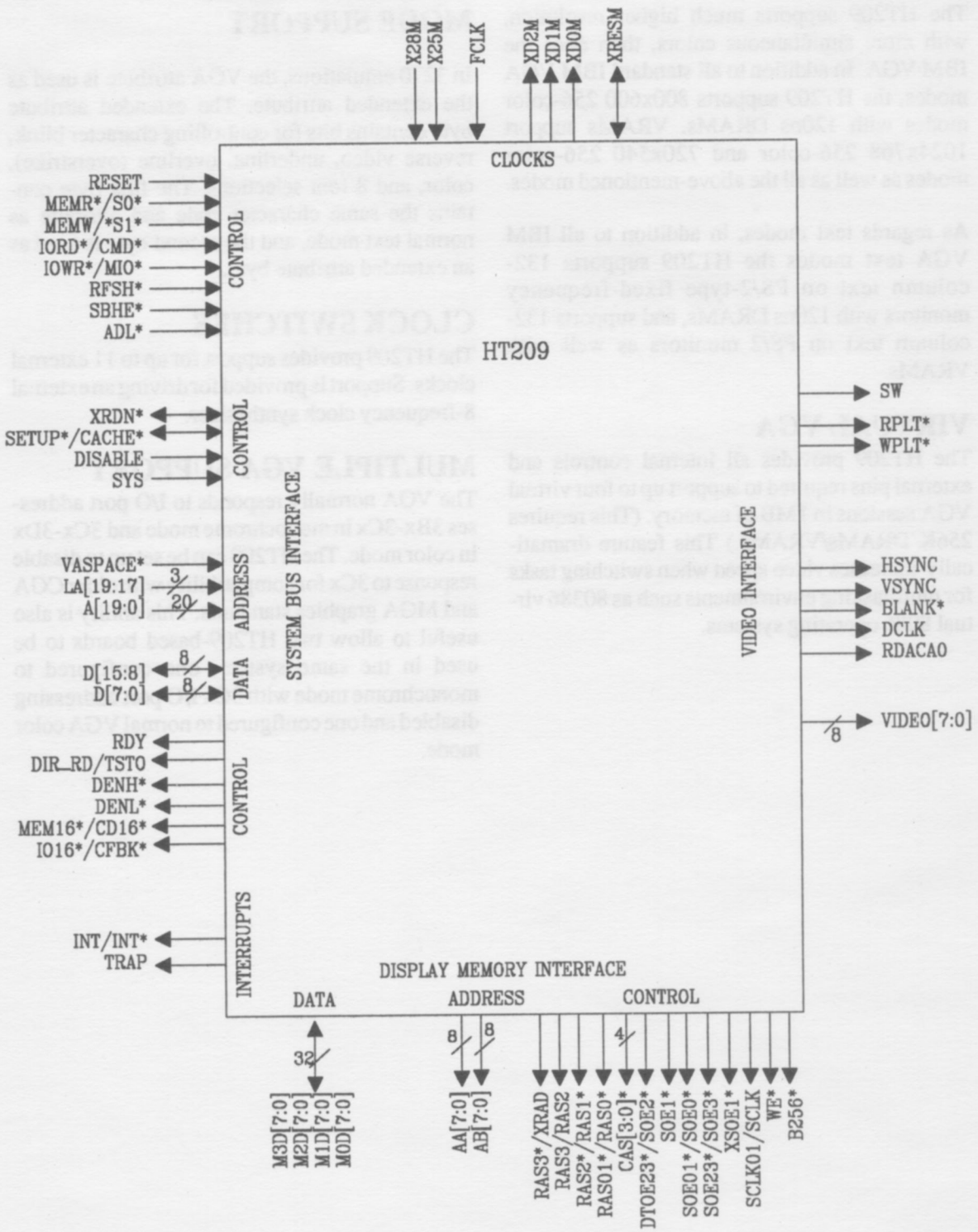
In 3270 emulations, the VGA attribute is used as the extended attribute. The extended attribute byte contains bits for controlling character blink, reverse video, underline, overline (overstrike), color, and 8 font selections. The first byte contains the same character code and attribute as normal text mode, and the second byte is used as an extended attribute byte.

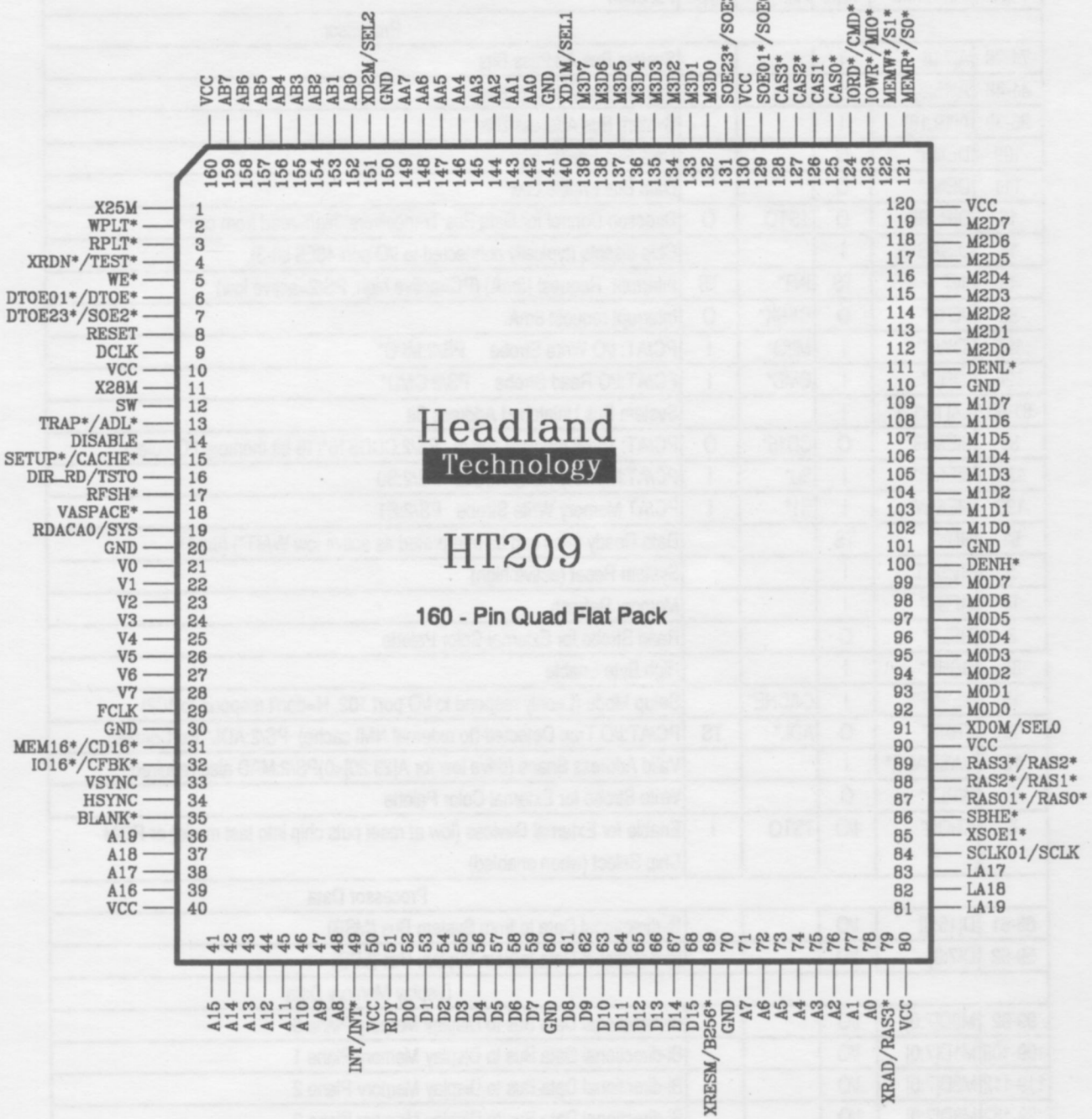
CLOCK SWITCHES

The HT209 provides support for up to 11 external clocks. Support is provided for driving an external 8-frequency clock synthesizer.

MULTIPLE VGA SUPPORT

The VGA normally responds to I/O port addresses 3Bx-3Cx in monochrome mode and 3Cx-3Dx in color mode. The HT209 can be set up to disable response to 3Cx for compatibility with older CGA and MGA graphics standards. This ability is also useful to allow two HT209-based boards to be used in the same system, one configured to monochrome mode with 3Cx I/O port addressing disabled and one configured to normal VGA color mode.


X28M
X25M
FCLK
XD2M
XD1M
XD0M
XRESM
CLOCKS
RESET
MEMR*/S0*
MEMW/*S1*
IORD*/CMD*
IOWR*/MIO*
RFSH*
SBHE*
ADL*
CONTROL
HT209
XRDN*
SETUP*/CACHE*
DISABLE
SYS
CONTROL
SYSTEM BUS INTERFACE
VASPACE*
LA[19:17]
A[19:0]
3
20
ADDRESS
D[15:8]
D[7:0]
8
8
DATA
RDY
DIR_RD/TSTO
DENH*
DENL*
MEM16*/CD16*
IO16*/CFBK*
CONTROL
INT/INT*
TRAP
INTERRUPTS
SW
RPLT*
WPLT*
VIDEO INTERFACE
HSYNC
VSYNC
BLANK*
DCLK
RDACA0
VIDEO[7:0]
8
DISPLAY MEMORY INTERFACE
DATA
ADDRESS
CONTROL
32
8
8
4
M3D[7:0]
M2D[7:0]
M1D[7:0]
M0D[7:0]
AA[7:0]
AB[7:0]
RAS3*/XRAD
RAS3/RAS2
RAS2*/RAS1*
RAS01*/RAS0*
CAS[3:0]*
DTOE23*/SOE2*
SOE1*
SOE01*/SOE0*
SOE23*/SOE3*
XSOE1*
SCLKO1/SCLK
WE*
B256*


Headland
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HT209
160 - Pin Quad Flat Pack
1 X25M
2 WPLT*
3 RPLT*
4 XRDN*/TEST*
5 WE*
6 DTOE01*/DTOE*
7 DTOE23*/SOE2*
8 RESET
9 DCLK
10 VCC
11 X28M
12 SW
13 TRAP*/ADL*
14 DISABLE
15 SETUP*/CACHE*
16 DIR_RD/TSTO
17 RFSH*
18 VASPACE*
19 RDACA0/SYS
20 GND
21 V0
22 V1
23 V2
24 V3
25 V4
26 V5
27 V6
28 V7
29 FCLK
30 GND
31 MEM16*/CD16*
32 IO16*/CFBK*
33 VSYNC
34 HSYNC
35 BLANK*
36 A19
37 A18
38 A17
39 A16
40 VCC
41 A15
42 A14
43 A13
44 A12
45 A11
46 A10
47 A9
48 A8
49 INT/INT*
50 VCC
51 RDY
52 D0
53 D1
54 D2
55 D3
56 D4
57 D5
58 D6
59 D7
60 GND
61 D8
62 D9
63 D10
64 D11
65 D12
66 D13
67 D14
68 D15
69 XRESM/B256*
70 GND
71 A7
72 A6
73 A5
74 A4
75 A3
76 A2
77 A1
78 A0
79 XRAD/RAS3*
80 VCC
81 LA19
82 LA18
83 LA17
84 SCLK01/SCLK
85 XSOE1*
86 SBHE*
87 RAS01*/RAS0*
88 RAS2*/RAS1*
89 RAS3*/RAS2*
90 VCC
91 XD0M/SEL0
92 M0D0
93 M0D1
94 M0D2
95 M0D3
96 M0D4
97 M0D5
98 M0D6
99 M0D7
100 DENH*
101 GND
102 M1D0
103 M1D1
104 M1D2
105 M1D3
106 M1D4
107 M1D5
108 M1D6
109 M1D7
110 GND
111 DENL*
112 M2D0
113 M2D1
114 M2D2
115 M2D3
116 M2D4
117 M2D5
118 M2D6
119 M2D7
120 VCC
121 MEMR*/S0*
122 MEMW*/S1*
123 IOWR*/M0*
124 IORD*/CMD*
125 CAS0*
126 CAS1*
127 CAS2*
128 CAS3*
129 SOE01*/SOE0*
130 VCC
131 SOE23*/SOE3*
132 M3D0
133 M3D1
134 M3D2
135 M3D3
136 M3D4
137 M3D5
138 M3D6
139 M3D7
140 XD1M/SEL1
141 GND
142 AA0
143 AA1
144 AA2
145 AA3
146 AA4
147 AA5
148 AA6
149 AA7
150 GND
151 XD2M/SEL2
152 AB0
153 AB1
154 AB2
155 AB3
156 AB4
157 AB5
158 AB6
159 AB7
160 VCC

Pin #	Pin Name	Type	Alt.	Type	Function
					Processor
71-78	A[7:0]	I			System Bus Address Bits
41-48	A[15:8]	I			System Bus Address Bits
36-39	A[19:16]	I			System Bus Address Bits
100	DENH*	O			Data Bus Enable High
111	DENL*	O			Data Bus Enable Low
16	DIR_RD	O	TSTO	O	Direction Control for Data Bus Tranceivers (high=read from chip)
14	DISABLE	I			Chip disable (typically connected to I/O port 46E8 bit-3)
49	INT	TS	INT*	TS	Interrupt Request (8mA) (PC=active high, PS/2=active low)
32	I/O16*	O	CFBK*	O	Interrupt request 8mA
123	IOWR*	I	MI/O*	I	PC/AT: I/O Write Strobe PS/2:MI/O*
124	IORD*	I	CMD*	I	PC/AT:I/O Read Strobe PS/2:CMD*
81-83	LA[19:17]	I			System Bus Unlatched Address Bit
31	MEM16*	O	CD16*	O	PC/AT: 16-bit memory select PS/2:CDDS16*(16-bit memory I/O select)
121	MEMR*	I	S0*	I	PC/AT:Memory Read Strobe PS/2:S0
122	MEMW*	I	S1*	I	PC/AT:Memory Write Strobe PS/2:S1
51	RDY	TS			Data Ready (also can be interpreted as active low WAIT*) (8mA)
8	RESET	I			System Reset (active high)
17	RFSH*	I			Memory Refresh
3	RPLT*	O			Read Strobe for External Color Palette
86	SBHE*	I			High Byte Enable
15	SETUP*	I	CACHE*		Setup Mode (L=only respond to I/O port 102, H=don't respond to 102)
13	TRAP*	O	ADL*	TS	PC/AT:I/O Trap Detected (to external NMI cache) PS/2:ADL* No Connect
18	VASPACE*	I			Valid Address Space (drive low for A[23:20]=0)PS/2:MAD also required
2	WPLT*	O			Write Strobe for External Color Palette
4	XRDN*	I/O	TSTO	I	Enable for External Devices (low at reset puts chip into test mode) or ROM Chip Select (when enabled)
					Processor Data
68-61	D[15:8]	I/O			Bi-directional Data to/from System Bus (MSB)
59-52	D[7:0]	I/O			Bi-directional Data to/from System Bus (LSB)
					Display Memory Data
99-92	M0D[7:0]	I/O			Bi-directional Data Bus to Display Memory Plane 0
109-102	M1D[7:0]	I/O			Bi-directional Data Bus to Display Memory Plane 1
119-112	M2D[7:0]	I/O			Bi-directional Data Bus to Display Memory Plane 2
139-132	M3D[7:0]	I/O			Bi-directional Data Bus to Display Memory Plane 3

Chip Pinout Summary

Pin #	Pin Name	Type	Alt.	Type	Function
					Display Memory Address
149-142	AA[7:0]	O			Address Bus to Display Memory Planes 0 and 1
159-152	AB[7:0]	O			Address Bus to Display Memory Planes 2 and 3
128-125	CAS*[3:0]	O			Display Memory Column Address Strobe Planes 3-0
6	DTOE01*	O	DTOE*	O	Display Memory Data Transfer/Output Enable Planes 0-1 (banked DTOE)
7	DTOE23*	O	SOE2*	O	Display Memory Data Transfer/Output Enable Planes 2-3 (banked SOE2)
87	RAS01*	O	RAS0*	O	Display Memory Row Address Strobe Planes 0 and 1 (banked mode Ras0)
88	RAS2*	O	RAS1*	O	Display Memory Row Address Strobe Plane 2 (banked mode Ras1)
89	RAS3*	O	RAS2*	O	Display Memory Row Address Strobe Plane 3 (banked mode Ras2)
129	SOE01*	O	SOE0*	O	Display Memory Serial Output Enable Planes 0 and 1 (banked mode SOE0)
131	SOE23*	O	SOE1*	O	Serial Output Enable to Upper 512K of memory (128k x 8 VRAMs)
79	XRAD	O	RAS3*	O	1M RAM mode: A8 all planes; Banked mode: RAS 3
					Display Memory Control
84	SCLK01	O	SCLK	O	Display Memory Serial Clock Planes 0 and 1 (banked SCLK)
85	SOE23*	O		O	Serial Output Enable to Upper 512k of Memory (128kx8 VRAMs).
5	WE*	O			Display Memory Write Enable (8mA)
69	XRESM	I	B256*/ URAS*	TS	Clock Input 3 if Enabled; If not L=Banked Memory Mode or URAS* (RAS to upper 512k if using 128kx8's)
					Clocks
19	RDACA0	O	SYS	I	High during reset = PC/AT, L=PS/2) (Internal 100k PU)
9	DCLK	O			Video Dot Clock to External Color Palette
29	FCLK	I			Feature Connector Dot Clock (clock input 2 and 6)
12	SW	I			Switch Input (Feature Read 4) (typically from RGB Output Comparator)
1	X25M	I			Clock Input 0 - 25.175MHz
11	X28M	I			Clock Input 1 - 28.322MHz
91	XD0M	I	SEL0	TS	Clock Input 4 - 50.350MHz (clock/switch select output 0)
140	XD1M	I	SEL1	TS	Clock Input 5 - 65.000MHz (clock/switch select output 1)
151	XD2M	I	SEL2	TS	Clock Input 7 - 40.000MHz (clock/switch select output 2)
					Video Interface
35	BLANK*	O			Video Blanking to External Color Palette
34	HSYNC	O			Horizontal Sync
28-21	V[7:0]	O			Video Output to External Color Palette
33	VSYNC	O			Vertical Sync
10,40,50,80,90,120,130,160					VCC
20,30,60,70,101,110,141,150					GND

Pin Symbol	Pin Number	Pin Type	Pull Up/Dn*	Description
A[0:19]	78-71, 48-41, 39-36	I		Address Bus: System address bus for memory and I/O operations. Address latches are provided in the HT209 chip for PS/2 mode, so unlatched addresses must be provided (LA19 may be connected to A19, LA18 to A18, and LA17 to A17). In PC/AT mode, A[0:19] are connected to the latched address lines provided by the PC/AT bios and LA[17:19] are connected to unlatched address lines provided by the PC/AT bus.
AA[0:7]	142-149	O		Address bus A:Display Memory Address Bus A - Address bus for planes 0 and 1
AB[0:7]	152-159	O		Address bus B:Display Memory Address Bus B - Address bus for planes 2 and 3
BLANK*	35	O		Blanking Video - a low on this pin indicates that video data is blanked (the screen is black). This pin is normally connected to the blanking input of the external color palette.
CAS*[0:3]	125-128	O		Column Address Strobe[0:3]:In all modes, these pins are Column Address Strobes. The falling edge of CAS latches column addresses from the AA and AB address buses into the RAM chips.
D[0:15]	52-59, 61-68	I/O		Data bus: From CPU[0:7] LSB, [8:15] MSB, Bidirectional bus for I/O and memory data.
DCLK	9	O		Dot CLocK: this signal is used to shift video data. All video data timing is referenced to this signal. This pin is normally connected to the clock input of the external color palette.
DENH*	100	O		Data ENable High: Data bus transceiver enable for D[15:8].Also used as output enable high for BIOS ROMs.
DENL*	111	O		Data ENable Low - Data bus transceiver enable for D[7:0].Also used as output enable low for BIOS ROMs.

Pin Descriptions

Pin Symbol	Pin Number	Pin Type	Pull Up/Dn*	Description
DIR_RD/TST0	16	O		DIRection: This pin controls the direction of data transfers on the data bus. It is driven high when an I/O or memory read cycle is being performed by the system processor. This signal may also be used for slot-8 control in PC/XT systems if connected to an inverting open collector driver whose output drives PC bus pin AA7. In chip test mode (see XRDN*/TEST pin), this pin is the test output.
DISABLE	14	I		DISABLE: this pin may be driven high to disable all memory and I/O operations to the chip. In a display adapter configuration this pin is normally driven from register bit-3 of I/O port 46E8 (inverted). This emulates the function of PS/2 Model 50 and 60 I/O port 3C3 bit 0 (Video Subsystem Enable).
DTOE01*/ DTOE*	6	O		Data Transfer Output Enable for planes 0 and 1 in non-banked mode. Data Transfer Output Enable for all planes in banked mode.
DTOE23*/ SOE2*	7	O		Data Transfer Output Enable for planes 2 & 3 in non-banked mode. Serial Output Enable for plane 2 in banked mode.
FCLK	29	I		Feature CLocK: (Clock input 2 and 6) - Connect to feature connector clock input pin if available, otherwise connect to ground or other clock source as desired.
HSYNC	34	O		Horizontal SYNC: The polarity of this signal is controlled by bit-6 of the Miscellaneous output register (I/O address 3C2h).
INT/INT*	49	TS		INTerrupt: CPU interrupt - in a PC/AT this pin is active high; in a PS/2 it is active low. The interrupt will occur at the start of the vertical retrace interval if enabled by clearing Vertical Retrace End Register (CR11) bit-5 and setting bit-4. This signal will then stay active until reset by clearing CR11 bit-4. (Bit-4 must then be set to enable the next vertical retrace interrupt). This pin is either driven low or not driven at all: PC/AT: interrupt disabled - output floats interrupt enabled & interrupting - output floats interrupt enabled & not interrupting - output driven low

Pin Symbol	Pin Number	Pin Type	Pull Up/Dn*	Description
				PS/2 interrupt disabled - output floats interrupt enabled & interrupting - output driven low interrupt enabled & not interrupting - output floats This pin has 8 mA source and sink capability and can be connected directly to the system bus.
IO16*/CFBK*	32	O		Input/Output 16-bit select: In a PC/AT this pin is asserted to indicate that the current I/O operation is transferring 16 bits. Card Select FeedBacK: In a PS/2 this pin is connected to CDSFDBK* and is asserted by the chip for any I/O or memory access to the graphics card. The PC/AT bus requires 24mA drive on its IOCS16* signal, so this pin is used to enable an external bus driver.
IORD*/CMD*	124	I		I/O ReaD: In a PC/AT this pin indicates that an I/O read operation is in progress. In a PS/2 this pin is the CoMmanD strobe input.
IOWR*/MIO*	123	I		I/O WRite: In a PC/AT this pin indicates that an I/O write operation is in progress. In a PS/2 this pin is the Memory I/O select input.
LA[17:19]	83-81	I		UnLatched Address bus for memory and I/O operations (PC/AT)
M0D[0:7]	92-99	I/O	*	Memory Display data bus 0: Bidirectional data for plane 0

*Note: This is a list of PU's on the display memory data lines to ensure that the chip is reset properly to AT mode.

RDB7=BKPGC Block PGC address decode in ROM decode space (if internal ROM decode is enabled) i.e., limit ROM decode to 0xC0000 - 0xC5FFF and 0xC6800-0xC7FFF (2K hole at 0XC6000)

RDB6=EIROM Enable internal ROM decode

RDB[5,4]=MEMCFG[1,0] (Memory configuration bits, as follows:

RDB5	RDB4	Memory Configuration
0	0	64K x 4
0	1	128K x 8
1	0	256K X 4
1	1	64K X 16

RDB3=I46E8 46E8 decoded internally, with the SETUP and DISABLE register bits internal to the HT209. Note that in this mode, the external DISABLE pin still functions, but the SETUP pin becomes an output, indicating the status of the internal flag.

RDB2=LCK16 (Write protect 16 bit mode bits SRFF0, SRFF1, SRFF3, and SRC8:4)

RDB1=RDOB (RAMDAC on odd data bus)

RDB0=T16BI (Force bits SRFF0, SRFF1, SRFF2, to a true state on reset. Also force SRC8:4 if RDB1-1)

Pin Descriptions

Pin Symbol	Pin Number	Pin Type	Pull Up/Dn*	Description
M1D[0:7]	102-109	I/O		Memory Display data bus 1: Bidirectional data for plane 1.
M2D[0:7]	112-119	I/O		Memory Display data bus 2: Bidirectional data for plane 2.
M3D[0:7]	132-139	I/O		Memory Display data bus 3: Bidirectional data for plane 3.
MEMCS16*/ CDDS16*	31	O		MEMory select 16: in a PC/AT this pin is asserted to indicate that the current memory operation is transferring 16 bits. Card Data 16:in a PS/2 this pin is connected to CDDS16* (card data select 16) and indicates that the current memory I/O operation is transferring 16 bits. The PC/AT bus requires 24mA drive on its MEMCS16* signal, so this pin is used to enable an external bus driver.
MEMR*/S0*	121	I		MEMory Read: In a PC/AT this pin indicates that a memory read operation is in progress. In a PS/2 this pin is the S0* input.
MEMW*/S1*	122	I		MEMory Write: In a PC/AT this pin indicates that memory write operation is in progress. In a PS/2, this pin is the S1* input.
RAS01*/RAS0*	87	O		Row Address Strobe for Banks 0 and 1 in non-banked mode. Row Address Strobe for bank 0 in banked mode.
RAS2*/RAS1*	88	O		Row Address Strobe for bank 2 in non-banked mode. Row Address Strobe for bank 1 in banked mode.
RAS3*/RAS2*	89	O		Row Address Strobe for bank 3 in non-banked mode. Row Address Strobe for bank 2 in banked mode.
RDACA0/SYS	19	I/O		RAMDACA0-Output/SYStem Input: This pin is sampled by the chip at the end of reset to determine the system type. High indicates PC/AT and low indicates PS/2. This determines the function of many of the system interface signal pins. At all other times, this pin is theRAMDAC A0 Input. This pin is internally pulled up with 100K ohms so may be left unconnected in PC/AT systems; it should be connected to ground through a 10K ohm resistor in PS/2 systems.

Pin Symbol	Pin Number	Pin Type	Pull Up/Dn*	Description
RDY	51	TS		ReaDY: This pin is used to synchronize display memory read/write operations. This signal is in a high impedance state until a display memory read or write operation is initiated, then it is driven low. When the operation is completed, it is driven high until the strobe goes away, then released. If fast-write mode is selected, this pin is not driven for memory write operations. This pin has 8mA source and sink capability and can be connected directly to the system bus.
RESET	8	I		RESET: Chip hardware asynchronous reset.
RFSH*	17	I		ReFreSH: indicates that the current memory operation is a system RAM refresh operation and should be ignored.
RPLT*	3	O		Read PaLeTte external color strobe: active for I/O read operations to ports 3C6, 3C8 and 3C9.
SBHE*	86	I		System Byte High Enable
SCLK01/SCLK	84	O		Serial CLocK for banks 0 and 1 in non-banked mode. Serial CLocK for all banks 128K x 8 VRAM mode - SCLK to all memory.
SETUP*/CACHE*	15	I		SETUP: pin is driven low to place the chip in "setup" mode. In setup mode, the chip only responds to I/O port 102; if not in setup mode, the chip does not respond to I/O port 102. If Internal 46E8 decode is used, this pin is an output and indicates that the FastWrite cache is empty and therefore the current write cycle can be 0WS. Refer to the PS/2 Model 50/60 Technical Reference Manual page 2-24 for further explanation of the setup mechanism.
SOE01*/ SOE0*	129	O		Serial Output Enable planes 0 and 1 in non-banked mode. Serial Output Enable plane 0 in banked mode.
SOE23*/ SOE3*	131	O		Serial Output Enable - non banked mode to planes 2 and 3, banked mode to bank 3.
SW	12	I		SWitch: the state of this pin may be read in Feature Read Register bit-4 (I/O Address 3C2). This pin is typically connected to the RGB output comparator.

Pin Descriptions

Pin Symbol	Pin Number	Pin Type	Pull Up/Dn*	Description
TRAP*/ADL*	13	I/O		TRAP:pin can be used for software trapping on any I/O accesses and can also be used for NMI based emulation in PC mode. In microchannel mode this is a no connect pin. The TRAP*/ADL* is downward compatible with previous designs and can be left connected to the ADL*.
V[0:7]	21-28	O		Video output bus: these pins are the 8 bits of video data out and are typically connected to the video data inputs of the external color palette.
VASPACE*	18	I		Valid Address SPACE: must be asserted to indicate that the current address is in the proper range (determined by decode of the upper address bits). In a PC/AT this is typically when A23 through A20 are low. In a PS/2 this must also be qualified with the memory address valid signal (MADE24 in the IBM PS/2 documentation). This is a chip select for memory operations. Functionality in AT mode is determined by extended register Bit for 1M linear decode Mode 1: Normal, VASPACE* used only to qualify MEMCS16* Mode2:1M linear decode qualifies all memory reads and writes (i.e. chip select)
VSYNC	33	O		Vertical SYNC: The polarity of this signal is controlled by bit-7 of the Miscellaneous output register (I/O address 3C2).
WE*	5	O		Write Enable: In all modes, this pin is write enable for display memory planes 0-3. When low, display memory writes are enabled to occur on the falling edge of CAS* to the plane(s) selected by the RAS* signals.
WPLT*	2	O		Write PaLeTte: write strobe for external color palette. Active for I/O write operations to ports 3C6-3C9.

Pin Symbol	Pin Number	Pin Type	Pull Up/Dn*	
X25M	1	I		Clock Input 0 - Connect to 25.175MHz or external clock generator output if used (see description of XD0-2M signals for selection of the clock frequency generated for input on this pin). Summary of clock connections for use with Video Seven standard VGA BIOS: Clk / Pin / F/W & VRAM VGA 0 / X25M / 25.175MHz 1 / X28M / 28.322MHz 2 / FCLK / Feature Connector Clock 3 / XRESM / External Clock or 0MHz 4 / XD0M / 50.350MHz 5 / XD1M / 65.000MHz 6 / FCLK / Feature Connector Clock 7 / XD2M / 40.000MHz
X28M	11	I		Clock input 1 - Connect to 28.322MHz.
XD0M/SEL0	91	I/O		Clock input 4 if "Extended Clock Direction"(Index F8) bit = 0, otherwise this pin is external clock SELect output bit-0 (for connection to an external clock generator).
XD1M/SEL1	140	I/O		Clock input 5 if "Extended Clock Direction" (Index F8) bit = 0, otherwise this pin is external clock SELect output bit-1 (for connection to an external clock generator).
XD2M/SEL2	151	I/O		Clock input 7 if "Extended Clock Direction" (Index F8) bit = 0, otherwise this pin is external clock SELect output bit-2 (for connection to an external clock generator).
XRAD/RAS3*	79	O		EXtRa ADdress/Row Address Strobe 3 - In non-banked 256K mode this pin is unused. In banked 256K mode it is RAS for bank 3 if SRC8.7=0. It is RAS for bank 1 for SRC8.7=1. In 1M mode it is display memory address A8 to all planes.

Pin Descriptions

Pin Symbol	Pin Number	Pin Type	Pull Up/Dn*	Description
XRDN*/TEST	4	I		External Device Enable: normally, the chip only enables the data bus drivers (via DENH* and DENL*) for on-chip I/O registers (and external palette) at 3Bx, 3Cx, and 3Dx plus memory addresses in the currently selected RAM address range. This signal may be asserted to enable the data bus for other external devices (such as the BIOS ROM). If this pin is low when reset goes away, the chip will go into test mode (for parametric chip test at the factory).Can also be ROM chip select output (if enabled) at C000.
XRESM/ B256*/ URAS*	69	I/O		Clock Input 3 if enabled by the "Extended Clock Control"(Index F8) register. If not enabled, clock source 3 is grounded (0MHz is selected) and this pin becomes an output for control of display memory bank selection. If low, banked mode is selected; if high non-banked mode is selected. This pin is an input on power up. In 128 x 8 VRAM mode - RAS to upper 512K of VRAM.
XSOE1*	85	O		Serial Output Enable to upper 512K VRAM with 128Kx8s.

Port Address	VGA Port
3B0	
3B1	
3B2	
3B3	
3B4	CRTC Index (RW)
3B5	CRTC Data (RW)
3B6	
3B7	
3B8	
3B9	
3BA	Feature Control (W), Input Status 1 (R)
3BB	
3BC	
3BD	
3BE	
3BF	
3C0	Attribute Controller Index/Data (W), Index (R)
3C1	Attribute Controller Data (R)
3C2	Miscellaneous Output (W), Input Status 0 (R)
3C3	Video Subsystem Enable (RW)
3C4	Sequencer/Extensions Index (RW)
3C5	Sequencer/Extensions Data (RW)
3C6	Palette Pixel Mask (RW) (IMSG176 register)
3C7	Palette Address Register Read Mode (W) (IMSG176 register) Dac State (R)
3C8	Palette Address Register Write Mode (RW) (IMSG176 register)
3C9	Palette Data (RW) (IMSG176 register)
3CA	Feature Control (R)
3CG	
3CC	Miscellaneous Output (R)
3CD	
3CE	Graphics Controller Index (RW)
3CF	Graphics Controller Data (RW)
3D0	
3D1	
3D2	
3D3	
3D4	CRTC Index (RW)
3D5	CRTC Data (RW)
3D6	
3D7	
3D8	
3D9	
3DA	Feature Control (W), Input Status 1 R)
3DB	
3DC	
3DD	
3DE	
3DF	

VGA Register Summary

General Registers

DESC.	REGISTER NAME	BITS	READ/WRITE	INDEX	PORTS MONO	PORTS COLOR
MISC	Miscellaneous Output	7	R/W	--	3C2(W),3CC(R)	3C2(W),3CC(R
FC	Feature Control	3	R/W	--	3BA(W),3CA(R)	3DA(W),3CA(I
FEAT	Feature Read (Input Status 0)	4	R	--	3C2	3C2
STAT	Display Status (Input Status 1)	7	R	--	3BA	3DA
DACMASK	Palette Pixel Mask	8	R/W	--	3C6	3C6
DACSTATE	Palette State	2	R	--	3C7	3C7
DACRX	Color Palette Read Mode Index	8	W	--	3C7	3C7
DACWX	Color Palette Write Mode Index	8	R/W	--	3C8	3C8
DACDATA	Color Palette Data	6	R/W	--	3C9	3C9
ALTVSE	Alternate Video Subsystem Enable	1	R/W	--	3C3	3C3
STUP	Setup	1	R/W	--	Port 102	Port 102
ALT16	Alternate 16-bit Set Up Mode	5	R/W	--	Port 104	Port 104
PRC	Power On Reset Configuration	6	R/W	--	Port 106	Port 106
ROMMAP	ROM Mapping and Video Subsystem Control	2	W	--	Port 46E8	Port 46E8

Sequencer Index Registers

					MONO	COLOR
SRX	Sequencer/Extensions Index	8	R/W	--	3C4	3C4
SR0	Reset	2	R/W	00	3C5	3C5
SR1	Clocking Mode	5	R/W	01	3C5	3C5
SR2	Plane Mask	4	R/W	02	3C5	3C5
SR3	Character Map Select	6	R/W	03	3C5	3C5
SR4	Memory Mode	3	R/W	04	3C5	3C5
SR5	Reserved	0	R/W	05	3C5	3C5
SR6	Extension Control Register	1	R/W	06	3C5	3C5
SR7	Reset Horizontal Character Counter	0	W	07	3C5	3C5

Graphics Control Registers

					PORTS	
GRX	Graphics Controller Index Register	4	R/W	--	3CE	3CE
GR0	Set/Reset	4	R/W	00	3CF	3CF
GR1	Enable Set/Reset	4	R/W	01	3CF	3CF
GR2	Color Compare	4	R/W	02	3CF	3CF
GR3	Data Rotate	5	R/W	03	3CF	3CF
GR4	Read Map Select	2	R/W	04	3CF	3CF
GR5	Mode	6	R/W	05	3CF	3CF
GR6	Miscellaneous	4	R/W	06	3CF	3CF
GR7	Color Don't Care	4	R/W	07	3CF	3CF
GR8	Bit Mask	8	R/W	08	3CF	3CF

Attribute Controller Registers

ABBREV	REGISTER NAME	BITS	READ/WRITE	INDEX	PORTS	
ARX	Attribute Controller Index	6	R/W	--/83	3C0	3C5
AR0-F	Palette Regs [0:15]	8	R/W	00-0F	3C0(W)	3C1(R)
AR10	Mode Control	7	R/W	10	3C0(W)	3C1(R)
AR11	Overscan Color	8	R/W	11	3C0(W)	3C1(R)
AR12	Color Plane Enable	6	R/W	12	3C0(W)	3C1(R)
AR13	Horizontal Pixel Panning	4	R/W	13	3C0(W)	3C1(R)
AR14	Color Select	4	R/W	14	3C0(W)	3C1(R)

CRT Controller Registers

ABBREV	REGISTER NAME	BITS	READ/WRITE	INDEX	MONO	COLOR
CRX	CRTC Index	6	R/W	--	3B4	3D4
CR0	Horizontal Total	8	R/W	00	3B5	3D5
CR1	Horizontal Disply Enable End	8	R/W	01	3B5	3D5
CR2	Horizontal Blanking Start	8	R/W	02	3B5	3D5
CR3	Horizontal Blanking End	8	R/W	03	3B5	3D5
CR4	Horizontal Retrace Start	8	R/W	04	3B5	3D5
CR5	Horizontal Retrace End	8	R/W	05	3B5	3D5
CR6	Vertical Total	8	R/W	06	3B5	3D5
CR7	Overflow	8	R/W	07	3B5	3D5
CR8	Preset Row Scan	7	R/W	08	3B5	3D5
CR9	Character Cell Height	8	R/W	09	3B5	3D5
CRA	Cursor Start	6	R/W	0A	3B5	3D5
CRB	Cursor End	7	R/W	0B	3B5	3D5
CRC	Start Address High	8	R/W	0C	3B5	3D5
CRD	Start Address Low	8	R/W	0D	3B5	3D5
CRE	Cursor Location High	8	R/W	0E	3B5	3D5
CRF	Cursor Location Low	8	R/W	0F	3B5	3D5
CR10	Vertical Retrace Start	8	W/RW	10	3B5	3D5
CR11	Vertical Retrace End	8	W/RW	11	3B5	3D5
CR12	Vertical Display Enable End	8	R/W	12	3B5	3D5
CR13	Offset	8	R/W	13	3B5	3D5
CR14	Underline Row Scan	7	R/W	14	3B5	3D5
CR15	Vertical Blanking Start	8	R/W	15	3B5	3D5
CR16	Vertical Blanking End	8	R/W	16	3B5	3D5
CR17	CRTC Mode Control	7	R/W	17	3B5	3D5
CR18	Line Compare	8	R/W	18	3B5	3D5
CR1F	Identification Register	8	R	1F	3B5	3D5
CR22	Graphics Controller Data Latch	8	R	22	3B5	3D5
CR24	Attribute Controller Index/ Data Latch	7	R	24	3B5	3D5
CR3x	Clear Vertical Display Enable Flip Flop	1	W	3x	3B5	3D5

VGA Register Summary

EXTENSION REGISTER SUMMARY

REG. #	DES	REGISTER NAME	BITS	R/W	INDEX	PORT
ER80-ER82		Reserved	0	-	80-82	3C5
ER83	ARX	*Attribute Controller Index	7	R/W	83	3C5
ER84-ER89		Reserved	0	-	84-89	3C5
ER8A-ER8D		Reserved	0	-	8A-8D	3C5
ER8E	REV	ChipRevision Register	8	R	8E	3C5
ER8F	REV	Chip Family Register	8	R	8F	3C5
ER90-ER93		Reserved	0	-	90-93	3C5
ER94	PPA	Pointer Pattern Address	8	R/W	94	3C5
ER95-ER99		Reserved	0	-	95-99	3C5
ER9A-ER9B		Reserved	0	-	9A-9B	3C5
ER9C	PXH	Pointer Horizontal Position High	3	R/W	9C	3C5
ER9D	PXL	Pointer Horizontal Position Low	8	R/W	9D	3C5
ER9E	PYH	Pointer Vertical Position High	2	R/W	9E	3C5
ER9F	PYL	Pointer Vertical Position Low	8	R/W	9F	3C5
ERA0	GRL0	Graphics Controller Memory Latch 0	8	R/W	A0	3C5
ERA1	GRL1	Graphics Controller Memory Latch 1	8	R/W	A1	3C5
ERA2	GRL2	Graphics Controller Memory Latch 2	8	R/W	A2	3C5
ERA3	GRL3	Graphics Controller Memory Latch 3	8	R/W	A3	3C5
ERA4	CLK	Extended Clock Select	3	R/W	A4	3C5
ERA5	CURS	Cursor Attributes	3	R/W	A5	3C5
ERB3	SCRAM	Scratch RAM Register	8	R/W	B3	3C5
ERC0	MNLCK	Monochrome Lock	8	R/W	C0	3C5
ERC8	MSCRTRLII	Miscellaneous Control II	4	R/W	C8	3C5
ERC9		Reserved	--	R/W	C9	3C5
ERCA	HOFL	Horizontal Overflow	5	R/W	CA	3C5
ERE0	MSCTRLI	Miscellaneous Control I	8	R/W	E0	3C5
ERE1	INTLC	Interlace Value	8	R/W	E1	3C5
ERE2	TRAPCTL	Trap Control Register	5	R/W	E2	3C5
ERE3	WRTPRTC	Write Protect Control	6	R/W	E3	3C5
ERE8	LWRSPLT	Lower Split Bank	8	R/W	E8	3C5
ERE9	UPRSPLT	Upper Split Bank	8	R/W	E9	3C5
EREA	SWSTB	Switch Strobe**	--	W	EA	3C5
EREB	OVRLN	Overline Control	5	R/W	EB	3C5
EREC	FGLAT0	Foreground Latch 0	8	R/W	EC	3C5
ERED	FGLAT1	Foreground Latch 1	8	R/W	ED	3C5
EREE	FGLAT2	Foreground Latch 2	8	R/W	EE	3C5
EREF	FGLAT3	Foreground Latch 3	8	R/W	EF	3C5
ERF3	MWCTRL	Masked Write Control	3	R/W	F3	3C5
ERF4	MWMASK	Masked Write Mask	8	R/W	F4	3C5
ERF5	FBPAT	Foreground/Background Pattern	8	R/W	F5	3C5
ERF6	RAMBANK	MB DRAM Bank	8	R/W	F6	3C5
ERF7	SWITCH	Switch Readback Register	8	R/W	F7	3C5

VGA Register Summary

REG. #	DES	REGISTER NAME	BITS	R/W	INDEX	PORT
ERF8	CLKCTRL	Extended Clock Control	8	R/W	F8	3C5
ERF9	PGSEL	Extended Page Select	1	R/W	F9	3C5
ERFA	FGCOLOR	Extended Foreground Color	4	R/W	FA	3C5
ERFB	BGColor	Extended Background Color	4	R/W	FB	3C5
ERFC	COMPAT	Compatibility Control	8	R/W	FC	3C5
ERFD	TIMING	Extended Timing Select	8	R/W	FD	3C5
ERFE	FBCTRL	Foreground/Background Control	7	R/W	FE	3C5
ERFF	16BIT	16-Bit Interface Control	8	R,R/W	FF	3C5

*Duplicated VGA registers also accessible as extension registers for state save/restore

** A byte-sized I/O write decode only; no bits of this register exist. Byte writes to this register cause the switch settings on CPU data bus bits 15-8 to be strobed into the Switch Readback register (ERF7).

NOTE: Registers ER80 - ERFF are only accessible when extensions are enabled, see SR6.

General Registers

There are twelve General registers. Each register contains a separate port address to allow direct programming access.

Desc.	Register Name	Bits	Access	Index	Ports	
MISC	Miscellaneous Output Register	7	R/W	--	3C2(W)	3CC(R)
FC	Feature Control	3	R/W	--	3BA/3DA(W)	3CA(R)
FEAT	Feature Read (Input Status 0)	4	R		3C2	3C2
STAT	Display Status (Input Status 1)	6	R		3BA	3DA
DACMASK	Palette Pixel Mask	8	R/W		3C6	3C6
DACSTATE	Palette State	2	R		3C7	3C7
DACRX	Color Palette Read Mode Index	8	W		3C7	3C7
DACWX	Color Palette Write Mode Index	8	R/W		3C8	3C8
VSE	Video Subsystem Enable	1	R/W		3C3	3C3
ALT16	Alternate 16-bit Set Up Mode	6	R/W		Port 104	Port 104
PRC	Power On Reset Configuration	6	R/W		Port 106	Port 106
ROMMAP	ROM Mapping and Video Subsystem Control	2	W		Port 46E8	Port 46E8

MISC Miscellaneous Output Register 3CC(R) 3C2(W)

Bit	Description
7	Vertical Retrace Polarity
6	Horizontal Retrace Polarity
5	Page Select
4	Reserved
3	Clock Select
2	Clock Select
1	Enable RAM
0	CRTC I/O Address

The functions in this register include setting the polarity of horizontal and vertical retrace signals and the video clock source. This register can be read back at I/O address 3CCh in the HT209.

Bit 7 Vertical Retrace Polarity
0 = Selects active high
1 = Selects active low

Bit 6 Horizontal Retrace Polarity
0 = Selects active high
1 = Selects active low

Bit 5 Page Select
0 = Selects odd memory locations
1 = Selects even memory locations

This bit is the LSB of the display memory address when in 'Odd/Even' modes SR4 bit 2 = 1). It is set for modes 0, 1, 2, 3, and 7 (text modes). This bit has no effect if Chain (GR6 bit 1 or Chain 4 (SR4 bit 3) are enabled.

Bit 4 Reserved (reads back 0)

Bits[3:2] Clock Select

If Extension Register F8 bit 1 = 0 , then use the following table:

Clock Select Source Settings

Bit-3	Bit-2	Extension Reg. A4 bit 4 = 0	Extension Reg. A4 bit 4 = 1
0	0	25.175MHz (X25M pin)	50.350MHz (XD0M pin)
0	1	28.322MHz (X28M pin)	65.000MHz (XD1M)
1	0	Feature Connector Input (FCLK pin)	Feature Connector Input (FCLK pin)
1	1	0MHz (XRESM_ pin)_	40.000 MHz (XD2M pin)

If Extension Register F8 bit 1 = 1, then XD0M, XD1M and XD2M are outputs that drive selects on a programmable clock chip. The XD0M, XD1M and XD2M pins are driven by port 3C2 bit 2, 3C2 bit 3, and Extension register A4 bit 4 respectively. The clock chip output drives the selected frequency into the X25M input. The clock chip must drive the input with a 25.175MHz clock during power-up for the HT209 to be properly initialized.

Note: All Clock Select bits (3C2 bit[3:2], Extension Register A4 bit 4, and Extension Register F8 bit 1) should only be changed during synchronous reset (SR0 bit 1 = 0) or display memory contents may be corrupted.

Bit 1 — Enable RAM
0 = Disables processor access to Display RAM
1 = Display RAM responds at addresses set by the value programmed into the Control Data Select of the Graphics Controller.

Bit 0 — CRTC I/O Address
0 = Sets the CRTC to 3Bxh and the Input Status Register 1 to 3BAh for monochrome mode.
1 = Sets the CRTC to 3Dxh and the Input Status Register 1 to 3DAh for color mode.

This bit selects I/O addresses for monochrome (3Bx) or color mode (3Dx). The following registers are affected by this bit: the Display Status Register, the Feature Control Register, the CRT Controller Index Register, and the CRT Controller Data Register.

FC Feature Control Register 3BA/3DA (W) 3CA(R)

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	VSync Select
2	Reserved
1	Feature Control
0	Feature Control

This register is write only . Writing I/O port 3BA/3DA returns the contents of the Display Status Register. For state save/restore and VGA compatibility, this register can be read at I/O port 3CA.

Bit 3 — Vertical Sync Select
0 = Enables normal vertical sync output to the monitor. This bit should always be set to 0.
1 = Output is the logical OR of vertical sync and vertical display enable.

Bits[1:0] — Feature Control
These bits drive the Feature Control 1 and Feature Control 0 pins of the Feature connector.

FEAT Feature Read Register(Input Status 0) 3C2(R)

Bit	Description
7	Vertical Interrupt
6	Feature Code
5	Feature Code
4	Switch Sense
3	Reserved
2	Reserved
1	Reserved
0	Reserved

This register is read only. It reads two pin locations on the Feature Connector plus Switch Sense and Vertical Interrupt.

Bit 7 — Vertical Interrupt
0 = No interrupt is pending
1 = An interrupt is pending
Note: When set to 0, CR11 bit 5 enables CRT interrupts to occur at the leading edge of vertical sync. The interrupt is normally connected to IRQ2 in a PC/AT.

Bit[6:5] — Feature Code
These bits are input from the feature connector as feature code. These bit normally read back as 1 if nothing is connected to the feature connector.

Bit 4 Switch Sense
This bit returns the state of the SWITCH pin. The SWITCH pin is connected to the output of the LM339 monitor ID comparator.

STAT Display Status Register(Input Status 1) 3BA/3DA (R)

Bit	Description
7	Not Vertical Retrace
6	Reserved
5	Diagnostic Use Bit
4	Diagnostic Use Bit
3	Vertical Retrace
2	Fake Light Pen Switch(1)
1	Fake Light Pen Flip-Flop(0)
0	Display Disabled

This register is read only at 3BA/3DA and sets the Attribute Controller index/data toggle to index state.

Bit 7 Not Vertical Retrace
0 = Vertical Retrace is active
1 = Vertical Retrace is inactive

Bits[5:4] Diagnostic
These bits are connected to 2 of the 8 outputs of the Attribute Controller (V7:0] video output data during display periods and overscan color during non-display periods). Selection of one of the four pairs of bits is controlled by bits[5:4] of Color Plane register AR12.

Input Status Diagnostic Use Settings

Color Plane Register		Display Status	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	Video 2	Video 0
0	1	Video 5	Video 4
1	0	Video 3	Video 1
1	1	Video 7	Video 6

Bit 2 'Fake' Light Pen Switch
This bit always reads as 1 since the light pen is not implemented in the HT209.

Bit 1 'Fake' Light Pen Flip-Flop
This bit always reads as 0 since the light pen is not implemented in the HT209.

Bit 0 Display Disabled
0 = Display of video data is enabled
1 = Vertical or horizontal retrace interval is in progress

DACMASK Palette Pixel Mask Register 3C6 (R/W)

Bit	Description
7	Palette Pixel Mask
6	Palette Pixel Mask
5	Palette Pixel Mask
4	Palette Pixel Mask
3	Palette Pixel Mask
2	Palette Pixel Mask
1	Palette Pixel Mask
0	Palette Pixel Mask

Located in the Color Palette chip. The contents of this register are ANDed with the 8 bits of video data coming into the Color Palette to allow displayed colors to be altered without changing display memory or the contents of the Color Palette. Rapid animation, overlays, and flashing objects can be produced by partitioning color information by one or more bits in the color palette.

DACSTATE Palette State Register 3C7 (R)

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Palette State
0	Palette State

Implemented in the HT209 in contrast to the other registers in the 3C6-3C9 range which are implemented in the Color Palette chip. The Color Palette chip automatically increments the index register when the index is written at 3C7 or 3C8.

Automatic incrementing is used to save and restore the color values and eliminates the need to reload the index every three bytes. The index value is written to this register and saved in an internal register where it is automatically incremented. The save register is used to point at the current data register until the 3-byte read sequence is completed. When the blue value is read, the save register is updated and incremented again. The entire palette (or any subset) is read by writing the index of the first color in the set, then reading the values for each color.

This register used to write index to read color data values. Port 3C8 is used to write the index to write color data values. The index is read back at 3C8 only. Read accesses to this register are intercepted and substituted by the DACSTATE register contents. Certain information such as whether the chip is being read or written to, is required for saving and restoring the state of the video system during interrupt service. Data values must therefore be accessed in 3-byte sequences. When a color palette register is written, any 3-byte read or write sequence in progress is aborted and a new one is started.

Bits[1:0] Palette State
These bits are the low-order bits of the last I/O write to ports 3C6-3C9.

00 - The last I/O write was to 3C8, the color palette 'write-mode' index register
11 - The last I/O write was to 3C7, the color palette 'read-mode' index register

DACRX Color Palette "Read Mode" Index 3C7(W)

Bit	Description
7	Color Palette Index
6	Color Palette Index
5	Color Palette Index
4	Color Palette Index
3	Color Palette Index
2	Color Palette Index
1	Color Palette Index
0	Color Palette Index

Contains the index value for read access to the 256 Register in the Color Palette. These registers are 18 bits in length (6 bits each for red, green, and blue). Each register is accessed as a sequence of 3 bytes. See I/O Port 3C7 (R) for a description of how this register functions.

DACWX Color Palette "Write Mode" Index 3C8(R/W)

Bit	Description
7	Color Palette Index
6	Color Palette Index
5	Color Palette Index
4	Color Palette Index
3	Color Palette Index
2	Color Palette Index
1	Color Palette Index
0	Color Palette Index

This register contains the index value for write access to the 256 registers in the Color Palette. These registers are 18 bits in length (6 bits each for red, green, and blue). Each register is accessed as a sequence of 3 bytes.

Note: See I/O Port 3C7 (R) for a description of how this register functions.

DACDATA Color Palette Data Registers 3C9 (R/W)

Bit	Description
7	Reserved
6	Reserved
5	Color Palette 0-5 Red, Green or Blue
4	Color Palette 0-5 Red, Green or Blue
3	Color Palette 0-5 Red, Green or Blue
2	Color Palette 0-5 Red, Green or Blue
1	Color Palette 0-5 Red, Green or Blue
0	Color Palette 0-5 Red, Green or Blue

The Color Palette registers are 18 bits in length (6 bits each for red, green and blue). Each register is accessed as a sequence of 3 bytes. After writing the index to the DACRX, or DACWX register (port 3C7 or 3C8), data values are read from or written to port 3C9 in sequence: 1) red, 2) green, 3) blue. The index register is automatically incremented for each 3 byte set, allowing multiple color registers to be read from or written to eliminating the need to reload the index every three bytes.

Note: See I/O Port 3C7 (R) for a description of how this register functions.

ALTVSE Alternate Video Subsystem Enable 3C3(R/W)

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	Video Subsystem Enable

This register enables memory and I/O addressing. The HT209 must be in setup mode (SETUP* pin=1) to access this register.

Bit 0 VGA Subsystem Enable
0 = Disables memory and I/O addressing (Ports 102 & 3C3 are not disabled to allow the HT209 to be re-enabled.)
1 = Enables memory and I/O addressing

Note: In PC/AT systems where the VGA is implemented as an optional board (for installation in a slot on the bus), the SETUP* pin is driven by 46E8H bit 4. In PS/2 Systems where the VGA is implemented as a standard feature (as part of the motherboard logic), the SETUP* pin is driven by I/O port 94h bit 5. See Port 3C3 for additional information.

ALT16 Alternate 16 bit Set Up Mode Port 104 (R/W)

Bit	Description
7	Alternate (R) ERFF 16-bit Interface Control bit 7 (16-bit Status)
6	Reserved
5	Reserved
4	Alternate (R/W) ERFF Miscellaneous Control II bit 4 (word DAC)
3	Alternate (R/W) ERC8 16-bit Interface Control bit 3 (word ROM)
2	Reserved
1	Alternate (R/W) ERFF 16-bit Interface Control bit 1 (word I/O)
0	Alternate (R/W) ERFF 16-bit Interface Control bit 1 (word memory)

Provides alternate R/W locations for selected bits in two Extension registers: the 16-bit Interface Control Register and the Miscellaneous Control II Register. This register is only accessible when the HT209 is in set up mode (SETUP* pin=0) and the value of 05h has been written to the General Set Up register (102h).

PRC Power On Reset Configuration Port 106 (R/W)

Bit	Description
7	Reserved
6	Reserved
5	Memory Configuration bit 1
4	Memory Configuration bit 0
3	Internal 46E8 Decode (R)
2	Lock 16-bit Mode
1	RAMDAC Odd Data bus
0	True 16-bit Interface

This register reflects the state of the M0D[0:7] Pins 92-99 on Power On Reset. During RESET the state of M0D[0:7] is latched into this register bits [0:7].

Bit[5:4] Memory Configuration bits [0:1]
This field indicates the type of memory being accessed by the HT209

Value	Memory Configuration
00	64Kx4
01	128Kx8
10	256Kx4
11	64Kx16

Bit 3 Internal 46E8 Decode (R)
This bit indicates that the ROMMAP Register is decoded internally to the HT209.

1 = The SETUP* pin on the HT209 changes to output the state of the CPU memory access flag

Bit 2 Lock 16-bit Mode

1 = Lock Extension Register FF bit 0, bit 1 and bit 3. It also locks Register C8 bit 4, if bit 1 of this register is 1.

Bit 1 RAMDAC Odd Data bus

This bit informs the HT209 that RAMDAC is connected to the upper 8 bits of a 16-bit data bus.

1 = The HT209 provides all the necessary byte steering for 8-bit accesses in an 8-bit slot or 8/16 bit accesses in a 16-bit slot

Bit 0 True 16-bit Interface

This bit initializes the HT209 16-bit mode.

1 = If bit 1 of this register is 1 then, this bit forces ERFF bit0, ERFF bit 1, ERFF bit 3 and ERC8 bit 4 to 1.

ROMMAP ROM Mapping & Video Subsystem 46E8 (W)

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Setup Mode
3	Video Subsystem Enable
2	Reserved
1	Reserved
0	Reserved

Used to control memory mapping of the BIOS ROM,Control memory, and I/O addressing. It is implemented in PC/AT bus configurations and is not implemented in PS/2 systems. This register is set to 0Eh during initialization by the video BIOS (normal mode, video subsystem enabled, and ROM bank 6).

Note: In PS/2 systems, setup mode is controlled by I/O port 94h bit 5 and video subsystem enable/disable capability is provided by ports 3C3 and 102 only. Bit 3 in 46E8 is changed by the BIOS call to enable/disable the video subsystem.

Bit 4 Setup Mode
The complement of this bit is used to drive the HT209 SETUP* pin.

0 = Accesses to ALTVSE (port 102) are ignored.
1 = When in setup mode, setting port 102 bit 0 = 0 disables memory and I/O addressing (except for ports 102 and 3C3, which allow the HT209 to be re-enabled.)

Bit 3 Video Subsystem Enable
The complement of this bit is used to drive the HT209 DISABLE pin.

0 = All video memory and I/O port accesses with the exception of port 46E8, 100, 101, 102, 104, and 106 will be disabled. Video data continues to be displayed because memory and registers are "write protected".
1 = Enable all video memory

Sequencer Register

The eight Sequencer Registers generate all Memory timing for the display RAMs and the character clock for controlling display memory refresh reads. Timings controlled by the Sequencer registers includ horizontal count resolution, dot clock, and video load control.

Desc.	Register Name	Bits	Access	Index	Ports	
SRX	Sequencer/Extensions Index	8	R/W	--	3C4	3C4
SR0	Reset Register	2	R/W	00	3C5	3C5
SR1	Clocking Mode	5	R/W	01	3C5	3C5
SR2	Plane Mask	4	R/W	02	3C5	3C5
SR3	Character Map Select	6	R/W	03	3C5	3C5
SR4	Memory Mode	3	R/W	04	3C5	3C5
SR6	Control Register	1	R/W	06	3C5	3C5
SR7	Reset Horizontal Character	--	W	07	3C5	3C5

SRX Sequencer /Extensions Register Index 3C4(R/W)

Bit	Description
7	Sequencer Extension Index Select
6	Sequencer/Extensions Index Bit
5	Sequencer/Extensions Index Bit
4	Sequencer/Extensions Index Bit
3	Sequencer/Extensions Index Bit
2	Sequencer/Extensions Index Bit
1	Sequencer/Extensions Index Bit
0	Sequencer/Extensions Index Bit

Bit 7 Sequencer/Extensions Index Select

0 = Disables Extensions Index
Enables access to Sequencer Registers through three least significant bits of this register.
1 = Enables write access to Extension Registers.

This register points to the Sequencer and the HT209 Extension registers if enabled. If bit 7= 0, the three low-order bits determine which Sequencer register will be pointed to in the next register read/write operation. If bit 7 = 1 then the eight bits determine which Extension Register will be pointed to in the next register read/write operation.

NOTE: If a value is written to the index register that points to SR[0:7] (0-FF with Extensions disabled or 0-7F with Extensions enabled), then read back of the index register will return a value from [0:7] (forcing bits[3:7] to 0). If a value is written to the index register that points to the Extension Registers (80-FF with Extensions enabled), readback of the index register will return the value written.

SR0 Reset Register 3C5(R/W)

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Synchronous Reset 2
0	Synchronous Reset 1

This register halts all timing including CRT timing. Both Reset Register bits must be set to 1 to allow the Sequencer to operate.

Bit 1 Synchronous Reset 1
0 = The Sequencer initiates a synchronous clear and halt. Display memory, refresh, and H/V sync signals to the display are disabled.
1 = The Sequencer operates as usual.

Note:This bit may be set to 0 for short periods of time (a few tens of microseconds at most). The following registers and associated bits can be changed only when this bit is 0:

Clocking Mode Register (SR1) bits 0 and 3
Misc Output register bits[2:3]
Extensions CLK Register bit 4
Extensions 'Extended Timing Select' Register bits[0:7]

Bit 0 Synchronous Reset 2
This bit performs identically to bit 1, however, when it transitions from 1 to 0, it also resets the Character Map Register (SR3) to 0.

SR1 Clocking Mode 3C5(R/W)

Bit	Description
7	Reserved
6	Reserved
5	Screen Off
4	Shift 32
3	Dot Clock
2	Shift Load
1	Reserved
0	8-9 Dot Clocks

This register configures the timing circuits of the Sequencer. Before this register can be modified, the Sequencer must be placed in a synchronous Reset state.

Bit 5 Screen Off

0 = Normal operation.
1 = Blanks the screen and disables the picture generating logic. This bit can be used for rapid scan update; disabling allows the video process uninterrupted access to memory.

Note: The blanking mechanism does not stop Horizontal and Vertical sync, blanking, or Display Enable signals. For example, the DE bit in the Display Status Register still toggles during screen blanking.

Bit 4 Shift 32

0 = Loads the display data serializers every 1 or 2 cycles of the character clock as determines by bit 2 of this register.
1 = Loads the display data serializers every 4 cycles of the character clock.

Note: This bit is typically set for high resolution monochrome graphics modes (32 pixels per CRTC memory access). It is not used in any currently defined standard or extended VGA mode.

Bit 3 Dot Clock

0 = Selects the Sequencer Master Clock to be output on the Dot Clock output pin of the HT209 chip.
1 = Divides the Sequencer master clock by 2 to generate the Dot Clock. The Dot Clock divided by 2 is used for 320 x 200 modes with the exception of 256 color mode.

Note: The Dot Clock is the primary clock used by the system. When the Dot Clock is modified, all other timings based on the Dot Clock will change accordingly.

Bit 2 Shift Load

The value of this bit is significant only when bit 4 is set to 0. If so:

0 = Loads the display serializers every character clock.
1 = Loads the display serializers every other character clock.

This bit is typically only set for monochrome graphics modes.

Bit 0 8/9 Dot Clocks

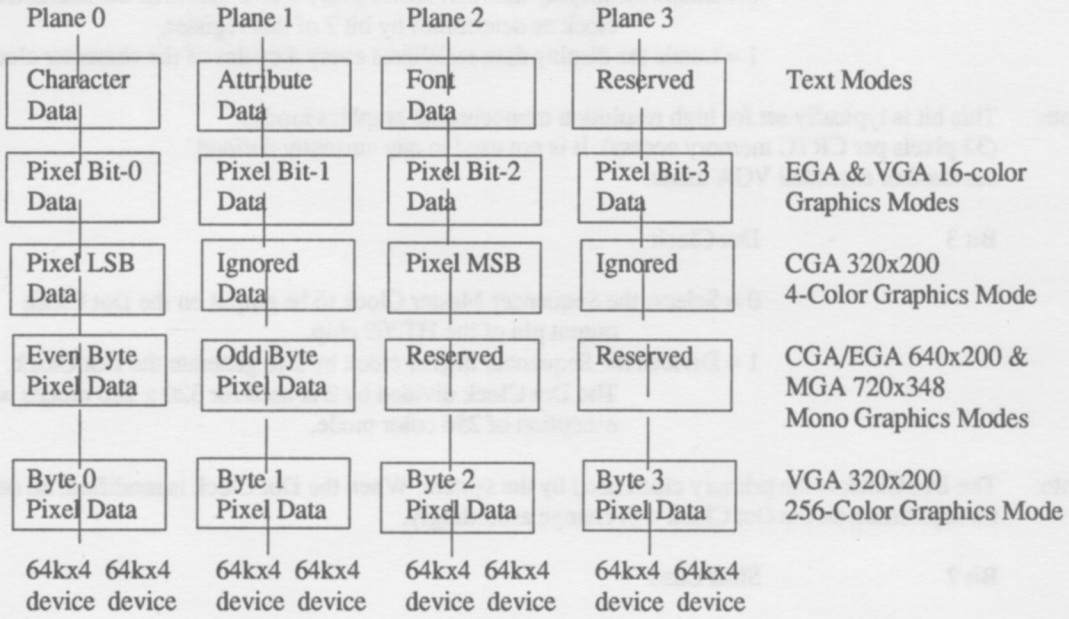
0 = The Sequencer generates 9-dot wide Character Clocks.
1 = The Sequencer generates 8-dot wide Character Clocks.

Note: Monochrome text modes (720 x 350 resolution), and VGA 400-line text modes (9 x 16 font, 40 x 25 and 80 x 25 text modes) use 9-dot character clocks; other standard modes use 8-dot character clocks.

SR2 Plane Mask 3C5(R/W)

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Enable Plane 3
2	Enable Plane 2
1	Enable Plane 1
0	Enable Plane 0

This register controls CPU write access to the four display memory planes. Any combination of planes may be enabled for writing at any time. It is important for graphics drawing operations.



In 4-bit per pixel graphics modes, set this register to 0Fh (planes [0:3] each contain 1 bit of the pixel value). In text modes, set this register to 3 (the CPU needs to access planes 0 and 1; the font information is retrieved directly by hardware, independent of the contents of this register).

Note: When odd/even modes are selected by clearing bits 2 and 3 of Memory Mode Register (SR4), planes 0/1 and planes 2/3 should have the same plane mask value.

In Odd/Even and Chain 4 modes, this register is still in effect, and is ANDed with the plane select generated by the Odd/Even circuitry. For example, in Odd/Even mode the circuitry causes planes 0 and 2 to be enabled on CPU writes to even addresses and planes 1 and 3 to be enabled on CPU writes to odd addresses. However, if the plane mask setting is 3, only plane 0 (even addresses) and plane 1 (odd addresses) can actually be written to.

SR3 Character Map Select 3C5(R/W)

Bit	Description
7	Reserved
6	Reserved
5	Secondary Character Map Select 0
4	Primary Character Map Select 0
3	Secondary Character Map Select 2
2	Secondary Character Map Select 1
1	Primary Character Map Select 2
0	Primary Character Map Select 1

This register is used with software that requires multiple character sets. It selects which RAM character sets will be displayed. In text modes, bit 3 of the attribute byte normally turns the foreground intensity on or off. This bit may be redefined to be a switch between character sets. This function is enabled when the Primary and Secondary Character Map Select bits are set to different values. Whenever the two values are the same, the character select function is disable.

Any change made to the contents of this register takes effect at the start of the next character line on the display.

Bits 3,2,5 Secondary Character Map Select
These bits select the bank used to generate text characters when the character attribute bit-3 is '1'.

SR3[3]	SR3[2]	SR3[5]	FONT #	Table Location
0	0	0	0	1st 8k of Plane 2
0	0	1	1	2nd 8k of Plane 2
0	1	0	2	3rd 8k of Plane 2
0	1	1	3	4th 8k of Plane 2
1	0	0	4	5th 8k of Plane 2
1	0	1	5	6th 8k of Plane 2
1	1	0	6	7th 8k of Plane 2
1	1	1	7	8th 8k of Plane 2

Bits 1,0,4 Primary Character Map Select
These bits select the bank used to generate text characters when the character attribute bit-3 is '0'.

SR3[1]	SR3[0]	SR3[4]	FONT #	Table Location
0	0	0	0	1st 8k of Plane 2
0	0	1	1	2nd 8k of Plane 2
0	1	0	2	3rd 8k of Plane 2
0	1	1	3	4th 8k of Plane 2
1	0	0	4	5th 8k of Plane 2
1	0	1	5	6th 8k of Plane 2
1	1	0	6	7th 8k of Plane 2
1	1	1	7	8th 8k of Plane 2

SR4 Memory Mode Register 3C5(R/W)

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Chain 4(Double Odd/Even)
2	Odd/Even
1	Extended Memory
0	Reserved

This register is initialized by the BIOS during a mode select operation and is used by the Sequencer to determine how the memory is structured for that mode. Before this register can be modified, the Sequencer must be placed in a synchronous Reset state.

Bit 3 Chain 4 (double odd/even)

This bit is used to generate display memory addresses in the implementation of 256-color modes. It affects display memory accesses from the CPU, not CRTC accesses.

0 = Enables the processor to access data sequentially in the bit map identified by the Map Mask register (SR3).
1 = A0 provides plane select bit-0 and A1 provides plane select bit-1. This bit takes priority over the Graphics Controller Read Map Register , GR5 bit-4, and bit 2 of this register (these bits are ignored).

Note: In order for writes to be accessed, the Plane Mask Register (SR2) bit for planes selected by Chain 4 must be set. The plane select generated by Chain 4 is logically ANDed with the Plane Mask Register to generate another plane select.

Chain 4 Memory Modes

A1	A2	Map
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2 Odd/Even

0 = The Sequencer is placed in the Odd/Even mode. Even CPU addresses access planes 0 and 2, and odd CPU addresses access planes 1 and 3.

1 = The CPU addresses data within a bit plane sequentially. The planes are accessed according to the value in the Plane Mask Register (SR2).

Note: Set this bit to 0 for text modes and when emulating CGA graphics modes. This bit tracks the function of the Graphics Controller Mode register (GR5) bit 4.

Bit 1 Extended Memory

0 = Allows emulation of EGA modes that assume a display memory size of 64k.
1 = Typical setting for standard VGA.

SR6 Extensions Control Register 3C5(R/W)

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	Extensions Access Enable

This register provides access to the HT209 Extended Registers (registers pointed to by Sequencer indices 80-FF). Access is enabled by writing 0EAh and disabled by writing 0AEh. Reading this register returns the state of the access enable flag in bit 0 (0 = disabled, 1 = enabled).

Note: Access to the Extension Registers is disabled on reset. This allows the on-board BIOS to initialize the HT209 chip to a particular mode of operation.

SR7 Reset Horizontal Character Counter 3C5(W)

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	Reserved

Writing to this register with any data will cause the horizontal character counter to be held in a reset condition (character counter output = 0). A write of any value to the Extensions Control Register (SR6) clears the latch that is holding the reset condition of the character counter.

Graphics Controller Registers

The Graphics Controller directs data from the display memory to the Attribute Controller and the CPU. There are ten read/write Graphics Controller Registers including one index register and nine data registers.

Desc.	Register Name	Bits	Access	Index	Ports	
GRX	Graphics Controller Index	4	R/W	--	3CE	3CE
GR0	Set/Reset Register	4	R/W	00	3CF	3CF
GR1	Enable Set/Reset	4	R/W	01	3CF	3CF
GR2	Color Compare	4	R/W	02	3CF	3CF
GR3	Data Rotate	5	R/W	03	3CF	3CF
GR4	Read Map Select	2	R/W	04	3CF	3CF
GR5	Graphics Mode	6	R/W	05	3CF	3CF
GR6	Miscellaneous Register	4	R/W	06	3CF	3CF
GR7	Color Don't Care	4	R/W	07	3CF	3CF
GR8	Bit Mask	8	R/W	08	3CF	3CF

GRX Graphics Controller Index 3CE (R/W)

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Graphics Controller Index Bit 3
2	Graphics Controller Index Bit 2
1	Graphics Controller Index Bit 1
0	Graphics Controller Index Bits 0

The Graphics Controller Index Register points to the internal data registers of the Graphics Controller. The four low-order bits determine which data register will be accessed when a read/write is performed using port address 3CF.

GR0 Set/Reset 3CF (R/W)

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Set/Reset Planes 3
2	Set/Reset Planes 2
1	Set/Reset Planes 1
0	Set/Reset Planes 0

This register is used to define a fill color written to display memory during any display memory write operation. The four low-order bits in this register enable the Set/Reset function in Write Mode 0. When Set/Reset is enabled for a bit plane, the Set/Reset Register writes to the plane. When disabled, processor data is written to the plane.

For example, if the Set/Reset Register contents are 1101, then a write to display memory will result in the following:

	7	6	5	4	3	2	1	0
Plane 3	1	1	1	1	1	1	1	1
Plane 2	1	1	1	1	1	1	1	1
Plane 1	0	0	0	0	0	0	0	0
Plane 0	1	1	1	1	1	1	1	1

Note: This assumes the Enable Set/Reset register (GR1) contents are 1111, all planes are enabled (Sequencer SR2 = 1111) and all bits are unmasked (GR8 = FFh).

GR1 Enable Set/Reset 3CF (R/W)

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Enable Set/Reset Plane 3
2	Enable Set/Reset Plane 2
1	Enable Set/Reset Plane 1
0	Enable Set/Reset Plane 0

This register defines which memory planes will receive fill data from the Set/Reset Register. The bits in this register function in conjunction with the Set/Reset Register (GR0) and the Mode Register (GR5). If the Mode Register is programmed to Write Mode 0, the contents of the Set/Reset register are written to the respective display memory planes. If the Write Mode is 0 and Set/Reset is not enabled on a plane, the plane is written with the data from the CPU data bus.

For example, if the Set/Reset Register (GR0) contents are 0100, the contents of the Enable Set/Reset Register are 0101 and a write of 11001101 is performed on display memory, the following settings will result:

	7	6	5	4	3	2	1	0
Plane 3	1	1	0	0	1	1	0	1
Plane 2	1	1	1	1	1	1	1	1
Plane 1	1	1	0	0	1	1	0	1
Plane 0	0	0	0	0	0	0	0	0

Note: 1. The settings above assume Write Mode = 0, all planes enabled (Sequencer SR2 = 1111), and all bits unmasked (GR8 = FFh).

Note: 2. Refer to the Mode Register, Port 3CF Bit[1:0] for additional information on Write Mode.

GR2 Color Compare Register 3CF (R/W)

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Color Compare Planes 3
2	Color Compare Planes 2
1	Color Compare Planes 1
0	Color Compare Planes 0

This register is used to implement graphics drawing algorithms that must find and identify objects by their colors. The 4 low-order bits of this register contain the value that video data is compared with during processor reads. The data returned from the comparison will be a logical 1 in each bit position where the 4 bit planes equal the compare value.

The Color Compare Register uses Read Mode 1 (GR5 bit 3) to match pixels with a specific color. If GR5 bit 3 = 1, the data read from display memory planes [0:3] is compared to the bits [0:3] in the Color Compare Register. A bit value of 1 is returned to the CPU when a match occurs for each pixel and a 0 is returned for each pixel that does not match the Color Compare Register.

For example, if the contents of the Color Compare Register are 0011 (to compare planes 0 and 1) and the contents of the plane are as follows:

	7	6	5	4	3	2	1	0
Plane 3	0	0	0	0	0	0	0	0
Plane 2	1	1	1	1	1	1	1	0
Plane 1	0	0	0	0	0	0	0	1
Plane 0	1	1	1	1	1	1	1	1

The data bus will contain the following (assuming GR7 = 1111):

	7	6	5	4	3	2	1	0
Bus	0	0	0	0	0	0	0	1

Notes:
1. Bit planes with the Color Don't Care (GR7) bit set return a logical 1 to a Color Compare.
2. Color Compare data has no meaning in mode 13h (320 x 200 x 256 colors).

GR3 Data Rotate 3CF(R/W)

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Function Select Bits
3	Function Select Bits
2	Rotate Count Bit 2
1	Rotate Count Bit 1
0	Rotate Count Bit 0

This register controls two independent functions; write data rotation, and logical functions performed on write data.

Bits[4:3] Function Select

These bits determine how the data latches in the processor affect video data that is being written into memory. The data rotation operation that results is shown below:

Bit-4	Bit-3	Operation
0	0	No change
0	1	Logical 'AND' between Data and latched data
1	0	Logical 'OR' between Data and latched data
1	1	Logical 'XOR' between Data and latched data

Data is defined as any option available with the Write Mode Register. Data cannot be the CPU latched data. For example, if the contents of the Data Rotate Register bits[2:0] are 011 and a program writes CAh to display memory:

PC Data =	1	1	0	0	1	0	1	0 = CAh
the Result Stored is =	0	1	0	1	1	0	0	1 = 59h

(the result is shifted 3 bits to the right)

If the contents of Data Rotate Register bits 3 and 4 are binary 11 (XOR function), and the Graphics CPU latches have been loaded (by a read of display memory) data will appear as follows:

	7	6	5	4	3	2	1	0
Plane 3	1	0	0	1	0	1	1	1
Plane 2	0	1	1	1	1	0	0	1
Plane 1	1	1	0	1	0	1	0	1
Plane 0	1	0	1	1	0	0	0	0

A write with data 00111100 will cause an XOR function to be performed on the PC data and the CPU latch, resulting in display memory being the following:

	7	6	5	4	3	2	1	0
Plane 3	1	0	1	0	1	0	1	1
Plane 2	0	1	0	0	0	1	0	1
Plane 1	1	1	1	0	1	0	0	1
Plane 0	1	0	0	0	1	1	0	0

The above condition assumes write modes=1, all planes enabled (SR2=1111) and all bits unmasked (GR8=FF)

Bits[2:0] Rotate Count

These bits perform a right rotate function on the data written by the CPU. If the Mode register (GR5) is programmed for Write Mode 0, the value in this field represents the number of bits the CPU data will be right rotated during CPU write cycles.

GR4 Read Map Select 3CF(R/W)

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Map Select Bit 1
0	Map Select Bit 0

The two low-order bits of this register designate the memory plane (0-3) from which the CPU reads data. The four memory planes are selected as follows:

Bit-1	Bit-2	Plane Selected
0	0	Plane 0
0	1	Plane 1
1	0	Plane 2
1	1	Plane 3

Note: If the double odd/even bit (SR4 bit-3, also called 'Chain 4') is set, the contents of this register are ignored.

GR5 Mode 3CF (R/W)

Bit	Description
7	Reserved
6	Shift 256
5	Shift Register
4	Odd/Even
3	Read Mode
2	Reserved
1	Write Mode Bit 1
0	Write Mode Bit 0

Bit 6 Shift 256

0 = Bit 5 of this register is ignored.
1 = The video shift register is set up for 256-color mode.

Bit 5

Shift Register
The data bits in the memory planes 0-3 are represented as M0D[7:0], M1D[7:0], M2D[7:0], and M3D[7:0].

0 = M0D[7:0], M1D[7:0], M2D[7:0], and M3D[7:0] are shifted out; bit 7 always shifts out first. The outputs for the M[0:3] planes are ATR[0:3].
1 = The data in the four serial shift registers will be formatted as follows (the LSB is shifted out first):

Shift Register Settings

MSB								LSB Output to:
M1D0	M1D2	M1D4	M1D6	M0D0	M0D2	M0D4	M0D6	ATR0
M1D1	M1D3	M1D5	M1D7	M0D1	M0D3	M0D5	M0D7	ATR1
M3D0	M3D2	M3D4	M3D6	M2D0	M2D2	M2D4	M2D6	ATR2
M3D1	M3D3	M3D5	M3D7	M2D1	M2D3	M2D5	M2D7	ATR3

Bit 4

Odd/Even

This bit is used to put the graphics controller in the Odd/Even addressing mode to emulate the CGA. This bit will track the function of Sequencer Memory Mode register bit 2, however the binary values will be opposite.

0 = Normal addressing mode.
1 = Odd/Even addressing mode.

Bit 3

Read Mode

0 = The CPU reads data from the display memory planes. The Read Map Select register (GR4) selects the plane.
1 = The CPU reads the result of the logical comparison between the data from the four display memory planes and the contents of the Color Compare register (GR2).

Bits[1:0]

Write Mode

0 = Each of the four display memory planes is written with the CPU data rotated right by the number of counts in the Rotate register, unless Set/Reset is enabled for any of the four planes. When Set/Reset is enabled, planes that are affected are written with 8 bits of the value contained in the Set/Reset register for that plane.

1 = Each display memory plane is written with the contents of the CPU latches. These latches are loaded by a CPU read operation. This operation overrides bit mask values.

2 = Memory planes [0:3] are filled with the value of data bits[0:3]. For example, memory plane 0 is filled with the value of Data Bus bit 0, memory plane 1 is filled with the value of Data Bus bit 1, etc.

3 = The CPU data is rotated, ANDed with the Bit Mask register, and written to the bit mask in place of the Bit Mask register. Set/Reset is enabled for all planes in this mode.

GR6 Miscellaneous 3CF (R/W)

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Memory Bit
2	Memory Bit
1	Chain Odd Maps to Even
0	Graphics Mode

This register is used to select the memory address range where display memory is mapped to the host and enables latches for the character generator.

Bit **Description**

Bits[3:2] Memory Map
This field controls the mapping of the address memory buffer into the CPU address space.

Memory Map 0: A000h for 128K
Memory Map 1: A000h for 64K
Memory Map 2: B000h for 32K
Memory Map 3: B800h for 32K

Bit 1 Chain Odd Maps to Even

0 = Planes 0 and 2 are selected.
1 = Planes 1 and 3 are selected. CPU address bit A0 is replaced by a higher order address bit and odd/even maps are selected with odd/even values of the address bit. The value of A0 determines which memory plane is selected.

Bit 0 Graphics Mode

0 = Selects text mode.
1 = Selects graphics mode and disables the character generator latches. In this mode, color data is serialized in the shift registers before it is passed to the Attribute Controller.

GR7 Color Don't Care 3CF (R/W)

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Color Don't Care 3
2	Color Don't Care 2
1	Color Don't Care 1
0	Color Don't Care 0

This register masks particular planes from being tested during color compare cycles. It is used in conjunction with the Color Compare Register (GR2).

Bits[3:0] The four low-order bits of this register control if a specific bit plane is examines in a color compare operation

0 = Disables color comparison
1 = Enables color comparison

For example, if the contents of the Color Compare Register (GR2) are 0011 (to compare planes 0 and 1) and the contents of the Color Don't Care register are 1011 (ignore plane 2) and the planes hold the following values:

	7	6	5	4	3	2	1	0
Plane 0	1	1	1	1	1	1	1	1
Plane 1	0	1	0	0	1	1	0	1
Plane 2	1	1	0	1	0	1	1	0
Plane 3	0	0	0	1	1	1	0	0

then the data bus will contain the following:

0	1	0	0	0	0	0	1

GR8 Bit Mask 3CF (R/W)

Bit	Description
7	Write Enable Data
6	Write Enable Data
5	Write Enable Data
4	Write Enable Data
3	Write Enable Data
2	Write Enable Data
1	Write Enable Data
0	Write Enable Data

This register is used to mask certain bit positions from being modified during read-modify-write cycles. However, it does not implement a true bit mask and must be used with care.

Bit[7:0] Write Enable Data

0 = Preserves the values of the corresponding bit in each of the four memory planes. The data read in the pervious cycle will be written into memory and stored in an internal latch within the Graphics Controller.

1 = Allows unrestricted manipulation of the data in the corresponding bit in each of the four memory planes.

The Bit Mask is applicable to any data written by the CPU, including rotate, logical functions (AND, OR, XOR), Set/Reset and No Change. The data must be latched internally by reading the location. The Bit Mask applies to all four planes simultaneously.

For example, if the contents of the Bit Mask register are 01101001 and the data latches have been loaded as in the following table:

	7	6	5	4	3	2	1	0
Plane 0	1	0	1	0	1	0	1	0
Plane 1	1	1	0	0	1	1	0	1
Plane 2	0	0	1	0	1	0	1	1
Plane 3	0	1	0	1	0	0	1	0

then,
A CPU write of 0100110 will result in display memory as follows:

	7	6	5	4	3	2	1	0
Plane 3	0	1	1	1	0	0	1	0
Plane 2	0	1	1	0	0	0	1	0
Plane 1	1	1	1	0	0	1	0	0
Plane 0	1	1	1	0	0	0	1	0
Effect	L	B	B	L	B	L	L	B

(L = Latched data, B = Bus Data)

Note: The above example assumes all planes are enabled (Sequencer SR2 = 1111).

Attribute Controller Registers

This section describes the seven Attribute Controller Registers. The Attribute Controller provides a palette of 16 colors selectable from a possible 64. It also controls blinking and underline operations.

The Attribute Controller Index Register (ARX) is read at Extension Index 83 for state save and restore. An extra bit is available (the data/index pointer) when reads are performed at the extension port. Writes to ARX at the 3C0 port togggle the data/index pointer. The Attribute Controller Index Register can also be read at CRTC index 24.

Desc.	Register Name	Bits	Access	Index	Ports	
ARX	Attribute Controller Index	6	R/W	--/83	3C0	3C5
AR0-F	Palette Registers 0-15	8	R/W	00-0F	3C0(W)	3C1(R)
AR10	Mode Control Register	7	R/W	10	3C0(W)	3C1(R)
AR11	Overscan Color	8	R/W	11	3C0(W)	3C1(R)
AR12	Color Plane Enable	6	R/W	12	3C0(W)	3C1(R)
AR13	Horizontal Pixel Panning	4	R/W	13	3C0(W)	3C1(R)
AR14	Color Select	4	R/W	14	3C0(W)	3C1(R)

ARX Index Register 3C0, 3C5 (R\W)

Bits	Description
7	Reserved
6	Reserved
5	Palette Address Source
4	Attribute Controller Bit
3	Attribute Controller Bit
2	Attribute Controller Bit
1	Attribute Controller Bit
0	Attribute Controller Bit

The five low-order bits of this register are used as an index to the data registers in the Attribute Controller. Accesses to 3C0 are directed to index and data on alternate accesses. The 3C0 I/O port index/data pointer is initialized for access of the index register by reading the Display Status Register (also called Status Register 1 at I/O port 3BA/3DA.

Bit 5 Palette Address Source

This bit selects the address source for the palette registers (0 = CPU, 1 = video data stream), which requires that CPU writes to the palette registers only take place when this bit is 0.

0 = Address source is CPU. The screen displays the color indicated by the Overscan Color register (AR11), normally black.
1 = Normal video display.

Bits[4:0] Attribute Controller Index

These bits form a 5 bit field for storing an index to the data registers in the Attribute Controller.

AR0-F Palette Registers 3C0(W), 3C1(R)

Bits	Description
7	Video 7
6	Video 6
5	Video 5
4	Video 4
3	Video 3
2	Video 2
1	Video 1
0	Video 0

These registers dynamically map the text attribute or graphic color input value to the display color.

The Palette registers enable the user to access 64 addresses in the DAC color table. This palette allows 16 colors to be displayed simultaneously. In 256K color modes, these registers remain in use to index the DAC color table and should not be modified from the default settings.

To support analog monitors, 8 bits of color value output from the Attribute Controller are remapped by the external color palette (DAC). The DAC uses the 8 bits from the Attribute Controller as an index into a group of 256 registers. When using color analog monitors, each register contains three six-bit color values (one each for Red, Green and Blue) that display 256K colors. Analog monochrome monitors connect to the Green output (Red and Blue) are ignored and display a maximum of 64 shades of grey.

AR10 Mode Control 3C0(W), 3C1(R)

Bits	Description
7	Alternate Video Source (1=AR14)
6	Pixel Width
5	Pixel Pan Compatibility
4	Reserved
3	Blink Enable
2	Line Graphics Enable
1	Monochrome Attributes Enable
0	Graphics Mode

This Register selects the graphics mode or monochrome attributes.

Bit 7 Alternate Video Source

This bit controls the source of video output bits 4 and 5. In 256-color mode, this bit is ignored and video outputs 4 and 5 are driven from bits 4 and 5 of the Palette registers (AR0-F).

0 = Video output bits 4 and 5 are driven from bits 4 and 5 of the Palette Registers (AR0-F).
1 = Video output bits 4 and 5 are driven by AR14 bits 0 and 1.

Bit 6 Pixel Width

0 = The video shift register is clocked at full speed.
1 = The video shift register is clocked at half speed for 256 color mode; the internal Attribute Controller Color Palette is by passed and the 8 video-bits are passed directly to the external palette.

Bit 5 Pixel Panning Capability

0 = Both Screen A and Screen B in split-screen mode will pan together.
1 = Only Screen A (upper screen) will pan.

Note: IBM VGA forces AR13 bits to be 0 even in 9-dot mode. A 1 bit left shift results.

Bit 3 Blink Enable

This bit functions in both text and graphics modes.

0 = Character blink is disabled.
1 = Character blink is enabled at a rate determined by the current vertical retrace frequency divided by 32 (16 frames in one state and 16 frames in the other state). This is the same rate as the cursor 'slow' blink (approximately 1/4 of a second each at 60Hz and about 1/3 of a second at 50Hz).

Bit 2 Line Graphics Enable

0 = Special line graphics character are disabled.
1 = Enables special line graphics characters by forcing the ninth dot of a line graphics character to be identical to the eighth dot of the character. The line graphics character codes are C0h through DFh.

Note: This bit is ignored in graphics modes.

Bit 1 Monochrome Attributes Enable
This bit works in graphics modes only.

0 = Selects color character attributes.
1 = Controls blinking in monochrome 4-color modes. Pixel patterns in graphics 4-color mode (mode 'F') are black (00), white (01), blinking (10), and intensified white (11). These patterns map to palette entries 0,1,4, and 5 if plane 3 is off and 8, 9, C, and D if plane 3 is on (2 bits per pixel get mapped to planes 0 and 2 with planes 1 and 3 = 0).

Bit 0 Graphics Mode

0 = Selects text mode.
1 = Selects graphics mode.

Summary of Operation of AR10

Bit 3	Bit 2	Bit 1	Bit 0	Mode	Description
0	x	x	1	Graphics	Plane 3 selects palette A3
1	x	0	1	Graphics	If plane 3 data = 0 then palette input A[3:1] If plane 3 data = 1 then palette input A3 is blinked
1	x	1	1	Graphics	Palette input A3 is blinked (toggled on/off at the blink rate)
BL	BG	x	0	Text	If BL = 0 characters don't blink (attribute bit 7 controls BG intensity) If BL = 1 characters blink if attribute bit 7 = 1 (BG is non-intensified) Character blink toggles the character between foreground color (AR10 bits[0:3]) and normal background color (AR10 bits[4:6])

AR11 Overscan Color 3C0(W), 3C1(R)

Bits	Description
7	Video 7
6	Video 6
5	Video 5
4	Video 4
3	Video 3
2	Video 2
1	Video 1
0	Video 0

This register defines the overscan or border color displayed on the CRT screen. The overscan color is displayed when both the Blank and Display Enable signals are inactive.

Note: Refer to AR0-F for information on how the video output bits are connected, especially bit[7:4], and how they interact with AR14.

AR12 Color Plane Enable 3C0 (R/W)

Bits	Description
7	Reserved
6	Reserved
5	Display Status Mux
4	Display Status Mux
3	Enable Color Planes
2	Enable Color Planes
1	Enable Color Planes
0	Enable Color Planes

This Register enables color planes and runs diagnostics.

Bits[5:4] Display Status Mux

These bits are used to run diagnostics on the color subsystem card. These bits select video output data during display periods and overscan color during non-display periods as shown below:

Display Status Mux Summary

Color Plane Register		Display Status Register	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	Video 2	Video 0
0	1	Video 5	Video 4
1	0	Video 3	Video 1
1	1	Video 7	Video 6

Setting bit 4 disables the cursor blink counter.

Bits[3:0] Color Plane Enable

These bits control whether the data read from a specific bit plane is used for video output.

0 = Disables the bit plane output
1 = Enables the bit plane output.

AR13 Horizontal Panning 3C0(W), 3C1(R)

Bits	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Horizontal Pixel Panning Shift Count
2	Horizontal Pixel Panning Shift Count
1	Horizontal Pixel Panning Shift Count
0	Horizontal Pixel Panning Shift Count

This register is used to select how many pixels of display data are to be shifted left or right horizontally. Pixel panning is available in both text and graphics modes.

Bits[3:0] Horizontal Pixel Panning Shift Count

The amount of shift varies with the character width according to the following table:

Count	9-bit Characters	8-bit Characters	256-color Mode
0	1 pixel left	no shift	no shift
1	2 pixels left	1 pixel left	no shift
2	3 pixels left	2 pixels left	1 pixel left
3	4 pixels left	3 pixels left	2 pixels left
4	5 pixels left	4 pixels left	2 pixels left
5	6 pixels left	5 pixels left	3 pixels left
6	7 pixels left	6 pixels left	3 pixels left
7	8 pixels left	7 pixels left	3 pixels left
8-F	no shift	1 pixel right	1 pixel right

Notes:
1. Only change this register during Vertical Retrace intervals to prevent distortion of the displayed images.
2. Set the Offset register (CR13) to at least one more than normal, when characters are not aligned with the character cell.
3. When AR10 bit 7 = 1, the output of this register is forced to 0 (no shift) by a successful line compare and remains in that state until the end of Vertical Retrace.

AR14 Color Select 3C0(W), 3C1(R)

Bits	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Video 3
2	Video 2
1	Video 1
0	Video 0

This register is used to provide video output information.

Bits[2:3] Video [7:6]
These bits drive video output bits [6:7].

Bits[0:1] Video [5:4]
When AR10 bit 7 = 1, these bits drive Video Output bits [5:4] instead of AR0-F (Color Palette Register) bits [4:5]. When AR10 bit 7 = 0, bits [5:4] of the internal palette are used for color bits C5 and C4.

CRT Controller Registers

The CRT Controller registers generate the syncing and blanking signals that define the display raster. These registers consist of one index register and 29 internal data registers. Two port addresses are used; the index address selects a data register, and the data address reads or writes data to the selected data register. In monochrome modes, the index register is mapped at port address 3B4 and the data register is mapped at port address 3B5. In color modes, the index register is mapped at port address 3D4 and the data register is mapped at port address 3D5.

The CRT Controller Registers are listed in the following table:

Desc.	Register Name	Bits	Access	Index	Ports	
CRX	Index Register	6	R/W	--	3B4	3D4
CR0	Horizontal Total Register	8	R/W	00	3B5	3D5
CR1	Horizontal Display Enable End	8	R/W	01	3B5	3D5
CR2	Horizontal Blanking Start	8	R/W	02	3B5	3D5
CR3	Horizontal Blanking End	8	R/W	03	3B5	3D5
CR4	Horizontal Retrace Start	8	R/W	04	3B5	3D5
CR5	Horizontal Retrace End	8	R/W	05	3B5	3D5
CR6	Vertical Total	8	R/W	06	3B5	3D5
CR7	Overflow	8	R/W	07	3B5	3D5
CR8	Preset Row Scan	7	R/W	08	3B5	3D5
CR9	Character Cell Height	8	R/W	09	3B5	3D5
CRA	Cursor Start	6	R/W	0A	3B5	3D5
CRB	Cursor End	7	R/W	0B	3B5	3D5
CRC	Start Address High	8	R/W	0C	3B5	3D5
CRD	Start Address Low	8	R/W	0D	3B5	3D5
CRE	Cursor Location High	8	R/W	0E	3B5	3D5
CRF	Cursor Location Low	8	R/W	0F	3B5	3D5
CR10	Vertical Retrace Start	8	(W, R/W)	10	3B5	3D5
CR11	Vertical Retrace End	8	(W, R/W)	11	3B5	3D5
CR12	Vertical Display End	8	R/W	12	3B5	3D5
CR13	Offset Register	8	R/W	13	3B5	3D5
CR14	Underline Row Scan Register	7	R/W	14	3B5	3D5
CR15	Vertical Blanking Start Register	8	R/W	15	3B5	3D5
CR16	Vertical Blanking End Register	8	R/W	16	3B5	3D5
CR17	Mode Register	7	R/W	17	3B5	3D5
CR18	Line Compare Register	8	R/W	18	3B5	3D5
CR1F	Identification Register	8	R	1F	3B5	3D5
CR22	Graphics Controller Data Latches	8	R	22	3B5	3D5
CR24	Attribute Controller Index/Data Latch	7	R	24	3B5	3D5
CR3x	Clear Vertical Display Enable Flip-Flop	1	W	30-3F	3B5	3D5

CRX CRT Controller Index Register 3B5/3D5(R/W)

Bits	Description
7	Reserved
6	Reserved
5	CRTC Index Bit 5
4	CRTC Index Bit 4
3	CRTC Index Bit 3
2	CRTC Index Bit 2
1	CRTC Index Bit 1
0	CRTC Index Bit 0

This register selects which of the 29 internal CRTC data registers will be accessed during the next read/write operation at port address 3B5 (mono) or 3D5 (color).

CR0 Horizontal Total Register 3B5/3D5(R/W)

Index 00 Write Protected by Extension Register EB(5) and CR11(7)

Bits	Description
7	Horizontal Total Bit 7
6	Horizontal Total Bit 6
5	Horizontal Total Bit 5
4	Horizontal Total Bit 4
3	Horizontal Total Bit 3
2	Horizontal Total Bit 2
1	Horizontal Total Bit 1
0	Horizontal Total Bit 0

This register defines the total number of character clocks in a horizontal scan line, including blanking and retrace. All horizontal and vertical timing is based upon the contents of this register.

Horizontal Total = (Total number of character clocks in one scan line) - 5

CR1 Horizontal Display Enable End Register 3B5/3D5(R/W)

Index 01 Write Protected by Extension Register EB(5) and CR11(7)

Bits	Description
7	Horizontal Display Enable End Bit 7
6	Horizontal Display Enable End Bit 6
5	Horizontal Display Enable End Bit 5
4	Horizontal Display Enable End Bit 4
3	Horizontal Display Enable End Bit 3
2	Horizontal Display Enable End Bit 2
1	Horizontal Display Enable End Bit 1
0	Horizontal Display Enable End Bit 0

This register controls the duration of the Horizontal Display Enable pulse. The contents of this register define the total number of displayed characters in one horizontal scan line.

Horizontal Display Enable End = (Total number of characters per scan line) - 1

CR2 Horizontal Blanking Start Register 3B5/3D5(R/W)

Index 02 Write Protected by Extension Register EB(5) and CR11(7)

Bits	Description
7	Horizontal Blanking Start Bit 7
6	Horizontal Blanking Start Bit 6
5	Horizontal Blanking Start Bit 5
4	Horizontal Blanking Start Bit 4
3	Horizontal Blanking Start Bit 3
2	Horizontal Blanking Start Bit 2
1	Horizontal Blanking Start Bit 1
0	Horizontal Blanking Start Bit 0

The contents of this register trigger the start of the Horizontal Blanking pulse. The Horizontal Blanking signal becomes active when the internal horizontal character counter is equal to the contents of this register.

Horizontal Blanking Start = Horizontal Display End (CR1) + 1

CR3 Horizontal Blanking End Register 3B5/3D5 (R/W)

Index 03 Write Protected by Extension Register EB(5) and CR11(7)

Bits	Description
7	Compatibility Read
6	Display Enable Skew Control Bit
5	Display Enable Skew Control Bit
4	Horizontal Blanking End Bit 4
3	Horizontal Blanking End Bit 3
2	Horizontal Blanking End Bit 2
1	Horizontal Blanking End Bit 1
0	Horizontal Blanking End Bit 0

This register determines the duration of the Horizontal Blanking pulse and provides a mechanism for display enable skewing in text modes.

Bit 7 — Compatibility Read

1 = Enables read access to CRTC registers CR10 and CR11. This bit must be set for all standard and extended VGA modes.

Bits[6:5] — Display Enable Skew

The CRT Controller must access the display buffer, the attribute code, and the character generator font information prior to displaying data on the screen. These bits allow the Display Enable signal to be skewed up to 3 character clocks. Typically this field is set to 0. In 1024 x 768 extended modes, the Display Enable signal is skewed by one character clock to allow for synchronization with Horizontal and Vertical Retrace.

Bits[4:0] — Horizontal Blanking End

These bits and CR5 bit 7 comprise a 6-bit register that determines the duration of the Horizontal Blanking pulse in character clocks. The Horizontal Blanking pulse becomes inactive when the contents of the internal character counter match these bits.

Horizontal Blanking End = Horizontal Blanking Start (CR2) + width of Horizontal Blanking pulse in character clocks

CR4 Horizontal Retrace Start Register 3B5/3D5(R/W)

Index 04 — Write Protected by Extension Register EB(5) and CR11(7)

Bits	Description
7	Horizontal Retrace Start Bits 7
6	Horizontal Retrace Start Bits 6
5	Horizontal Retrace Start Bits 5
4	Horizontal Retrace Start Bits 4
3	Horizontal Retrace Start Bits 3
2	Horizontal Retrace Start Bits 2
1	Horizontal Retrace Start Bits 1
0	Horizontal Retrace Start Bits 0

This register triggers the horizontal character position at which the Horizontal Retrace pulse starts. When the contents of this register match the internal Horizontal Character Counter, the Horizontal Retrace pulse becomes inactive. It is used to center the image on the monitor screen.

CR5 Horizontal Retrace End Register 3B5/3D5(R/W)

Index 05 Write Protected by Extension Register EB(5) and CR11(7)

Bits	Description
7	Horizontal Blanking End
6	Horizontal Retrace Delay Bit
5	Horizontal Retrace Delay Bit
4	Horizontal Retrace End Bit 4
3	Horizontal Retrace End Bit 3
2	Horizontal Retrace End Bit 2
1	Horizontal Retrace End Bit 1
0	Horizontal Retrace End Bit 0

This register is used to skew Horizontal Retrace with respect to Display Enable to end Horizontal Retrace, and contains the msb of the Horizontal Blanking End register.

Bit 7 Horizontal Blanking End Bit

This bit in conjunction with CR3 bits [4:0] determines the duration of the Horizontal Blanking pulse in character clocks.

Bits[6:5] Horizontal Retrace Delay

These bits allow the Horizontal Retrace pulse to be skewed (delayed) by up to 3 character clocks. This field is set to 0 in most cases.

Bits[4:0] Horizontal Retrace End

The Horizontal Retrace pulse becomes inactive when the internal character counter equal the value of this field.

Horizontal Retrace End = Horizontal Retrace End (CR3) + width of Horizontal Retrace pulse in character clocks.

CR6 Vertical Total Register 3B5/3D5(R/W)

Index 06 Write Protected by Extension Register EB(5) and CR11(7)

Bits	Description
7	Vertical Total Bit 7
6	Vertical Total Bit 6
5	Vertical Total Bit 5
4	Vertical Total Bit 4
3	Vertical Total Bit 3
2	Vertical Total Bit 2
1	Vertical Total Bit 1
0	Vertical Total Bit 0

The Vertical Total register defines the total number of horizontal scan lines on the CRT, including the period during Vertical Retrace. This register contains the low-order 8 bits of a 10-bit register. The ninth and tenth bits are located in the Overflow register (CR7).

Vertical Total = number of horizontal scan lines + Vertical Retrace in character clocks - 2

CR7 Overflow Register 3B5/3D5(R/W)

Index 07 Write Protected by Extension Register EB(5) and CR11(7)

Bits	Description
7	Vertical Retrace Start Bit 9
6	Vertical Display End Bit 9
5	Vertical Total Bit 9
4	Line Compare Bit 8
3	Vertical Blanking Start Bit 8
2	Vertical Retrace Start Bit 8
1	Vertical Display End Bit 8
0	Vertical Total Bit 8

The Overflow register contains the high-order overflow bits for CRTC registers that require more than eight bits.

CR8 Preset Row Scan Register 3B5/3D5 (R/W)

Index 08 Write Protected by Extension Register EB(5) and CR11(7)

Bits	Description
7	Reserved
6	Byte Panning Control Bit
5	Byte Panning Control Bit
4	Preset Row Scan Bit 4
3	Preset Row Scan Bit 3
2	Preset Row Scan Bit 2
1	Preset Row Scan Bit 1
0	Preset Row Scan Bit 0

This register is used to customize the display format. It provides a mechanism for smooth scrolling and byte panning control.

Note: This register should only be changed during Vertical Retrace.

Bit[6:5] Byte Panning Control

These bits extend the capability of the Horizontal Panning register (AR13). Up to 8 pixels can be panned horizontally by AR13. This field increases horizontal panning capability by up to 24 pixels, resulting in a total panning capability of 1-32 pixels. The table below shows the display shift that results from setting Byte Panning Bit 6 and Bit 5.

Bit-6	Bit-5	Byte Panning
0	0	0 bytes (display shifts 0 pixels left)
0	1	1 byte (display shifts 8 pixels left)
1	0	2 bytes (display shifts 16 pixels left)
1	1	3 bytes (display shifts 24 pixels left)

Bits[4:0] Preset Row Scan

These bits are used for smooth scrolling in text modes and certain graphics modes. For example, by setting the Preset Row Scan to 1 the next frame will start at scan line 1 of the character cell, giving an appearance of shifting the screen up one scan line.

CR9 Character Cell Height Register 3B5/3D5(R/W)

Index 09 Write Protected by Extension Register EB(4)

Bits	Description
7	Double Scan
6	Vertical Blank Start Bit 9
5	Line Compare Bit 9
4	Character Cell Height Bit 4
3	Character Cell Height Bit 3
2	Character Cell Height Bit 2
1	Character Cell Height Bit 1
0	Character Cell Height Bit 0

This register improves the quality of CGA text modes by allowing the VGA to double scan CGA 200 line modes. It also specifies the number of scan lines per character row and contains bit 9 from the Line Compare and Vertical Blank Start registers.

Bit 7 Double Scan

0 = Normal scan line generation.
1 = Double Scan enabled. Each scan line is displayed twice in succession, enhancing CGA 200-line modes by double scanning to 400 lines. Character, height, cursor and underline locations double.

Bit 6 — Line Compare Bit 9

This is bit 9 of the Line Compare register; CR18 contains bits [7:0] and CR7 bit 4 contains bit 8.

Bit 5 — Vertical Blanking Start Bit 9

This is bit 9 of the Vertical Blanking Start register; CR15 contains bits [7:0] and CR7 bit 3 contains bit 8.

Bits[4:0] — Character Cell Height

These bits specify the number of scan lines per character row.

Character Cell Height = Number of scan lines per character cell - 1

CRA Cursor Start Register 3B5/3D5(R/W)

Index 0A — Write Protected by Extension Register EB(4)

Bits	Description
7	Reserved
6	Reserved
5	Cursor Disable
4	Cursor Start Bit4
3	Cursor Start Bit 3
2	Cursor Start Bit 2
1	Cursor Start Bit 1
0	Cursor Start Bit 0

This register determines the scan line within a character cell at which the cursor will begin. When used with the Cursor End register this register defines the size of the cursor with respect to a character cell.

Bit 5 — Cursor Disable

0 = Cursor enabled.
1 = Cursor disabled.

Bits[4:0] — Cursor Start

These bits determine the scan line where the cursor will start within a character cell. When used with the Cursor End register these bits define the size of the cursor. For example:

Cursor Start (CRA) = 0 Cursor End (CRB) = 7
The cursor will occupy scan lines 0 - 7 within a character cell, appearing as a block.

Cursor Start (CRA) = 11 Cursor End (CRB) = 12
The cursor will occupy scan lines 11 & 12 within a character cell, appearing as an underline.

Cursor Start (CRA) = 9 Cursor End (CRB) = 6
The cursor will not be visible.

CRB Cursor End Register 3B5/3D5(R/W)

Index 0B

Write Protected by Extension Register EB(4)

Bits	Description
7	Reserved
6	Control Skew Bit
5	Control Skew Bit
4	Cursor End Bit
3	Cursor End Bit
2	Cursor End Bit
1	Cursor End Bit
0	Cursor End Bit

This register specifies the scan line within a character cell at which the cursor will end. When used with the Cursor Start register, this register defines the size of the cursor with respect to a character cell.

Bits[6:5] Cursor Skew Control

These bits control the cursor skew. Set this field to 0 for all VGA and extended modes. Typical bit settings and skews are shown below:

Cursor End Skew

Bit 6	Bit 5	Skew
0	0	Zero character skew
0	1	Zero character skew
1	0	One character skew
1	1	Two character skew

Bits[4:0] Cursor End

This field determines the scan line within a character cell where the cursor will end. Refer to the Cursor Start register (CRA) for programming examples.

CRC Start Address High Register 3B5/3D5(R/W)

Index 0C

Bits	Description
7	Start Address High Bit 15
6	Start Address High Bit 14
5	Start Address High Bit 13
4	Start Address High Bit 12
3	Start Address High Bit 11
2	Start Address High Bit 10
1	Start Address High Bit 9
0	Start Address High Bit 8

The Start Address High Register is used to pan an image on the screen, or move between display pages in memory. In conjunction with the Start Address Low Register (CRD) it defines the address in display memory of the data that will be displayed in the upper left corner of the screen (starting position).

If the VGA is using split screen mode, the Start Address registers specify the start address of Screen A (upper portion). The start address of Screen B (lower portion) is always 0. The Start Scan Line of Screen B is determined by the Line Compare Register (CR18).

Note: This register is also used to identify the HT209 chip. Any value written to this register can be read back exclusive-OR'd with EAh (binary 11101010) at the VGA Identification register (CR1F).

CRD Start Address Low Register 3B5/3D5(R/W)

Index 0D

Bits	Description
7	Start Address Low Bit 7
6	Start Address Low Bit 6
5	Start Address Low Bit 5
4	Start Address Low Bit 4
3	Start Address Low Bit 3
2	Start Address Low Bit 2
1	Start Address Low Bit 1
0	Start Address Low Bit 0

This register contains the 8 low-order bits of the Start Address register. See the Start Address High register (CRC) for a full description.

CRE Cursor Location High Register 3B5/3D5(R/W)

Index 0E

Bits	Description
7	Cursor Location High Bit 15
6	Cursor Location High Bit 14
5	Cursor Location High Bit 13
4	Cursor Location High Bit 12
3	Cursor Location High Bit 11
2	Cursor Location High Bit 10
1	Cursor Location High Bit 9
0	Cursor Location High Bit 8

The Cursor Location High Register together with the Cursor Location Low Register (CRF) comprise a 16-bit field that specifies the offset of the cursor location from the start of physical display memory in character positions.

The value of the Cursor Location Registers is relative to the start of physical display memory, not to the start of the screen. When the Screen Start Address Registers (CRC & CRD) and the Cursor Location Registers are set to 0, the cursor is positioned over the upper left character on the screen (row 1, column 1). If the screen start registers are set to 1, the cursor will remain pointed to the same character.

Note: Since text information is stored in display memory as character/attribute pairs, the address of the character under the cursor will be exactly two times the value in the Cursor Location Registers plus the base address of the screen.

CRF Cursor Location Low Register 3B5/3D5(R/W)

Index 0F

Bits	Description
7	Cursor Location Low Bit 7
6	Cursor Location Low Bit 6
5	Cursor Location Low Bit 5
4	Cursor Location Low Bit 4
3	Cursor Location Low Bit 3
2	Cursor Location Low Bit 2
1	Cursor Location Low Bit 1
0	Cursor Location Low Bit 0

This register contains the 8 low-order bits of the 16-bit Cursor Location Register used to specify the offset of the cursor location from the start of physical display memory in character positions. See the Cursor Location High Register (CRE) for additional information.

CR10 Vertical Retrace Start 3B5/3D5(W, R/W)

Index 10

Bits	Description
7	Vertical Retrace Start Bit
6	Vertical Retrace Start Bit
5	Vertical Retrace Start Bit
4	Vertical Retrace Start Bit
3	Vertical Retrace Start Bit
2	Vertical Retrace Start Bit
1	Vertical Retrace Start Bit
0	Vertical Retrace Start Bit

This register contains the 8 low-order bits of a 10-bit scan line count that triggers the start of the Vertical Retrace pulse. The two high-order bits are accessed through the Overflow Register (CR7).

Note: This register can be read only when CR3 bit 7 = 1

CR11 Vertical Retrace End Register 3B5/3D5(W, R/W)

Index 11

Bits	Description
7	Write Protect CR[0:7]
6	Refresh Cycle Select
5	Enable Vertical Interrupt
4	Clear Vertical Interrupt
3	Vertical Retrace End Bit
2	Vertical Retrace End Bit
1	Vertical Retrace End Bit
0	Vertical Retrace End Bit

This register determines the vertical refresh rate.

Bit 7 Write Protect CR[0:7]

0 = No write protection of CRTC registers CR[0:7].
1= Write protect CR[0:7].

Bit 6 Refresh Cycle Select

0 = Selects three DRAM refresh cycles per horizontal retrace.
1 = Five DRAM refresh cycles.

Bit 5 Vertical Interrupt Enable

This bit controls whether interrupts are generated on the INT pin of the HT209 chip. This pin is typically connected to IRQ2 of the system bus. IRQ2 is used to identify the start of a vertical retrace. Once a Vertical Interrupt occurs; it can be cleared when a 0 is written to bit 4 of this register.

0 = Enables vertical interrupts.
1 = Disables vertical interrupts. The interrupt status can still be read at the Input Status Register 0 (port 3C2 bit 7).

Bit 4 Clear Vertical Interrupt

0 = Clears the vertical interrupt flip-flop and reasserts the interrupt signal.
1 = Allows the vertical interrupt flip-flop to be set at the start of the next Vertical Retrace interval.

Bits 3-0 Vertical Retrace End

The Vertical Retrace pulse becomes inactive when these bits match the lower four bits of the internal scan line counter. The width of the Vertical Retrace pulse is determined as follows:

Vertical Retrace End = Vertical Retrace Start (CR10) + the width of the Vertical Retrace pulse in horizontal scan units.

Note: This register can be read only when CR3 bit 7 = 1

CR12 Vertical Display Enable End Register 3B5/3D5(R/W)

Index 12

Bits	Description
7	Vertical Display End Bit
6	Vertical Display End Bit
5	Vertical Display End Bit
4	Vertical Display End Bit
3	Vertical Display End Bit
2	Vertical Display End Bit
1	Vertical Display End Bit
0	Vertical Display End Bit

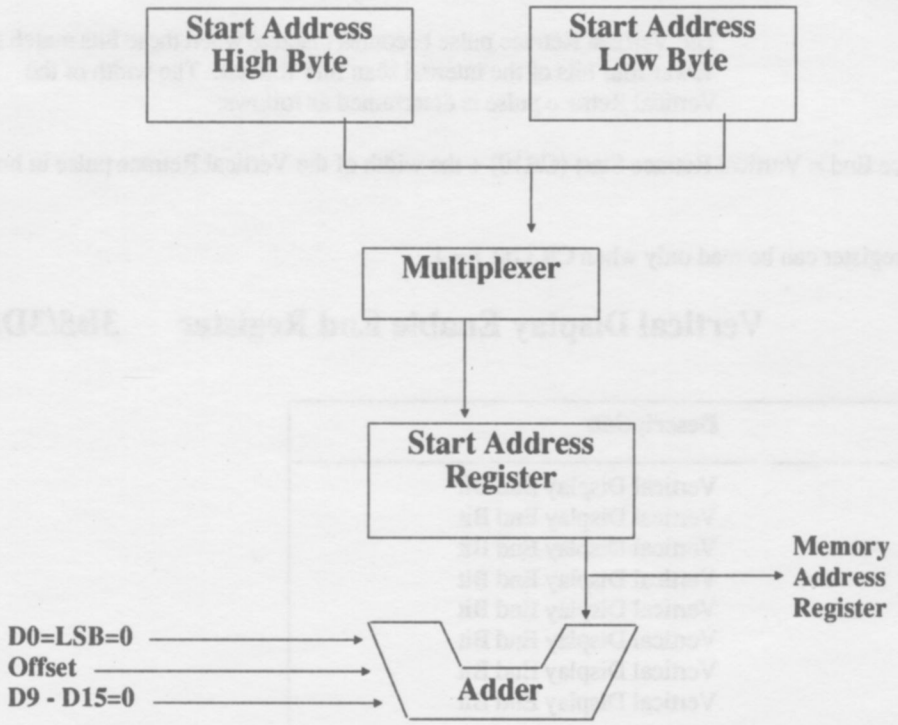
This register contains the 8 low-order bits of the 10-bit Vertical Display Enable End Register. The value in this register defines the point in a vertical scan at which vertical display enable ends and blanking begins. The ninth and tenth bits are located in the Overflow register (CR7).

CR13 Offset Register 3B5/3D5(R/W)

Index 13

Bits	Description
7	Logical Screen Line Width Bit
6	Logical Screen Line Width Bit
5	Logical Screen Line Width Bit
4	Logical Screen Line Width Bit
3	Logical Screen Line Width Bit
2	Logical Screen Line Width Bit
1	Logical Screen Line Width Bit
0	Logical Screen Line Width Bit

The Offset Register contents define the logical line width of the screen. The starting address of the next character row is determined by the value in this register.



The above figure is a functional diagram of how the Offset register is used. The register start address is sent to the memory address counter. When the memory address counter counts bytes, the next line address is the current line start address + two times the Offset register contents. This is shown in the figure by the fact that the adder has one of the input port's least significant bits forced to 0. When the memory address counter in counting words, the next line address is the current line start address + four times the Offset register contents. The byte or word mode for the memory address counter is selected by the Mode Control Register (CR17), bit 6. The Start Address High and Low bytes correspond to the first address after a Vertical Retrace starts.

CR14 Underline Row Scan Register 3B5/3D5(R/W)

Index 14

Bits	Description
7	Reserved
6	Doubleword Mode
5	Count by 4
4	Underline Row Scan Bit
3	Underline Row Scan Bit
2	Underline Row Scan Bit
1	Underline Row Scan Bit
0	Underline Row Scan Bit

This register defines which line of a character cell will be illuminated when the underline attribute is set. It is used in text modes only.

Bit 6 Doubleword Mode

0 = Allows Mode register (CR17) bit-6 to control the addressing mode.

1 = Forces Doubleword mode. The CRTC memory address counter is shifted up two bits to provide the linear address to display memory. The display memory address bit-0 is driven from CRTC memory address counter bit-12 and display memory address bit-1 is driven from CRTC memory address counter bit-13. The Byte Mode bit (CR17 bit-6) is ignored.

Bit 5 Count By 4

0 = Character clock not divided by 4.
1 = Divides the character clock input to the memory address counter by 4 when double addresses are used.

Note: If CR17 bit 3 (Count by 2) is 0, the memory address counter is clocked by the character clock /4. If "Count by 1' is 1, the memory address counter is clocked by the character clock/2 and 'Count by 4' is ignored. When 'Count by 2' and 'Count by 4' are both 0, the memory address counter is clocked by the unmodified character clock.

Bits[4:0] Underline Row Scan

These bits specify the horizontal row scan in a character cell at which underlining will occur. The scan lines of the character cell are assumed to be numbered from the top of the cell starting at 0.

Note: Underlining is enabled while in monochrome modes (EGA/VGA mode 7 and Hercules/MGA text modes) by setting this field to 13 (the last scan line of the 8x14 character cell). For color modes, this field is normally programmed to a value larger than the size of the character cell to effectively disable underlining.

CR15 Vertical Blanking Start Register 3B5/3D5(R/W)

Index 15

Bits	Description
7	Vertical Blanking Start Bit 7
6	Vertical Blanking Start Bit 6
5	Vertical Blanking Start Bit 5
4	Vertical Blanking Start Bit 4
3	Vertical Blanking Start Bit 3
2	Vertical Blanking Start Bit 2
1	Vertical Blanking Start Bit 1
0	Vertical Blanking Start Bit 0

This register contains the low-order 8 bits of the horizontal scan line count of the 10-bit Vertical Blanking Start Register. The ninth bit is located in the Overflow register (CR7 bit-3) and the tenth bit is located in the Character Cell Height Register (CR9 bit-5).

CR16 Vertical Blanking End Register 3B5/3D5(R/W)

Index 16

Bits	Description
7	Vertical Blanking End Bit
6	Vertical Blanking End Bit
5	Vertical Blanking End Bit
4	Vertical Blanking End Bit
3	Vertical Blanking End Bit
2	Vertical Blanking End Bit
1	Vertical Blanking End Bit
0	Vertical Blanking End Bit

These bits specify the horizontal scan line count at which the Vertical Blanking pulse becomes inactive. The vertical blanking width (w) is determined from the following algorithm:

Value programmed into the Vertical Blanking End = The value of the Vertical Blanking Start (CR15) + width of blanking pulse in character clocks

CR17 CRT Mode Register 3B5/3D5(R/W)

Index 17

Bits	Description
7	H/V Retrace Enable
6	Word/Byte Mode
5	Address Wrap
4	Reserved
3	Count by Two
2	Multiply Vertical by 2
1	Select Row Scan Counter
0	Compatibility Mode Support

The Mode control register is a multifunction register. Each bit defines a different option.

Bit 7 Horizontal/Vertical Retrace Enable

0 = Disables Horizontal and Vertical Retrace.
1 = Enables Horizontal and Vertical Retrace.

Bit 6 Byte/Word Mode

0 = Selects Byte mode.
1 = Selects Word mode.

Word mode causes the address counter bits to shift down one bit, and the MSB of the counter appears on the LSB of the memory address output.

If Doubleword Mode (CR14 bit 6) is set, this bit is ignored.

Internal Memory Address Counter/Output Multiplexer Relationship:

	CRTC Output Pin	Byte Address Mode	Word Address Mode	Doubleword Address Mode
RAM Row Address	xA15	MA15	MA14	MA13
	xA15	MA14	MA13	MA12
	xA15	MA8	MA8	MA8
RAM Column Address	xA3	MA3	MA2	MA1
	xA2	MA2	MA1	MA0
	xA1	MA1	MA0	MA13
	xA0	MA0	MA13/MA15	MA12

Bit 5 Address Wrap

The Address Wrap bit selects the correct memory address counter bit to be output on xA0 in word mode. This bit must always be set to 1. In word mode, this bit controls the output from the memory address counter to the address bus and enables the full 256K of memory on the adapter.

Bit 3 Count By 2

0 = The memory address counter is clocked by the character clock.
1 = The memory address counter is clocked by the character clock divided by 2.

This bit also creates either a byte or word refresh address for display memory.

Bit 2 Multiply Vertical By 2

0 = Selects the horizontal retrace clock
1 = Selects the horizontal retrace clock divided by 2. The following vertical registers must be programmed to half their normal value to result in the same number of scan lines:

CR6 Vertical Total
CR10 Vertical Retrace Start
CR12 Vertical Display End
CR15 Vertical Blanking Start
CR18 Line Compare

Note: These registers have overflow bits in the Overflow Register (CR7)

Bit 1 — Select Row Scan Counter

This bit allows compatibility with the Hercules graphics card and other 400 line graphics systems.

0 = Row scan counter bit 1 is substituted for memory address bit 14 during active display time.
1 = No substitution takes place.

Bit 0 — Compatibility Mode

This bit allows compatibility with the IBM Color Graphics Adapter.

0 = Row scan counter bit 0 is substituted for memory address bit 13 during active display time.
1 = No substitution takes place.

CR18 Line Compare Register 3B5/3D5(R/W)

Index 18

Bits	Description
7	Line Compare Bit 7
6	Line Compare Bit 6
5	Line Compare Bit 5
4	Line Compare Bit 4
3	Line Compare Bit 3
2	Line Compare Bit 2
1	Line Compare Bit 1
0	Line Compare Bit 0

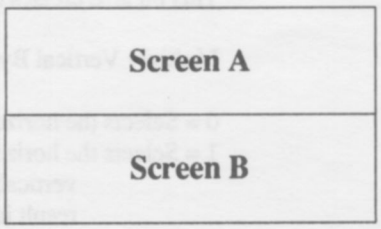
This register contains the 8 low-order bits of the 10 bit Line Compare register. CR7 bit 4 contains bit 9 of this register and CR9 bit 6 contains bit 10. When the horizontal scan line counter value is equal to the contents of the Line Compare register, the memory address generator and the character row scan count are cleared.

Split Screen Definition

CR8 (Preset Row Scan)
CRC-D (Start Address)

CR18 Line Compare

0 (Preset Row Scan)
0 (Start Address)



Note:The screen A may be smooth scrolled vertically and panned horizontally, but Screen B cannot. Screen B pans with Screen A and is stationary when Screen A is panned (AR10 bit 5)

CR1F Identification Register 3B5/3D5(R)

Index 1F

Bits	Description
7	HT209 Identification Bit
6	HT209 Identification Bit
5	HT209 Identification Bit
4	HT209 Identification Bit
3	HT209 Identification Bit
2	HT209 Identification Bit
1	HT209 Identification Bit
0	HT209 Identification Bit

This read-only register is used to determine if a graphics adapter supports the HT extension registers. The exact nature and capabilities of the chip installed can be determined by reading the chip revision registers (ER8E and ER8F). The value read back from this register is the current value in the Start Address High Register (CRC) exclusive OR'd with EAh. For example, if CRC contains 0, this register will read back as EAh; if CRC contains FFh, this register will read back as 15h; etc..

CR22 Graphics Controller Data Latches 3B5/3D5(R)

Index 22

Bits	Description
7	Graphics Controller Data Latch Bit
6	Graphics Controller Data Latch Bit
5	Graphics Controller Data Latch Bit
4	Graphics Controller Data Latch Bit
3	Graphics Controller Data Latch Bit
2	Graphics Controller Data Latch Bit
1	Graphics Controller Data Latch Bit
0	Graphics Controller Data Latch Bit

This register is used to read the state of the Graphics Controller Data Latch 'n', where 'n' is controlled by the Graphics Controller Read Map Select Register (GR4 bits [1:0]) and is in the range 0-3.

CR24 Attribute Controller Index/Data Latch 3B5/3D5(R)

Index 24

Bits	Description
7	Index (0), Data (1)
6	Reserved
5	Palette Address Source
4	Attribute Controller Index
3	Attribute Controller Index
2	Attribute Controller Index
1	Attribute Controller Index
0	Attribute Controller Index

This register is used to read back the state of the attribute controller index/data latch.

Note: A read from this register returns the same information as a read returned by Extension Register 83.

CR3x Clear Vertical Display Enable Flip-Flop 3B5/3D5(W)

Index 30-3F

Bits	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	Clear Display Enable Flip-Flop

This register clears the display. Writing odd values to this register causes the Vertical Display Enable Flip-Flop to be cleared. The flip-flop is automatically set by reaching vertical total. The effect of this is to force a longer retrace period. When the vertical display is terminated early, the screen blanks early for one frame causing a minor visual disturbance and the Sequencer directs more display memory cycles to the CPU.

Extension Registers

The Extension Registers provide additional functionality to the HT209 chip beyond standard VGA.

There are 45 Extension registers including one index register and 44 data registers. Indexing Extension Registers is accomplished through the Sequencer/Extensions Index Register (SRX) at port address 3C4. The Extension data registers are accessed at port address 3C5. A listing of the Extension Registers is provided in the following table:

EXTENSION REGISTER SUMMARY

Port	Abbr.	Name	Bits	Access	Index	Register
ER80-ER82		Reserved	0	-	80-82	3C5
ER83	ARX	*Attribute Controller Index	7	R/W	83	3C5
ER84-ER89		Reserved	0	-	84-89	3C5
ER8A-ER8D		Reserved	0	-	8A-8D	3C5
ER8E	REV	ChipRevision Register	8	R	8E	3C5
ER8F	REV	Chip Revision Register	8	R	8F	3C5
ER90-ER93		Reserved	0	-	90-93	3C5
ER94	PPA	Pointer Pattern Address	8	R/W	94	3C5
ER95-ER99		Reserved	0	-	95-99	3C5
ER9A-ER9B		Reserved	0	-	9A-9B	3C5
ER9CTPXH		Pointer Horizontal Position High	3	R/W	9C	3C5
ER9D	PXL	Pointer Horizontal Position Low	8	R/W	9D	3C5
ER9E	PYH	Pointer Vertical Position High	2	R/W	9E	3C5
ER9F	PYL	Pointer Vertical Position Low	8	R/W	9F	3C5
ERA0	GRL0	Graphics Controller Memory Latch 0	8	R/W	A0	3C5
ERA1	GRL1	Graphics Controller Memory Latch 1	8	R/W	A1	3C5
ERA2	GRL2	Graphics Controller Memory Latch 2	8	R/W	A2	3C5
ERA3	GRL3	Graphics Controller Memory Latch 3	8	R/W	A3	3C5
ERA4	CLK	Extended Clock Select	3	R/W	A4	3C5
ERA5	CURS	Cursor Attributes	3	R/W	A5	3C5
ERB3	SCRAM	Scratch RAM Register	8	R/W	B3	3C5
ERC0	MNLCK	Monochrome Lock	8	R/W	C0	3C5
ERC8	MSCRTRLII	Miscellaneous Control II	4	R/W	C8	3C5
ERC9		Reserved	0	-	C9	3C5

Port	Abbr.	Name	Bits	Access	Index	Register
ERCA	HOFL	Horizontal Overflow	5	R/W	CA	3C5
ERE0	MSCTRLI	Miscellaneous Control I	8	R/W	E0	3C5
ERE1	INTLC	Interlace Value	8	R/W	E1	3C5
ERE2	TRAPCTL	Trap Control Register	5	R/W	E2	3C5
ERE3	WRTPRT	Write Protect Control	6	R/W	E3	3C5
ERE8	LWRSPLT	Lower Split Bank	8	R/W	E8	3C5
ERE9	UPRSPLT	Upper Split Bank	8	R/W	E9	3C5
EREA	SWSTB	Switch Strobe**	--	W	EA	3C5
EREB	OVRLN	Overline Control	5	R/W	EB	3C5
EREC	FGLAT0	Foreground Latch 0	8	R/W	EC	3C5
ERED	FGLAT1	Foreground Latch 1	8	R/W	ED	3C5
EREE	FGLAT2	Foreground Latch 2	8	R/W	EE	3C5
EREF	FGLAT3	Foreground Latch 3	8	R/W	EF	3C5
ERF3	MWCTRL	Masked Write Control	3	R/W	F3	3C5
ERF4	MWMASK	Masked Write Mask	8	R/W	F4	3C5
ERF5	FBPAT	Foreground/Background Pattern	8	R/W	F5	3C5
ERF6	RAMBANK	MB DRAM Bank	8	R/W	F6	3C5
ERF7	SWITCH	Switch Readback	8	R/W	F7	3C5
ERF8	CLKCTRL	Extended Clock Control	8	R/W	F8	3C5
ERF9	PGSEL	Extended Page Select	1	R/W	F9	3C5
ERFA	FGCOLOR	Extended Foreground Color	4	R/W	FA	3C5
ERFB	BGColor	Extended Background Color	4	R/W	FB	3C5
ERFC	COMPAT	Compatibility Control	8	R/W	FC	3C5
ERFD	TIMING	Extended Timing Select	8	R/W	FD	3C5
ERFE	FBCTRL	Foreground/Background Control	7	R/W	FE	3C5
ERFF	16BIT	16-Bit Interface Control	8	R,R/W	FF	3C5

*Duplicated VGA registers also accessible as extension registers for state save/restore

** A byte-sized I/O write decode only; no bits of this register exist. Byte writes to this register cause the switch settings on CPU data but bits 15-8 to be strobed into the Switch Readback register (Extension Register F7).

Note: The Extension registers are only accessible when they are enabled by writing EAh to the Extensions Control Register (SR6).

The Sequencer/Extensions Index register points to the Sequencer data registers and to the HT209 Extension data registers.

REV Chip Revision Register 3C5(R)

Index 8E

Bit	Description
7	Major Revision level
6	Major Revision level
5	Major Revision level
4	Major Revision level
3	Minor Revision level
2	Minor Revision level
1	Minor Revision level
0	Minor Revision level

The HT209 chip revision level is determined by reading this register. The 4 high-order bits return the value of the major revision level and the 4 low-order bits return the value of the minor revision level.

HT209 Product Family = 0 1 0 1 x x x x

REV Chip Identification Register 3C5(R)

Index 8F

Bit	Description
7	Identification bit 7
6	Identification bit 6
5	Identification bit 5
4	Identification bit 4
3	Product Family bit 3
2	Product Family bit 2
1	Product Family bit 1
0	Product Family bit 0

This register is similar to Extension register 8E except the 4 high-order bits always return 0111 (7) and the 4 low-order bits return the product family level.

HT209 Product Family = 0 1 1 1 0 0 x x

PPA Pointer Pattern Address 3C5(R/W)

Index 94

Bit	Description
7	Pointer Pattern Address bit 13
6	Pointer Pattern Address bit 12
5	Pointer Pattern Address bit 11
4	Pointer Pattern Address bit 10
3	Pointer Pattern Address bit 9
2	Pointer Pattern Address bit 8
1	Pointer Pattern Address bit 7
0	Pointer Pattern Address bit 6

This register contains the high order bits [13:6] of the graphics pointer pattern address in display memory. This register allows the user to place the 32x32 pointer pattern on any 64-byte boundary in the display memory linear address range 0C000h through 0FFFFh.
The 64Kx32 display memory address is determined as follows:

Bit	Description
17	Extension register FF bit 6
16	Extension register FF bit 5
15	1
14	1
13	Pointer Pattern Address bit 7
12	Pointer Pattern Address bit 6
11	Pointer Pattern Address bit 5
10	Pointer Pattern Address bit 4
9	Pointer Pattern Address bit 3
8	Pointer Pattern Address bit 2
7	Pointer Pattern Address bit 1
6	Pointer Pattern Address bit 0
5	Mask (0 = AND mask, 1 = XOR mask)
4	Pattern line # bit 4 (MSB)
3	Pattern line # bit 3
2	Pattern line # bit 2
1	Pattern line # bit 1
0	Pattern line # bit 0 (LSB)

The pointer is a graphics image that is displayed in a plane in front of normal video data. It does not interfere with bit map manipulation, and removes the need to preserve the pointer or the bit map while drawing.

The pointer pattern modifies 8 bits of video data that appear on output pins V[7:0]. The pointer pattern takes up 256 bytes. It allocates 64 bytes to each of the four planes that comprise the display memory address space. Its location defaults to the last 64 bytes of display memory.

The pointer pattern consists of a 128-byte AND mask followed by a 128-byte XOR mask. Each pattern consists of 32 consecutive 32-bit values which represent the 32 successive lines of the pointer pattern. An individual pointer pattern is fetched with two memory read operations (the AND mask and the XOR mask) during the two successive memory accesses immediately following refresh during horizontal non-display enable interval. For each scan line, the 32 bits of AND mask data and the 32 bits of XOR mask data provide the 32 pixel pointer information as follows: Bit 7 of plane 0 is shifted out first (for the left most pixel of the pointer), followed by bit 6 of plane 0; bit 0 of plane 3 is shifted out last.

Correspondence between the display memory address and the location of the pattern in the system memory space is determined by the values in the Graphics Controller Registers. Typically, the pointer is loaded in a mode in which display memory is mapped as four linear planes in the range A000:0000 through A000:FFFF, with the pointer pattern AND mask (in the default case) loaded at A000:FFC0 through A000:FFDF and the pointer pattern for the XOR mask loaded at A000:FFE0 through A000:FFFF. Once the pointer pattern is loaded, the sequencer always uses the contents of the Pointer Pattern Address register to construct a linear display memory address and to fetch pointer pattern data.

Truth table for mask data:

AND Mask	XOR Mask	Resulting Screen Pixel
0	0	Black
0	1	White
1	0	Same as original pixel (pointer transparent)
1	1	Inverse of original pixel

Notes:
1. The upper left corner of the 32 x 32 pixel region of the screen at which the pointer appears is controlled by Extension registers ER9C through ER9F.
2. If the pointer is positioned so that its right or bottom edge is off the screen, that part of the pointer is not seen. Such portions of the pointer are suppressed in hardware.
3. If double scanning is enabled, the pointer double scans along with other video data. Double scanning VGA mode 13h (the maximum scan line is set to 1) does not affect the cursor. The pointer pattern scan line advances each time the scan address counter counts or turns over.
4. The Pointer Pattern Address register is set to 0FFh on power-up.

PXH Pointer Horizontal Position High 3C5(R/W)

Index 9C

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Pointer Horizontal Position Bits 10
1	Pointer Horizontal Position Bits 9
0	Pointer Horizontal Position Bits 8

This register contains the 3 high-order bits of the 11-bit Pointer Horizontal Position Register. The contents of this register in conjunction with the Pointer Horizontal Position Low Register (Extension Register 9D) specify the position of the pointer in pixels from the left edge of the display screen. A value of 0 in horizontal position bits 0 -10 places the left-most pixel of the pointer pattern over the left most pixel of the display screen.

PXH Pointer Horizontal Position Low 3C5(R/W)

Index 9D

Bits	Description
7	Pointer Horizontal Position Bit 7
6	Pointer Horizontal Position Bit 6
5	Pointer Horizontal Position Bit 5
4	Pointer Horizontal Position Bit 4
3	Pointer Horizontal Position Bit 3
2	Pointer Horizontal Position Bit 2
1	Pointer Horizontal Position Bit 1
0	Pointer Horizontal Position Bit 0

This register contains the 8 low-order bits of the 11-bit Pointer Horizontal Position Register. The contents of this register in conjunction with the Pointer Horizontal Position High Register (Extension Register 9C) specify the position of the pointer in pixels from the left edge of the display screen.

PYH Pointer Vertical Position High 3C5(R/W)

Index 9E

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Pointer Vertical Position Bit 9
0	Pointer Vertical Position Bit 8

This register contains the 2 high-order bits of the 10-bit Pointer Vertical Position Register. The contents of this register in conjunction with the Pointer Vertical Position Low register (9F) specify the position of the pointer in scan lines from the upper edge of the display screen. A value of 0 in vertical position bit [0:9] places the upper most pixel of the pointer pattern over the upper most pixel of the display screen.

PYL Pointer Vertical Position Low 3C5(R/W)

Index 9F

Bit	Description
7	Pointer Vertical Position Bit 7
6	Pointer Vertical Position Bit 6
5	Pointer Vertical Position Bit 5
4	Pointer Vertical Position Bit 4
3	Pointer Vertical Position Bit 3
2	Pointer Vertical Position Bit 2
1	Pointer Vertical Position Bit 1
0	Pointer Vertical Position Bit 0

This register contains the 8 low-order bits of the 10-bit Pointer Vertical Position Register. The contents of this register in conjunction with the Pointer Vertical Position High Register (9E) specify the position of the pointer in pixels from the upper edge of the display screen. A value of 0 in vertical position bits [0:9] places the upper most pixel of the pointer pattern over the upper most pixel of the display screen.

GRL[0:3] Graphics Controller Memory Latch[0:3] 3C5(R/W)

Index A[0:3]

Bit	Description
7	Graphics Controller Memory Latch[0:3] bit
6	Graphics Controller Memory Latch[0:3] bit
5	Graphics Controller Memory Latch[0:3] bit
4	Graphics Controller Memory Latch[0:3] bit
3	Graphics Controller Memory Latch[0:3] bit
2	Graphics Controller Memory Latch[0:3] bit
1	Graphics Controller Memory Latch[0:3] bit
0	Graphics Controller Memory Latch[0:3] bit

This extended index directly accesses the display memory plane[0:3] CPU latch in the graphic controller.

CLK Extended Clock Select Register 3C5(R/W)

Index A4

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Clock Select
3	Bit 3 of Misc. Output Register
2	Bit 2 of Misc. Output Register
1	Reserved
0	Reserved

This register selects one of 8 clock sources available to the HT209 chip. Bit 2 and Bit 3 of this register provides alternate read/write access to 3C2 bits 2-3.

Selects clock sources with the Miscellaneous Output Register clock select bits (bits 2:3)

Index A4 Bit-4	MISC Output Bit-3	MISC Output Bit-2	Clock Source	Pin Name
0	0	0	25.175MHz VGA Standard	X25M
0	0	1	28.322MHz VGA Standard	X28M
0	1	0	Feature Connector	FCLK
0	1	1	0MHz VGA Standard	XRESM
1	0	0	50.35 MHz Extended	XD0M
1	0	1	65MHz Extended	XD1M
1	1	0	Feature Con. VGA Standard	FCLK
1	1	1	40MHz Extended	XD2M

CURS Cursor Attribute Register 3C5(R/W)

Index A5

Bit	Description
7	Pointer Enable
6	Reserved
5	Reserved
4	Reserved
3	Cursor Mode
2	Reserved
1	Reserved
0	Cursor Blink Disable

This register is used to enable and disable the mouse pointer.

Bit 7 Pointer Enable

0 = Disables the pointer.
1 = Enables the pointer logic to display the 32 x 32-pixel hardware mouse pointer on the screen at a location determined by the Pointer Horizontal and Vertical Position registers (ER9C-ER9F).

Note: Refer to the Pointer Pattern Address Register in the Extension Registers for an explanation of how this bit functions.

Bit 3 Cursor Mode

0 = The text cursor replaces the pixels at the position of the cursor.
1 = The text cursor is XORed with the pixels at the position of the cursor.

Bit 0 Cursor Blink Disable

0 = The text cursor blinks normally.
(Refer to CR0A, CR0B, CR0E, CR0F, and AR10, bit3)
1 = The text cursor is always on and does not blink.

SCRAM Scratch RAM 3C5 (R/W)

Index B3

Bit	Description
7	Scratch RAM Bit 7
6	Scratch RAM Bit 6
5	Scratch RAM Bit 5
4	Scratch RAM Bit 4
3	Scratch RAM Bit 3
2	Scratch RAM Bit 2
1	Scratch RAM Bit 1
0	Scratch RAM Bit 0

This 8-bit register is a storage byte, which is typically used by the BIOS to store miscellaneous information.

MNLCK Monochrome Lock Register 3C5(R/W)

Index C0

Bit	Description
7	Monochrome Lock Bit 7
6	Monochrome Lock Bit 6
5	Monochrome Lock Bit 5
4	Monochrome Lock Bit 4
3	Monochrome Lock Bit 3
2	Monochrome Lock Bit 2
1	Monochrome Lock Bit 1
0	Monochrome Lock Bit 0

This register is used to lock the VGA when it is in monochrome emulation mode. To arm this register, write a 9h to 3C5 Index C0. To lock the VGA, write an 18h to 3C5 Index C0. Once armed, any other register read or write an 18h to 3C5 will disarm this mode. Once the HT209 is locked in monochrome mode, one or two conditions can unlock it: Power on RESET or if the DISABLE pin is strobed.

MSCRTRLII Miscellaneous Control Register II 3C5(R\W)

Index C8

Bit	Description
7	Extended RAS Mode Enable
6	Extended Linear Address Enable
5	Reserved
4	Word DAC I/O Enable
3	True 9 Dot Text Enable
2	Reserved
1	Reserved
0	Reserved

This register provides control for 9 Dot Text, Word DAC I/O, Extended Linear Address Enable, Extended RAS Mode Enable.

Bit 7 Extended RAS Mode Enable

0 = XRAD pin enabled
1 = If bit 4 of Extension register FF (16-Bit Interface Control)is a 1, then the XRAD pin of the HT209 chip drives RAS to the upper 256K bank of memory in a board populated with 512K of RAM.

Bit 6 Extended Linear Address Enable

0 = Disables 1MB linear address mode.
1 = Enables 1MB linear address mode. This bit samples the "VASPACE" pin to determine if a valid 1MB address range is being accessed. Address pins A[19:4] are used to linearly access the display memory with this 1MB space.

Bit 4 Word DAC I/O Enable

0 = Disables word access to the RAMDAC.
1 = The HT209 chip will perform all the necessary byte steering that enables the RAMDAC to be accessed as a word device. To set this bit, Port 106 bit 1 must be a 1 and the RAMDAC must be tied to the upper 8 bits of a 16-bit bus.

Bit 3 True 9-Dot Text Enable

0 = Normal 8-dot text.
1 = Chains text-mode font information contained in planes 2 and 3 together to form a 9-dot or 16-dot font.

HOFL Horizontal Overflow Register 3C5(R/W)

Index CA

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Interlace (SRE1) bit 7
3	Horizontal Sync Start (CR4) bit 8
2	Horizontal Block start (CR2) bit 8
1	Horizontal Display End (CR1) bit 8
0	Horizontal Total (CR00) bit 8

If the Hercules Bit Map is enabled (ERE0 bit 1 = 1), this register provides the necessary one bit extensions to the Horizontal Timing Registers.

Bit 4 Interlace (SRE1) bit 7

Bit 3 Horizontal Sync Start (CR4) bit 8

Bit 2 Horizontal Block start (CR2) bit 8

Bit 1 Horizontal Display End (CR1) bit 8

Bit 0 Horizontal Total (CR00) bit 8

MISCTRLI Miscellaneous Control I 3C5(R/W)

Index E0

Bit	Description
7	Split Bank Address Enable
6	Allow Access to 3B9
5	Divide Character Clock by 2
4	Word Access Enable
3	128K Linear Bit Map
2	Add Byte Offset
1	Hercules Bit Map Enable
0	Interlace Enable

This register provides miscellaneous control for Interlace Enable, Hercules Bit Map Enable, Byte Offset, 128K Linear Bit Map, Word Access Enable, Half Character Clock, Access to 3B9 and Split Bank Enable.

Bit 7 Split Bank Address Enable

0 = Disable Split Bank address mode.
1 = Enable Split Bank address mode. In this mode, Extension Register E8 provides an offset when addressing the lower 32K of the selected display memory address space (typically A000-AFFF in graphics modes). Extension Register E9 provides an offset when addressing the upper 32K of the selected display memory address space.

Bit 6 Allow Access to Port 3B9

0 = Disable Port 3B9 access
1 = Port 3B9 is accessed as the Mono Mode Color Register

Bit 5 Enable Horizontal Overflow Register

0 = Disable the Horizontal Overflow register (ERCA).
1 = Enable the Horizontal Overflow register (ERCA).

Bit 4 Word Access Enable

0 = True word access disabled.
1 = Enables true word access to display memory under the following conditions:

During memory writes:
Odd/Even mode (SR4 bit 2 = 0)
OR
Chain 4 mode (SR4 bit 4 = 1)
AND
Write modes 0 or 1 (GR5 bit 1 = 0)
AND
Data Rotate (GR3 bits 2-0 = 0)

During memory reads:
Odd/Even mode (GR4 bit 4 = 1)
OR
Chain 4 mode (SR4 bit 4 = 1)

Bit 3 128K Linear Bit Map

0 = No 128K linear bit map.
1 = Allows a 128K linear bit map from A0000 - BFFFF in planar modes.

Bit 2 Add Byte Offset

1 = Add a one to the address offset

Bit 1 Hercules Bit Map Enable

0 = Disables 64K linear bit map.
1 = Enables a 64K linear bit map at B0000 if Extension Register FE bit 7 = 1.

Bit 0 Interlace Enable

0 = Disables the CRTC interlace mode.
1 = Enables the CRTC interlace mode.

INTLC Interlace Value 3C5(R/W)

Index E1

Bit	Description
7	Nibble Offset
6	Character Offset 6
5	Character Offset 5
4	Character Offset 4
3	Character Offset 3
2	Character Offset 2
1	Character Offset 1
0	Character Offset 0

This register is used to fine tune interlaced video modes.

Bit 7 Nibble Offset

Bits 6-0 Character Offset

These bits are used to "fine tune" the interlaced video modes. In most cases these bits should be set to:

Horizontal Blanking Start (CR2) - (Horizontal Total(CR0)+5)/2)

TRAPCTL Trap Control Register 3C5(R/W)

Index E2)

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Trap on: 3C4, 3C5 Index C8, 3C5 Index C9
3	Trap on:3D8/3BF/3D8/3D9/3DE
2	Trap on:3B4/5 or 3D4/5
1	Trap on:3C6-3C9
0	Trap on:3C0/2, 3C3,3CE/F, 3C4/5, 3xA

This register is used to strobe the TRAP pins on the HT209 chip when certain port addresses are written to.

Bit 4 Trap on: 3C4, 3C5 Index C8, 3C5 Index C9

This address range is used to facilitate enabling/disabling the extended linear address mode (see Extended Register C8 bit 6).

1 = The TRAP pin will strobe low when the above ports are written to.

Bit 3 Trap on: 3B8, 3BF, 3D8, 3D9, 3DE

1 = The Trap pin will strobe low when the above ports are written to.

Bit 2 Trap on: 3B4/5, or 3D4/5

1 = The TRAP pin will strobe low when the addresses 3B4/5 (monochrome mode) or 3D4/5 (color mode) are written to.

Bit 1 Trap on: 3C6-3C9

1 = The TRAP pin will strobe low when the above ports are written to.

Bit 0 Trap on: 3C0/2, 3C3, 3CE/F, 3C4/5, 3xA

1 = The TRAP pin will strobe low when ports 3C0/2, 3C3, 3CE/F, 3C4/5 and 3xA are written to.

WRTPRTC Write Protect Control 3C5(R/W)

Index E3

Bit	Description
7	Reserved
6	Reserved
5	Write Protect 3C0 Index 11
4	Write Protect 3C5 Indexes C8, C9
3	Write Protect:3D8/3BF or 3D8/3D9
2	Write Protect:3B4/5 or 3D4/5
1	Write Protect:3C6-3C9
0	Write Protect:3C0/2, 3C3, 3CE/F, 3C4/5, or 3BA/3DA

This register is used to Write Protect selected registers.

Bit 5 Write Protect: 3C0 Index 11

1 = Contents of the Overscan Color register (AR11) cannot be changed.

Bit 4 Write Protect: 3C5 Indexes C8 and C9

1 = The Miscellaneous Control 2 register (ERC8) and the Extended Linear Address Offset register (ERC9) cannot be changed.

Bit 3 Write Protect:3B8, 3BF, 3D8, 3D9

1 = Contents of the registers 3B8/3BF or 3D8/3D9 cannot be changed. These registers are used for MDA/CGA emulation.

Bit 2 Write Protect: 3B4/5, 3D4/5

1 = Write protect all CRT Controller registers.

Bit 1 Write Protect: 3C6-3C9

1 = Write protect all RAMDAC registers.

Bit 0 Write Protect: 3C0/2, 3C3, 3CE/F, 3C4/5, 3xA

1 = Write protect all Attribute Controller, Graphics Controller, Sequencer and Feature Port Registers. The Extension Control Register (SR6) and Headland specific Extension Registers are not write protected.

LWRSPLT Lower Split Bank 3C5(R/W)

Index E8

Bit	Description
7	CPU Bank Select 1
6	CPU Bank Select 0
5	Page Select (MISC5)
4	Extended Page Select
3	4K Start Address 3
2	4K Start Address 2
1	4K Start Address 1
0	4K Start Address 0

This register is used to split lower memory bank.

Bits 7-6	CPU Bank Select
Bit 5	Page Select
Bit 4	Extended Page Select
Bit 3-0	4K Start Address

UPRSPLT Upper Split Bank 3C5(R/W)

Index E9

Bit	Description
7	Alternate CPU Bank Select 1
6	Alternate CPU Bank Select 0
5	Alternate Page Select (MISC5)
4	Alternate Extended Page Select
3	Alternate 4K Start Address 3
2	Alternate 4K Start Address 2
1	Alternate 4K Start Address 1
0	Alternate 4K Start Address 0

This register is used to split upper memory bank.

Bits 7-6	Alternate CPU Bank Select 0-1
Bit 5	Alternate Page Select (MISC5)
Bit 4	Alternate Extended Page Select
Bits 3-0	Alternate 4K Start Address 0-3

SWSTB Switch Strobe Register 3C5(W)

Index EA

Bits	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	Reserved

This register has no read/write bits. It is used to strobe the state of the on-board switches into the Switch Readback Register (Extension Register F7). If written to with any data value, the state of data bus bits[15:8] are written into this register. Data bus bits [15:8] are typically connected to on-board switches. During the write to this register, the bus data buffer for bits[15:8] are disabled so that the state of the switches determines the state of the data pins connected to the HT209 chip.

The Switch Strobe Register is nothing more than an I/O decode, and is decoded only on I/O writes; the value written into this register is ignored.

This register may be written at any time, but is usually done only once at BIOS initialization to determine the initial state of various power-up configuration options.

This register is only accessible when access to the HT209 extensions registers is enabled by writing 0EAh to SR6.

OVRLN Overline 3C5(R/W)

Index EB

Bits	Description
7	Reserved
6	Reserved
5	Reserved
4	Overline bit 4
3	Overline bit 3
2	Overline bit 2
1	Overline bit 1
0	Overline bit 0

This register controls the position of the Overline attribute when in IBM 3270 emulation mode.

FGLAT[0:3] Foreground Latch Registers[0:3] 3C5(R/W)

Index EC-EF

Bit	Description
7	Foreground Latch Bits 7
6	Foreground Latch Bits 6
5	Foreground Latch Bits 5
4	Foreground Latch Bits 4
3	Foreground Latch Bits 3
2	Foreground Latch Bits 2
1	Foreground Latch Bits 1
0	Foreground Latch Bits 0

These registers provide the CPU-side ALU input bytes for planes [0:3] Extension Register FE3 = 1 and 2 = 0.

These registers are only accessible when access to the HT209 extension registers is enabled by writing 0EAh to SR6.

MWCTRL Masked Write Control Register 3C5(R/W)

Index F3

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Masked Write Source
0	Masked Write Enable

This register enables masked writes to VRAMs and controls the source of the mask.

Bit
Description

Bit 1 — Masked Write Source
This bit selects the source of the Masked Write Register:

0 = The Masked Write Mask register (Extension Register F4) provides the mask.
1 = The rotated CPU byte provides the Masked Write mask.

Bit 0 — Masked Write Enable
This bit allows selected bits of a memory byte to be modified without first reading the byte. The 8-bit mask is applied equally to each of the four bytes going to the four planes.

0 = Masked Write operation is disabled.
1 = Masked Write operation is enabled.

MWMASK Masked Write Mask 3C5(R/W)

Index F4

Bit	Description
7	Masked Write Mask Bit 7
6	Masked Write Mask Bit 6
5	Masked Write Mask Bit 5
4	Masked Write Mask Bit 4
3	Masked Write Mask Bit 3
2	Masked Write Mask Bit 2
1	Masked Write Mask Bit 1
0	Masked Write Mask Bit 0

The Masked Write Mask Register provides the byte used to mask off bits in each plane during masked writes to VRAM. This register is significant only when Extension Register F3 bit 0 = 1.

For each bit of either the Masked Write register (if Extension Register F3, bit 1 = 0) or the rotated CPU byte (if Extension Register F3, bit 1 = 1) that is 0, the corresponding bit in each byte of display memory is unchanged. For each bit of the Masked Write Register or the rotated CPU byte that is 1, the corresponding bit in display memory bytes is replaced with the data written by the processor.

FBPAT Foreground/ Background Pattern 3C5(R/W)

Index F5

Bit	Description
7	Foreground/Background Pattern bit 7
6	Foreground/Background Pattern bit 6
5	Foreground/Background Pattern bit 5
4	Foreground/Background Pattern bit 4
3	Foreground/Background Pattern bit 3
2	Foreground/Background Pattern bit 2
1	Foreground/Background Pattern bit 1
0	Foreground/Background Pattern bit 0

This register is the source of the 8-bit pattern used in Solid Foreground/Background Mode. This register is active when bits 3 and 2 of the Foreground/Background Control Register (Extension Register FE) are 0 and 1, respectively.

This register is only accessible when access to the Extension Registers is enabled.

RAMBANK 1MB DRAM Bank Select 3C5(R/W)

Index F6

Bit	Description
7	Line Compare Bank Reset
6	Counter Bank Enable
5	CRTC Read Bank Select [1:0]
4	CRTC Read Bank Select [1:0]
3	CPU Read Bank Select [1:0]
2	CPU Read Bank Select [1:0]
1	CPU Write Bank Select [1:0]
0	CPU Write Bank Select [1:0]

This register is used to control bank selection in 1MB RAM chip configurations. The contents of this register are automatically invoked when 1MB RAMs are attached.

This register also supports independent selection of 256K banks in 1MB RAMs where CPU reads, writes, and CRTC reads occur. Bit-map sparring banks are also supported. Up to four virtual VGAs or high-resolution modes can be supported when four banks of 256K DRAMs or VRAMs are attached and Extension Register FF = 1.

Note: Bit-maps can span across 256K boundaries when using 1MB RAMs.

Bit 7 Line Compare Bank Reset
This bit allows the split-screen Line Compare to either reset to the beginning of RAM bank 0 or to the start of the current bank.

0 = Bits 17 and 16 of the memory address counter are loaded from bits 5 and 4 of Extension Register F6. The line compare can now reset to the beginning of bank 0 of 1MB DRAMs or to the start of the current bank.
1 = Bits 17 and 16 of the memory address counter are reset to 0.

Bit 6 Counter Bank Enable

0 = Memory address bits 17 and 16 are accessed by 1MB DRAMs bits 5 and 4 of Extension Register F6. This bit enables display memory scanning to cross bank boundaries or wrap back to the start of the current bank.
1 = Memory address bits 17 and 16 are accessed by 1MB DRAMs or used to generate the one of four bank select output by memory address counter bits 17 and 16.

Note: In a font fetch, memory address bits 17 and 16 are always accessed from bits 5 and 4 of Extension Register F6. In text mode, Bit 6 should be set to 0.

Bits [5:4] CRTC Read Bank Select

These bits select one of four 256K banks that the CRT Controller uses to read video data from display memory

Bits [3:2] CPU Read Bank Select

These bits select one of four 256K banks the CPU uses to write display memory.

Bits [1:0] CPU Write Bank Select

These bits select one of four 256K banks the CPU uses to write to display memory.

SWITCH Switch Readback Register 3C5(R/W)

Index F7

Bit	Description
7	Switch Readback 7
6	Switch Readback 6
5	Switch Readback 5
4	Switch Readback 4
3	Switch Readback 3
2	Switch Readback 2
1	Switch Readback 1
0	Switch Readback 0

The Switch Readback register is used to determine the state of up to 8 dip switches connected to CPU data line bits [15:8]. When a byte (8-bit) OUT is written to the Switch Strobe register (Extension Register EA), the buffer controlling the CPU data lines [15:8] is disabled. These 8 lines are loaded into the Switch Readback register at any time. The Switch Readback register can also be written to at Extension Register F7.

CLKCTRL Extended Clock Control 3C5(R/W)

Index F8

Bit	Description
7	Extended Clock Output 2
6	Extended Clock Output 1
5	Extended Clock Output 0
4	Clock 3 On
3	External Clock Override
2	Extended Clock Output Source
1	Extended Clock Direction
0	Clock 0 Only

This register controls the multiplexing of clock inputs, and the direction and placement of data on the three high-order extended clock pins.

Note: Synchronous reset must be in effect when this register is written to or display memory may be randomly altered.

Bits [7:5] Extended Clock Output

The value written into this field will be output on pins XD2M, XD1M, and XD0M of the HT209 chip. For this to occur, pins XD2M, XD1M, and XD0M must be made outputs by setting the Extended Clock Direction bit and the Extended Clock Output Source bit of this register to a 1. When the Extended Clock Direction bit is 0, then clock select bits 2-0 (bit 4 of extension register A4 and bits [3:2] of 3C2 are placed on the XD2M, XD1M and XD0M pins.

Bit 4 Clock 3 On

If Miscellaneous Output Register (3C2h) bit 3 = 1 and bit 2 = 1:

0 = The clock selected is forced to ground.
1 = Whatever clock input is selected by the Extended Clock Select Register and bits [2:0] of the Extended Clock Control Register is active.

Bit 3 External Clock Override

If Miscellaneous Output Register 3C2h bit 3 = 1 and bit 2 = 0:

0 = The External Clock input is selected regardless of the mode selected by the Extended Clock Select Register and bits 2-0 of the Extended Clock Control Register.

1 = The clock input selected by the Extended Clock Select Register and bits 2-0 of the Extended Clock Control Register is active.

Bit 2 Extended Clock Output Source

When bit 1 of this register is 1, the XD2M, XD1M, and XD0M pins become outputs and this bit selects the data to be placed on those pins.

0 = The XD pins output the following signals:
XD2M = Clock Select Register (ERA4) bit 4
XD1M = Miscellaneous Output Register (MISC) bit 3
XD0M = Miscellaneous Output Register (MISC) bit 2

1 = The Extended Clock Output bits of this register (bits 7-5) are output on pins XD2M, XD1M, and XD0M, respectively.

Note: When the Extended Clock Direction is 0, the Extended Clock Output bits have no effect.

Bit 1 Extended Clock Direction
0 = Clock select bits 2-0 (A4 bit 4 and 3C2h bits 3-2) are placed on the XD2M, XD1M and XD0M pin. The XD2M, XD1M, and XD0M pins become inputs. These clock inputs can be selected as the current clock driving the HT209 via clock select bits 2-0, as described in the discussion of Extension Register A4 and I/O Port 3C2h.

1 = When bit 2 of this register is 1, then the Extended Clock Output bits (bits 7-5 of this register) are placed on the XD2M, XD1M, and XD0M pins.

Bit 0 Clock 0 Only

0 = The clock select bits 4, 3, and 1 of this register determine which clock drives the HT209.
1 = The X25M pin selects the CPU clock that allows an external dot clock generator chip to be attached to the X25M pin, with the clock select bits going out on XD2M-XD0M to program the generator. To an application program, it will still appear as if several crystals are attached to the various clock pins as the program sets 3C2h bit 3-2.

Note: This bit can be overridden by two conditions controlled by this register. These overrides provide full IBM VGA compatibility with a single external clock generator attached to X25M and driven by the clock select bits via XD2M, XD1M, and XD0M. If bit 4 of this register is 0, and 3C2h bit 3=1 and bit 2=1. the clock input to the HT209 is grounded (no clock). If the bit 3 of this register is 0 and 3C2h bit 3 = 1 and bit 2 = 0 then the clock input to the HT209 comes from the FCLK pin.

Note: Up to 11 different clocks can be selected by using the XD2M-XD0M pins as outputs to a clock generator chip, allowing the selection of eight different frequencies. The remaining three clocks are input on the X28M, FCLK, and XRESM pins.

PGSEL Page Select 3C5(R/W)

Index F9

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Reserved
2	Reserved
1	Reserved
0	Extended Page Select

The Extended Page Select bit is used to support the extended 256 color modes, by mapping display memory into a 64K CPU address space.

Bit 0 Page Select

If this bit is a 1 and:

Extended 256-Color Enable (Extension Register FC bit 2) = 1
Chain 4 (SR4 bit 3) = 1
Extended 256-Color Mode (Extension Register FC bit 1) = 0

then the Extended Page Select bit is placed on address bit 0 during CPU accesses. If any of the above conditions are not true, this bit has no effect.

FGCOLOR Extended Foreground Color 3C5(R/W)

Index FA

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Foreground Color Bit 3
2	Foreground Color Bit 2
1	Foreground Color Bit 1
0	Foreground Color Bit 0

This register provides the foreground color used in the Solid Foreground/Background mode, which is active when bits 3 and 2 of the Foreground/Background Control Register (Extension Register FE) are 0 and 1, respectively. See Extension Register FE for additional details.

BGCOLOR Extended Background Color Register 3C5(R/W)

Index FB

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Reserved
3	Foreground Color Bit 3
2	Foreground Color Bit 2
1	Foreground Color Bit 1
0	Foreground Color Bit 0

This register provides the background color used in the Solid Foreground/Background mode, which is active when bits 3 and 2 of the Foreground/Background Control Register (Extension Register FE) are 0 and 1, respectively. See Extension Register FE for additional details.

When the above condition is false, the Extended Background Color Register has no effect.

COMPAT Compatibility Control 3C5(R/W)

Index FC

Bit	Description
7	Internal 3C3 Enable
6	Extended Display Enable
5	Sequential Chain
4	Refresh Skew Control
3	Sequential Chain 4
2	Extended 256 Color Enable
1	Extended 256 Color Mode
0	Extended Attribute Enable

This register enables enhanced 256 color graphics modes, enhanced attributes in text mode, refresh and extended display enable skews, and masked VRAM writes.

Bit 7 Internal 3C3 Enable (ARMVSE)

0 = (DISABLE Pin = 1, 3C3h bit 0 has no effect) All I/O and memory addressing is disabled.
1 = (DISABLE Pin = 1, 3C3h bit 0 = 1) All I/O and memory addressing is enabled (DISABLE Pin = 1, 3C3h bit 0 = 0) Memory addressing is disabled, I/O addressing is enabled.

Note: When the DISABLE Pin is 0, all I/O and memory addressing is disabled.

Bit 6 Extended Display Enable Skew

0 = No affect on Display Enable Skew.
1 = The Display Enable Skew is 1 greater than the skew selected by bits 6 and 5 of the Horizontal Blanking End Register (CR3).

Bit 5 Sequential Chain 4

This bit is used to support high-resolution doubleword modes, such as 256-color modes, with VRAMs, to work with 1:2 or 1:4 interleave. The Sequential Chain bit is insignificant when the Chain 4 bit SR4 bit 3 = 0.

0 = Chain 4 mode operates as described under bit 3 of the Memory Mode Register (SR4) and bit 1 of GR6.
1 = Chain 4 bit-maps are stored at consecutive display memory addresses where they can be scanned in byte mode.

Note: This bit has no effect when the Chain 4 bit (bit 3 of SR4) is 0.

For a full description of substitution in chain 4 and sequential chain 4 modes, refer to the discussion GR6 bit 1.

Bit 4 — Sequential Chain

This bit is used to support high-resolution doubleword modes, such as 256-color modes, with V-RAMs, which are not capable of working in word or doubleword mode with 1:2 or 1:4 interleave.

0 = Chain mode operates as described under bit 1 of GR6.
1 = The nature of Chain mode (SR4.3=0 and GR6.1=1) changes. Instead of routing CPU address bits A[15:2] to internal linear address bits SA[15:2], they are routed to SA[13:0]. A[1:0] are routed to SA[15:14]. Chain bit maps can now be stored at consecutive display memory addresses, where they can be scanned in byte mode.

For a full description of substitution bits in chain and sequential modes, refer to the discussion under GR6.1.

Note: This bit has no effect when the Chain 4 bit (bit 3 of SR4) is 1 or the Chain bit (bit 1 of GR6) is 0.

Bit 3 — Refresh Skew Control

This bit allows the proper refresh in modes that use Display Enable Skew. The IBM VGA starts refresh immediately after display enable end, causing problems in modes that use display enable skewed such as shift 4 and shift load modes. This bit controls whether the start of refresh occurs one character after the end of the skewed display enable signal or one character after the end of the unskewed display enable signal.

0 = Refresh starts one character after the end of the skewed Display Enable signal.
1 = Refresh occurs one character after the end of the unskewed Display Enable signal. The skew is controlled by bits 6 and 5 of CR3.

Bit 2 — Extended 256-Color Enable

This bit enables or disables the enhanced 256-color mode selected by bit 1 of this register.

0 = The standard IBM 256-color CPU address multiplexing is in effect whenever the Chain 4 bit (bit 3 of SR4) is set to 1. The standard IBM 256-color CRTC address multiplexing is in effect whenever the Doubleword Mode bit (bit 6 of CR14) is 1.
1 = The enhanced 256-color mode is in effect for CPU addressing whenever the Chain 4 bit (bit 3 of SR4) is 1 and enhanced CRTC 256-color mode (memory address counter bit 15 is placed on linear address bit 1 and memory address counter bit 14 is placed on linear address bit 0) is in effect for CRTC addressing whenever the CR14 bit 6 = 1.

Bit 1 Extended 256-Color Mode

This bit selects the type of extended 256-color CPU addressing mode that is in effect when the Extended 256-Color Enable bit (bit 2 of this register) is 1 and when the Chain 4 bit (bit 3 of SR4) is 1. The extended modes support 256-color bit maps larger than 64K, supporting resolutions of 320 x 400 and 640 x 400.

0 = 64K extended 256-Color Mode . In this mode, if the Chain 4 bit is 1, then during CPU reads and writes, CPU address bits 15 through 2 are placed on linear address bits 15 through 2, the Miscellaneous Output Register (3C2h) bit 1 is placed on linear address bit 1, and the Extended Page Select bit (bit 3 of this register) is placed on linear address bit 0.

1 = Selects 128K Extended 256-Color Mode. If the SR4.3=1, CPU address bits 15 through 2 are placed on linear address bits 15 through 2, the non-inverted Page Select bit is placed on linear address bit 1, and CPU address bit 16 is placed on linear address bit 0.

NOTE: When SR4.3=0, the selected extended 256-color mode has no effect on CPU addressing. The extended 256 color modes substitutes new CPU and CRTC address multiplexing in place of IBMs default 256 color multiplexing.

Bit 0 Extended Attribute Enable

0 = Extended text attributes are disabled, and the extended attribute byte has no effect. This is the IBM VGA compatible mode of operation.

1 = Extended text attributes are enabled. The extended attribute contains the following options:
Bit 7 = Underline
Bit 6 = Reverse Video
Bit 5 = Overline (See Extension Register EB)
Bit 4 = Blink
Bit 3 = Alternate Palette
Bits [2:0] = Font Select

TIMING Extended Timing Select 3C5(R/W)

Index FD

Bit	Description
7	Graphics Timing Select bit 3
6	Graphics Timing Select bit 2
5	Graphics Timing Select bit 1
4	Graphics Timing Select bit 0
3	Text Timing Select bit 3
2	Text Timing Select bit 2
1	Text Timing Select bit 1
0	Text Timing Select bit 0

The Extended Timing Select Register controls the timing mode in text and graphics 8-dot sequencer modes of operation.

Note: 1. In 9-dot mode (SR1.0=0), this register is ignored and a 1:4 timing state is selected. The 1:4 timing is the only one supported in text and graphics 9-dot mode. This state supports maximum dot clocks of 33 MHz with 120ns RAMs and 40 MHz with 100ns RAMs.

2. If field is changed during timing state selection, synchronous reset must be set, or display memory may be randomly altered.

Bits[7:4] Graphics 8-Dot Timing Select

8-dot graphics mode is selected when SR1.0=0 and GR6.0=1. See table below:

Timing state selection in 8-dot graphics mode

				Max Dot Clock (MHz)			
Bits[7:4]	RAM Type	Timing State	Interleave	80ns	100ns	120ns	150ns
0	DRAM	8-dot Graphics	1:4	45	35	29	20
1	DRAM	invalid	none	n/a	n/a	n/a	n/a
2	DRAM	8-dot Graphics	1:2	38	30	25	18
3	DRAM	8-dot Graphics	Paged 1:4	65	50	41	29
4	DRAM	8-dot Graphics	1:4	n/a	n/a	n/a	n/a
5-7	DRAM	invalid	none	n/a	n/a	n/a	n/a

Note: 1. In paged 1:4 interleave, 4 paged accesses by the CRTC are performed per CPU access. Panning and virtual screen sizes are incompletely supported, since the start address can vary only by multiples of 4 and the Offset register can vary only by multiples of 2.

2. The 8-dot 1:4 VRAM and 8-dot Paged 1:4 DRAM graphics timing states do not fully support byte panning (not all offset and start address settings work properly).

Bits[3:0] Text 8-Dot Timing Select

8-dot text mode is selected when SR1 bit 0 = 1 and of GR6.0=0. See table below:

				Max Dot Clock(MHz)			
Bits[7:4]	RAM Type	Timing State	Interleave	80ns	100ns	120ns	150ns
0	DRAM	8-dot Text	1:4	45	35	29	20
1	DRAM	invalid	none	n/a	n/a	n/a	n/a
2	DRAM	8-dot Text	1:2	38	30	25	18
3	DRAM	8-dot Text	1:4	n/a	n/a	n/a	n/a
4-7	DRAM	invalid	none	n/a	n/a	n/a	n/a

FBCTRL Foreground/Background Control Register 3C5(R/W)

Index FE

Bit	Description
7	Emulation Enable
6	Internal Emulation
5	Palette Select
4	Arm Write Protect Enable
3	Foreground/Background Mode 1
2	Foreground/Background Mode 0
1	Foreground/Background Source
0	Reserved

This Foreground/Background Control Register selects between three modes of foreground/background operation. It also selects the use of the output from the set/reset circuitry, and the data source for one foreground/background mode.

Bit 7 Emulation Enable

Bit 6 Internal Emulation

Bit 5 Palette Select

Bit 4 Arm Write Protect Enable

Bits 3-2 Foreground/Background Mode

These bits generate a solid foreground against a solid background with a single write by expanding a binary (monochrome) pattern to a color pattern. A byte is placed into the foreground/background select circuitry. Bit 1 of the byte selects the foreground color stored in Extension Register FA and bit 0 selects the background color stored in Extension Register FB. This byte becomes the CPU-side input to each planes ALU. The source of the selection byte in this mode is the Foreground/Background Pattern Register (Extension Register F5) if FE bit 1 = 0, and is the rotated CPU byte if FE bit 1 = 1.

CPU-Side ALU Input Settings and Modes

Bit 3	Bit 2	Mode of CPU-Side ALU Input Operation
0	0	Black
0	1	White
1	0	Same as original pixel (pointer transparent)
1	1	Inverse of original pixel

In dithered foreground mode, the foreground latch byte for each plane (from extension registers EC-EF) is input directly to that plane's CPU-side ALU input. This mode supports fully dithered foreground patterns optionally stored in the normal latches and the two combined via the bit mask.

Bit 1 Foreground/Background Source

0 = The Foreground/Background Pattern Register is the source
1 = The rotated CPU byte is the source

In solid Foreground/Background mode (bit 3 = 0 and Bit 2 = 1), the 8-bit pattern used to select the foreground color in Extension Register FA or the background color in Extension Register FB can use the Foreground/Background Pattern Register (Extension Register F5) or the rotated CPU byte as its source.

16 BIT 16-Bit Interface Control 3C5(R/W)

Index FF

Bit	Description
7	16-Bit Bus Status
6	Pointer Bank Select[0:1]
5	Pointer Bank Select[0:1]
4	256K Bank Enable
3	16-Bit ROM Interface Enable
2	Fast Write Enable
1	16-Bit I/O Interface Enable
0	16-Bit Memory Interface Enable

This register is used to control 16-bit options in HT209 chips and associated components to the system bus. Internally, HT209 is an 8-bit device (because VGA is inherently an 8-bit device), but present a 16-bit interface to the system. The 16-bit accesses are broken into two 8 bit accesses internally to save wait states and can eliminate wait states inserted while performing 8-bit bus emulation.

Bit 7 16-Bit Bus Status

0 = The HT209 is installed in an 8-bit bus
1 = The HT209 is installed in a 16-bit bus

Bits [6:5] Pointer Bank Select

These bits provide linear address bits 17 and 16 used when addressing the pointer pattern. These bits select 1MB DRAMs or one of up to four banks of 256K each depending on how bit 4 of this register is set.

Bit 4 256K Bank Enable

This bit enables the HT209 to operate with up to four banks of 256K display memory attached.

0 = RAS pins[3:0] operate in non-banked modes, and 256K/4 bank support is disabled. Four banks within 1 M DRAMs are supported (via the XRAD pin).
1 = RAS is generated on one of the four pins RAS*[0:3] for the one of the four 256K banks selected by Extension Register F6 (During refresh, all four lines are driven.) Additional controls are provided for VRAM banks on SOE*[0:2], SCLK*, and DTOE* pins. 1M DRAMs are not supported.

Bit 3 — 16-Bit ROM Interface Enable

HT209 chips always accept ROM decodes on the XRDN* pin and generate the appropriate buffer enables.

0 = HT209 generates an enable for the lower byte of the data bus (for an 8-bit bus).
1 = HT209 generates MEM16* when ROM decode occurs, and generates the appropriate buffer enables based on SHBE* and A0.

Bit 2 — FastWrite Enable

This bit provides the equivalent of zero-wait state latency for CPU writes. This bit has no effect on CPU reads.

0 = The CPU is held until the current display memory write is completed.
1 = The address and data are latched internally on CPU writes and the CPU is released immediately. The display memory write is completed whenever a CPU access becomes available. If the CPU attempts to access display memory again before a pending write is completed, the CPU is waited.

Bit 1 — 16-Bit I/O Interface Enable

This bit determines if the i/o interface is an 8 or 16 bit

0 = The I/O interface is 8 bits
1 = The I/O interface is 16 bits

Bit 0 — 16-Bit Memory Interface Enable

This bit determines if the memory interface is 8 or 16 bits

0 = The memory interface is 8 bits
1 = The memory interface is 16 bits

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DRAM Performance - Max Dot Clock Frequency

DRAM Access Time	Paged 1:4 8-dot 4/16/ 256-color Graphics	1:4 8-dot 4/16/ 256-color Graphics	1:2 8-dot 4/16/ 256-color Graphics	Paged 1:4 8-dot 16-color Text	1:4 8-dot 16-color Text	1:4 9-dot 16-color Text	1:2 9-dot 16-color Text	1:2 8-dot 16-color Text
80ns	64MHz	45MHz	38MHz	65MHz	50MHz	45MHz	45MHz	38MHz
100ns	50MHz	35MHz	30MHz	50MHz	40MHz	37.5MHz	35MHz	30MHz
120ns	40MHz	28MHz	25MHz	40MHz	33MHz	33MHz	28MHz	25MHz

Note:To use paged 1:4 mode, the horizontal resolution (in8-dot characters) must be divisible by 4
Note: Horizontal panning cannot be done in paged 1:4 mode
Note:The effective video rate using the special 1:4 256-color mode is double the frequency shown above

VRAM Performance - Max Dot Clock Frequency

VRAM Access Time	1:4 8-dot 4/16/256-color Graphics	1:2 8-dot 4/16/256-color Graphics	1:1 8-dot 4/16/256-color Graphics	1:4 8-dot 16-color Text
80ns	-	60MHz	30MHz	65MHz
100ns	80MHz	50MHz	25MHz	50MHz

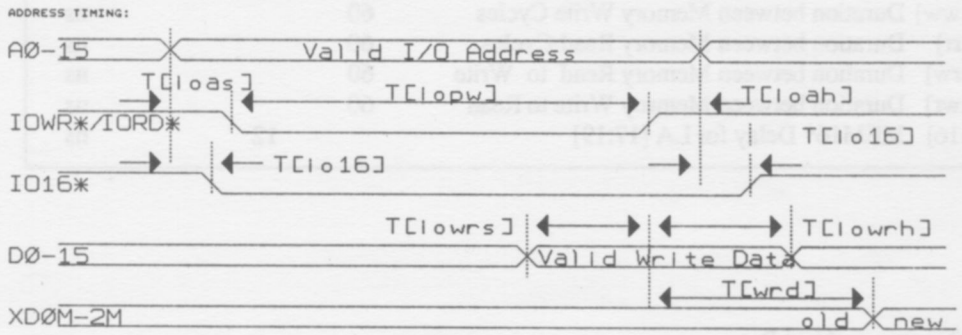
Note: All DRAM modes may also be used with VRAMs (for 9-dot text, DRAM modes must be used as there is no 9-dot VRAM text mode available)

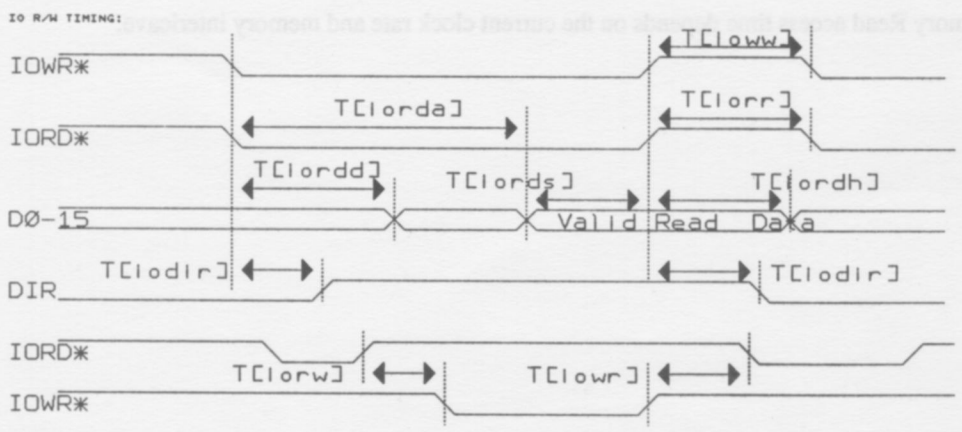
RAM Performance - Allowable Timing

RAM Access Time	Maximum Dot Clock Frequency	DRAM 256-color Graphics	DRAM 16-color Graphics	DRAM 9-dot Text	DRAM 8-dot Text	VRAM 256-color Graphics	VRAM 16-color Graphics	VRAM 8-dot Text
80ns	38MHz	1:2	1:2	1:2	1:2	1:1	1:1	1:4
	45MHz	1:4	1:4	1:2	1:4	1:1	1:1	1:4
	50MHz	Paged 1:4	Paged 1:4	1:4	Paged 1:4	1:1	1:1	1:4
	65MHz	Paged 1:4	Paged 1:4	none	Paged 1:4	1:2	1:2	1:4
100ns	30MHz	1:2	1:2	1:2	1:2	1:1	1:1	1:4
	35MHz	1:4	1:4	1:2	1:4	1:1	1:1	1:4
	40MHz	Paged 1:4	Paged 1:4	1:4	Paged 1:4	1:1	1:1	1:4
	50MHz	Paged 1:4	Paged 1:4	none	Paged 1:4	1:2	1:2	1:4
	65MHz	none	none	none	none	1:2	1:2	none
120ns	25MHz	1:2	1:2	1:2	1:2			
	28MHz	1:4	1:4	1:2	1:4			
	33MHz	Paged 1:4	Paged 1:4	1:4	Paged 1:4			
	40MHz	Paged 1:4	Paged 1:4	1:4	Paged 1:4			
	50MHz	none	none	none	none			
	65MHz	none	none	none	none			

PC/AT IO Read/Write

Symbol	Parameter	Min	Typ	Max	Units
Address Timing					
T[io16]	IO16* Delay for A[15:0]		15		ns
T[ioas]	Address Setup to IORD* or IOWR* Low	0			ns
T[ioah]	Address Hold from IOR* or IOWR* High	30			ns
T[iopw]	IORD*, IOWR* Low Pulse Width	50			ns
T[iowrs]	Data Setup to IOWR* High	50			ns
T[iowrh]	Data Hold from IOWR* High	30			ns
T[wrd]	IOWR* High to XD[2:0]M			30	ns
IO Read Write Timing					
T[iordd]	IORD* Low to Data Driven			15	ns
T[iorda]	IORD* Low to Data Valid		30	60	ns
T[iordh]	IORD* High to Data Floated			15	ns
T[iodir]	DIR Delay from IORD*		25	50	ns
T[iorr]	IORD* High to IORD* Low	60			ns
T[iorw]	IORD* High to IOWR* Low	60			ns
T[iowr]	IOWR* High to IORD* Low	60			ns
T[ioww]	IOWR* High to IOWR* Low	60			ns





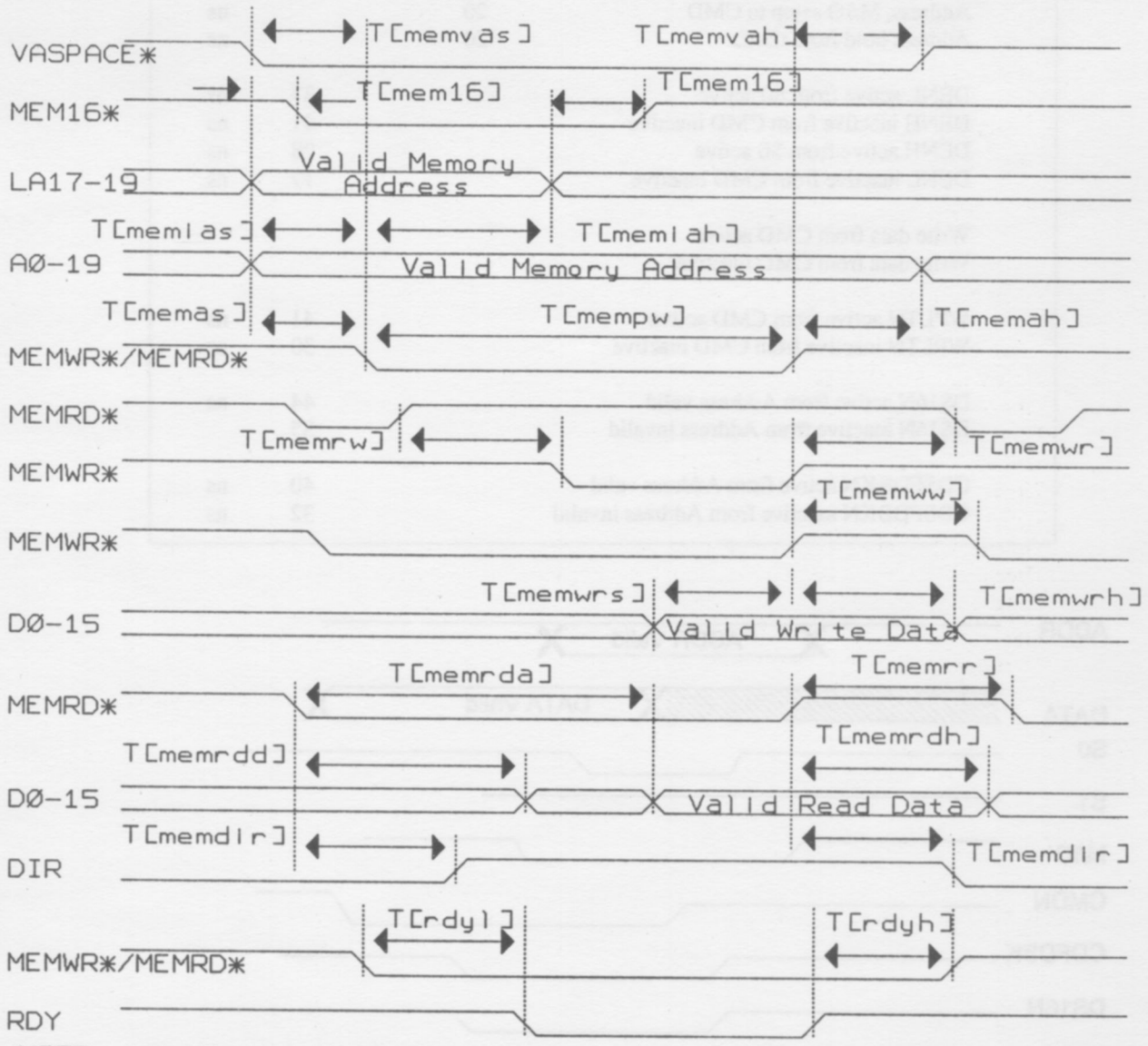
Note: Not Drawn to scale.

PC/AT Memory Read/Write

Symbol	Parameter	Min	Typ	Max	Units
Address Timing					
T[memas]	Address Setup to Memory Cycle Start	30			ns
T[memah]	Address Hold from Memory Cycle End	30			ns
T[memlas]	Address Setup to Memory Cycle Start	30			ns
T[memlah]	Address Hold from Memory Cycle Start	30			ns
T[memvas]	Address Setup to Memory Cycle Start	30			ns
T[memvah]	Address Hold from Memory Cycle End	30			ns
Memory Read & Write Timings					
T[mempw]	MEMRd*, MEMWr* Low Pulse Width	50			ns
T[memwrs]	Data Setup to MEMW* High	50			ns
T[memwrh]	Data Hold from MEMW* High	30			ns
T[memrdd]	MEMR* Low to Data Driven			15	ns
T[memrda]	MEMR* Low to Data Valid		(see note 1 below)		
T[memrdh]	MEMR* High to Data Floated			15	ns
T[mdir]	DIR Delay from MEMR*			25	ns
T[rdyl]	RDY Low from MEMR* Low			25	ns
T[rdyh]	RDY High to MEMR* High			25	ns
T[memww]	Duration between Memory Write Cycles	60			ns
T[memrr]	Duration between Memory Read Cycles	60			ns
T[memrw]	Duration between Memory Read to Write	60			ns
T[memwr]	Duration between Memroy Write to Read	60			ns
T[mem16]	MEM16* Delay for LA [17:19]		12		ns

See Timing Diagram on Next Page

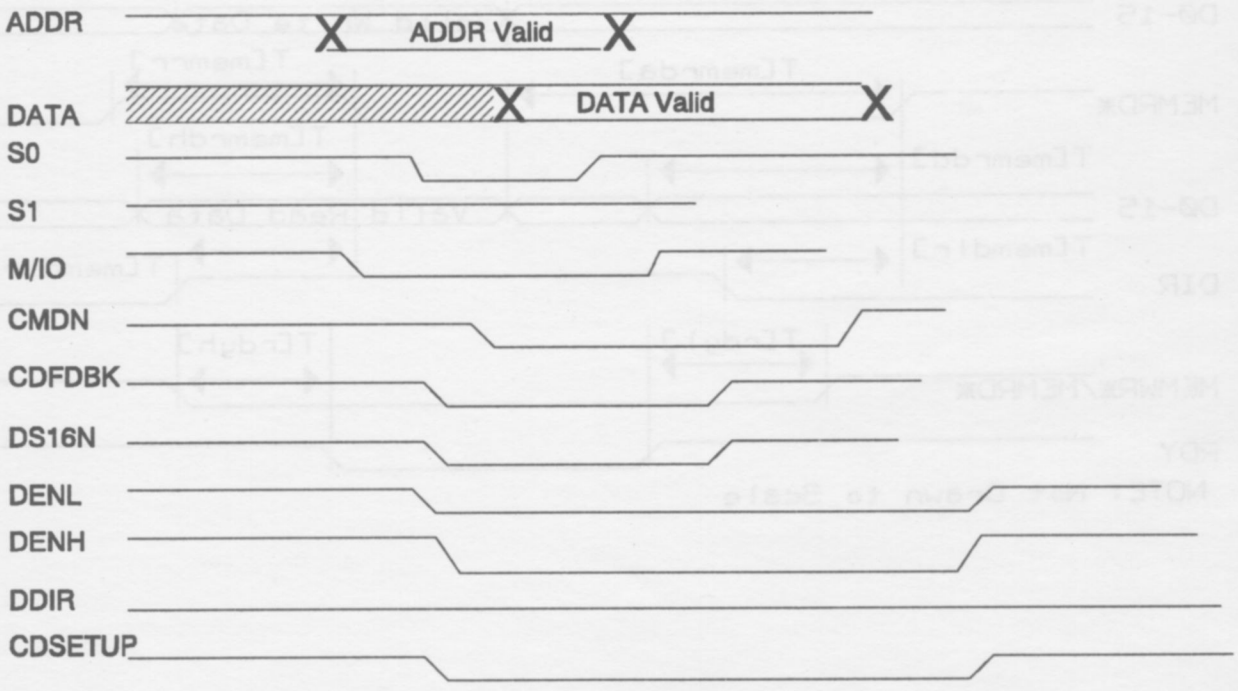
Note 1: Memory Read access time depends on the current clock rate and memory interleave.



NOTE: Not Drawn to Scale

Micro-Channel I/O Write

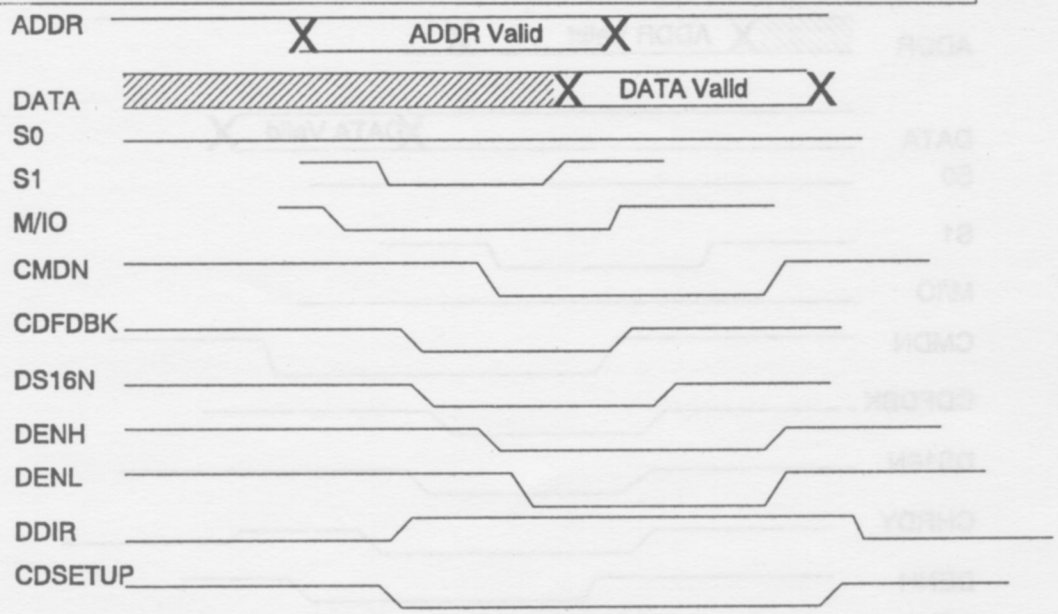
Parameter	Min	Typ	Max	Units
Address, M/IO setup to CMD	20			ns
Address hold from CMD	20			ns
DENL active from S0 active			37	ns
DENH inactive from CMD inactive			41	ns
DENH active from S0 active			28	ns
DENL inactive from CMD inactive			17	ns
Write data from CMD active				
Write data from CMD inactive				
WPLTN active from CMD active			41	ns
WPLTN inactive from CMD inactive			30	ns
DS16N active from Address valid			44	ns
DS16N inactive from Address invalid			35	
CDSFDBKN active from Address valid			40	ns
CDSFDBKN inactive from Address invalid			32	ns



* CDSETUP is for setup mode use only
* CDFDBK and DS16N will not be active during the setup mode

Micro-Channel I/O Read

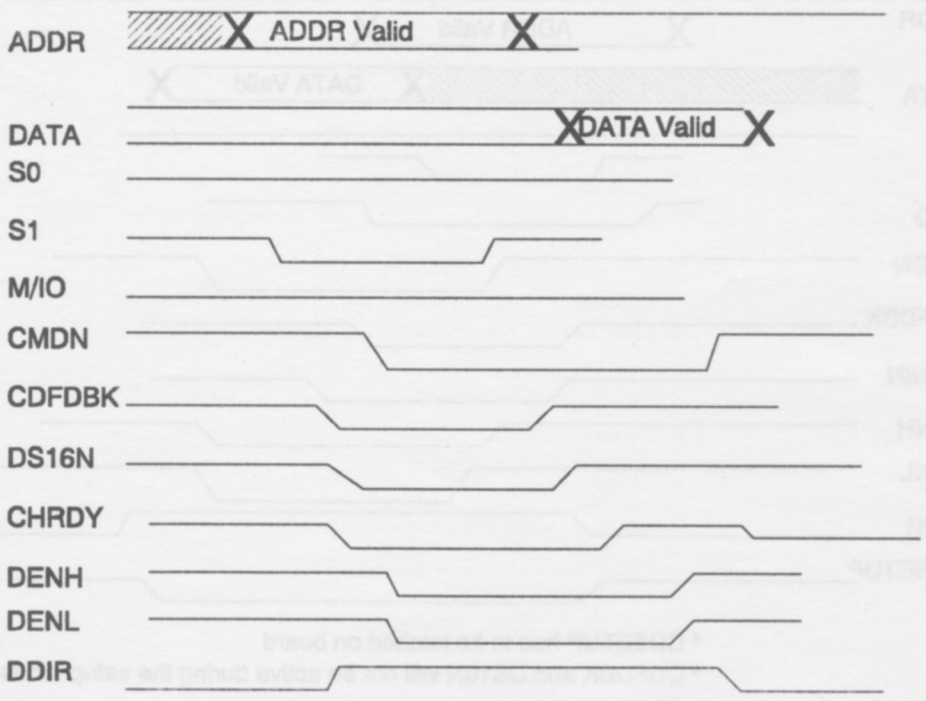
Parameter	Min	Typ	Max	Units
Address M/IO setup to CMD	20			ns
Address hold from CMD	20			ns
Read data valid from CMD active			43	ns
Read data hold from CMD inactive	8		27	ns
RPLTN active from CMD active			39	ns
RPLTN inactive from CMD inactive	8		29	ns
DDIR active from S1 active			29	ns
DDIR inactive from CMD inactive	11		37	ns
DENL active from CMD active			31	ns
DENL inactive from CMD inactive	6		20	ns
DENH active from CMD active			30	ns
DENH inactive from CMD inactive	6		20	ns
DS16N active from Address valid			63	ns
DS16N inactive from Address invalid	11		35	ns
CDSFDBKN active from Address valid			40	ns
CDSFDBKN inactive from Address invalid	9		32	ns
CMD pulsewidth			200	ns
CMD inactive to next CMD active			80	ns



* CDSETUP has to be latched on board
* CDFDBK and DS16N will not be active during the setup mode

Micro-Channel MEMRD

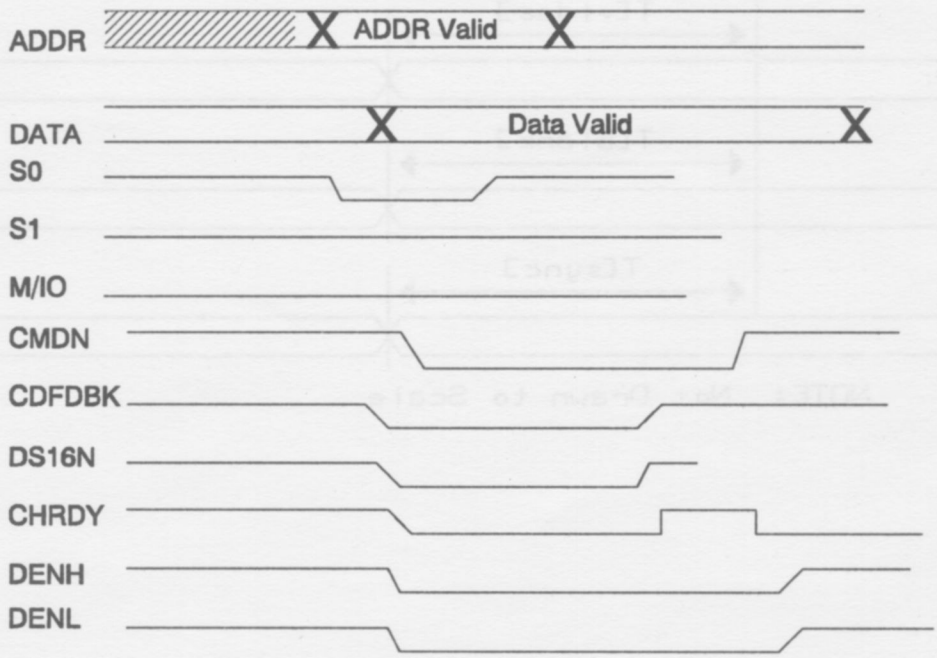
Parameter	Min	Typ	Max	Units
Address setup to CMD Active	20			ns
Address hold to CMD active	20			ns
S1 active to CMD active				
S1 and M/IO inactive from CMD				
DS16N active from Address valid			35	ns
DS16N inactive from Address invalid			26	ns
CDSFDBKN active from Address valid			32	ns
CDSFDBKN inactive from Address invalid			23	ns
RDY inactive from active status			31.3	ns
RDY active high from CMD active			2000	ns
RDY inactive (tri-state) from CMD inactive			21	ns
DENL, DENH active from CMD active			33.4	ns
DENL, DENH inactive from CMD inactive			20	ns
DDIR active from status active			30.4	ns
DDIR inactive from CMD inactive			37.2	ns
Read Data valid setup to RDY	10			ns
Read Data invalid to CMD inactive			27	ns



Micro-Channel MEMWR

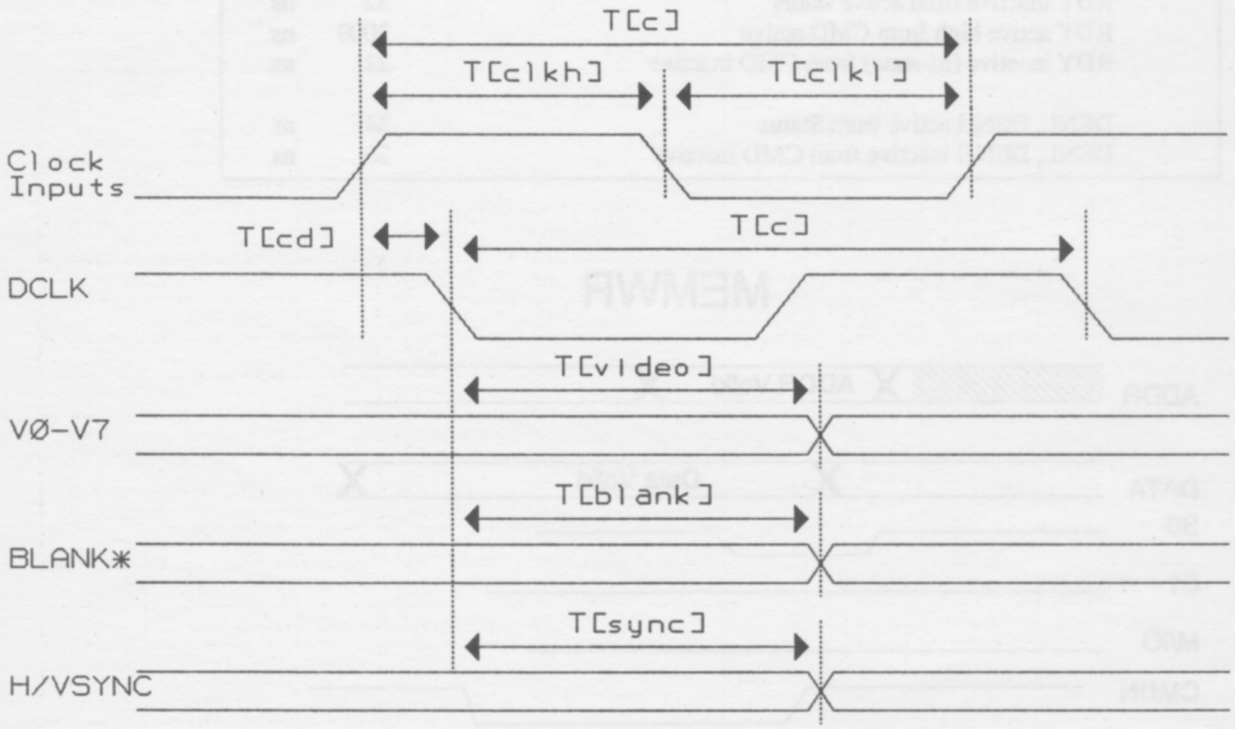
Parameter	Min	Typ	Max	Units
Address setup to CMD active	20			ns
Address hold to CMD active	20			ns
S0 active to CMD active S1 and M/IO inactive from CMD active				
DS16N active from Address valid			35	ns
DS16N inactive from Address valid			26	ns
CDSFDBKN active from Address invalid			32	ns
CDSFDBKN inactive from Address invalid			23	ns
RDY inactive from active status			32	ns
RDY active high from CMD active			2000	ns
RDY inactive (tri-state) from CMD inactive			22	ns
DENL, DENH active from Status			34	ns
DENL, DENH inactive from CMD inactive			20	ns

MEMWR



Clock and Video

Symbol	Parameter	Min	Typ	Max	Units	
T[c}	Clock Cycle	15.4			ns	(65MHz)
T[cd]	Clock to DCLK Delay		3	15	ns	
T[clkhi]	Clock High (measured at 2.0V)	[Tc/2] - 5%				
T[clkl]	Clock (measured at 2.0V)	[Tc/2] - 5%				
T[video]	Video Output Delay	1	2	4	ns	
T[blank]	Blank* Output Delay	1	2	4	ns	
T[sync]	Vsync, Hsync Output Delay	1	2	4	ns	



NOTE: Not Drawn to Scale

DC Specifications

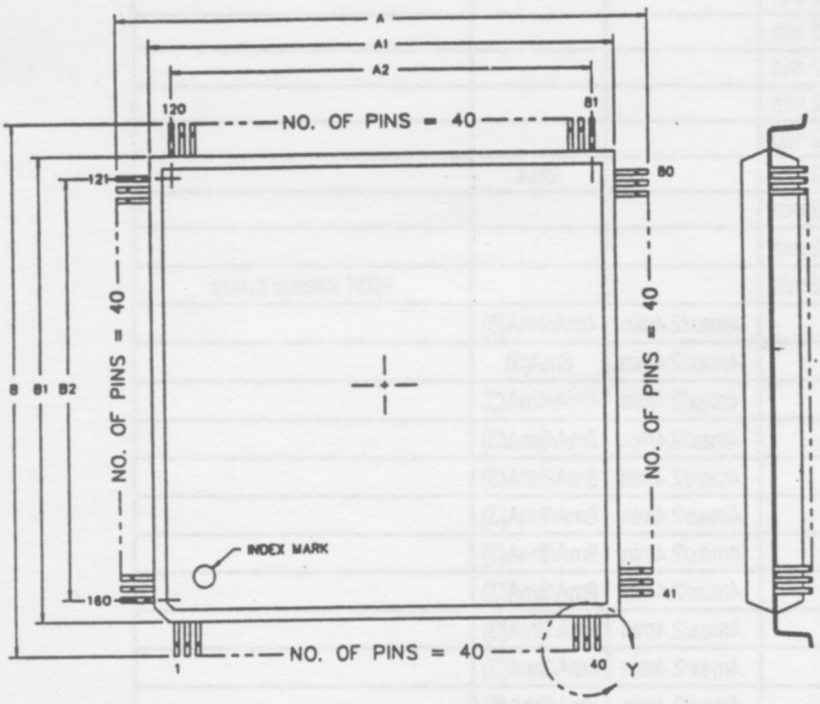
Pin Name	Pin Type	Vil/Vih	Vol/Voh	Iol/Ioh	Load Characteristics
IORD*/CMD*	Input	.8max/2 min			
IOWR*/MIO*	Input	.8max/2 min			
MEMR*/S0*, MEMW*/S1*	Input	.8max/2 min			
RFSH*,SBHE*,VASPACE	Input	.8max/2 min			
RESET,SW	Input	.8max/2 min			
DISABLE,SETUP*	Input	.8max/2 min		2mA	
LA[19:17], A[19:0]	Input	.8max/2 min			
FCLK,X25M,X28M	Input	.8max/2 min			
XRDN*/TEST*	Input	.8max/2 min			100K internal pullup
DIR_RD/TSTO	Out		.4max/2.4min	4mA/4mA(3)	
MEM16*IO16*	Out		.4max/2.4min	8mA(3)	
DENH*,DENL*,WPLT*,RPLT*	Out		.4max/2.4min	4mA/4mA(3)	
AA[7:0], AB[7:0]	Out		.4max/2.4min	8mA/8mA(3)	
XRAD/RAS3*	Out		.4max/2.4min	8mA/8mA(3)	
RAS3*/RAS2*	Out		.4max/2.4min	8mA/8mA(3)	
RAS2*/RAS1*	Out		.4max/2.4min	8mA/8mA(3)	
RAS01*/RAS0*	Out		.4max/2.4min	8mA/8mA(3)	
CAS*[3:0]	Out		.4max/2.4min	8mA/8mA(3)	
WE*	Out		.4max/2.4min	8mA/8mA(3)	
DTOE23*/SOE2*	Out		.4max/2.4min	8mA/8mA(3)	
DTOE01*/DTOE	Out		.4max/2.4min	8mA/8mA(3)	
XSOE1*	Out		.4max/2.4min	8mA/8mA(3)	
SOE01*/SOE0*	Out		.4max/2.4min	8mA/8mA(3)	
SOE23*/SOE3*	Out		.4max/2.4min	8mA/8mA(3)	
SCLK01/SCLK	Out		.4max/2.4min	8mA/8mA(3)	
V[7:0]	Out		.4max/2.4min	4mA/4mA(3)	
HSYNC,VSYNC,BLANK*,DCLK	Out		.4max/2.4min	4mA/4mA(3)	
RDACA0/SYS	In/Tri-out		.4max/2.4min	4mA/4mA(3)	100K internal pullup
TRAP*/ADL*	In/Tri-out		.4max/2.4min	4mA/4mA(3)	100K internal pullup
D[15:0]	In/Tri-out		.4max/2.4min	2mA	100K internal pullup
M0-3D[0:7]	In/Tri-out		.4max/2.4min	8mA/8mA(3)	100K internal pullup
XD2M,XD1M,XD0M	In/Tri-out	.8max/2 min	.4max/2.4min	2mA	100K internal pulldown
XRESM/B256*	In/Tri-out	.8max/2 min	.4max/2.4min	8mA(3)	100K internal pulldown
INT/INT*	Tri-out	.8max/2 min	.4max	8mA	100K internal pullup
RDY	Tri-out	.8max/2 min	.4max/2.4min	8mA/8mA	100K internal pullup
VCC		.8max/2 min			5V+/- 5%, 200-350mA max
GND		.8max/2 min			

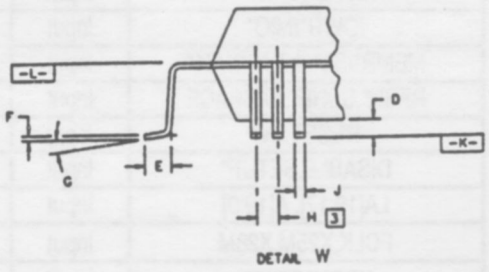
Note 1: Input capacitance = 10pF; output capacitance = 10pF; input leakage = 10uA except CCLK (100uA)

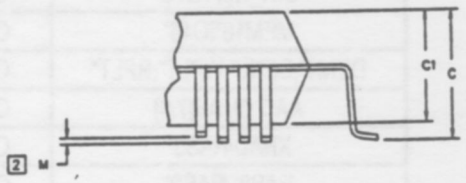
Note 2: All outputs are specified assuming 50pF load unless otherwise specified

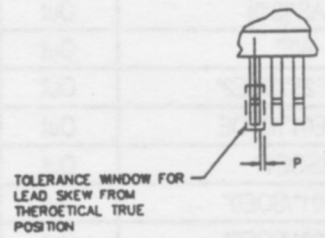
Note 3: (3) indicates outputs for which slew rate is modified to reduce FCC emissions

Package Outline









NOTES: UNLESS OTHERWISE SPECIFIED

1. NOMINAL DIMENSIONS IN MILLIMETERS. INCHES ROUNDED TO THE NEAREST .001 INCH.
2. COPLANARITY OF ALL LEADS SHALL BE WITHIN 0.1 MM (0.004") (DIFFERENCE BETWEEN HIGHEST AND LOWEST LEAD WITH SEATING PLANE -K- AS REFERENCE)
3. LEAD PITCH DETERMINED AT DATUM -L-
4. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.

[1]

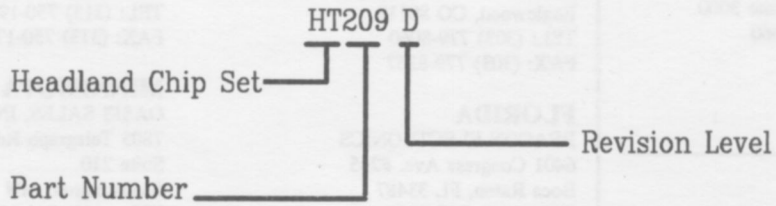
DIMENSIONS IN MM		
SYM	MINIMUM	MAXIMUM
A	31.60	32.40
A1	27.90	28.10
A2	25.35 REF	
B	31.60	32.40
B1	27.90	28.10
B2	25.35 REF	
C	3.68	4.01
C1	3.43	3.66
D	0.25	0.36
E	0.60	1.00
F	0.10	0.25
G	0°	10°
H	0.65 ±0.15	
J	0.25	0.35
M	0.10 MAX	
P	0.05 MAX	
TOTAL NO. OF PINS	160	

[1]

DIMENSIONS IN INCHES		
SYM	MINIMUM	MAXIMUM
A	1.244	1.276
A1	1.098	1.106
A2	0.998 REF	
B	1.244	1.276
B1	1.098	1.106
B2	0.998 REF	
C	0.145	0.158
C1	0.135	0.144
D	0.010	0.014
E	0.024	0.039
F	0.004	0.010
G	0°	10°
H	0.026 ±0.006	
J	0.010	0.014
M	0.004 MAX	
P	0.002 MAX	
TOTAL NO. OF PINS	160	

Product Order Information

Product Ordering Information



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