CH9201 PC Graphics Clock Generator

Features

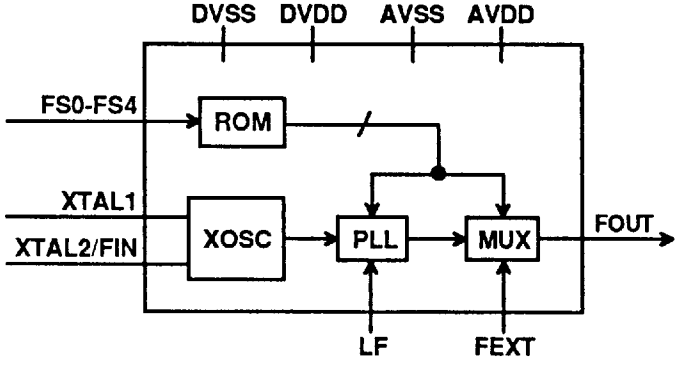
- Synthesizes 32 preset frequencies
- 5V power supply
- Requires only 3 external components: one crystal and two 0.1 µF capacitors
- Supports graphics standards such as MDA, CGA, VGA, SuperVGA, and 8514A
- Supports output frequencies up to 110 MHz
- Provision for an external frequency input
- Advanced PLL design with low phase jitter
- Internal PLL remains locked while external frequency is selected
- Backward pin compatible with CH9201 and ICS1394 (same basic pinout)
- High performance, low power CMOS technology
- Available in 20 pin plastic DIP or SOIC
- 5V and 3.3V supply

Description

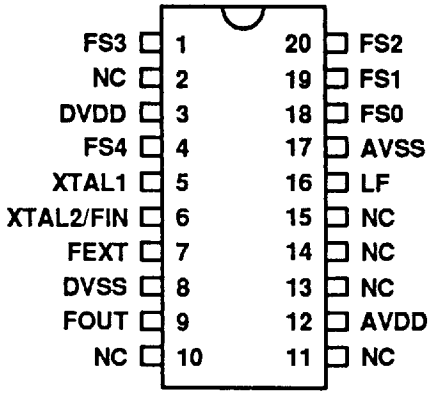
The Chrontel CH9201 is a high performance frequency synthesizer designed for use in high performance graphics systems and in applications where selection of multiple frequencies is desired. The output frequency can be selected from a set of 32 frequencies by externally setting the Frequency Select pins to ground. The CH9201 uses a 14.318 MHz reference frequency, however, other input frequencies can also be used to obtain non-standard output frequencies. Chrontel supports frequency tables required by many graphics controllers and also offers its customers the option of defining the frequency table by mask programming the internal ROM.

The CH9201 reduces system costs by replacing multiple external clock oscillators, reducing board layout space, eliminating external components, and lowering inventory costs.

The CH9201 has the capability to multiplex externally generated signal sources into the signal path. For multimedia applications, this feature allows the device to overlay text or graphics with an external VCR or frame grabber. Thus, real time images can be superimposed.



BLOCK DIAGRAM



PINOUT DIAGRAM

CH9201 Frequency Tables (Version A shown below)

FS4	FS3	FS2	FS1	FS0	FOUT (MHz)
0	0	0	0	0	25.175
0	0	0	0	1	28.322
0	0	0	1	0	40.0
0	0	0	1	1	32.514
0	0	1	0	0	50.35
0	0	1	0	1	65.0
0	0	1	1	0	38.0
0	0	1	1	1	44.9
0	1	0	0	0	25.175
0	1	0	0	1	44.9
0	1	0	1	0	50.35
0	1	0	1	1	65.0
0	1	1	0	0	40.0
0	1	1	0	1	FEXT**
0	1	1	1	0	50.35
0	1	1	1	1	80.0

FS4	FS3	FS2	FS1	FS0	FOUT (MHz)
1	0	0	0	0	25.175
1	0	0	0	1	28.322
1	0	0	1	0	32.514
1	0	0	1	1	36.0
1	0	1	0	0	40.0
1	0	1	0	1	44.9
1	0	1	1	0	50.35
1	0	1	1	1	65.0
1	1	0	0	0	25.175
1	1	0	0	1	28.322
1	1	0	1	0	32.514
1	1	0	1	1	36.0
1	1	1	0	0	40.0
1	1	1	0	1	44.9
1	1	1	1	0	50.35
1	1	1	1	1	62.0

** PLL remains locked at specified frequency.

Pin Description

Pin	Type	Symbol	Description
1, 4, 18-20	In	FS3, FS4, FS0-2	Frequency select inputs (internal pull-up)
2, 10, 11, 13, 15	—	NC	No connection
3	Power	DVDD	Digital 5V supply
5	In	XTAL1	Crystal input
6	Out/In	XTAL2 / FIN	Crystal output/external FREF input
7	In	FEXT	External frequency input (internal pull-down)
8	Power	DVSS	Digital ground
9	Out	FOUT	Synthesized frequency output
12	Power	AVDD	Analog 5V supply
14	—	NC	No connection, **MUST BE LEFT OPEN**
16	In	LF	External loop filter
17	Power	AVSS	Analog ground

Custom Frequency Option

Customers can specify up to 32 custom frequencies by mask programming the ROM. Although the frequency range of CH9201 spans from 5 MHz to 110 MHz, the output stage is able to maintain TTL levels only up to 90 MHz. At frequencies above 90 MHz, we recommend the following options:

(a) in most cases, an AC coupling circuit as shown in our application note

(b) an ECL differential line receiver that can be used to buffer the output to ECL levels.

Layout Considerations

The following layout rules should be followed for best phase-noise performance:

1. Place all power supply bypass capacitors in close proximity to their respective power pins.
2. Use a ground plane to connect DVSS, AVSS and all external component grounds. Isolate this ground plane from other circuits by connecting it to ground at the card edge.
3. Use a low inductance trace to connect AVDD, the loop filter capacitor, and the decoupling capacitor.
4. Place the loop filter capacitor and the reference crystal close to the CH9201.
5. Do not run any signal lines through the synthesizer section of the board, especially, node LF.

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	Power supply voltage with respect to Vss	−0.5 to +7.0	V
V_{IN}	Input voltage on any pins with respect to Vss	−0.5 to V_{DD}+0.5	V
T_{STOR}	Storage temperature	−55 to +150	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated under parametric values of the DC or AC Specifications below is not recommended or guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

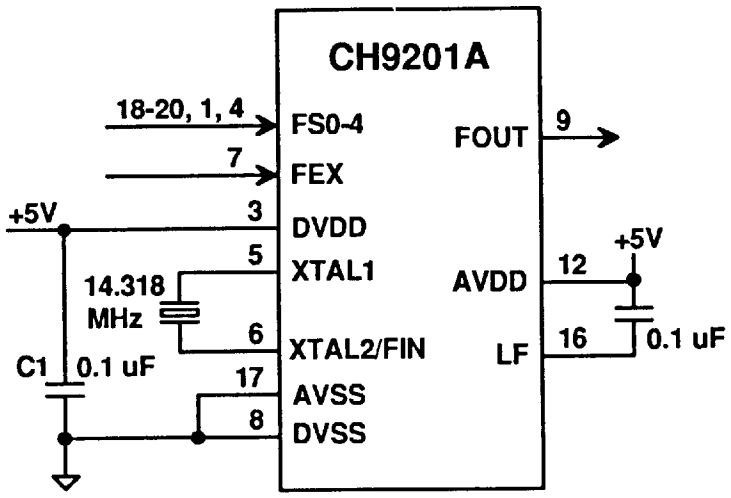
DC Specifications (T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @T_A=25°C	Min	Typ	Max	Unit
V_{OH}	Output high voltage	V_{DD}=4.75V, I_{OH}=4mA	2.4			V
V_{OL}	Output low voltage	V_{DD}=4.75V, I_{OL}=8mA			0.4	V
V_{IH}	Input high voltage		2.0			V
V_{IL}	Input low voltage				0.8	V
I_{PU}	Input pull-up current			5	20	µA
I_L	Input leakage		−10		10	µA
I_{DD}	Operating current	F_{OUT}=50MHz, V_{DD}=5.0V		20		mA

AC Specifications (T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @T_A=25°C	Min	Typ	Max	Unit
F_{IN}	Crystal/F_{REF} input		10	14.318	20	MHz
F_{OUT}	Output frequency	Synthesized output frequency	5		110	MHz *
T_R, T_F	Output clock rise/fall time	C_L=25pF, V_{OL} – V_{OH}		2		ns
T_{DC}	Output clock duty cycle	@V_{DD}/2, V_{DD}=5.0V	40	50	60	%

Note: * Output levels are guaranteed up to 90 MHz. Please consult Chrontel for suggested circuit implementations for frequencies higher than 90 MHz.



CH9201A APPLICATION SCHEMATIC

Note:

C1 should be placed in close proximity to the power pins

ORDERING INFORMATION	
Part Number	Package Type
CH9201x-NC	300 mil PDIP
CH9201x-SC	300 mil SOIC
Note: x = Frequency table version	

For the location of the sales office nearest you, contact:

Chrontel, Inc
2210 O'Toole Avenue
San Jose, CA 95131-1326
TEL: (408) 383-9328
FAX: (408) 383-9338

PDIP PACKAGES

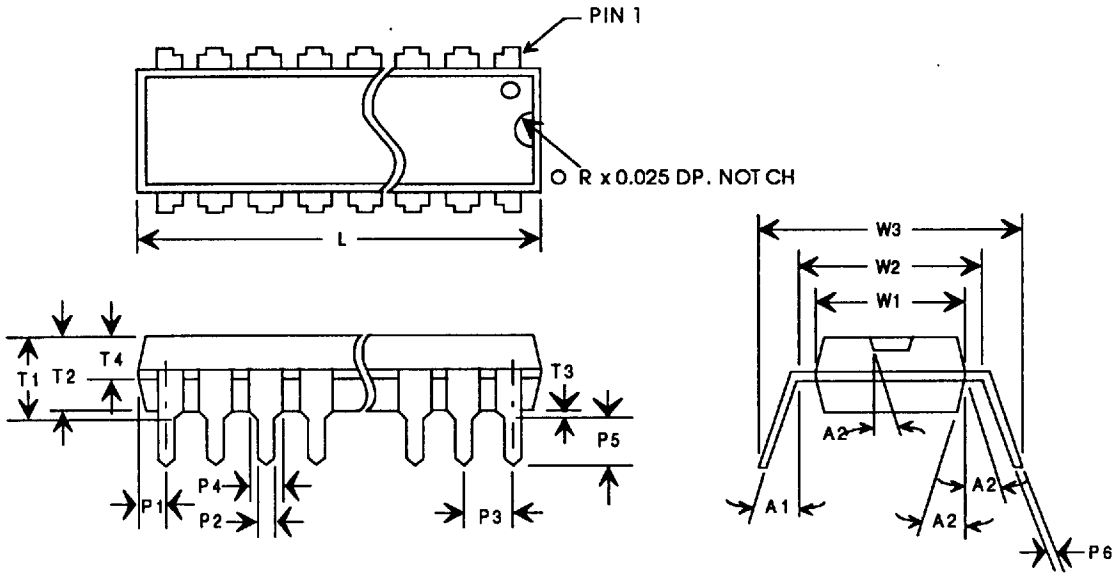


TABLE OF DIMENSIONS (INCHES, UNLESS OTHERWISE SPECIFIED)										
SYMBOL	PACKAGE VARIATION									
	8 PIN, 300 MILS		14 PIN, 300 MILS		16 PIN, 300 MILS		20 PIN, 300 MILS		32 PIN, 600 MILS	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
L	0.368	0.372	0.738	0.742	0.748	0.752	1.028	1.032	1.648	1.652
P1	0.038	0.042	0.044	0.048	0.073	0.077	0.063	0.067	0.083	0.087
P2	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020	0.016	0.020
P3	0.100 REF.		0.100 REF.		0.100 REF.		0.100 REF.		0.100 REF.	
P4	0.058	0.062	0.058	0.062	0.058	0.062	0.058	0.062	0.055	0.060
P5	0.128	0.132	0.128	0.132	0.128	0.132	0.128	0.132	0.128	0.132
P6	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
T1	0.145	0.155	0.145	0.155	0.145	0.155	0.145	0.155	0.205	0.215
T2	0.128	0.132	0.128	0.132	0.128	0.132	0.128	0.132	0.150	0.165
T3	0.010	0.020	0.010	0.020	0.010	0.020	0.010	0.020	0.010	0.020
T4	0.059	0.061	0.059	0.061	0.059	0.061	0.059	0.061	0.068	0.072
W1	0.248	0.252	0.248	0.252	0.248	0.252	0.248	0.252	0.540	0.550
W2	0.298	0.302	0.298	0.302	0.298	0.302	0.298	0.302	0.590	0.610
W3	0.335	0.355	0.335	0.355	0.335	0.355	0.335	0.355	0.635	0.655
A1	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°
A2	7° ± 1°		7° ± 1°		7° ± 1°		7° ± 1°		7° ± 1°	
R	0.031 REF.		0.031 REF.		0.031 REF.		0.031 REF.		0.062 REF.	

NOTE:
1. LEAD FRAME ALLOY 42 OR COPPER
2. LEAD FINISH SOLDER PLATED OR SOLDER DIP
3. BACK EJECTOR PIN
4. CONTROLLING DIMENSION IS IN INCHES, UNLESS OTHERWISE SPECIFIED
5. TOLERANCES: LINEAR ± 0.003, ANGLES ± 1°, RADII UNLESS NOTED ± 0.007

SOIC PACKAGES

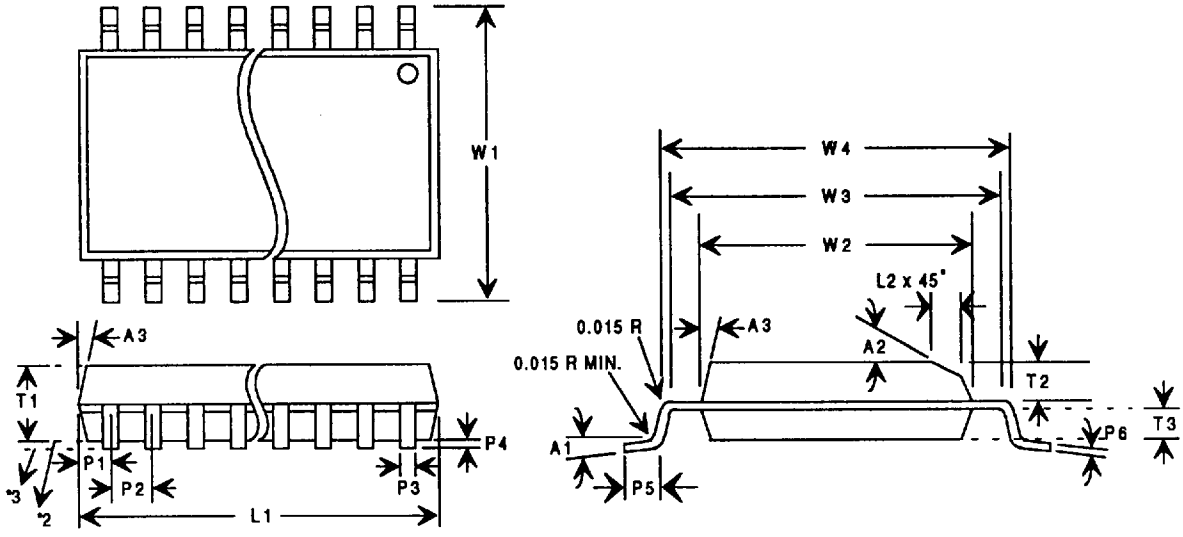


TABLE OF DIMENSIONS (INCHES, UNLESS SPECIFIED)												
SYMBOL	PACKAGE VARIATION IN 150 MILS						PACKAGE VARIATION IN 300 MILS					
	8 PIN		14 PIN		16 PIN		16 PIN		20 PIN		32 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
L1*1	0.190	0.194	0.334	0.338	0.384	0.388	0.400	0.450	0.500	0.550	0.800	0.850
L2	0.014	0.018	0.014	0.018	0.014	0.018	0.014	0.018	0.014	0.018	0.014	0.018
P1	0.020	0.022	0.017	0.019	0.017	0.019	0.022	0.032	0.022	0.032	0.022	0.032
P2	0.050		0.050		0.050		0.050		0.050		0.050	
P3	0.014	0.018	0.014	0.018	0.014	0.018	0.014	0.018	0.014	0.018	0.014	0.018
P4	0.004	0.008	0.004	0.008	0.004	0.008	0.004	0.010	0.004	0.010	0.004	0.010
P5	0.022	0.026	0.022	0.026	0.022	0.026	0.022	0.026	0.022	0.026	0.022	0.026
P6	0.009		0.009		0.009		0.009		0.009		0.009	
T1	0.054	0.058	0.054	0.058	0.054	0.058	0.090	0.094	0.090	0.094	0.090	0.094
T2	0.022	0.025	0.022	0.025	0.022	0.025	0.040	0.042	0.040	0.042	0.040	0.042
T3	0.022	0.025	0.022	0.025	0.022	0.025	0.040	0.042	0.040	0.042	0.040	0.042
W1	0.232	0.244	0.232	0.244	0.232	0.244	0.398	0.415	0.398	0.415	0.398	0.415
W2*1	0.152	0.156	0.152	0.156	0.152	0.156	0.291	0.299	0.291	0.299	0.291	0.299
W3	0.181	0.185	0.181	0.185	0.181	0.185	0.325	0.330	0.325	0.330	0.325	0.330
W4	0.190	0.194	0.190	0.194	0.190	0.194	0.330	0.334	0.330	0.334	0.330	0.334
A1	0° ± 8°		0° ± 8°		0° ± 8°		0° ± 8°		0° ± 8°		0° ± 8°	
A2	45°		45°		45°		45°		45°		45°	
A3	7° ± 1° (4X)		7° ± 1° (4X)		7° ± 1° (4X)		7° ± 1° (4X)		7° ± 1° (4X)		7° ± 1° (4X)	

NOTE:
*1. THE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
*2. REFERENCE DATUM
*3. LEAD COPLANARITY; ERROR FROM SEATING PLANE 2 MILS MAXIMUM
4. CONTROLLING DIMENSION IS IN INCHES, UNLESS OTHERWISE SPECIFIED
5. LEAD FRAME OLIN 194, LEAD FINISH: SOLDER PLATED
6. FORMED LEAD SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.004 INCH
7. TOLERANCES: LINEAR ± 0.003, ANGLES ± 1°, RADII UNLESS NOTED ± 0.007

PLCC PACKAGES

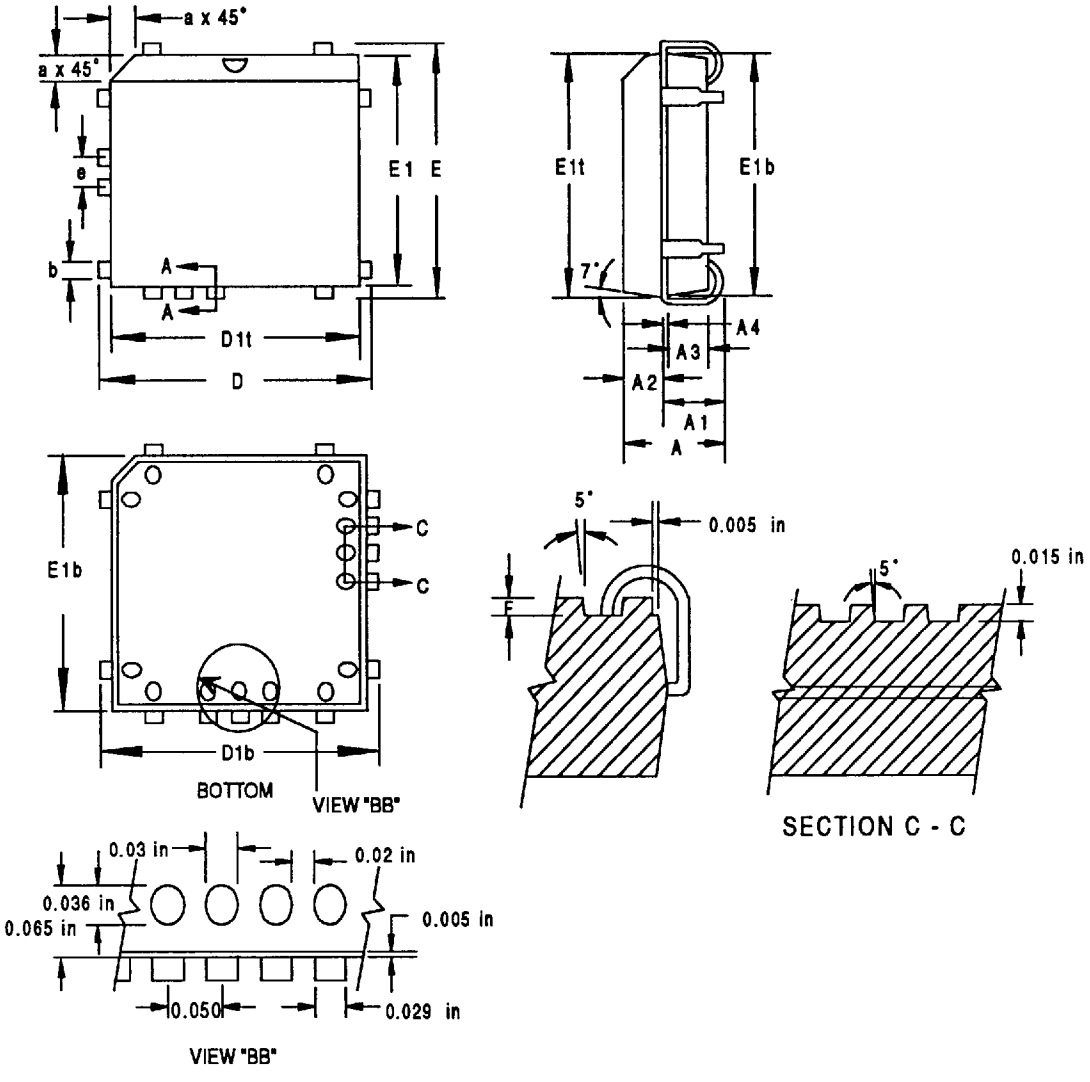


TABLE OF DIMENSIONS (INCHES, UNLESS SPECIFIED)													
SYMBOL		A	A1	A2	A3	A4	D, E	D1t, E1t	D1b, E1b	F	a	b	e
44	MIN	0.165	0.090	0.065	0.072	0.008	0.690	0.644	0.652	0.015	0.044	0.026	0.048
	MAX	0.180	0.120	0.070	0.074	0.011	0.695	0.648	0.656	0.020	0.046	0.030	0.052
68	MIN	0.165	0.090	0.065	0.072	0.008	0.990	0.944	0.652	0.015	0.044	0.026	0.048
	MAX	0.180	0.120	0.070	0.074	0.011	0.995	0.948	0.656	0.020	0.046	0.030	0.052

NOTE:
1. CONTROLLING DIMENSION IS IN INCHES, UNLESS OTHERWISE SPECIFIED
2. LEAD FRAME: Cu ALLOY 194
3. TOLERANCES: LINEAR ± 0.003, ANGLES ± 1°, RADII UNLESS NOTED ± 0.007