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- [54] **VISUAL FRAME BUFFER ARCHITECTURE**
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Related U.S. Application Data

- [63] Continuation of Ser. No. 275,644, Jul. 15, 1994, abandoned, which is a continuation of Ser. No. 870,564, Apr. 17, 1992, abandoned.
- [51] **Int. Cl.⁶** **G06F 12/00**
- [52] **U.S. Cl.** **395/164; 395/162; 345/185; 345/201**
- [58] **Field of Search** 395/162-166, 395/153, 168, 135, 157; 345/185, 189, 190, 196, 200, 201, 120, 119; 365/230.01, 230.03, 230.05, 230.09, 189.01, 189.04, 189.12

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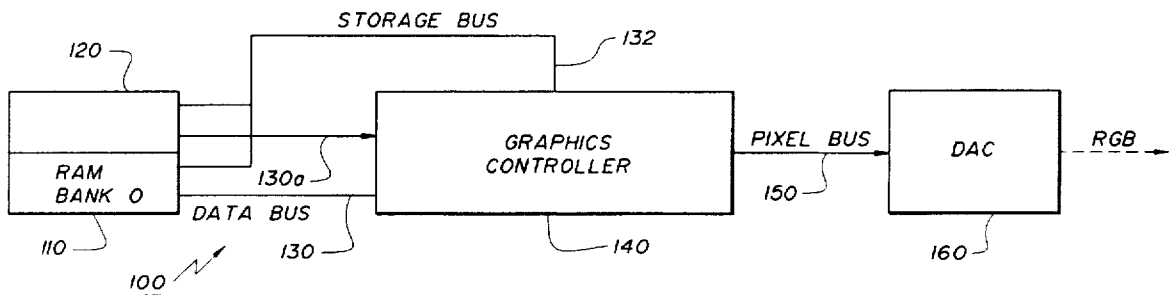
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[57] ABSTRACT

A graphics controller concurrently reads two streams of visual data stored in memory, where one of the streams is in a subsampled data format. The graphics controller upsamples the subsampled visual data and merges the two data streams to generate a merged pixel stream for display. One data stream may be graphics data in an 8-bit CLUT format and the other data stream may be video data in an 8-bit YUV format. The graphics controller may apply chromakeying to generate the merged pixel stream.

56 Claims, 1 Drawing Sheet



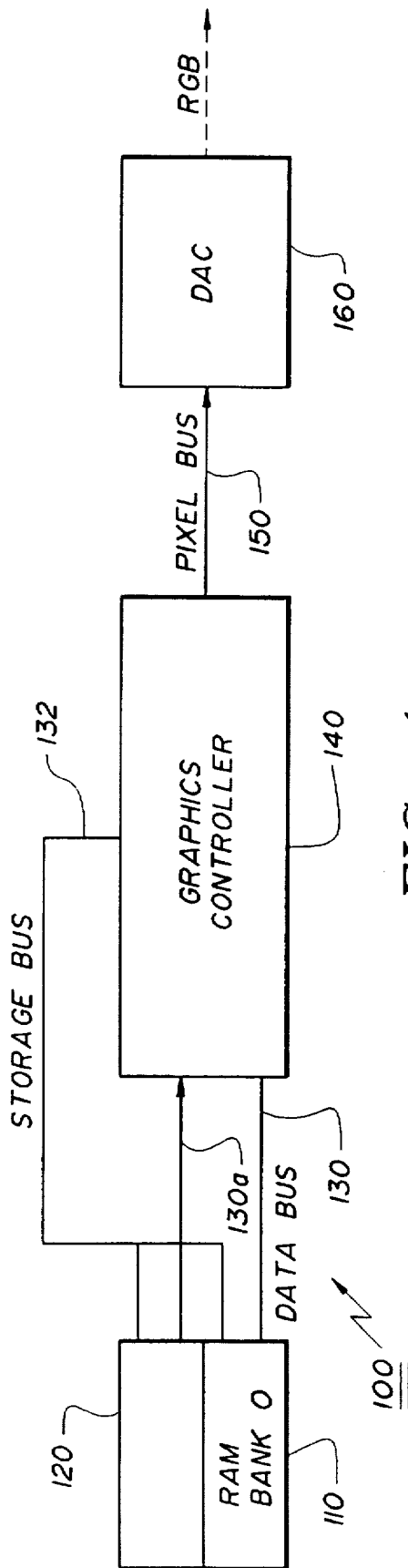


FIG. 1

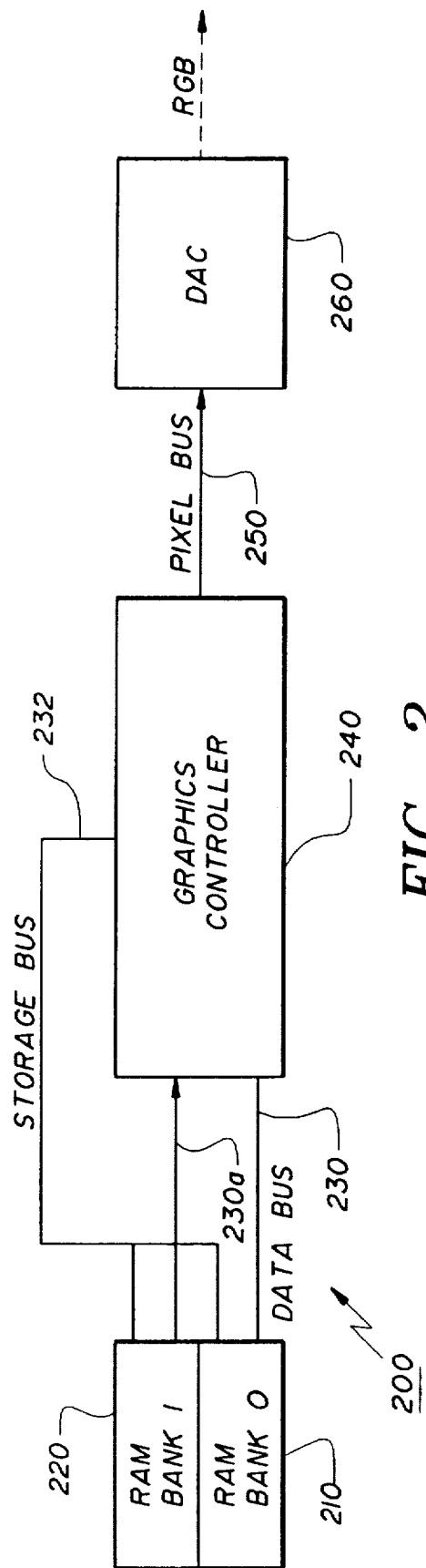


FIG. 2

VISUAL FRAME BUFFER ARCHITECTURE

This is a continuation of U.S. patent application Ser. No. 08/275,644, filed Jul. 15, 1994, now abandoned which is a file wrapper continuation of U.S. patent application Ser. No. 07/870,564, filed Apr. 17, 1992, now abandoned.

FIELD OF THE INVENTION

This invention relates to video signal processing generally and particularly to systems for providing a digital signal representative of video and graphics information.

BACKGROUND OF THE INVENTION

The goal of attaining an integrated video/graphics system (Integrated Visual Architecture) requires a system architect to balance often conflicting requirements of video subsystems and graphics subsystems. For example, while increasing horizontal and vertical resolution is beneficial to graphics images, in digital video subsystems increasing horizontal and vertical resolution can actually be detrimental to the overall image quality. Likewise, in graphics subsystems, the pixel depth, i.e. the number of simultaneous colors available, is not as important as it is for video systems. While it may be hard to justify the additional system cost of 16 bit, near-true-color pixels for the graphics system, a video system can arguably make use of deeper 24 bit pixels.

The performance budget of a video processor in a digital video subsystem during playback is divided and used to perform two tasks: creating the video image from a compressed data stream and copying/scaling the image to the display buffer. The performance budget of the video subsystem must be balanced between the copy/scale operation and the video decompression operation. Both operations must get performed thirty times a second for smooth, natural motion video. The division of the performance budget is usually done to worse case which results in an allocation of sufficient performance for a full screen motion video copy/scale operation with the remaining performance being dedicated to the video decompression operation. If the number of pixels (and/or bytes) that have to be written in the copy/scale operation are increased, the performance of the video decompression necessarily decreases. In ever increasing resolutions, for a given level of video technology, a point will be reached where the video image starts to degrade because the information content in the decompressed image is too low. Increasing the resolution beyond this point would be analogous to playing back a poor copy of a VHS tape on the most expensive, highest-quality TV available; the TV would reproduce the low-quality images perfectly.

Several formats have been presented for storing pixel data in a video subsystem. One approach is to simply have 24 bits of RGB information per pixel. This approach yields the maximum color space required for video at the expense of three bytes per pixel. Depending on the number of pixels in the video subsystem, the copy/scale operation could be overburdened.

A second approach is a compromise of the 24 bit system and is based on 16 bits of RGB information per pixel. Such systems have less bytes for the copy/scale operation but also have less color depth. Additionally, since the intensity and color information are encoded equally in the R, G and B components of the pixel, the approach does not take advantage of the human eye's sensitivity to intensity and insensitivity to color saturation. Other 16 bit systems have been

proposed that encode the pixels in a YUV format such as 6, 5, 5 and 8, 4, 4. Although somewhat better than 16 bit RGB, the 16 bit YUV format does not come close to the performance of 24 bit systems.

The 8 bit CLUT provides a third approach. This method uses 8 bits per pixel as an index into a color map that typically has 24 bits of color space as the entry. This approach has the advantages of low byte count and 24 bit color space. However, since there are only 256 colors available on the screen, image quality suffers. Techniques that use adjacent pixels to "create" other colors have been demonstrated to have excellent image quality, even for still images. However, this dithering technique often requires complicated algorithms and "custom" palette entries in the DAC as well as almost exclusive use of the CLUT. The overhead of running the dithering algorithm must be added to the copy/scale operation.

One approach for storing pixel data in a video subsystem has been to represent the intensity information with more bits than is used to represent the color saturation information. The color information is subsampled in memory and interpolated up to 24 bits per pixel by the display controller as the information is being displayed. This technique has the advantage of full color space while maintaining a low number of bits per pixel. All of the pixel depth/density tradeoffs are made in the color saturation domain where the effects are less noticeable. Several variations of this method exist and have been implemented in a display processor from Intel. In the Intel system, pixel depths typically range from 4.5 to 32 bits per pixel.

Motion video on the Intel system is displayed in a 4:1:1 format called the "9 bit format". The 4:1:1 means there are 4 Y samples horizontally for each UV sample and 4 Y samples vertically for each UV sample. If each sample is 8 bits then a 4x4 block of pixels uses 18 bytes of information or 9 bits per pixel. Although image quality is quite good for motion video the 9 bit format may be deemed unacceptable for display of high-quality stills. In addition, it was found that the 9 bit format does not integrate well with graphics subsystems. Other variations of the YUV subsampled approach include an 8 bit format.

As noted above, the requirements for a graphics system include high horizontal and vertical resolution with shallow pixels. A graphics system in which the display was 1280x1024 with 8 bit clut pixels would likely meet the needs of all but the most demanding applications. In contrast, the requirements for the video system include the ability to generate 24 bit true color pixels with a minimum of bytes in the display buffer. A video system in which the display was 640x512x8 bit (YUV interpolated to 24 bits and upsampled to 1280x1024) would also meet the needs of most applications.

Systems integrating a graphics subsystem display buffer with a video subsystem display buffer generally fall into two categories. The two types of approaches are known as Single Frame Buffer Architectures and Dual Frame Buffer Architectures.

The Single Frame Buffer Architecture (SFBA) is the most straight forward approach and consists of a single graphics controller, a single DAC and a single frame buffer. In its simplest form, the SFBA has each pixel on the display represented by bits in the display buffer that are consistent in their format regardless of the meaning of the pixel on the display. In other words, graphics pixels and video pixels are indistinguishable in the frame buffer RAM. The SFBA graphics/video subsystem, i.e. the SFBA visual system, does

not address the requirements of the video subsystem very well. Full screen motion video on the SFBA visual system requires updating every pixel in the display buffer (30 times a second) which is most likely on the order of 1280×1024 by 8 bits. Even without the burden of writing over 30M Bytes per second to the display buffer, it has been established that 8 bit video by itself does not provide the required video quality. This means the SFBA system can either move up to 16 bits per pixel or implement the 8 bit YUV subsampled technique. Since 16 bits per pixel will yield over 60M Bytes per second into the frame buffer, it is clearly an unacceptable alternative.

A visual system must be able to mix video and graphics together on a display which requires the display to show on occasion a single video pixel located in between graphics pixels. Because of the need to mix video and graphics there is a hard and fast rule dictating that every pixel in the display buffer be a stand-alone, self-sustaining pixel on the screen. The very nature of the 8 bit YUV subsampled technique makes it necessary to have several 8 bit samples before one video pixel can be generated, making the technique unsuitable for the SFBA visual system.

The second category of architectures integrating video and graphics is the Dual Frame Buffer Architecture (DFBA). The DFBA visual system involves mixing two otherwise free-standing single frame buffer systems at the analog back end with a high-speed analog switch. Since the video and graphics subsystems are both single frame buffer designs each one can make the necessary tradeoffs in spatial resolution and pixel depth with almost complete disregard for the other subsystem. DFBA visual systems also include the feature of being loosely-coupled. Since the only connection of the two systems is in the final output stage, the two subsystems can be on different buses in the system. The fact that the DFBA video subsystem is loosely-coupled to the graphics subsystem is usually the overriding reason such systems, which have significant disadvantages, are typically employed.

DFBA designs typically operate in a mode that has the video subsystem genlocked to the graphics subsystem. Genlocked in this case means having both subsystems start to display their first pixel at the same time. If both subsystems are running at exactly the same horizontal line frequency with the same number of lines, then mixing of the two separate video streams can be done with very predictable results.

Since both pixel streams are running at the same time, the process can be thought of as having video pixels underlying the graphics pixels. If a determination is made not to show a graphics pixel, then the video information will show through. In DFBA designs, it is not necessary for the two subsystems to have the same number of horizontal pixels. As an example, it is quite possible to have 352 video pixels underneath 1024 graphics pixels. The Intel ActionMedia™ boards are DFBA designs and can display an arbitrary number of video pixels while genlocked to an arbitrary line rate graphics subsystem. The only restrictions are that the frequency required to support the configuration be within the 82750DB's 12 MHz to 45 Mhz range.

The decision whether to show the video information or the graphics information in DFBA visual systems is typically made on a pixel by pixel basis in the graphics subsystem. A technique often used is called "chroma keying". Chroma keying involves detecting a specific color (or color entry in the CLUT) in the graphics digital pixel stream. Another approach referred to as "black detect", uses the

graphics analog pixel stream to detect black, since black is the easiest graphics level to detect. In either case, keying information is used to control the high-speed analog switch and the task of integrating video and graphics on the display is reduced to painting the keying color in the graphics display where video pixels are desired. Intel's ActionMedia II™ product implements chroma keying and black detect.

There are several disadvantages to DFBA visual systems. The goal of high-integration is often thwarted by the need to have two separate, free-standing subsystems. The cost of having duplicate DACs, display buffers, and CRT controllers is undesirable. The difficulty of genlocking and the cost of the high-speed analog switch are two more disadvantages. In addition, placing the analog switch in the graphics path will have detrimental effects on the quality of the graphics display. This becomes an ever increasing problem as the spatial resolution and/or line rate of the graphics subsystem grows.

It is an object of the present invention to provide an integrated system for storing and displaying graphics and video information.

It is further object of the present invention to provide a system for storing and displaying either graphics or video information, which system can be easily upgraded into an integrated system for storing and displaying graphics and video information by merely augmenting the system with additional memory.

Further objects and advantages of the invention will become apparent from the description of the invention which follows.

SUMMARY OF THE INVENTION

The present invention comprises a method and apparatus for processing visual data. According to a preferred embodiment, a first memory device stores visual data in a first data format and a second memory device stores visual data in a second data format different from the first data format. A graphics controller, coupled to the first and second memory devices, receives m bits of the visual data in the first data format from the first memory device concurrently with n bits of the visual data in the second data format from the second memory device. The graphics controller merges the visual data in the first data format with the visual data in the second data format to generate a merged pixel stream for display.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating the operation of a first preferred embodiment of the present invention.

FIG. 2 is a block diagram illustrating the operation of a second preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to FIG. 1, there is shown a block diagram illustrating the operation of an apparatus, designated generally 100, for processing visual data according to a first preferred embodiment of the present invention. The invention shown includes first storage means 110 for storing a first bit plane of visual data in a first format. First storage means 110 is coupled to graphics controller 140 through storage bus 132. First storage means 110 and graphics controller 140 are also coupled by data bus 130. The invention also includes means 120 for receiving a second storage means for storing a second bit plane of visual data in a second format

different from the first format. Means 120 is adapted to couple a second storage means to graphics controller 140 through the storage bus 132. Means 120 is also adapted to couple the second storage means to graphics controller 140 by data bus 130a. Graphics controller 140 includes means for forming a merged pixel stream from visual data stored on said first and second storage means. Means 160 for displaying the merged pixel stream is also provided. Means 160 is coupled to graphics controller 140 by pixel bus 150. In the preferred embodiment, data bus 130 and data bus 130a are separate 8 bit buses. In an alternative embodiment, a single 16 bit data bus may be used to couple both first storage means 110 and a second storage means to graphics controller 140. Data buses of other widths may also be used.

FIG. 1 shows a base configuration of the present invention in which first storage means 110 is represented by RAM BANK 0. This base configuration may operate in an 8-bit CLUT mode. This mode allows operation of RAM BANK 0 as a Single Frame Buffer Architecture, similar to a VGA or XGA system in 8 bits per pixel mode. The 8-bit CLUT mode allows for operation of the base configuration as a video only or graphics only subsystem. The base configuration may also operate as a SFBA system with limited graphics/video integration (8 bits/pixel) as described in the Background section above. In the 8-bit CLUT mode, the bandwidth of data bus 130 is the same as would be required for a stand alone 8 bit CLUT graphics subsystem.

Means 120 for receiving a second storage means allows the base configuration of the present invention to be easily upgraded by the mere addition of a second storage means to operate either as (i) an integrated system for storing and displaying both graphics and video information ("the Dual Color Space Mode"), or as (ii) an expanded single frame buffer for storing and displaying either graphics only or video only information at a deepened pixel depth and/or increased resolution level ("the Expanded Single Frame Buffer Mode"). In the Dual Color Space Mode, a first type of visual data may be stored in first storage means 110 in a first format, and a second type of visual data may be stored in a second storage means in a second format which is different from the first format. For example, graphics data may be stored in first storage means 110 in RGB format, and video data may be stored in the second storage means in YUV format. In the Expanded Single Frame Buffer Mode, first storage means 110 and a second storage means preferably provide for operation of the system as a video only system or a graphics only subsystem with 16 bits per pixel. The Expanded Single Frame Buffer Mode may also operate as a SFBA system with limited graphics/video integration (16 bits/pixel) as described in the Background section above.

Graphics controller 140 includes means for forming a merged pixel stream from data in a first format stored on storage means 110 and data which may be stored in a second format on a second storage means, once a second storage means is received by means 120. According to a preferred embodiment, when the base system is upgraded (e.g., when a second storage means is received by means 120) and operating in the Dual Color Space Mode, graphics data is stored in one of the storage means in 8-bit CLUT format, and video data is stored in the other storage means as 8 bit YUV data. The preferred format of the 8 bit YUV data in the Dual

TABLE I

Y_a	U_a	Y_b	V_a	Y_c	U_b	Y_d	V_b	Y_e	U_c	...
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In the Dual Color Space Mode, a first pixel stream representing the RGB graphics pixels (GP_n) is processed in parallel with a second pixel stream representing YUV video pixels. The two parallel pixel streams are stored in parallel in accordance with the format shown in Table II below:

TABLE II

GP_1	GP_2	GP_3	GP_4	GP_5	GP_6	GP_7	GP_8	GP_9	...
Y_a	U_a	Y_b	V_a	Y_c	U_b	Y_d	V_b	Y_e	...

The pixels generated by the video subsystem (VP_n) in the Dual Color Space Mode are preferably 24 bit RGB values derived from 24 bit YUV pixels. The 24 bit YUV pixels are determined for each video pixel VP_n in accordance with the formula shown in Table III below:

TABLE III

$$Y = Y_a, U = U_a, \text{ and } V = V_a \text{ for } VP_1;$$

$$Y = .5Y_a + .5Y_b, U = .75U_a + .25U_b, \text{ and } V = .75V_a + .25V_b \text{ for } VP_2;$$

$$Y = Y_b, U = .5U_a + .5U_b, \text{ and } V = .5V_a + .5V_b \text{ for } VP_3;$$

$$Y = .5Y_b + .5Y_c, U = .25U_a + .75U_b, \text{ and } V = .25V_a + .75V_b \text{ for } VP_4;$$

$$Y = Y_c, U = U_b, \text{ and } V = V_b \text{ or } VP_5, \text{ and so on.}$$

Other subsampling techniques may be used to build the RGB values.

In the preferred embodiment, chroma keying is preferably used on the graphics pixel stream to determine whether to show a graphics pixel or a video pixel. In the example of Table II, if GP_3 and GP_n held pixel values equal to the chroma key value, then the merged graphics and video pixel stream (the visual pixel stream) provided to the DAC would have the format shown in Table IV below:

TABLE IV

GP_1	GP_2	VP_3	VP_4	GP_5	GP_6	GP_7	GP_8	GP_9	...
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Referring now to FIG. 2, there is shown a block diagram illustrating the operation of an apparatus, designated generally 200, for processing visual data according to a second preferred embodiment of the present invention. The invention shown includes first storage means 210 for storing a first bit plane of visual data in a first format. First storage means 210 is coupled to graphics controller 240 through storage bus 232. First storage means 210 and graphics controller 240 are also coupled by data bus 230. The invention also includes second storage means 220 for storing a second bit plane of visual data in a second format different from the first format. Second storage means 220 is coupled to graphics controller 240 through storage bus 232. Second storage means 220 and graphics controller 240 are also coupled by data bus 230a. Graphics controller 240 includes means for forming a merged pixel stream from visual data stored on said first and second storage means. Means 260 for displaying the merged pixel stream is also provided. Means 260 is coupled to graphics controller 240 by pixel bus 250. In the preferred embodiment, data bus 230 and data bus 230a are separate eight bit buses. In an alternative embodiment, a single 16 bit data bus may be used to couple both first storage means 210 and second storage means 220 to graphics controller 240. Data buses of other widths may also be

used. Apparatus **200** functions substantially in accordance with apparatus **100**, with a second storage means having been received by means **120**. Apparatus **200** is thus configured to operate either in the Dual Color Space or the Expanded Single Frame Buffer Modes described above.

The present invention may be embodied in other specific forms without departing from the spirit or essential attributes of the invention. Accordingly, reference should be made to the appended claims, rather than the foregoing specification, as indicating the scope of the invention.

What is claimed is:

1. An apparatus for processing visual data, comprising:
 - (a) a first storage means;
 - (b) a second storage means; and
 - (c) a graphics controller coupled to the first and second storage means, wherein:
 - the first storage means stores visual data in a first data format;
 - the second storage means stores visual data in a second data format;
 - the graphics controller receives m bits of the visual data in the first data format from the first storage means concurrently with n bits of the visual data in the second data format from the second storage means and merges the visual data in the first data format with the visual data in the second data format to generate a merged pixel stream for display;
 - the visual data in the second data format is in a subsampled data format; and
 - the graphics controller upsamples the visual data in the second data format to generate the merged pixel stream.
2. The apparatus of claim 1, further comprising data transfer means for transmitting the visual data in the first data format from the first storage means to the graphics controller and for transmitting the visual data in the second data format from the second storage means to the graphics controller.
3. The apparatus of claim 2, wherein:
 - the first storage means is a first random access memory (RAM) device; and
 - the second storage means is a second RAM device.
4. The apparatus of claim 2, wherein:
 - the visual data in the first data format comprises graphics data; and
 - the visual data in the second data format comprises video data.
5. The apparatus of claim 4, wherein:
 - the graphics data is in an 8-bit CLUT format;
 - the video data is in an 8-bit YUV format; and
 - m equals n .
6. The apparatus of claim 2, wherein the visual data in the second data format is in an 8-bit YUV format.
7. The apparatus of claim 2, wherein the visual data in the first data format comprises the same number of bits per pixel as the visual data in the second data format and m equals n .
8. The apparatus of claim 2, wherein the first and second storage means are part of a single memory bank.
9. The apparatus of claim 2, wherein the graphics controller performs chromakeying to generate the merged pixel stream.
10. The apparatus of claim 2, wherein:
 - the data transfer means comprises a first data bus and a second data bus;
 - the first data bus transmits the visual data in the first data format from the first storage means to the graphics controller; and

the second data bus transmits the visual data in the second data format from the second storage means to the graphics controller concurrently with the transmission of the visual data in the first data format from the first storage means to the graphics controller through the first data bus.

11. The apparatus of claim 10, wherein the first data bus and the second data bus are the same size and m equals n .

12. The apparatus of claim 11, wherein the first data bus is an 8-bit data bus.

13. The apparatus of claim 2, wherein:

the data transfer means comprises a single data bus; the single data bus transmits the visual data in the first data format from the first storage means to the graphics controller; and

the single data bus transmits the visual data in the second data format from the second storage means to the graphics controller concurrently with the transmission of the visual data in the first data format from the first storage means to the graphics controller through the single data bus.

14. The apparatus of claim 13, wherein the single data bus is a 16-bit data bus.

15. The apparatus of claim 2, wherein:

the first storage means is a first random access memory (RAM) device;

the second storage means is a second RAM device;

the visual data in the first data format comprises graphics data;

the visual data in the second data format comprises video data in the subsampled format;

the graphics data comprises the same number of bits per pixel as the video data;

m equals n ; and

the graphics controller upsamples the video data.

16. The apparatus of claim 15, wherein:

the graphics data is in an 8-bit CLUT format; and

the video data is in an 8-bit YUV format.

17. The apparatus of claim 15, wherein the graphics controller performs chromakeying to generate the merged pixel stream.

18. The apparatus of claim 15, wherein:

the data transfer means comprises a first 8-bit data bus and a second 8-bit data bus;

the first 8-bit data bus transmits the graphics data from the first RAM device to the graphics controller; and

the second 8-bit data bus transmits the video data from the second RAM device to the graphics controller concurrently with the transmission of the graphics data from the first RAM device to the graphics controller through the first 8-bit data bus.

19. The apparatus of claim 15, wherein:

the data transfer means comprises a single 16-bit data bus;

the single 16-bit data bus transmits the graphics data from the first RAM device to the graphics controller; and

the single 16-bit data bus transmits the video data from the second RAM device to the graphics controller concurrently with the transmission of the graphics data from the first RAM device to the graphics controller through the single 16-bit data bus.

20. A method for processing visual data, comprising the steps of:

(a) storing visual data in a first data format in a first storage means;

- (b) storing visual data in a second data format in a second storage means;
- (c) transmitting m bits of the visual data in the first data format from the first storage means to a graphics controller;
- (d) transmitting n bits of the visual data in the second data format from the second storage means to the graphics controller, wherein step (c) is implemented concurrently with step (d); and
- (e) merging, with the graphics controller, the visual data in the first data format and the visual data in the second data format to generate a merged pixel stream for display, wherein;
- the visual data in the second data format is in a subsampled data format; and
- step (e) further comprises the step of upsampling, with the graphics controller, the visual data in the second data format.
- 21.** The method of claim **20**, wherein:
- step (c) comprises the step of transmitting the visual data in the first data format from the first storage means to a graphics controller through a data transfer means; and
- step (d) comprises the step of transmitting the visual data in the second data format from the second storage means to the graphics controller through the data transfer means.
- 22.** The method of claim **21**, wherein:
- the first storage means is a first random access memory (RAM) device; and
- the second storage means is a second RAM device.
- 23.** The method of claim **21**, wherein:
- the visual data in the first data format comprises graphics data; and
- the visual data in the second data format comprises video data.
- 24.** The method of claim **23**, wherein:
- the graphics data is in an 8-bit CLUT format;
- the video data is in an 8-bit YUV format; and
- m equals n .
- 25.** The method of claim **21**, wherein the visual data in the second data format is in an 8-bit YUV format.
- 26.** The method of claim **21**, wherein the visual data in the first data format comprises the same number of bits per pixel as the visual data in the second data format and m equals n .
- 27.** The method of claim **21**, wherein the first and second storage means are part of a single memory bank.
- 28.** The method of claim **21**, wherein step (e) comprises the step of performing chromakeying, with the graphics controller, to generate the merged pixel stream.
- 29.** The method of claim **21**, wherein:
- the data transfer means comprises a first data bus and a second data bus;
- step (c) comprises the step of transmitting the visual data in the first data format from the first storage means to the graphics controller through the first data bus; and
- step (d) comprises the step of transmitting the visual data in the second data format from the second storage means to the graphics controller through the second data bus concurrently with step (c).
- 30.** The method of claim **29**, wherein the first data bus and the second data bus are the same size and m equals n .
- 31.** The method of claim **30**, wherein the first data bus is an 8-bit data bus.
- 32.** The method of claim **21**, wherein:

- the data transfer means comprises a single data bus;
- step (c) comprises the step of transmitting the visual data in the first data format from the first storage means to the graphics controller through the single data bus; and
- step (d) comprises the step of transmitting the visual data in the second data format from the second storage means to the graphics controller through the single data bus concurrently with step (c).
- 33.** The method of claim **32**, wherein the single data bus is a 16-bit data bus.
- 34.** The method of claim **21**, wherein:
- the first storage means is a first random access memory (RAM) device;
- the second storage means is a second RAM device;
- the visual data in the first data format comprises graphics data;
- the visual data in the second data format comprises video data in the subsampled format;
- the graphics data comprises the same number of bits per pixel as the video data;
- m equals n ; and
- step (e) further comprises the step of upsampling, with the graphics controller, the video data.
- 35.** The method of claim **34**, wherein:
- the graphics data is in an 8-bit CLUT format; and
- the video data is in an 8-bit YUV format.
- 36.** The method of claim **34**, wherein step (e) comprises the step of performing chromakeying, with the graphics controller, to generate the merged pixel stream.
- 37.** The method of claim **34**, wherein:
- the data transfer means comprises a first 8-bit data bus and a second 8-bit data bus;
- step (c) comprises the step of transmitting the graphics data from the first RAM device to the graphics controller through the first 8-bit data bus; and
- step (d) comprises the step of transmitting the video data from the second RAM device to the graphics controller through the second 8-bit data bus concurrently with step (c).
- 38.** The method of claim **34**, wherein:
- the data transfer means comprises a single 16-bit data bus;
- step (c) comprises the step of transmitting the graphics data from the first RAM device to the graphics controller through the single 16-bit data bus; and
- step (d) comprises the step of transmitting the video data from the second RAM device to the graphics controller through the single 16-bit data bus concurrently with step (c).
- 39.** An apparatus for processing visual data, comprising:
- (a) means for storing visual data in a first data format;
- (b) means for storing visual data in a second data format;
- (c) means for transmitting m bits of the visual data in the first data format from means (a);
- (d) means for transmitting n bits of the visual data in the second data format from means (b) concurrently with the transmitting of means (c); and
- (e) means for concurrently receiving the visual data in the first data format from means (a) through means (c) and the visual data in the second data format from means (b) through means (d) and for merging the visual data in the first data format and the visual data in the second data format to generate a merged pixel stream for display, wherein;

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the visual data in the second data format is in a subsampled data format; and means (e) upsamples the visual data in the second data format.

40. The apparatus of claim 39, wherein:

means (a) is a first random access memory (RAM) device; and

means (b) is a second RAM device.

41. The apparatus of claim 39, wherein:

the visual data in the first data format comprises graphics data; and

the visual data in the second data format comprises video data.

42. The apparatus of claim 41, wherein:

the graphics data is in an 8-bit CLUT format;

the video data is in an 8-bit YUV format; and

m equals n.

43. The apparatus of claim 39, wherein the visual data in the second data format is in an 8-bit YUV format.

44. The apparatus of claim 39, wherein the visual data in the first data format comprises the same number of bits per pixel as the visual data in the second data format and m equals n.

45. The apparatus of claim 39, wherein the means (a) and means (b) are part of a single memory bank.

46. The apparatus of claim 39, wherein means (e) performs chromakeying to generate the merged pixel stream.

47. The apparatus of claim 39, wherein:

means (c) comprises a first data bus;

means (d) comprises a second data bus;

the first data bus transmits the visual data in the first data format from means (a) to means (e); and

the second data bus transmits the visual data in the second data format from means (b) to means (e) concurrently with the transmission of the visual data in the first data format through the first data bus.

48. The apparatus of claim 47, wherein the first data bus and the second data bus are the same size and m equals n.

49. The apparatus of claim 48, wherein the first data bus is an 8-bit data bus.

50. The apparatus of claim 39, wherein:

means (c) and (d) are part of a single data bus;

the single data bus transmits the visual data in the first data format from means (a) to means (e); and

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the single data bus transmits the visual data in the second data format from means (b) to means (e) concurrently with the transmission of the visual data in the first data format through the single data bus.

51. The apparatus of claim 50, wherein the single data bus is a 16-bit data bus.

52. The apparatus of claim 39, wherein:

means (a) is a first random access memory (RAM) device;

means (b) is a second RAM device;

the visual data in the first data format comprises graphics data;

the visual data in the second data format comprises video data in the subsampled format;

the graphics data comprises the same number of bits per pixel as the video data;

m equals n; and

means (e) upsamples the video data.

53. The apparatus of claim 52, wherein:

the graphics data is in an 8-bit CLUT format; and

the video data is in an 8-bit YUV format.

54. The apparatus of claim 52, wherein means (e) performs chromakeying to generate the merged pixel stream.

55. The apparatus of claim 52, wherein:

means (c) comprises a first 8-bit data bus;

means (d) comprises a second 8-bit data bus;

the first 8-bit data bus transmits the graphics data from the first RAM device to means (e); and

the second 8-bit data bus transmits the video data from the second RAM device to means (e) concurrently with the transmission of the graphics data from the first RAM device to means (e) through the first 8-bit data bus.

56. The apparatus of claim 52, wherein:

means (c) and (d) are part of a single 16-bit data bus;

the single 16-bit data bus transmits the graphics data from the first RAM device to means (e); and

the single 16-bit data bus transmits the video data from the second RAM device to means (e) concurrently with the transmission of the graphics data from the first RAM device to means (e) through the single 16-bit data bus.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 5,546,531
APPLICATION NO. : 08/425785
DATED : August 13, 1996
INVENTOR(S) : Lippincott

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 6, at line 29, delete "or" and insert --for--.
In column 6, at line 35, delete "GP_n" and insert --GP₄--.
In column 6, at line 54, delete "fermat" and insert --format--.

Signed and Sealed this

Seventeenth Day of July, 2007

A handwritten signature in black ink on a light gray dotted background. The signature reads "Jon W. Dudas" in a cursive style.

JON W. DUDAS
Director of the United States Patent and Trademark Office