TOSHIBA MOS MEMORY PRODUCTS

TC524256P/Z/J-10, TC524256P/Z/J-12

DESCRIPTION

The TC524256P/Z/J is a CMOS Multiport memory equipped with a 262,144-word × 4 bit dynamic random access memory(RAM) port and a 512-word × 4 bit static serial access memory(SAM) port. In addition to the conventional DRAM operation modes, the TC524256P/Z/J features a write-per-bit function on the RAM port; Bi-directional transfer capability between the DRAM memory array and the SAM data register and a high speed serial read/write capability on the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally. The TC524256P/Z/J is fabricated using TOSHIBA's CMOS silicon gate process technology as well as advanced circuitry to provide low power dissipation and wide operating margin. Multiplexed address inputs and a common input/output organization allow the TC524256P/Z/J to be housed in a standard 28-pin, 400-mil wide plastic DIP and 400-mil height ZIP and in a standard 32-pin 400-mil wide plastic SOJ. System oriented features include a single 5V±10% power supply operation and compatibility with high performance schottky TTL logic.

FEATURES

ITEM		TC524256P/Z/J	
		-10	-12
t_{RAC}	$\overline{RAS}$ Access Time (Max.)	100ns	120ns
t_{CAC}	$\overline{CAS}$ Access Time (Max.)	50ns	60ns
t_{RC}	Cycle Time (Min.)	190ns	220ns
t_{PC}	Page Mode Cycle Time(Min.)	90ns	105ns
t_{SCA}	Serial Access Time (Max.)	25ns	35ns
t_{SCC}	Serial Cycle Time (Min.)	30ns	40ns
I_{CC1}	RAM Operating Current (SAM: Standby)	70mA	60mA
I_{CC2A}	SAM Operating Current (RAM: Standby)	50mA	45mA
I_{CC2}	RAM/SAM Standby Current	10mA	

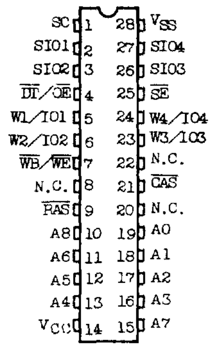
- Organization
  RAM port: 262,144 words × 4 bits
  SAM port: 512 words × 4 bits
- Single power supply of 5V±10% with a built-in V_{BB} generator
- Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, Page mode, Write-Per-Bit, Read transfer, Write transfer, Serial read, Serial Write capability
- All inputs and outputs TTL compatible
- 512 refresh cycle/8ms
- Package
  TC524256P: 0.4 inches 28 pins standard Plastic DIP
  TC524256Z: 0.4 inches 28 pins standard Plastic ZIP
  TC524256J: 0.4 inches 32 pins standard Plastic SOJ

PIN NAMES

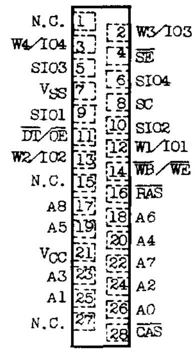
A0 ∿ A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
$\overline{WB}/\overline{WE}$	Write Per Bit/Write Enable
W1/IO1 ∿ W4/IO4	Write Mask/Data IN, OUT
SC	Serial Clock
$\overline{SE}$	Serial Enable
SIO1 ∿ SIO4	Serial Input Output
V_{CC}	Power (+5V)
V_{SS}	Ground
N.C.	No Connection

PIN CONNECTIONS (TOP VIEW)

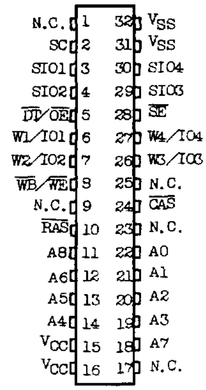
Plastic DIP



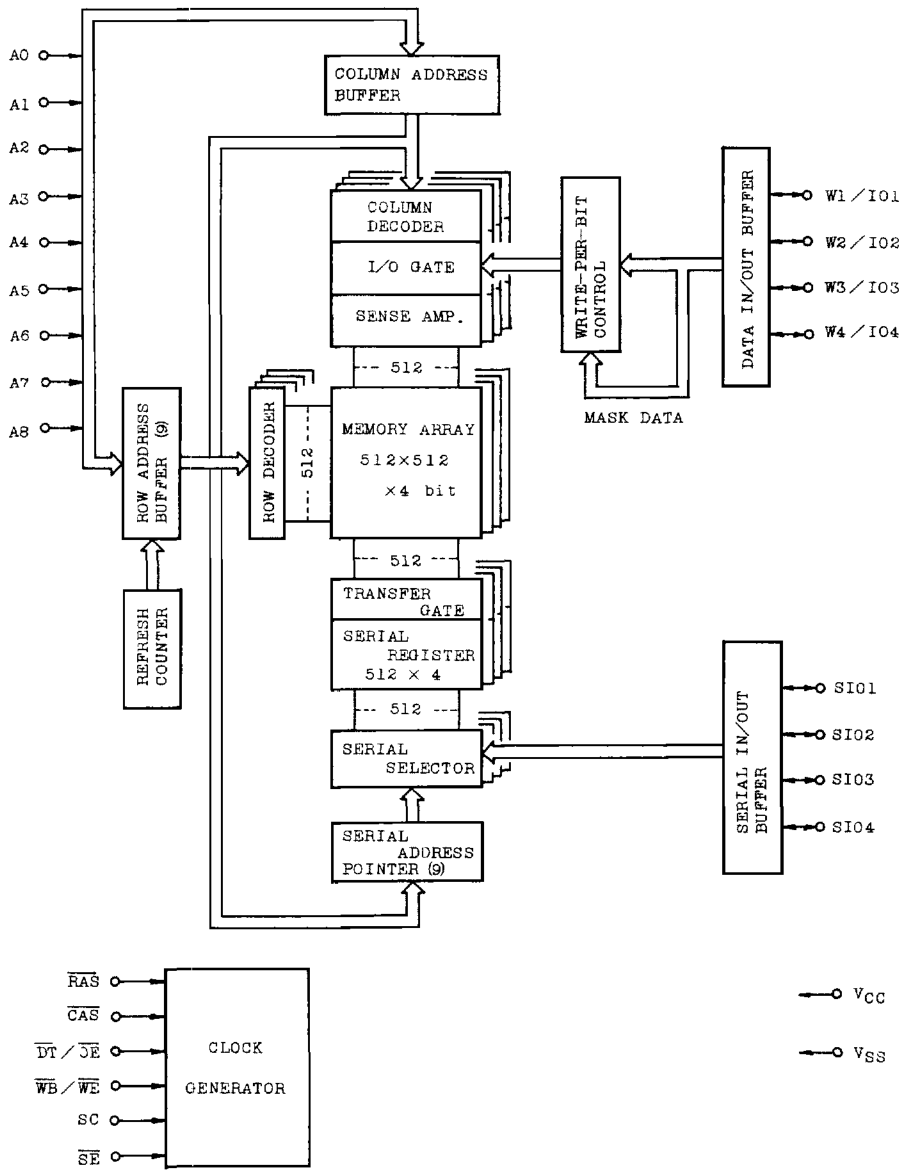
Plastic ZIP



Plastic SOJ



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNITS	NOTES
V_{IN}, V_{OUT}	Input Output Voltage	-1.0 ∿ 7.0	V	1
V_{CC}	Power Supply Voltage	-1.0 ∿ 7.0	V	1
T_{opr}	Operating Temperature	0 ∿ 70	°C	1
T_{stg}	Storage Temperature	-55 ∿ 150	°C	1
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C•sec	1
P_D	Power Dissipation	1	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

RECOMMENDED DC OPERATING CONDITION (Ta=0 ∿ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V	2
V_{IH}	Input High Voltage	2.4	-	6.5	V	2
V_{IL}	Input Low Voltage	-1.0	-	0.8	V	2

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 ∿ 70°C)

SYMBOL	ITEM (RAM Port)	SAM Port	TC524256P/Z/J-10		TC524256P/Z/J-12		UNITS	NOTES
			MIN.	MAX.	MIN.	MAX.		
I_{CC1}	OPERATING CURRENT	Standby	-	70	-	60	mA	3,4
I_{CC1A}	($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	Active	-	110	-	100		3,4
I_{CC2}	STANDBY CURRENT	Standby	-	10	-	10	mA	
I_{CC2A}	($\overline{RAS}$, $\overline{CAS}$=V_{IH})	Active	-	50	-	45		3,4
I_{CC3}	$\overline{RAS}$ ONLY REFRESH CURRENT	Standby	-	70	-	60	mA	3
I_{CC3A}	($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}: t_{RC}=t_{RC} MIN.)	Active	-	110	-	100		3,4
I_{CC4}	PAGE MODE CURRENT	Standby	-	60	-	50	mA	3,4
I_{CC4A}	($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling: t_{PC}=t_{PC} MIN.)	Active	-	100	-	90		3,4
I_{CC5}	$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CURRENT	Standby	-	70	-	60	mA	3
I_{CC5A}	($\overline{CAS}$ Before $\overline{RAS}$ Cycling: t_{RC}=t_{RC}MIN.)	Active	-	110	-	100		3,4
I_{CC6}	DATA TRANSFER CURRENT	Standby	-	80	-	75	mA	3
I_{CC6A}	($\overline{RAS}$, $\overline{CAS}$ Cycling: t_{RC}=t_{RC} MIN.)	Active	-	130	-	120		3,4

SYMBOL	ITEM	MIN.	TYP.	MAX.	UNITS	NOTES
$I_{I(L)}$	INPUT LEAKAGE CURRENT (0V ≤ V_{IN} ≤ 6.5V, All Other Pins Not Under Test=0V)	-10	0	10	μA	
$I_{O(L)}$	OUTPUT LEAKAGE CURRENT (Output is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	-10	0	10	μA	
V_{OH}	OUTPUT HIGH LEVEL VOLTAGE (Wi/IOi, SIOi ..... I_{OUT}=-2mA)	2.4	-	-	V	
V_{OL}	OUTPUT LOW LEVEL VOLTAGE (Wi/IOi .... I_{OUT}=+4.2mA, SIOi ..... I_{OUT}=+2mA)	-	-	0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=0∿70°C) (NOTES 5, 6, 7)

SYMBOL	PARAMETER	TC524256P/Z/J-10		TC524256P/Z/J-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	190		220		ns	
t_{RWC}	Read-Write Cycle Time	250		290			
t_{PC}	Page Mode Cycle Time	90		105			
t_{PRWC}	Page Mode Read-Write Cycle Time	150		175			
t_{RAC}	Access Time from $\overline{RAS}$		100		120		8,14
t_{CAC}	Access Time from $\overline{CAS}$		50		60		8,14
t_{OFF}	Output Buffer Turn-Off Delay	0	30	0	35		10
t_{T}	Transition Time (Rise and Fall)	3	35	3	35		7
t_{RP}	$\overline{RAS}$ Precharge Time	80		90			
t_{RAS}	$\overline{RAS}$ Pulse Width	100	10,000	120	10,000		
t_{RSH}	$\overline{RAS}$ Hold Time	50		60			
t_{CSH}	$\overline{CAS}$ Hold Time	100		120			
t_{CAS}	$\overline{CAS}$ Pulse Width	50		60			
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	60		
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10			
t_{CPN}	$\overline{CAS}$ Precharge Time	15		20			
t_{CP}	$\overline{CAS}$ Precharge Time (Page Mode)	30		35			
t_{ASR}	Row Address Set-Up Time	0		0			
t_{RAH}	Row Address Hold Time	10		15			
t_{ASC}	Column Address Set-Up Time	0		0			
t_{CAH}	Column Address Hold Time	20		25			
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	70		85			
t_{RCS}	Read Command Set-Up Time	0		0			
t_{RCH}	Read Command Hold Time	0		0			11
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	10		10			11
t_{WCH}	Write Command Hold Time	20		25			
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	70		85			
t_{WP}	Write Command Pulse Width	20		25			
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30		35			
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	30		35			
t_{DS}	Data Set-Up Time	0		0			12
t_{DH}	Data Hold Time	20		25			12
t_{RASP}	$\overline{RAS}$ Pulse Width (Page Mode)	190	100,000	225	100,000		

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITION (Continued)

SYMBOL	PARAMETER	TC524256P/ Z/J-10		TC524256P/ Z/J-12		UNITS	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{DHR}	Data Hold Time referenced to $\overline{\text{RAS}}$	70		85			
t_{WCS}	Write Command Set-Up Time	0		0			13
t_{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	125		150			13
t_{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	75		90			13
t_{DZC}	Data to $\overline{\text{CAS}}$ Delay Time	0		0			
t_{DZO}	Data to $\overline{\text{OE}}$ Delay Time	0		0			
t_{OEA}	Access Time from $\overline{\text{OE}}$		25		30		
t_{OEZ}	Output Buffer Turn-Off Delay from $\overline{\text{OE}}$	0	20	0	25	ns	10
t_{OED}	$\overline{\text{OE}}$ to Data Input Delay Time	20		25			
t_{OEH}	$\overline{\text{OE}}$ Command Hold Time	20		20			
t_{ROH}	$\overline{\text{RAS}}$ Hold Time referenced to $\overline{\text{OE}}$	20		20			
t_{CSR}	$\overline{\text{CAS}}$ Set-Up Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Cycle	10		10			
t_{CHR}	$\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Cycle	20		20			
t_{RPC}	$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time	0		0			
t_{CPT}	$\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Test	40		50			
t_{REF}	Refresh Period		8		8	ms	
t_{WSR}	$\overline{\text{WB}}$ Set-Up Time	0		0			
t_{RWH}	$\overline{\text{WB}}$ Hold Time	10		15			
t_{MS}	Write-Per-Bit Mask Data Set-Up Time	0		0			
t_{MH}	Write-Per-Bit Mask Data Hold Time	10		15			
t_{THS}	$\overline{\text{DT}}$ High Set-Up Time	0		0			
t_{THH}	$\overline{\text{DT}}$ High Hold Time	10		15			
t_{TLS}	$\overline{\text{DT}}$ Low Set-Up Time	0		0			
t_{TLH}	$\overline{\text{DT}}$ Low Hold Time	10		15		ns	
t_{RTH}	$\overline{\text{DT}}$ Low Hold Time referenced to $\overline{\text{RAS}}$ (Real Time Read Transfer)	80		95			
t_{CTH}	DT Low Hold Time referenced to $\overline{\text{CAS}}$ (Real Time Read Transfer)	30		35			
t_{ESR}	$\overline{\text{SE}}$ Set-Up Time referenced to $\overline{\text{RAS}}$	0		0			
t_{REH}	$\overline{\text{SE}}$ Hold Time referenced to $\overline{\text{RAS}}$	10		15			
t_{TRD}	$\overline{\text{DT}}$ to $\overline{\text{RAS}}$ Delay Time (Read Transfer)	0		0			
t_{RP}	$\overline{\text{DT}}$ Precharge Time	30		35			
t_{RSD}	$\overline{\text{RAS}}$ to First $\overline{\text{SC}}$ Delay Time (Read Transfer)	100		120			

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITION

SYMBOL	PARAMETER	TC524256P/Z/J-10		TC524256P/Z/J-12		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
t_{CSD}	$\overline{CAS}$ to First SC Delay Time (Read Transfer)	50		60			
t_{TSL}	Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	5		10			
t_{TSD}	$\overline{DT}$ to Frist SC Delay Time (Read Transfer)	15		20			
t_{SRS}	Last SC to $\overline{RAS}$ Set-Up Time (Serial Input)	30		40			
t_{SRD}	$\overline{RAS}$ to First SC Delay Time (Serial Input)	25		30			
t_{SDD}	$\overline{RAS}$ to Serial Input Delay Time	50		60			
t_{SDZ}	Serial Output Buffer Trun-Off Delay Time $\overline{RAS}$ (Pseudo Write Transfer)	10	50	10	60		10
t_{SZS}	Serial Input to First SC Delay Time	0		0			
t_{SCC}	SC Cycle Time	30		40			
t_{SC}	SC Pulse Width (SC High Time)	10		15			
t_{SCP}	SC Precharge Time (SC Low Time)	10		15		ns	
t_{SCA}	Access Time from SC		25		35		9
t_{SOH}	Serial Output Hold Time from SC	5		5			
t_{SDS}	Serial Input Set-Up Time	0		0			
t_{SDH}	Serial Input Hold Time	20		30			
t_{SEA}	Access Time from $\overline{SE}$		25		35		9
t_{SE}	$\overline{SE}$ Pulse Width	25		35			
t_{SEP}	$\overline{SE}$ Precharge Time	25		35			
t_{SEZ}	Serial Output Buffer Turn-Off Delay from $\overline{SE}$	0	20	0	30		10
t_{SZE}	Serial Input to $\overline{SE}$ Delay Time	0		0			
t_{SWS}	Serial Write Enable Set-Up Time	5		10			
t_{SEH}	Serial Write Enable Hold Time	15		20			
t_{SWIS}	Serial Write Disable Set-Up Time	5		10			
t_{SWIH}	Serial Write Disable Hold Time	15		20			

CAPACITANCE (V_{CC}=5V±10%, f=1MHz, Ta=0∿70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{I1}	Input Capacitance (A0∿A8)	-	8	pF
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, SC, $\overline{SE}$)	-	8	
C_{IO1}	Input/Output Capacitance (W1/IO1∿W4/IO4)	-	10	
C_{IO2}	Input/Output Capacitance (SIO1∿SIO4)	-	10	

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. These parameters depend on cycle rate.
4. These parameters depend on output loading. Specified values are obtained with the output open.
5. Power must be applied to the $\overline{RAS}$ and $\overline{DT/OE}$ input signals to pull them "high" before or at the same time as the VCC supply is turned on. After power-up, a pause of 200 μseconds minimum is required with $\overline{RAS}$ and $\overline{DT/OE}$ held "high." After the pause, a minimum of eight (8) $\overline{RAS}$ and (8) SC dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{DT/OE}$ signal must be held "high." If the internal refresh counter is used, a minimum (8) $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of (8) $\overline{RAS}$ cycles.
6. AC measurements assume t_T=5ns.
7. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. RAM port outputs are measured with a load equivalent to 2 TTL loads and 100pF.
9. SAM port outputs are measured with a load equivalent to 2 TTL loads and 30pF. D_{OUT} comparator level: V_{OH}/V_{OL}=2.0V/0.8V.
10. t_{OFF} (max.), t_{OEZ} (max.), t_{SDZ} (max.) and t_{SEZ} (max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
11. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB/WE}$ leading edge in read-write cycles.
13. t_{WCS}, t_{RWD} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{CWD} \geqq t_{CWD}$ (min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell: If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
14. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.

DEVICE INFORMATION

RAM PORT OPERATION

Operation Truth Table

All operation modes of TC524256P/Z/J are determined by $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$, and $\overline{SE}$ at the falling edge of $\overline{RAS}$. They are shown in the following table 1.

$\overline{RAS}$	$\overline{CAS}$	ADDRESS	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	FUNCTION
H	H	*	*	*	*	Standby
	H	Valid	H→L	H	*	Read
	H	Valid	H	H→L	*	Write
	H	Valid(Row add.)	H	*	*	$\overline{RAS}$ only refresh
↓	L	*	H(1)	*	*	$\overline{CAS}$-before-$\overline{RAS}$ Refresh
	H	Valid	H	L	*	Write-per-Bit
	H	Valid	L	H	*	Read Transfer
	H	Valid	L	L	L	Write Transfer
	H	Valid	L	L	H	Pseudo-Write Transfer

Note; H: V_{IH}, L: V_{IL}, *: V_{IH} or V_{IL}

(1) The input level of $\overline{DT}/\overline{OE}$ in the $\overline{CAS}$ before $\overline{RAS}$ timing is not ristricted. However it is recommended that $\overline{DT}/\overline{OE}$ be held 'High' because this input will be used for future expansion of the operation mode.

ADDRESSING

The 18 address bits required to decode 4-bits of the 1,048,576 cell locations within the Dynamic RAM memory array of the TC524256P/Z/J, are multiplexed onto 9 address input pins (A0∿A8). Nine row-address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).

DATA TRANSFER/OUTPUT ENABLE ($\overline{DT}/\overline{OE}$)

The $\overline{DT}/\overline{OE}$ input is a multifunction pin. When $\overline{DT}/\overline{OE}$ is 'High' at the falling edge of $\overline{RAS}$, a normal DRAM cycle is performed and this input is used as an output enable. When $\overline{DT}/\overline{OE}$ is 'Low' at the falling edge of $\overline{RAS}$, a data transfer operation is started between the RAM port and the SAM port.

WRITE-PER-BIT/WRITE-ENABLE ($\overline{WB}/\overline{WE}$)

The $\overline{WB}/\overline{WE}$ input is also a multifunction pin. For conventional DRAM cycle, the $\overline{WB}/\overline{WE}$ input is used in the same manner as standard DRAMs except when the write-per-bit function is used. When $\overline{WB}/\overline{WE}$ is 'low' at the falling edge of $\overline{RAS}$, the bit write-mask is enabled. When $\overline{WB}/\overline{WE}$ and $\overline{CAS}$ are 'low' at the falling edge of $\overline{RAS}$, the raster operation set-up cycle is executed.

The $\overline{WB}/\overline{WE}$ input also determines the direction of data transfer between the DRAM memory array and the serial register. When $\overline{WB}/\overline{WE}$ is 'high' at the falling edge of $\overline{RAS}$, the data is transferred from RAM to SAM (read-transfer cycle). When $\overline{WB}/\overline{WE}$ is 'low' at the falling edge of $\overline{RAS}$, the data is transferred from SAM to RAM (write-transfer cycle).

WRITE-MASK DATA/DATA INPUT/OUTPUT (W1/IO1 to W4/IO4)

When the write-per-bit function is enabled, the mask data on the W1/IO1 pins is latched into the write-mask register WM1 at the falling edge of $\overline{RAS}$. Data is written into the DRAM on data lines where the write-mask data is a logic '1'. Writing is inhibited on data lines where the write-mask data is a logic '0'. The write-mask data is valid for only one cycle.

PAGE MODE

The page mode feature of the TC524256P/Z/J allows data to be transferred into of multiple column locations of the same row by having multiple column cycles during a single active $\overline{RAS}$ cycle.

For the initial page mode access, the output data is valid after the specified access time from $\overline{RAS}$. For all subsequent page mode read operations, the output data is valid after the specified access time from $\overline{CAS}$. As a result, page mode operation reduces power dissipation and improves data access time.

When the write-per-bit function is enabled, the mask data specified in the first write operation, at the falling edge of $\overline{RAS}$, is maintained throughout the page mode write cycle.

$\overline{RAS}$-ONLY REFRESH

The data in the DRAM cycle requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of the 512 rows in the DRAM array within the specified 8ms refresh period. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with '$\overline{RAS}$-ONLY' cycles.

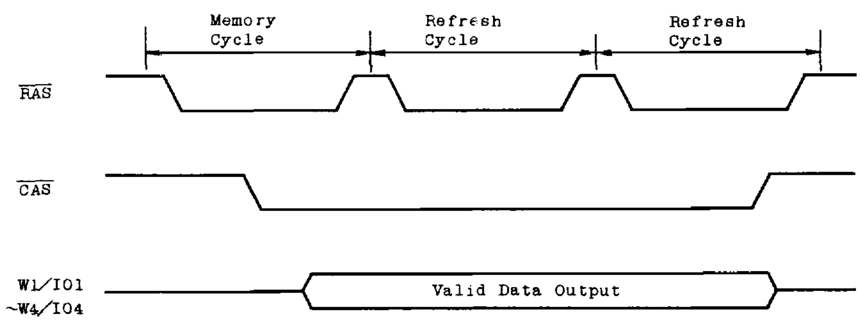
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH

The TC524256P/Z/J also offers an internal refresh function. Whe CAS in held 'low' for a specified period (t_{CSR}) before $\overline{\text{RAS}}$ goes low, an internal refresh address counter and on-chip refresh control clock generators are enabled and an internal refresh operation takes place. When the refresh operation is completed, the internal refresh address counter is automatically incremented in preparation for the next $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycle. For successive $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycles, $\overline{\text{CAS}}$ can remain low while cycling $\overline{\text{RAS}}$.

HIDDEN REFRESH

A hidden refresh is a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh performed by holding $\overline{\text{CAS}}$ 'low' from a previous read cycle. This allows for the output data from the previous memory cycle to remain valid while performing a refresh. The internal refresh address counter provides the address and the refresh is accomplished by cycling $\overline{\text{RAS}}$ after the specified $\overline{\text{RAS}}$-precharge period (refer to figure 1).

Figure 1: Hidden refresh cycle



WRITE-PER-BIT FUNCTION

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When $\overline{\text{WB}}/\overline{\text{WE}}$ is held 'low' at the falling edge of $\overline{\text{RAS}}$, during a random access operation, the write-mask is enabled. At the same time, the mask data on the Wi/IOi pins is latched onto the write-mask register (WM1). When a '0' is sensed on any of the Wi/IOi pins, their corresponding write circuits are disabled and new data will not be written.

When a '1' is sensed on any of the Wi/IOi pins, their corresponding write circuits will remain enabled so that new data is written. The truth table of the write-per-bit function is shown in table 2.

Table 2: Truth table for write-per-bit function

At the falling edge of $\overline{\text{RAS}}$				Function
$\overline{\text{CAS}}$	$\overline{\text{DT}}/\overline{\text{OE}}$	$\overline{\text{WB}}/\overline{\text{WE}}$	Wi/IOi (i=1∿4)	
H	H	H	*	Write Enable
H	H	L	1	Write Enable
			0	Write Mask

An example of the write-per-bit function illustrating its application to displays is shown in figures 2 and 3.

Figure 2: Write-per-bit timing cycle

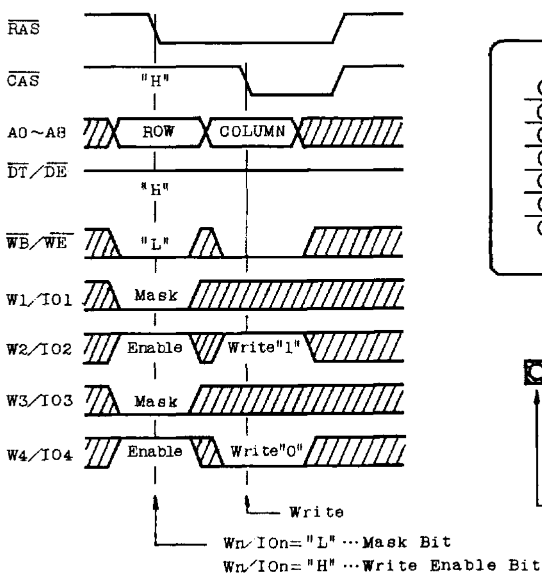
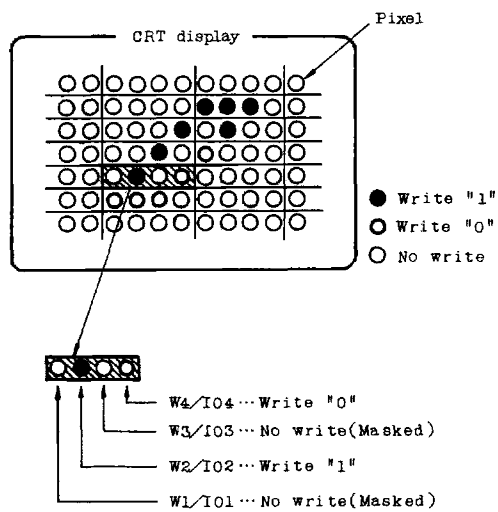


Figure 3: Corresponding bit-map



TRANSFER OPERATION

The TC524256P/Z/J features bi-directional transfer capability form RAM to SAM and from SAM to RAM. A transfer consists of loading 512 words by 4-bits of data from one port into the other. During a transfer cycle, RAM port and SAM port operations are restricted.

There are three types of transfer operations: read transfer, write transfer and pseudo-write transfer. As shown in table 3, the type of transfer operation is determined by $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ at the falling edge of $\overline{RAS}$.

Table 3: Truth table of transfer operation

At the falling edge of $\overline{RAS}$					Transfer direction
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$		
H	L	H	*	Read/real-time read transfer cycle	RAM → SAM
H	L	L	L	Write-transfer cycle	SAM → RAM
H	L	L	H	Pseudo-write transfer cycle	-

*: high or low

READ-TRANSFER CYCLE

A read-transfer consists of loading a selected row of data from the RAM array into the SAM register. A read-transfer is accomplished by holding $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low and $\overline{WB}/\overline{WE}$ high at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM.

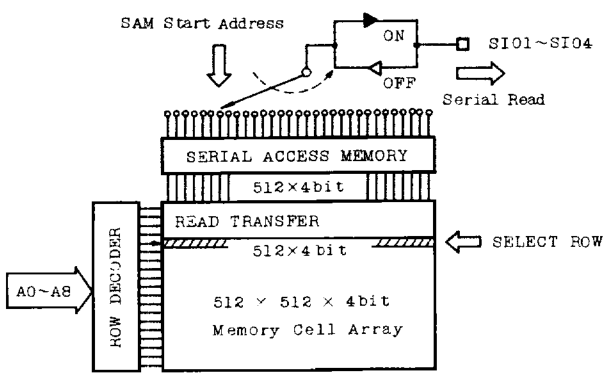
The actual data transfer completed at the rising edge of $\overline{DT}/\overline{OE}$.

When the transfer is completed, the SIO lines are set into the output mode.

In a read/real-time read-transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT}/\overline{OE}$ and becomes valid on the SIO lines after the specified access time t_{SCA} from the rising edge of the subsequent serial clock(SC) cycle.

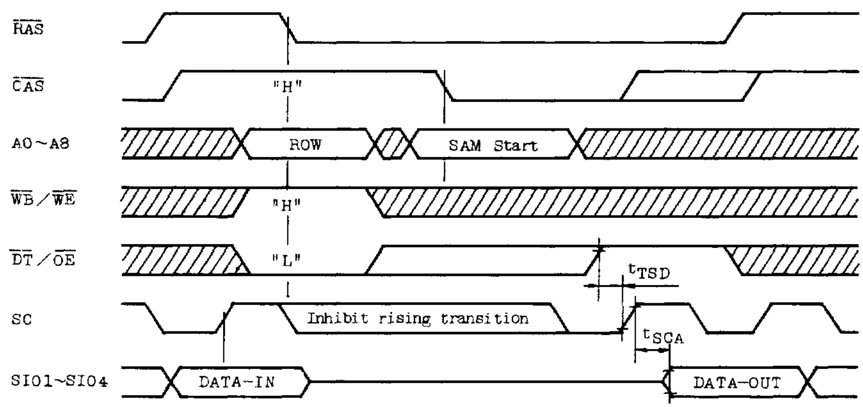
The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$. (refer to figure 4).

Figure 4: Block diagram of RAM port and SAM port during read transfer



In a read-transfer cycle (which is preceded by a write-transfer cycle), the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC precharge time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{TSD} from the rising edge of $\overline{DT}/\overline{OE}$ (refer to Figure 5).

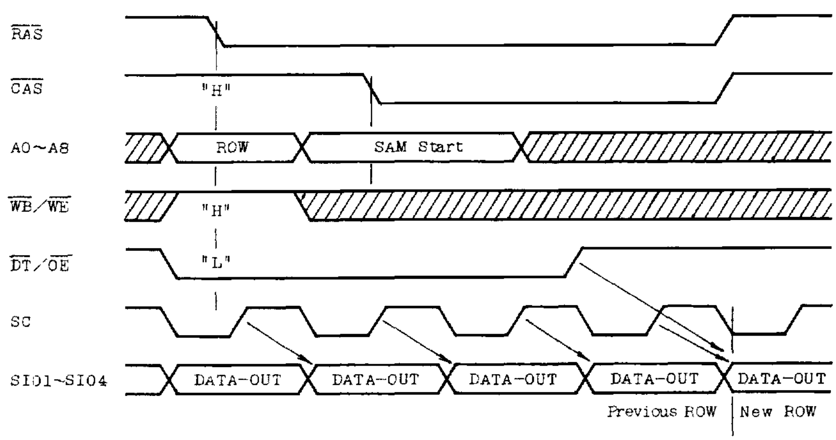
Figure 5: Read-transfer cycle (preceded by a write-transfer cycle)



In a real-time read-transfer cycle (which is preceded by another read-transfer cycle), the previous row data appears on the SIO lines until the specified t_{SCA} access time from the same rising edge of SC.

This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed, without any timing loss. To make this continuous data flow possible: the rising edge of $\overline{DT}/\overline{OE}$ must be synchronized with $\overline{RAS}$, $\overline{CAS}$ and the subsequent rising edge of SC (refer to Figure 6).

Figure 6: Real-time read transfer cycle

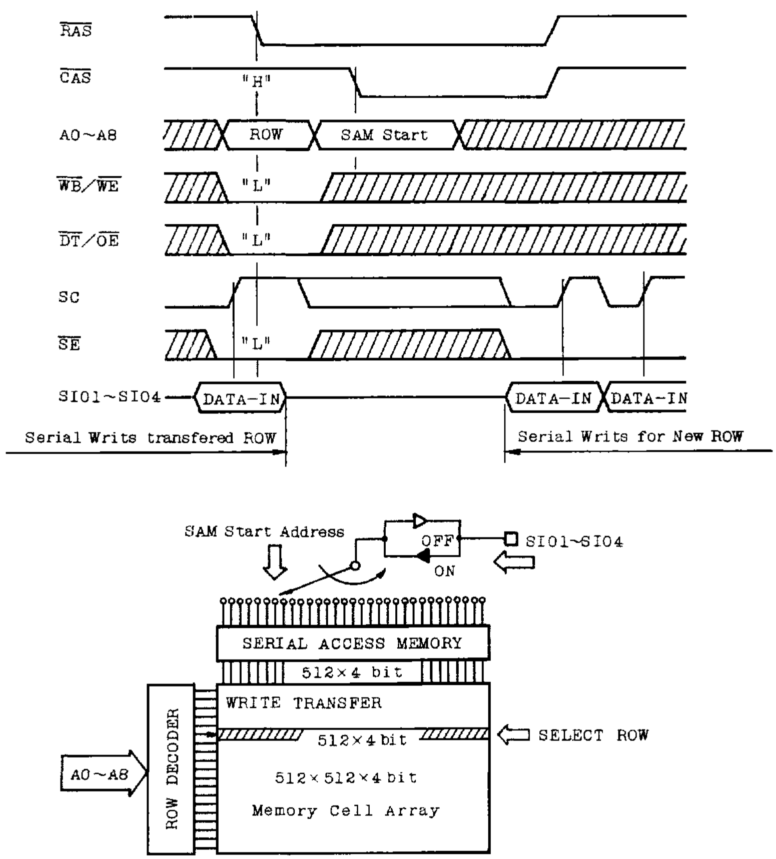


WRITE-TRANSFER CYCLE

A write-transfer cycle consists of loading the content of the SAM data register into a selected row or the RAM array. A write-transfer is accomplished by $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low and $\overline{SE}$ low at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write-transfer is completed, the SIO lines are in the input mode so that serial data synchronized with SC can be loaded.

When two consecutive write-transfer operations are performed, there is a delay in availability between the last bit of the previous row and the first bit of the new row. Consequently the SC clock must be held at a constant V_{IL} or V_{IH} after the SC precharge time t_{SC} has seen satisfied, a rising edge of the SC clock until after a specified delay t_{SRD} from the rising edge of $\overline{RAS}$ (refer to figure 7).

Figure 7: Write-transfer cycle

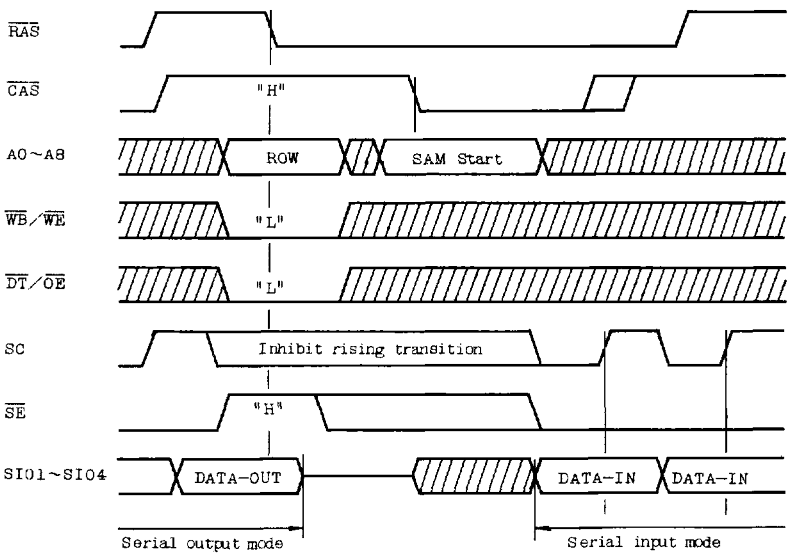


PSEUDO-WRITE-TRANSFER CYCLE

The pseudo-write-transfer cycle switches SIO lines from serial output mode to serial input mode. A pseudo-write-transfer is accomplished by holding $\overline{CAS}$ high, $\overline{DT}/\overline{OE}$ low, $\overline{WB}/\overline{WE}$ low and $\overline{SE}$ high at the falling edge of $\overline{RAS}$. The pseudo-write-transfer cycle must be performed after a read-transfer cycle if the subsequent operation is a write-transfer cycle.

There is a timing delay associated with the switching of the SIO lines from serisl output mode to serial input mode. During this period, the SC clock must be held at a constant V_{IL} or V_{IH} after the t_{SC} precharge time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay t_{SRD} from the rising edge of $\overline{RAS}$ (refer to Figure 8).

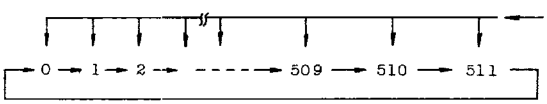
Figure 8: Pseudo-write-transfer cycle



SAM PORT OPERATION

The TC524256P/Z/J is provided with a 512-word by 4-bit serial access memory(SAM). High-speed read and write operation may be performed through the SAM port independent of the RAM port operations, except during transfer operations. The preceding transfer operation determines the direction of data flow through the SAM registers.

Data may be read out of the SAM port after a read-transfer cycle (RAM→SAM) has been performed. Data can be shifted out of the SAM port starting at any of the 512-bit locations. This tap location corresponds to the column address selected a the falling edge of $\overline{\text{CAS}}$ during the read-transfer cycle. The SAM registers are configured as circular data registers. The data is shifted out sequentially starting from the selected tap location to the most significant bit and then wraps around to the least significant bit.



Tap location determined by column address of read-transfer cycle.

Subsequent real-time-read-transfer may be performed on-the-fly as many times as desired within the refresh constrainst of the DRAM memory array.

A pseudo-write-transfer cycle must be performed in order to write data into the SAM port. This cycle switches the SAM port operation from output mode to input mode. Data is not transferred during a pseudo-write-transfer cycle. A write-transfer cycle (SAM→RAM) may then be performed. The data in the SAM registers is loaded into the RAM row selected by the row address at the falling edge of $\overline{\text{RAS}}$. The start address of SAM registers is determined by the column address selected at the falling edge of $\overline{\text{CAS}}$.

Table 4: Truth table for SAM operation

Preceding Transfer Cycle	SAM port operation	$\overline{\text{DT}}/\overline{\text{OE}}$ (at the falling edge of $\overline{\text{RAS}}$)	SC	$\overline{\text{SE}}$	Function
read-transfer	serial output mode	H*		L	enable serial read
				H	disable serial read
write-transfer	serial input mode			L	enable serial write
				H	disable serial write

* When simultaneous operation are being performed on the RAM port and the SAM port, $\overline{\text{DT}}/\overline{\text{OE}}$ must be held high at the falling edge of $\overline{\text{RAS}}$ so as not to perform a false transfer cycle.

SERIAL CLOCK (SC)

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial-read, the output data becomes valid on the SIO pins after the maximum specified serial access time t_{SCA} from the rising edge of SC.

The serial clock SC also increments the 9-bit serial pointer which is used to select the SAM address. The pointer address is incremented in a wrap-around mode to select sequential locations after the starting location which is determined by the column address in the read-transfer cycle. When the pointer reaches the most significant address location (decimal 511), the next SC clock will place it at the least significant address location (decimal 0).

SERIAL ENABLE ($\overline{SE}$)

The $\overline{SE}$ input is used to enable serial access operation. In a serial-read cycle, $\overline{SE}$ is used as an output control. In a serial-write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is high, serial access is disabled, however, the serial address pointer location is still incremented when SC is clocked even when $\overline{SE}$ is high.

SERIAL INPUT/OUTPUT (SIO1 ∿ SIO4)

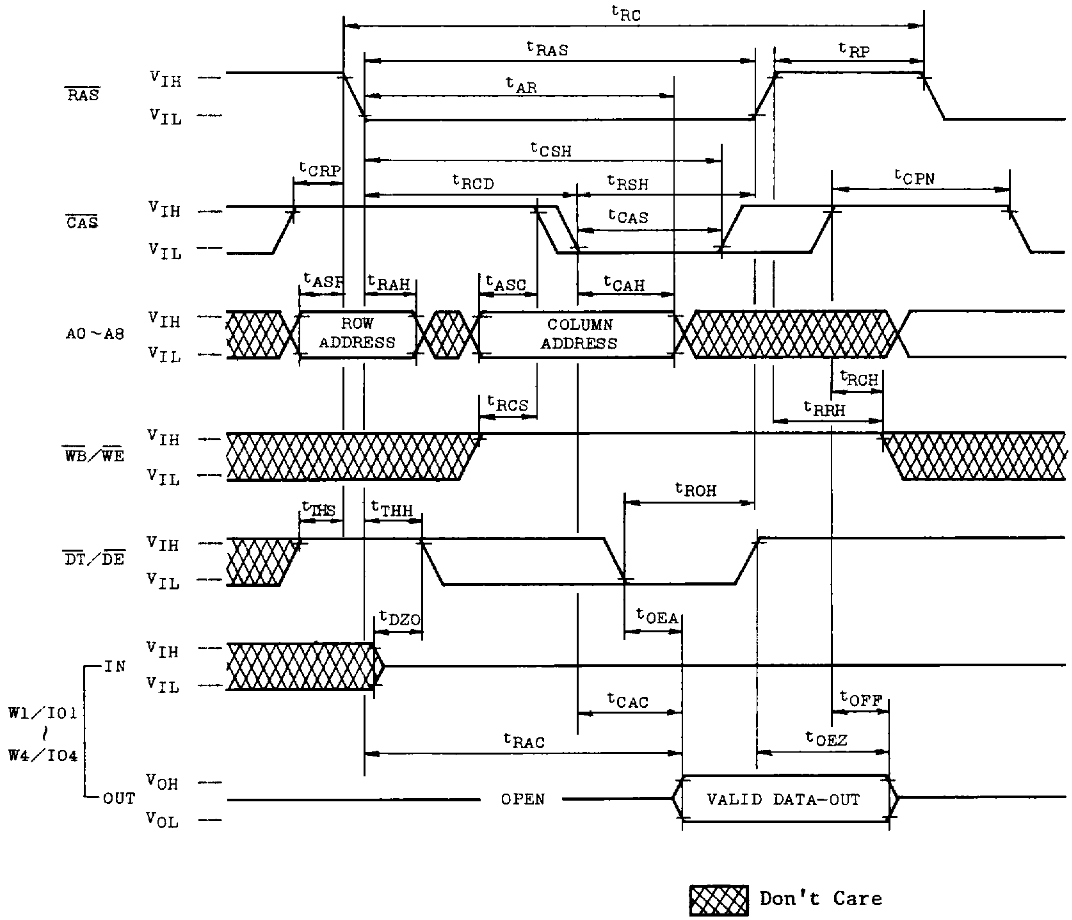
Serial input and serial output share common I/O pins. Serial input or output mode is determined by the most recent transfer cycle. When a read-transfer cycle is performed, the SAM port is in the output mode. When a pseudo-write cycle is performed, the SAM port operation is switched from output mode to input mode.
During subsequent write-transfer cycle, the SAM port remains in the input mode.

REFRESH

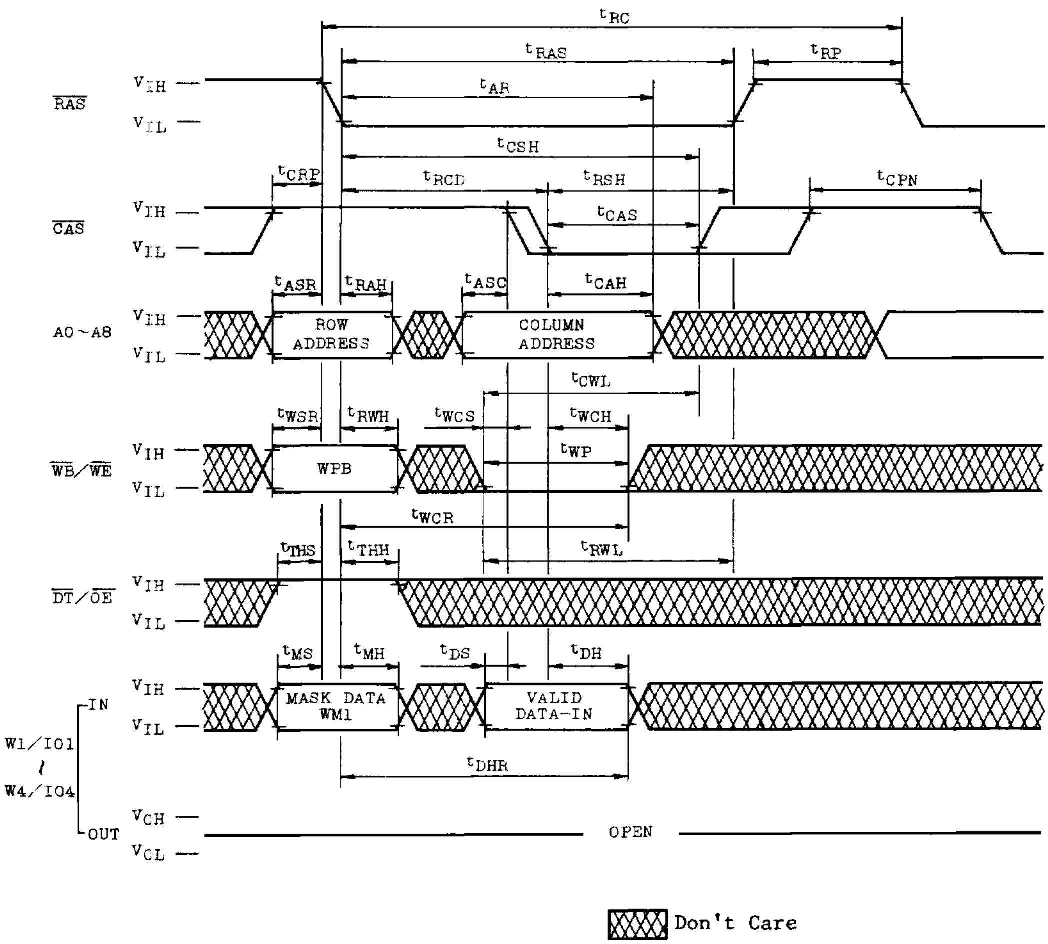
The SAM data registers are static flip-flops therfore a refresh is not required.

TIMING WAVEFORMS

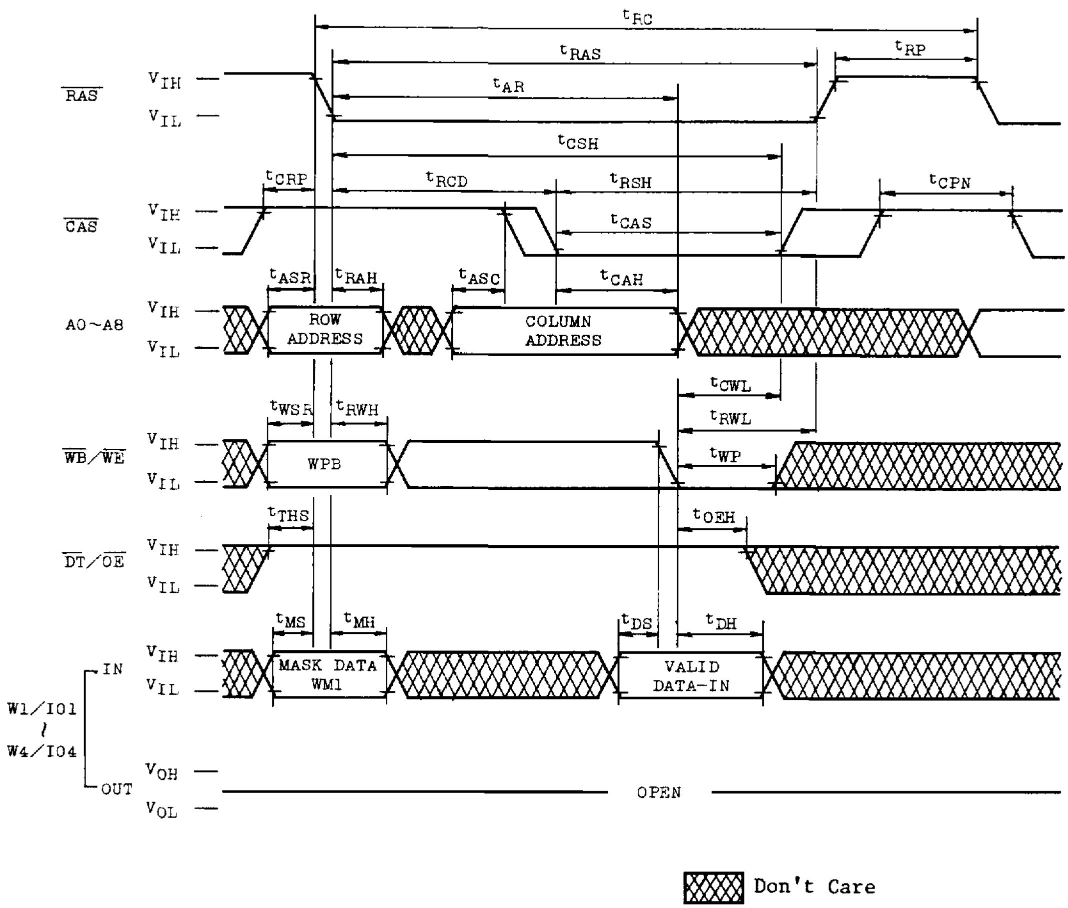
READ CYCLE



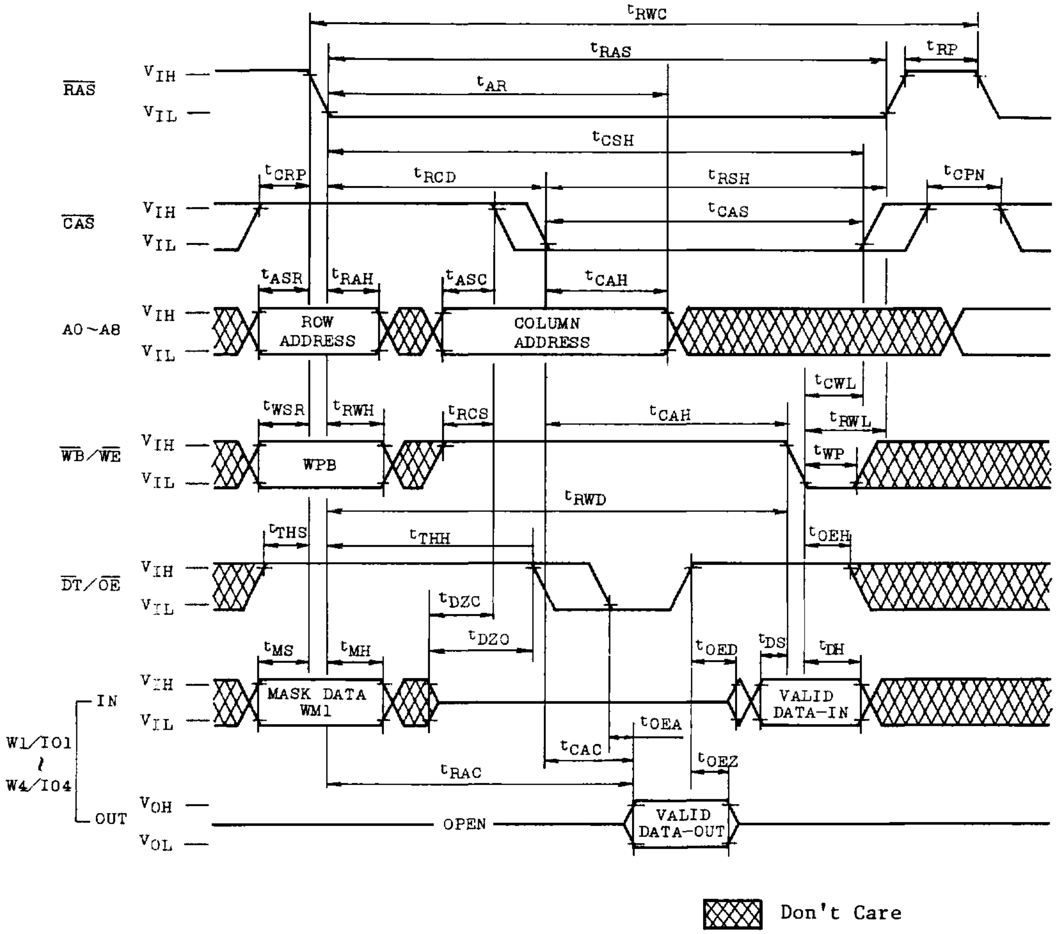
WRITE CYCLE (EARLY WRITE)



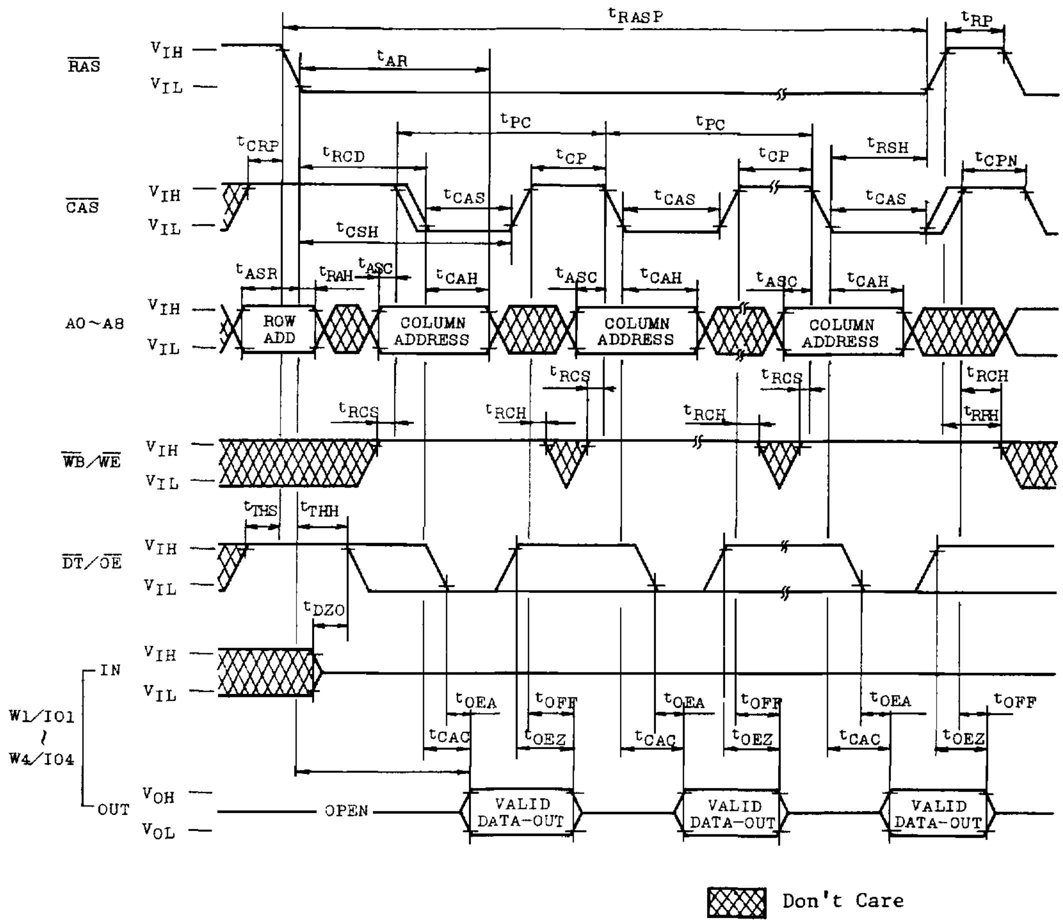
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



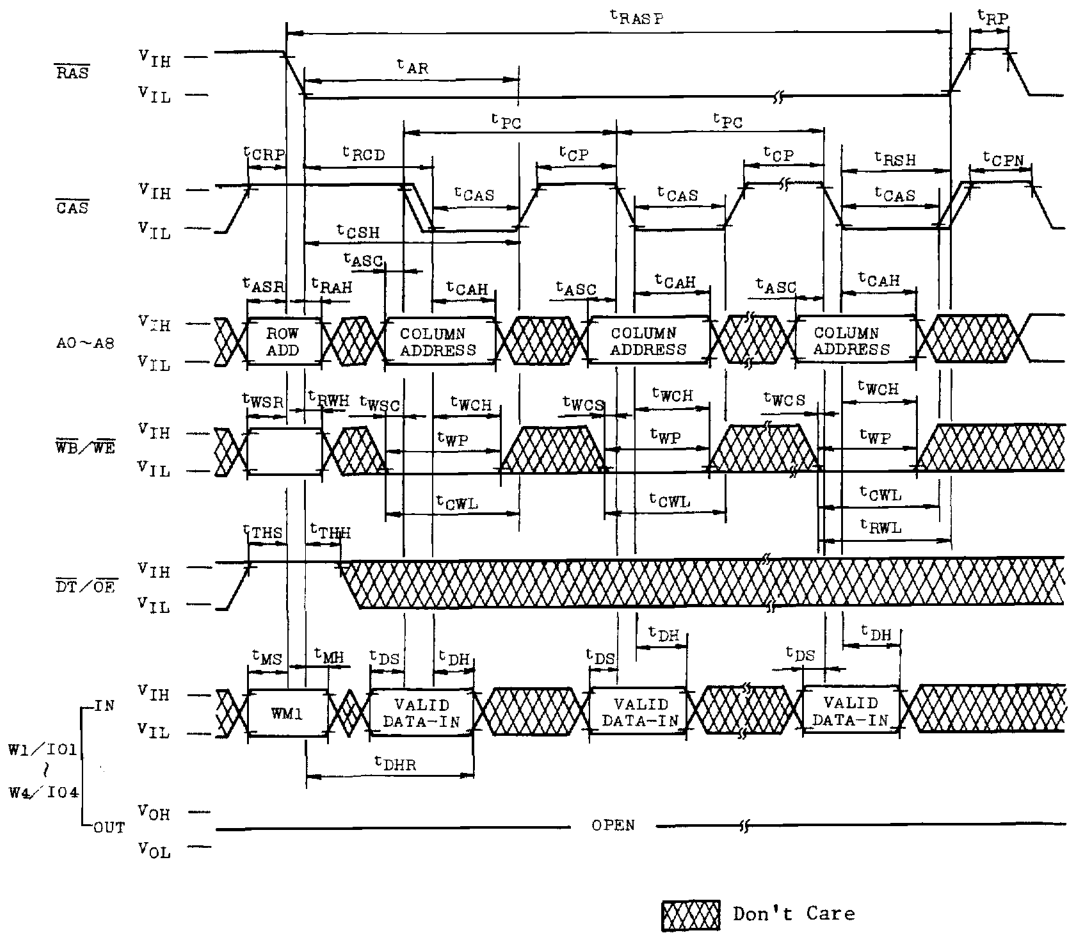
READ-WRITE/READ-MODIFY-WRITE CYCLE



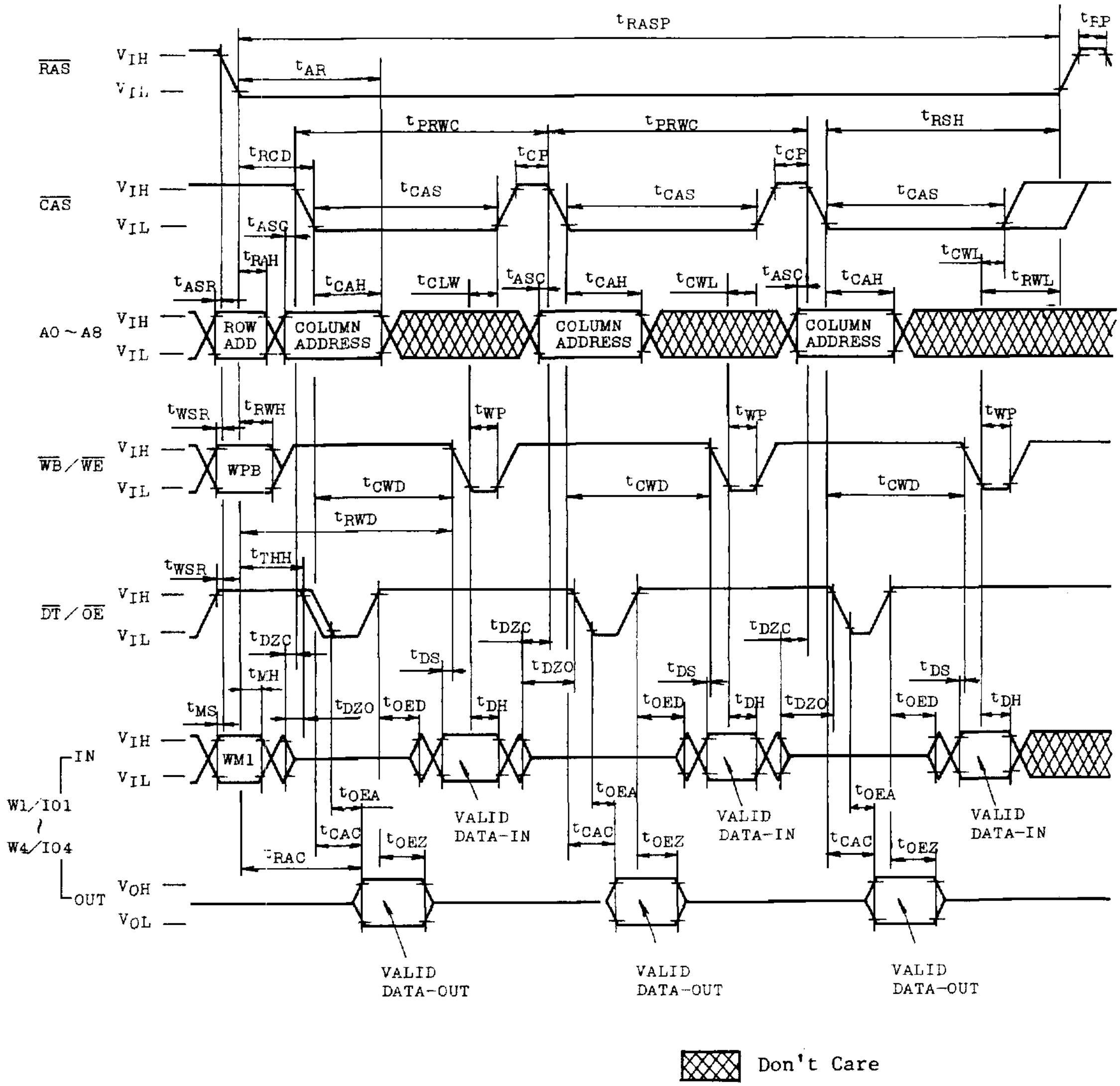
PAGE MODE READ CYCLE



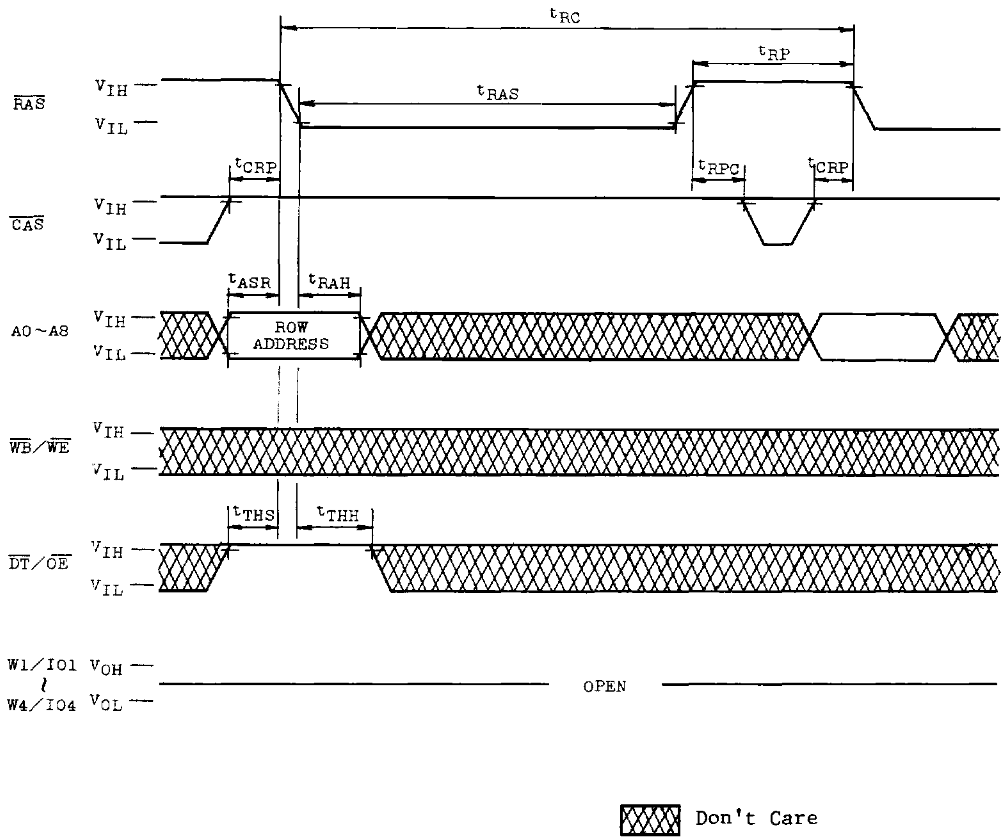
PAGE MODE WRITE CYCLE (EARLY WRITE)



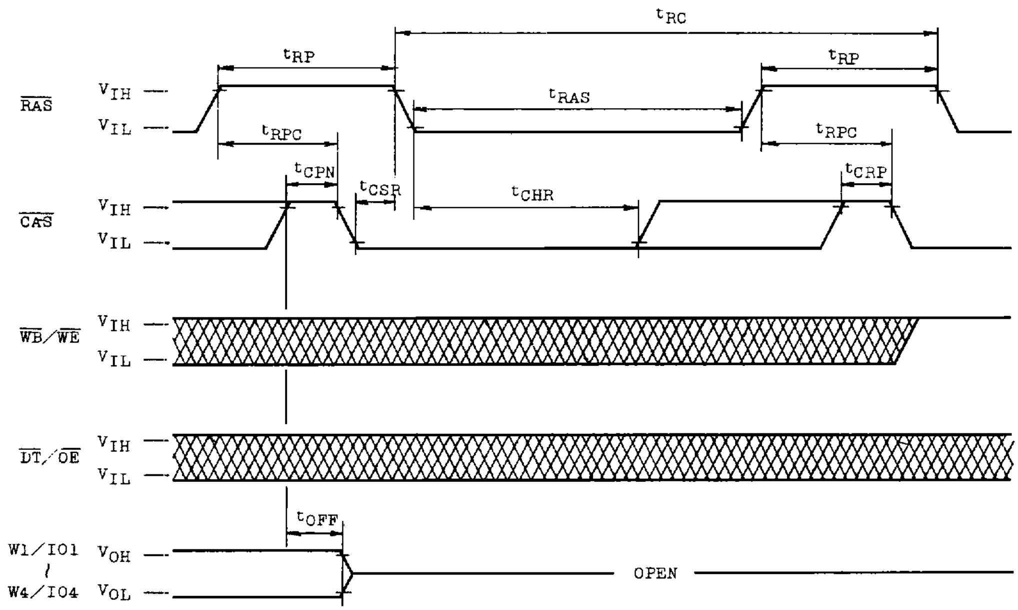
PAGE MODE READ-MODIFY-WRITE CYCLE



RAS ONLY REFRESH CYCLE



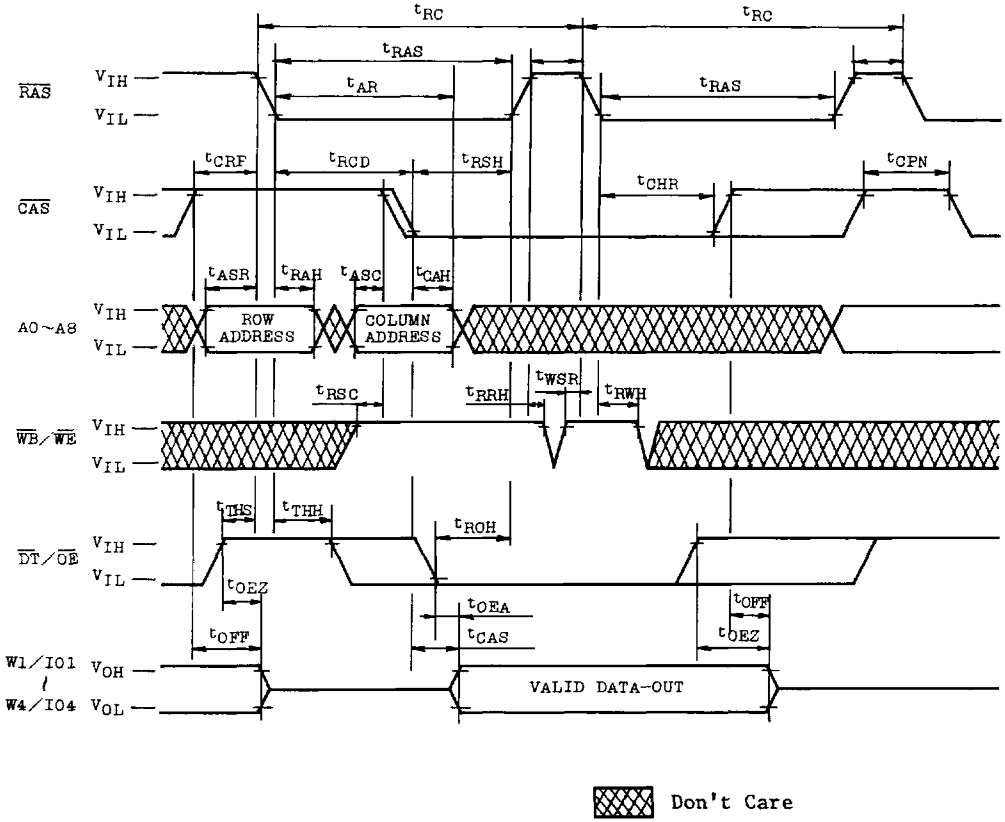
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



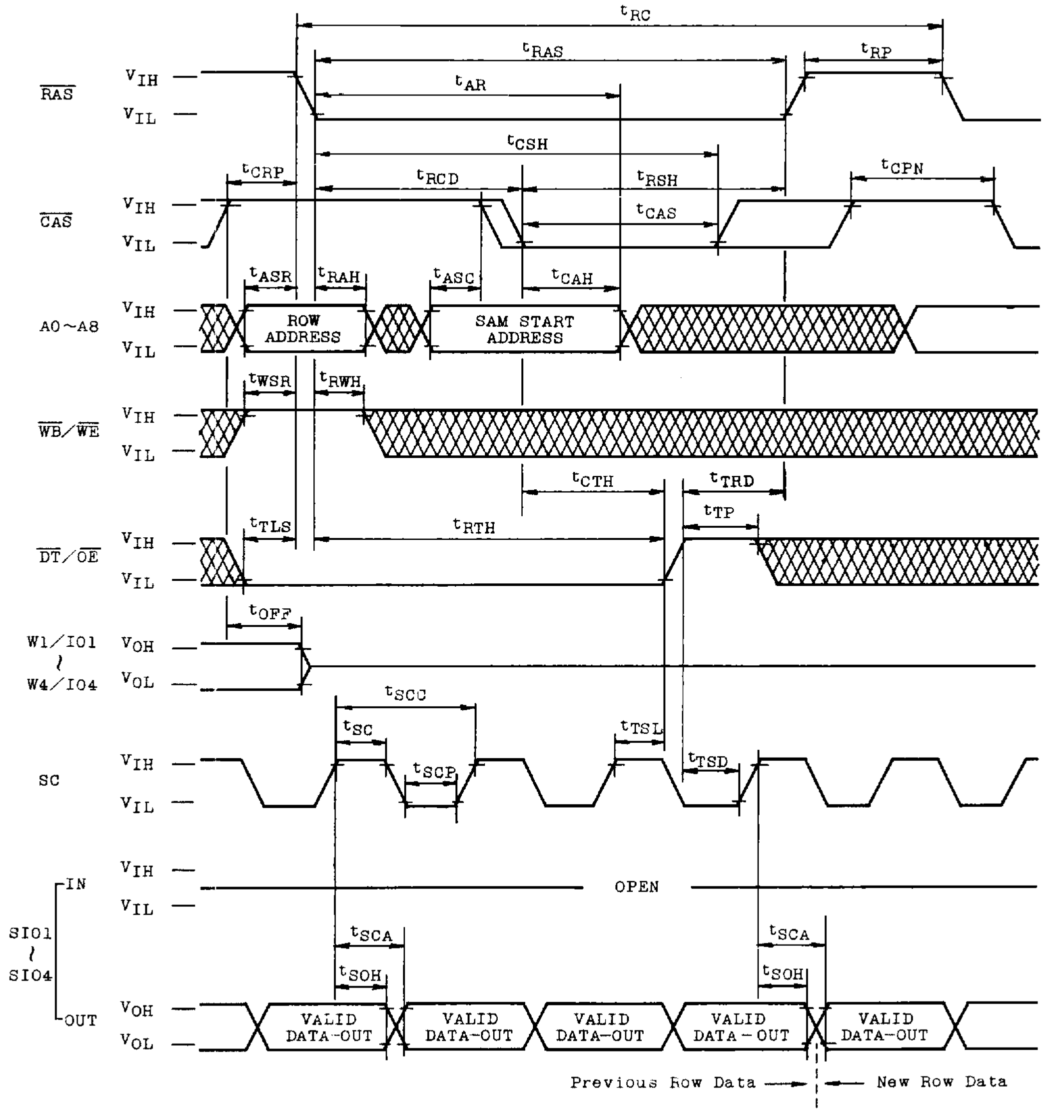
Note: A0 ∿ A8=Don't Care

Don't Care

HIDDEN REFRESH CYCLE

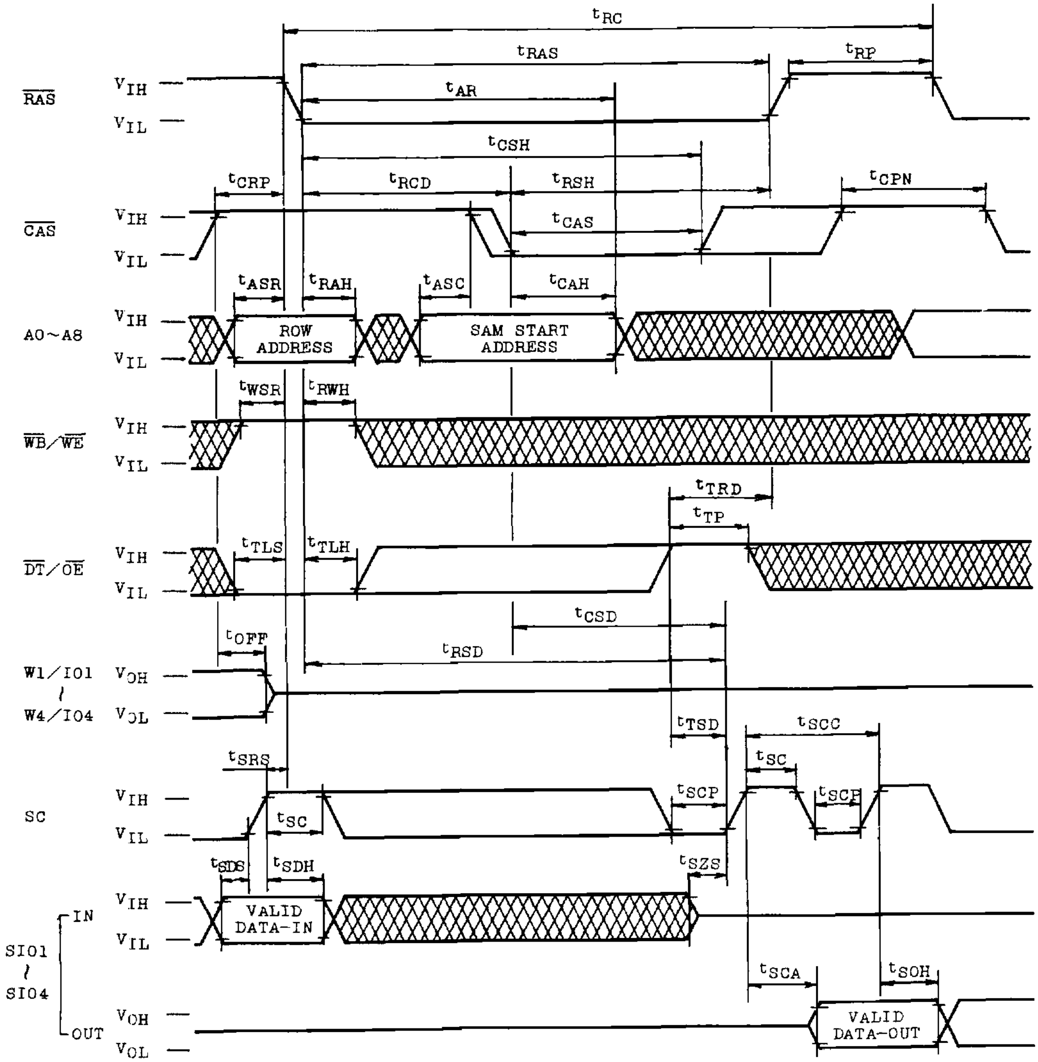


REAL TIME READ TRANSFER CYCLE



Note: $\overline{SE}$=V_{IL} ▩ Don't Care

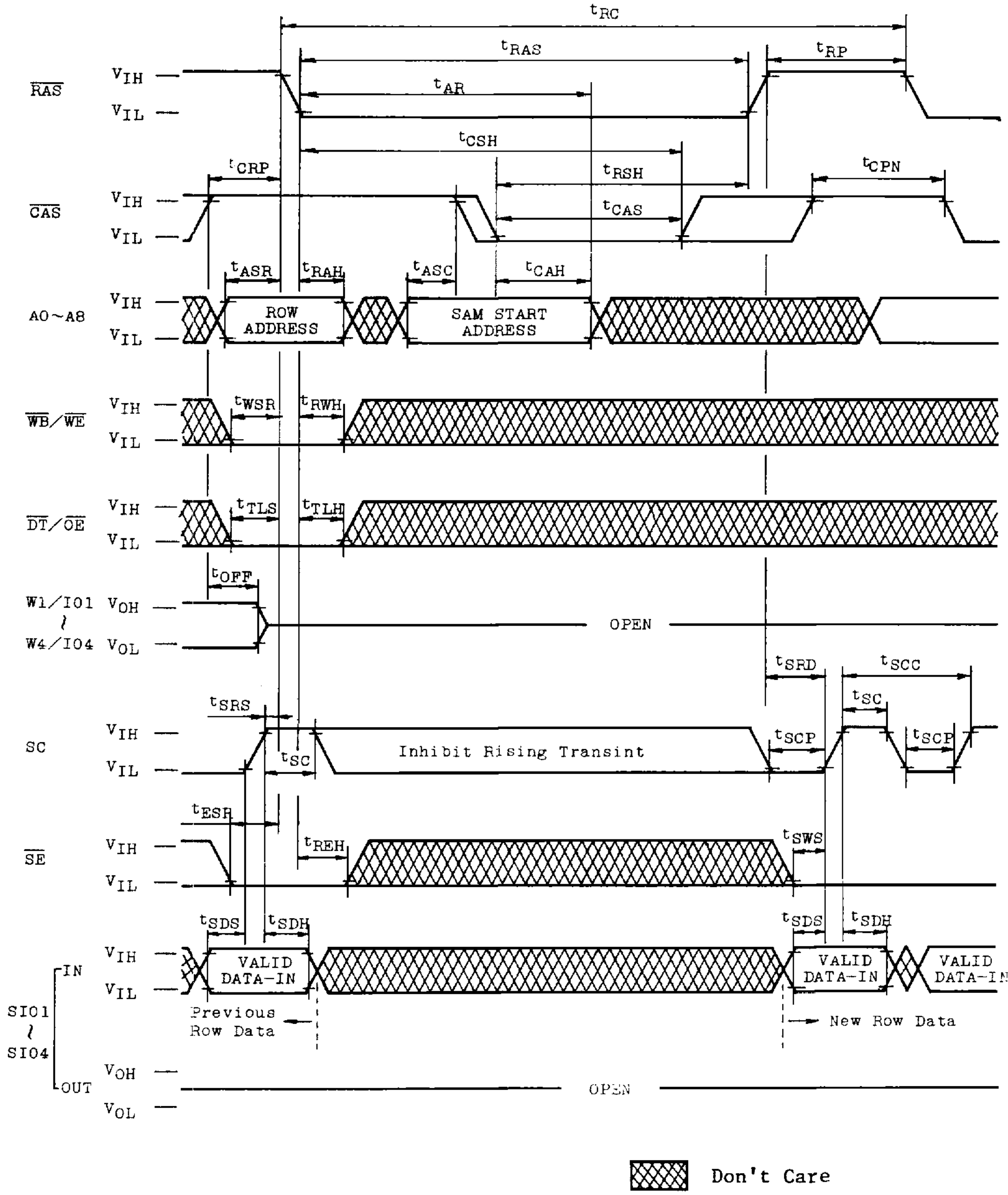
READ TRANSFER CYCLE (Previous transfer is write transfer)



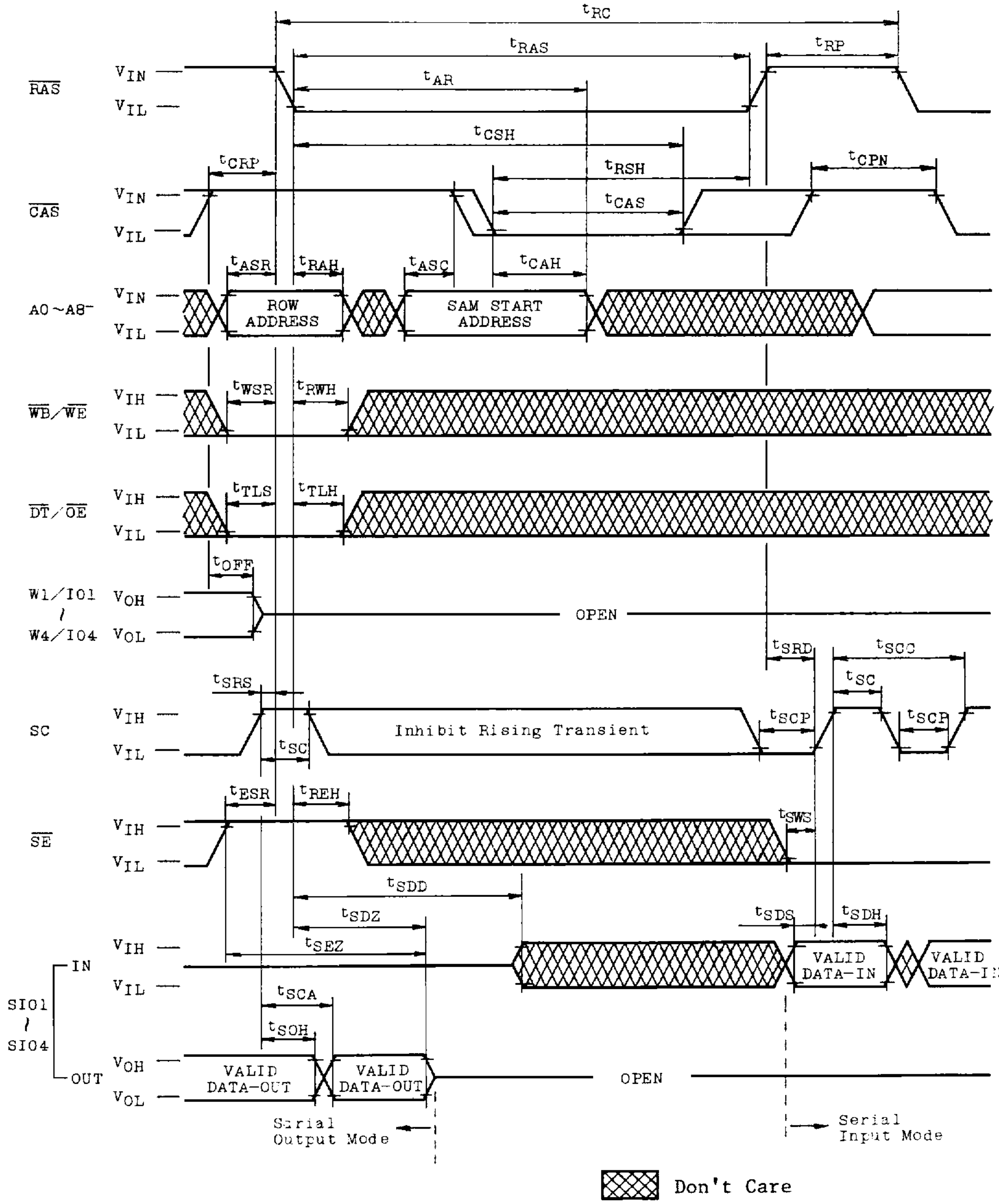
Note: $\overline{SE}$=V_{IL}

Don't Care

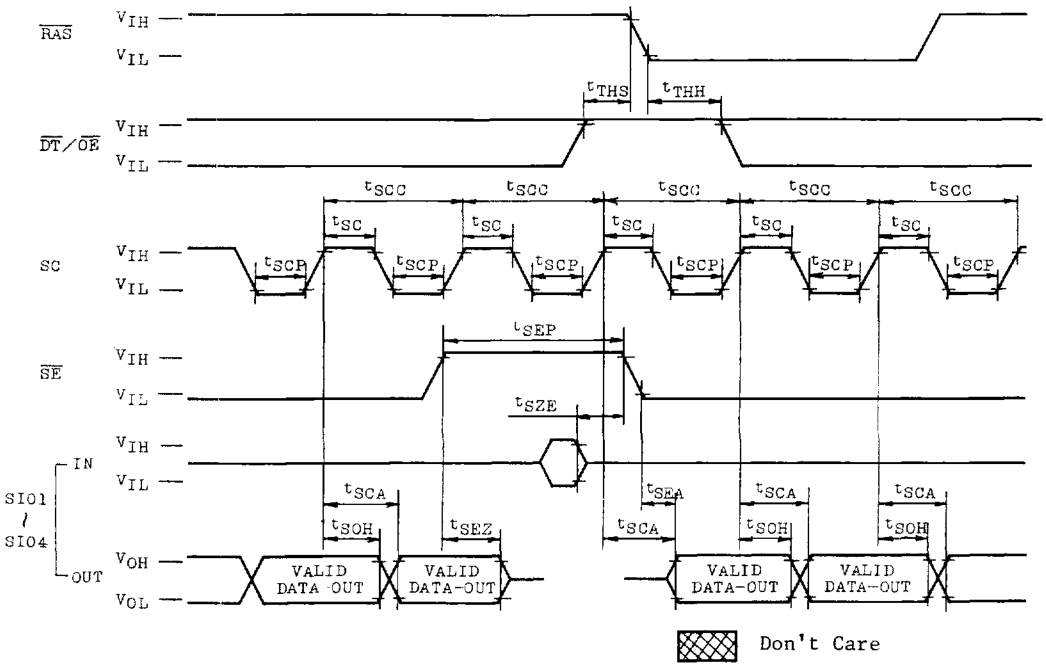
WRITE TRANSFER CYCLE



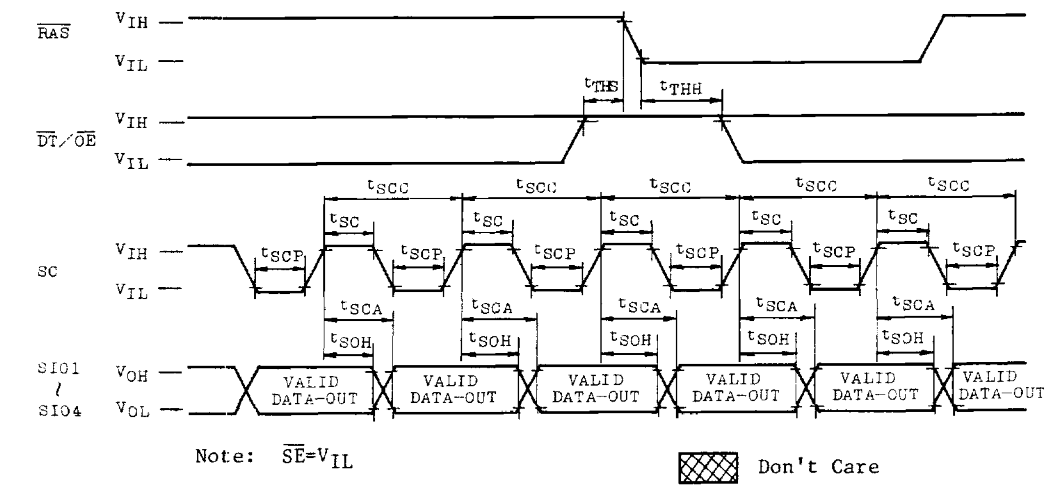
PSEUDO WRITE TRANSFER CYCLE



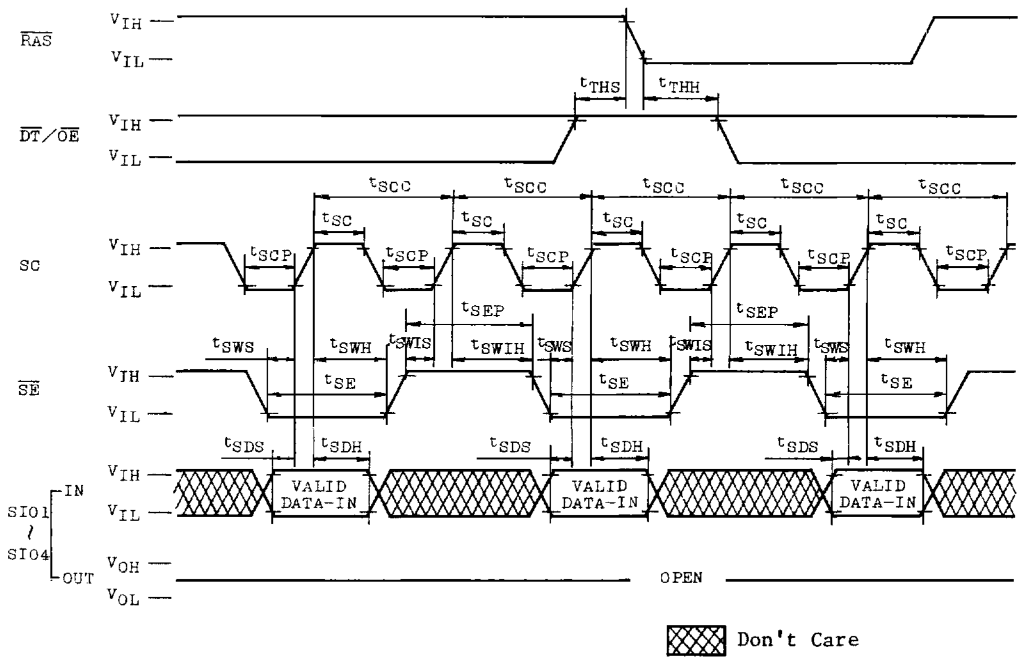
SERIAL READ CYCLE ($\overline{SE}$ CONTROLLED OUTPUTS)



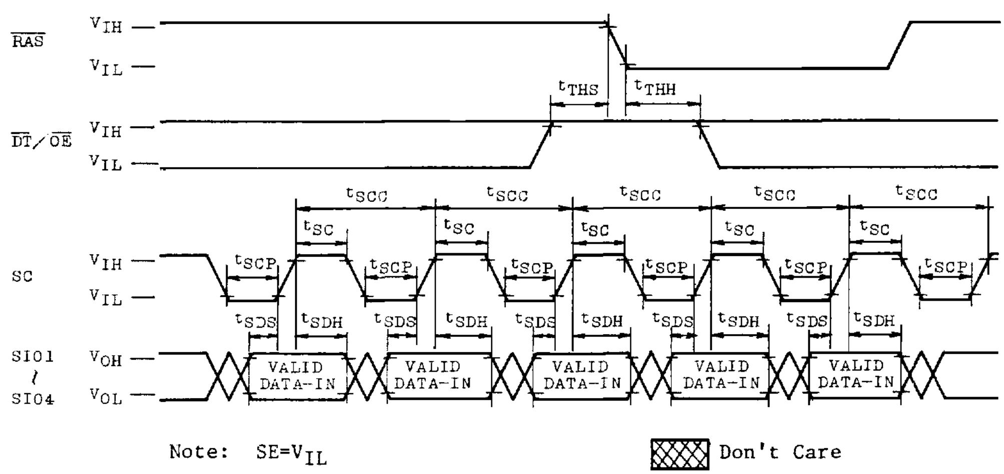
SERIAL READ CYCLE ($\overline{SE}$=V_{IL})



SERIAL WRITE CYCLE ($\overline{SE}$ CONTROLLED WRITE)



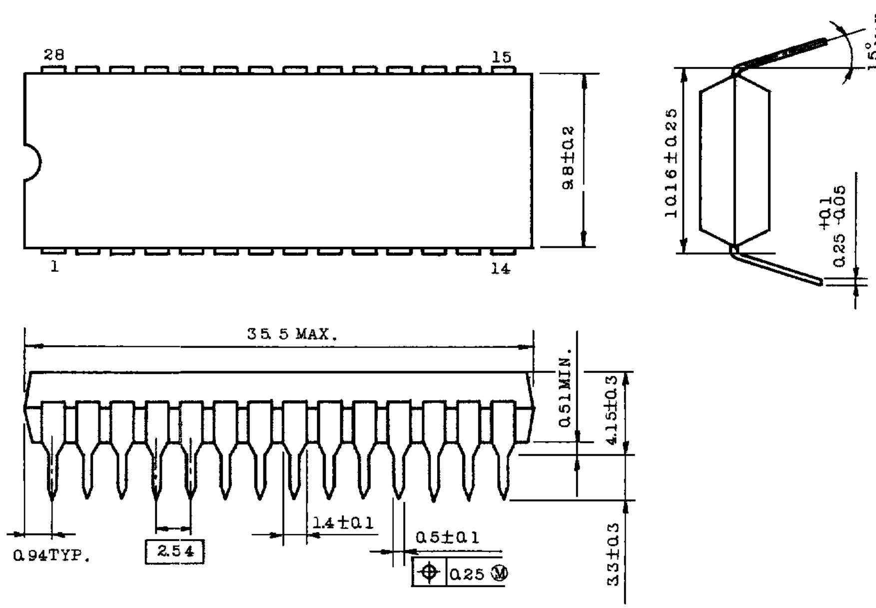
SERIAL WRITE CYCLE ($\overline{SE}=V_{IL}$)



OUTLINE DRAWINGS

• Plastic DIP

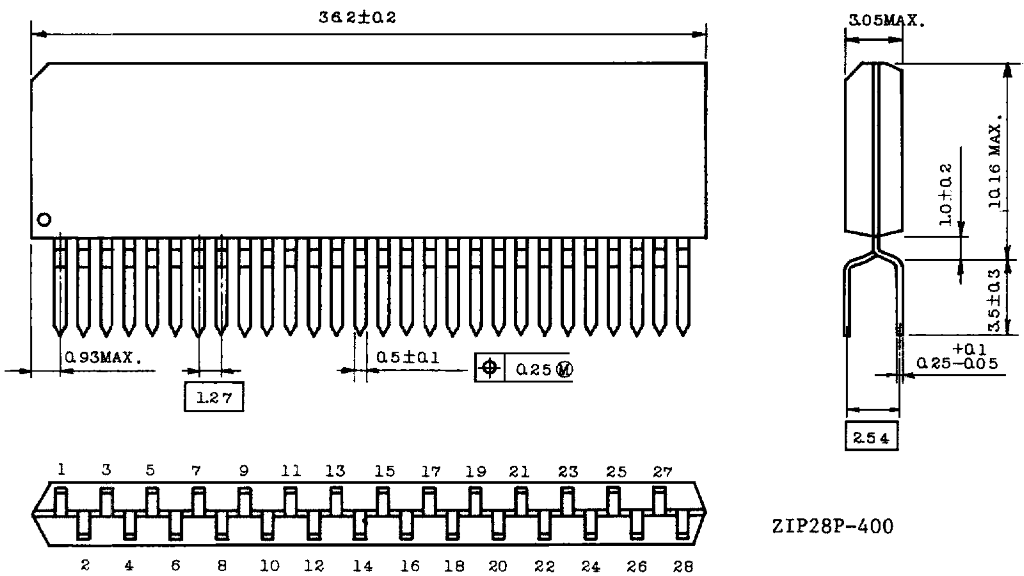
Unit in mm



Note: Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No.1 and No.28 leads.
All dimensions are in millimeters.

• Plastic ZIP

Unit in mm

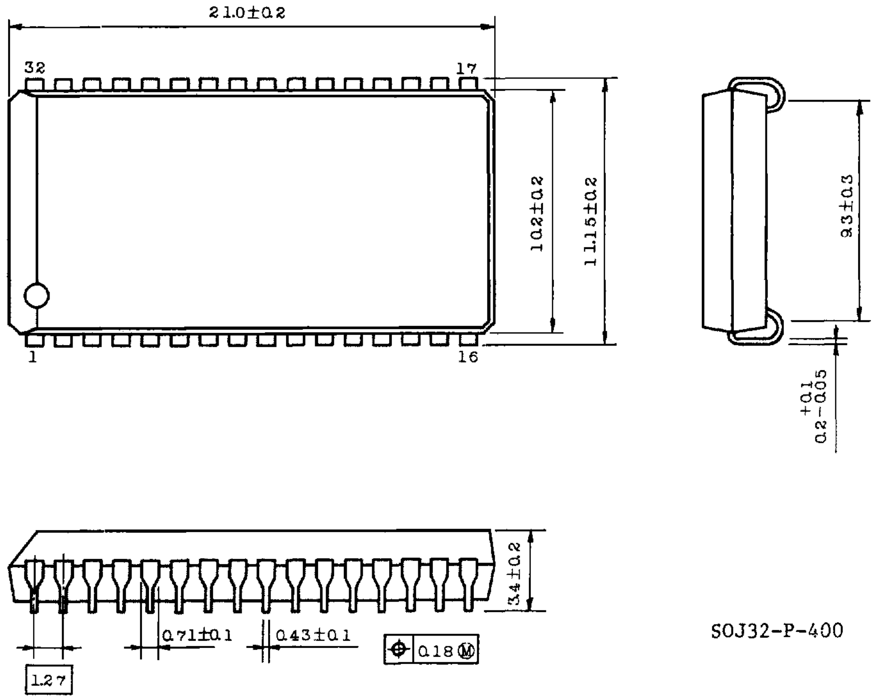


ZIP28P-400

Note: Each lead pitch is 1.27mm.
All dimensions are in millimeters.
Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

• Plastic SOJ

Unit in mm



SOJ32-P-400

Note: Each lead pitch is 1.27mm.

All dimensions are in millimeters.