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Getting the Best Performance From Video Digital-to-Analog Converters

When using high speed analog and digital logic, proper component selection, hardware, and printed circuit board layout becomes paramount in obtaining stable and noise-free performance.

Because VIDEODACs and RAMDACs contain part digital and part analog circuitry, the analog output signal is subject to degradation from power supply noise, ground loops, radiated pickup, and magnetic coupling. The mixture of digital and analog circuitry often requires some unique solutions due to the harmonic content of the waveforms. This application note will provide guidelines for both the design engineer and the printed circuit board designer to obtain the best performance from a VIDEODAC or RAMDAC.

For additional and more detailed product-specific layout considerations, refer to the specific product datasheet.

Ground Planes

In designing a board with high speed TTL logic, one should always use a ground plane under digital signal traces to minimize radiated noise and crosstalk.

Best performance from VIDEODACs is obtained by separating this ground plane into two separate areas, which are designated as digital ground and analog ground, with at least a 1/8" gap between the areas. The digital ground plane should encompass the area under all the digital logic including signal traces leading up to the DAC but excluding any ground pins on the DAC. The analog ground plane area should include all ground pins on the DAC, all reference circuitry (external reference if used, current setting resistors, etc.), the output traces and output connector(s).

The digital and analog ground plane areas should be connected at the lowest impedance source. For highly integrated devices, such as RAMDACs, it is recommended a common ground plane be used for both the digital and analog circuitry.

Power Planes

It is good design practice for dense PCB layout with high speed logic to include a power plane layer to minimize voltage drops, aid power supply decoupling, and improve noise margins.

For best DAC performance, the power plane should be separated into two areas, designated as analog and digital power, which lay on top of the analog and digital ground planes, respectively. The digital power plane will supply power to all digital logic on the board and the analog power plane will supply all power pins of the DAC, together with power for any reference circuitry.

It is important that portions of the digital power plane area do not overlay portions of the analog ground plane area and that portions of the analog power plane area do not overlap portions of the digital ground plane. This will prevent PCB plane-to-plane noise coupling. Finally, as with the ground planes, the analog and digital power plane areas should be tied together at a single point with a wire through a ferrite bead (such as Fair-Rite part no. 2743001111).

Power and ground return connections from the board to an external power supply should be made to the digital power and ground areas to minimize the DC current flowing through the ferrite beads connecting the analog and digital areas together.

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Supply Decoupling

Printed Circuit Boards

A four layer sandwich structure, with power and ground planes inside the board and signals on the top and bottom of the board, provides good high frequency decoupling by virtue of the distributed capacitance between the power and ground planes.

The addition of 0.1 μF ceramic capacitors at a density of one cap per one or two square inches is usually enough for lower frequency decoupling. For best DAC performance, a 0.1 μF ceramic capacitor should be placed as close to each DAC power pin as possible for bypassing the analog power and ground plane areas. For operation beyond 75 MHz, a 0.1 μF ceramic capacitor paralleled with a 0.001 μF chip capacitor is recommended.

If the display has "ghosting" problems, additional capacitance in parallel with the power supply and COMP capacitors may fix the problem.

Breadboards

In breadboards with a ground plane and point to point wiring for power, best DAC performance is achieved with chip capacitors in the 0.01 μF to 0.1 μF range connected between the power pins and ground (see discussion about sockets on next page). Also, in breadboards with point to point power wiring, a ferrite choke such as Ferroxcube part no. VK20019/4B should be placed between the DAC power pins and the power source for the digital logic. Breadboards with a prefabricated ground plane should have this plane cut into analog and digital areas as indicated in the earlier discussion on ground planes with a single point ferrite bead connection.

Signal Interconnect

Digital Inputs

The digital input signals to the DAC should be kept isolated as possible from the analog output(s) and other analog reference inputs to the DAC. Also, the digital input signals should run over the digital ground and power plane areas of the board (see earlier discussion on power and ground planes).

To minimize data undershoot, ringing, and resultant data feedthrough noise, interconnect distances should be kept as short as possible to the DAC inputs (less than 3 inches). Data feedthrough noise is also proportional to edge speed, so in lower speed applications, use of lower speed logic will reduce data related noise on the DAC output. Also one should avoid running long clock lines to the DAC since this is another source of noise pickup.

Finally, in some applications, use of parallel termination resistors at the DAC inputs can reduce digital noise. The terminating resistors, if used, should be the low inductance film type, and should be connected to the digital ground and power planes.

Analog Inputs

The DAC should be located as close as possible to its output connector(s) to minimize noise pickup on the analog output traces. Also it is usually more difficult to control the characteristic impedance on boards and minimizing the output line length will minimize reflections due to impedance mismatch. DAC reference circuitry should be kept close to the DAC to avoid stray pickup. DAC output signals should overlay the analog ground plane and not the analog power plane to maximize high frequency power supply rejection.

It is important to note that while DACs contain circuitry to reject power supply noise, this rejection decreases with increasing frequency. As an example, with a 0.01 μF compensation capacitor the power supply rejection on CMOS DACs flattens out to 20 dB at frequencies around 1 KHz. This means that if the user powers the DAC from a 20 KHz switching power supply with 100 mv of noise at 20 KHz and harmonics, that about 10 mV of this supply noise will be on the DAC output. If the designer does not use linear supplies, close attention should be paid to reducing supply noise and consider using a three terminal regulator for DAC power.

Bypass Capacitors

Probably the single most important external components which affect the noise performance of a DAC are the capacitors used to bypass the power supplies.

It is important to realize that at the frequencies generated by the logic that one wishes to bypass, most capacitors look like inductors. For example a 0.1 μF capacitor with 1/4 inch of lead length will self resonate at around 10 MHz and beyond this frequency will look inductive. Therefore the criterion for measuring the effectiveness of a given bypass capacitor is to note its lead inductance. In addition, bypass capacitors should be installed in printed circuit boards with the very shortest leads possible consistent with reliable operation.

Probably the most effective capacitor is the distributed capacitance between power and ground planes. However this capacitance is usually too small to sustain large current surges without excessive voltage change. Ceramic chip capacitors are the next most effective for bypassing applications and are highly recommended. The drawback of using chip capacitors in PCB applications are their tendency to crack in high shock and wide temperature ranges.

The third most effective capacitor type is the radial lead ceramic capacitor. Although they tend to be 5x to 10x larger then chip capacitors, they can still be acceptable when used in conjunction with ground and power planes. Capacitors which will not be effective for DAC bypassing include electrolytic and axial lead types.

In summary, there is no one right answer to bypassing which will suit all applications. However, the principle to keep in mind is that bypassing capacitors in conjunction with the distributed power supply plane inductance will determine the effectiveness of the decoupling.

Avoiding Latch-Up

Latch-up is a common concern with CMOS devices, where power supply differentials or sequences can induce the CMOS device to draw excessive current. Observe the following precautions to avoid latch-up in CMOS devices:

1. Tie all VAA pins together at the package pins.

2. Hold all logic inputs low until power to the device has settled to the specified tolerance. Avoid DAC power decoupling networks with large time constants which could ring indefinitely upon power.

Attenuation Beads

Ferrite beads are recommended to suppress interference due to the fast switching times of the DACs and decoupling noise on the power plane from getting to the DAC output. Some recommended attenuation beads are Ferroxcube part no. VK20019-4B, Fair-Rite part no. 2743001111, and Phillips part no. 431202036690. Figures 1 and 2 are the impedance and typical damping curves for several Ferroxcube brand wide band chokes.

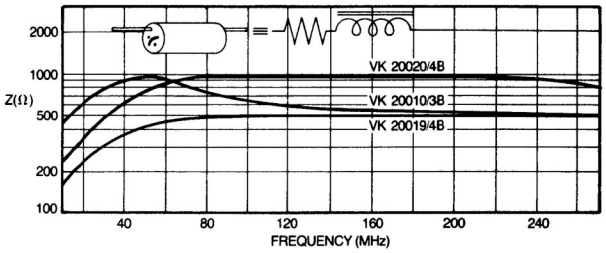

Figure 1. Impedance Curves of Wide-Band Chokes.

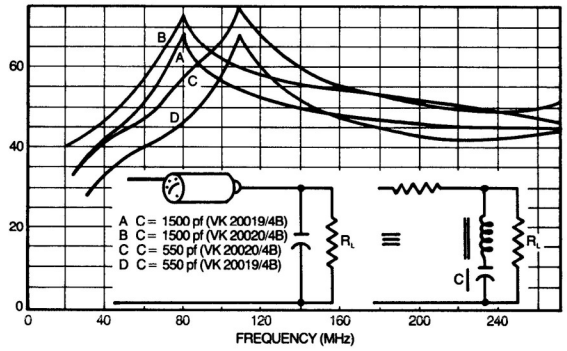

Figure 2. Typical Damping curves for VK Chokes with Additional Parallel Ceramic Capacitors.

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Note: The purpose of attenuator beads in the DAC ground path is to isolate DAC currents from high frequency system logic ground noise. The DAC must still have a low impedance return path to system ground to minimize logic threshold uncertainty and electromagnetic radiation. Bypassing the analog output sheaths to chassis ground is one method of accomplishing this.

Analog Output Protection

CMOS VIDEODACs and RAMDACs have no intrinsic protection on the analog outputs against high energy discharges, such as those from monitor arc-over or from "hot-switching" AC-coupled monitors.

The diode protection circuit shown in Figure 3 can prevent latch-up under severe discharge conditions without adversely degrading analog transition times. The 1N4148/9 are low capacitance, fast switching diodes, which are also available in multiple-device packages (FSA250X or FSA270X) or surface-mountable pairs (BAV99 or MMBD7001).

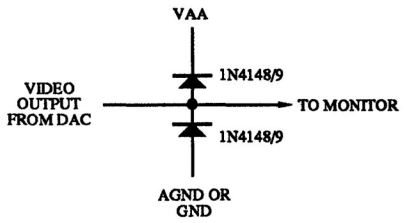

Figure 3. Output Protection Circuit.

Video DAC Essentials

A raster based graphics display terminal is comprised of a graphics controller, a frame buffer to hold the refresh data, optional color lookup tables, video DACs, and a CRT monitor. The video DAC subsystem has special requirements and performance parameters that will define the overall quality of the graphics presentation.

A simplified block diagram of a color graphics terminal using a color lookup table and three video DACs is shown in Figure 1. A monochrome or black and white monitor will use one lookup table and one video DAC. The interface to the computer system is the graphics display controller. The graphics controllers generates all the timing and interface signals to the video RAM, the color lookup tables, the video DACs and the deflection circuitry for the CRT.

The new generation of monolithic integrated circuits includes the color lookup RAM and the DAC, either as a single group or as a triple RAM and DAC combination (RAMDAC). The video amplifiers in the CRT block diagram are used to amplify the DAC output levels to the 40 to 200 volt levels required for the grids of the cathode ray tube. The deflection circuit block is used for the horizontal scanning and retrace portion of the video signal.

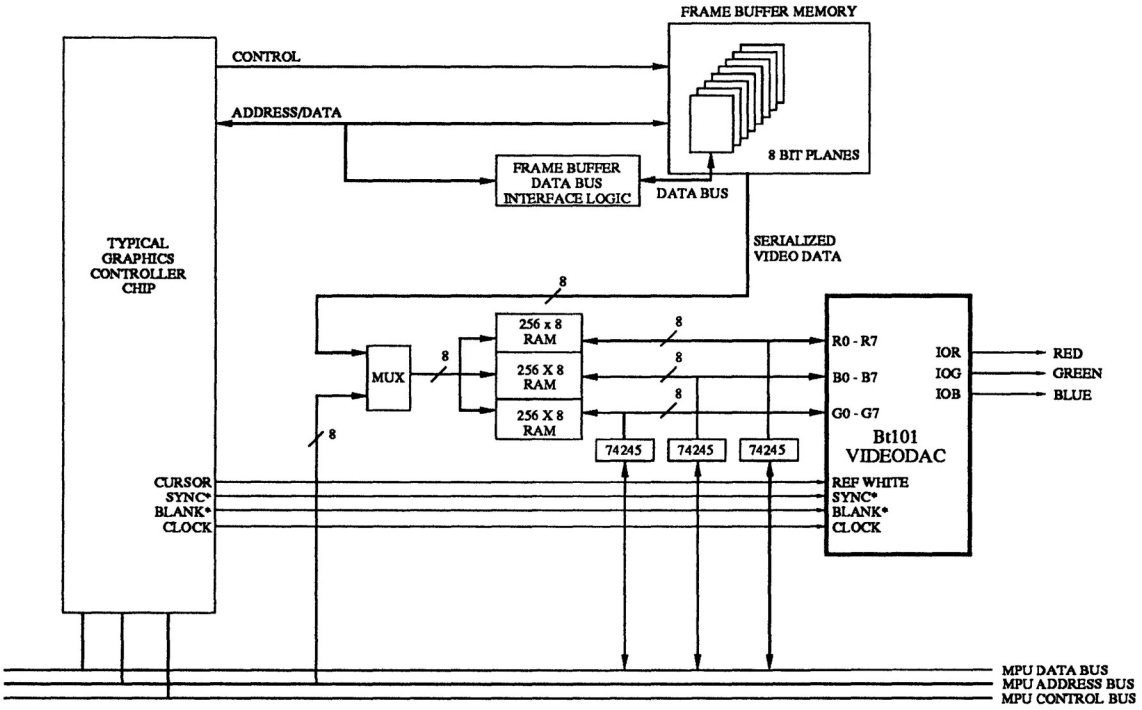

Figure 1. Simplified Block Diagram of a Color Graphics Terminal.

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Video Waveform

As raster scan video monitors are commonly used for computer graphics, a standard input signal (EIA standard RS-343A) has been defined. This standard defines the voltage level for each component of the video signal, as illustrated below in Figure 2. Note that the entire video signal is divided into three segments: sync, setup, and intensity information. A color CRT monitor requires three of these signals, one each for red, green, and blue.

In a color graphics system, the green video signal has a peak-to-peak amplitude of 1.0 volts. The red and blue video signals have a peak-to-peak amplitude of either 1.0 volts or 0.714 volts, depending on whether they have sync information present or not. Typically, sync information is present only on the green channel.

Sync information is defined to be 0.286v ± 0.05v, or 40+ IRE units. Sync is used to provide horizontal and vertical synchronization information to the CRT monitor. Separate sync monitors will have a fourth channel dedicated just to sync information.

The setup, which is the difference between the blank level and the reference black level, is defined as 7.5 ± 2.5 IRE units, or 0.054 ± 0.018 volts. At this level the CRT beam is visibly shut off, allowing it to retrace across the screen at the blank level to begin the next scan line.

DAC Bits	DAC Output Steps	Color Palette
1	2	8
2	4	64
3	8	512
4	16	4096
5	32	32,768
6	64	262,144
7	128	2,097,152
8	256	16,777,216

Table 1.

Intensity information, the interval between reference black and reference white, is assigned 92.5 ± 2.5 IRE units, or 0.660 ± 0.018 volts. It is typically composed of 16 discrete levels when 4-bit DACs are used, or 256 discrete levels when 8-bit DACs are used.

Thus, the DACs ultimately determine the number of colors available. Although many current systems use 4-bit DACs, most new designs are using 6- or 8-bit DACs to increase the number of available colors.

Table 1 illustrates the total number of available colors (color palette) for various DAC resolutions when used in a color graphics system. To substantially reduce system costs, most systems, compress data through the use of lookup table RAMs, allowing the user to display typically only 16 or 256 simultaneous colors of the total available color palette.

RED, BLUE		GREEN	
MA	V	MA	V
19.05	0.714	26.67	1.000
1.44	0.054	9.05	0.340
0.00	0.000	7.62	0.286
		0.00	0.000

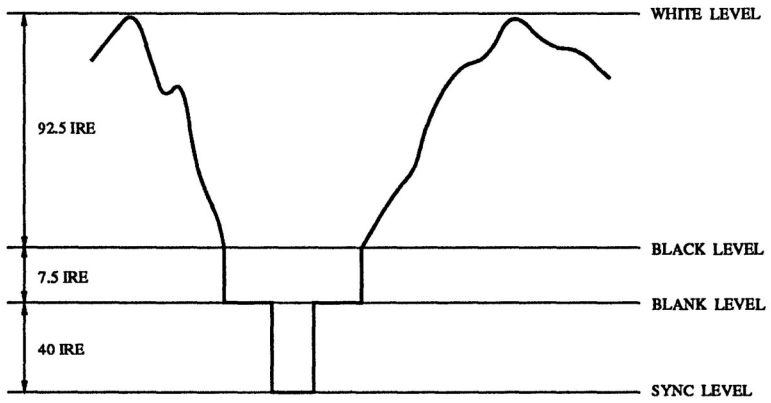

Figure 2. Standard Voltage Levels of RS-343A.

Video DAC

The video DAC converts the digital information to analog signals for the color guns in the CRT. A video DAC has several important parameters that will determine the overall performance of the display system. The update rate of the DAC sets the speed at which the pixels or dots can be displayed across the screen. The overall system speed is determined by the time it takes to scan across the screen and the time the monitor is blanked for retrace. Table 2 illustrates some of the common graphics resolutions and their video line rates.

Logic Interface

The type of logic interface can determine the overall system speed and the number of power supplies required. For a TTL type of system, the Schottky S series or the FAST series of logic must be used to obtain speeds up to 75 MHz. The regular Schottky families, such as LS or ALS, can be used in most cases up to 40 MHz. If the DAC is also compatible with CMOS logic levels, the 74HC series of gates can be used to 40 MHz. For speeds higher than 80 MHz, ECL logic is typically used. Either the 10K, 10KH, or 100K series will perform up to 125, 250, and 300 MHz respectively.

Resolution	Video Rate	Line Rate	# of 256K RAMs per Bit Plane
512 x 512	20 MHz	31.5 KHz	1
640 x 400	20 MHz	24 KHz	1
640 x 480	25 MHz	31.5 KHz	2
768 x 576	35 MHz	37 KHz	2
1024 x 800	75 MHz	52 KHz	4
1024 x 1024	95 MHz	63 KHz	4
1152 x 900	95 MHz	58 KHz	4
1280 x 1024	110 MHz	65 KHz	5
1600 x 1200	165 MHz	75 KHz	8
2048 x 1536	250 MHz	100 KHz	12

Table 2. Common Graphics Resolutions and Line Rates. (60 Hz Non-Interlaced Refresh Rate)

DAC Resolution

DAC resolution is a measure of how many individual steps there are between end points and a measure of how accurate each step relates to the next one. A 4-bit DAC output will have 16 discrete levels at 41.2 mV intervals, while an 8-bit DAC will have 256 discrete levels at 2.5 mV intervals (assuming 0.66 volts of color information). A typical video DAC will have a differential non-linearity of ±1 LSB or ±2.51 mV which determines the width of each step. The end result is a higher resolution and a smaller differential non-linearity value, which produces a more accurate control over the CRT beam intensity and the color quality.

In a TTL and CMOS system, only a single 5 volt power supply will be required. An ECL system will require a termination plane and a -5.2 volt power supply, while an ECL-TTL system will need a +5 volt, a VT, and -5.2 volt power supply.

DAC Termination

The video DACs output signal must interface properly with a video monitor and be able to drive a 75 ohm coax (the standard input impedance for the video monitors). Since the DAC is a current source, and the relation V = IR determines the signal level, the output is terminated into a 75 ohm load to develop the output voltage levels. As speeds increase, ringing and reflections in the cable may distort the waveform causing the termination at the monitor to be insufficient in maintaining the signal quality.

If termination is at the source and at the load, some video DACs will allow double termination. In such an instance, a 75-ohm resistor is placed near the output pin of the DAC to ground and the terminating impedance of the monitor serves as the load resistor. A diagram of the connections are shown in Figure 3.

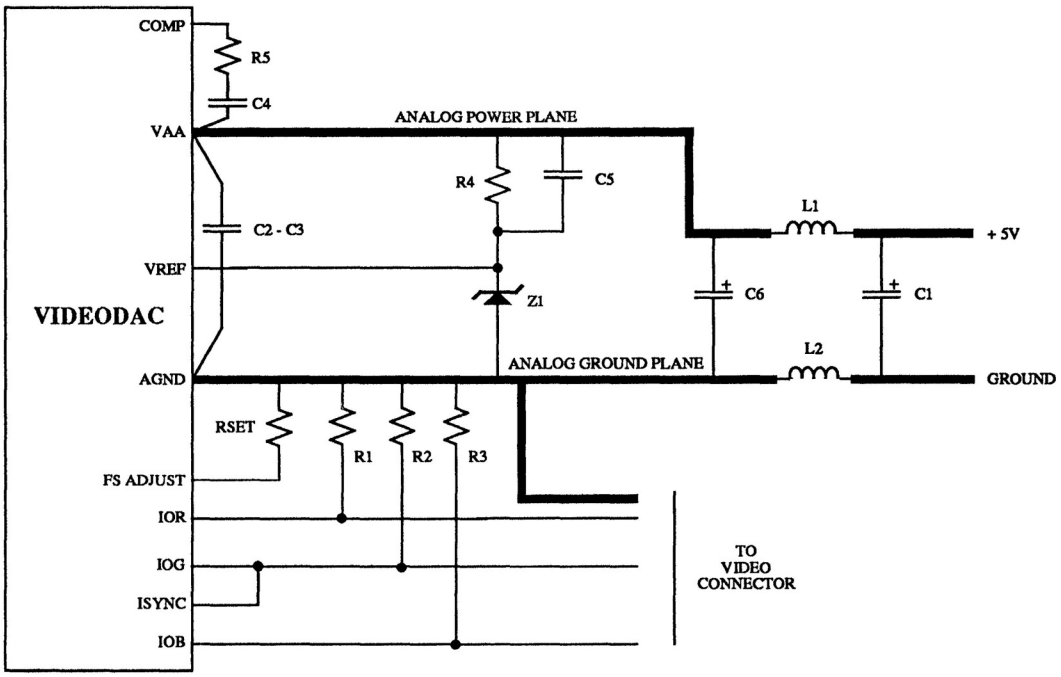

Figure 3. Typical Connection Circuit.

Glitch Impulse

Glitch impulse is a term used to define the area under the voltage-time curve of a single DAC step until the level has settled out to within the specified error band of the final value (the linearity error). Glitch impulse is important where subtle code changes can produce significant level changes, and is different from settling impulse which involves large amplitude changes.

Depending on the type of internal logic design in the DAC, the glitch energy can be very low (< 50 pV-sec) for a segmented architecture to as much as 250 pV-sec for a R-2R network. For many DACs, maximum glitch energy will occur when a transition is made between segments (which have the worst switching skew), where the count goes from 0111 1111 to 1000 0000. This is where all the internal registers will change and the current sources are turning on and off. Low glitch energy is necessary to avoid pixel color change or blurred pixels across the CRT. Figure 4 shows a typical DAC output glitch.

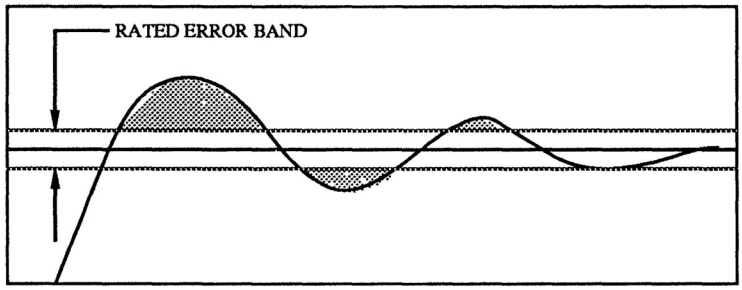

Figure 4. DAC Output Glitch.

In a video system, if the glitch energy is sufficiently low and repetitively consistent across all codes, it will be integrated over a period of time and will have no effect on the CRT screen. Other glitches generated by the DAC, such as data feedthrough and DAC-to-DAC noise may have a cumulative effect since the waveforms may not be repetitive. Therefore, good design practices in PC board design, power supply decoupling, and avoiding running digital signal lines near the DAC analog circuitry and output to the monitor should be observed. A suggested component placement is shown in Figure 5.

DAC-to-DAC skews greater than 1/4 pixel interval results in perceived color shift and resolution loss.

Rise/Fall Times

How fast a DAC output can switch from one voltage step to the next voltage step is measured from the 10% to 90% transition of the output waveform. In video applications, the faster the DAC the smaller this number will be. For a 30 MHz DAC, 3 to 10 ns would be typical, while for a 125 MHz DAC, 1 to 3 ns would be common. For very high speed DACs in the 250 MHz or greater speed range, rise and fall times under 1 ns are necessary. The output voltage slew rate is also a function of the load capacitance/termination and the addition of small values of capacitance can some times be used to reduce overshoot and ringing when very fast DACs are used.

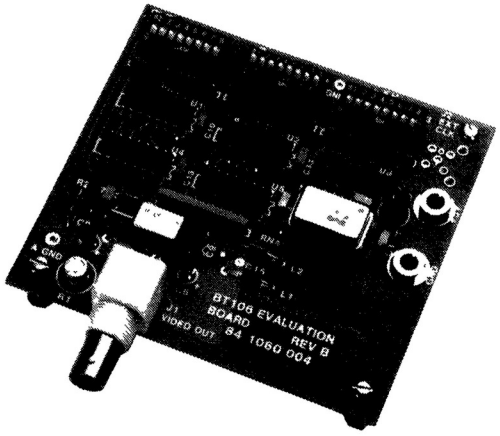

Figure 5. Typical Evaluation Module.

Settling Time

Settling time is a measurement of how fast a DAC output voltage from the mid-transition, settles to the desired value within an error band (e), typically ± 1/2 LSB.

In video applications, settling time is of moderate importance, since the CRT phosphors are being excited and the eye will not respond to the very small differences in light intensity of the pixel on the screen. Settling times greater than a pixel interval result in loss of color rendition or palette resolution.

Settling time is an important parameter if the DAC is being used in an instrumentation environment where it is necessary to have very accurate voltages as the input code is changed. Figure 6 describes both rise/fall time and settling measurements.

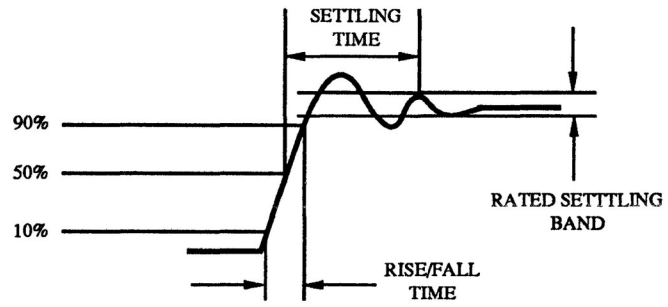

Figure 6. Rise/Fall Time and Settling Measurements.

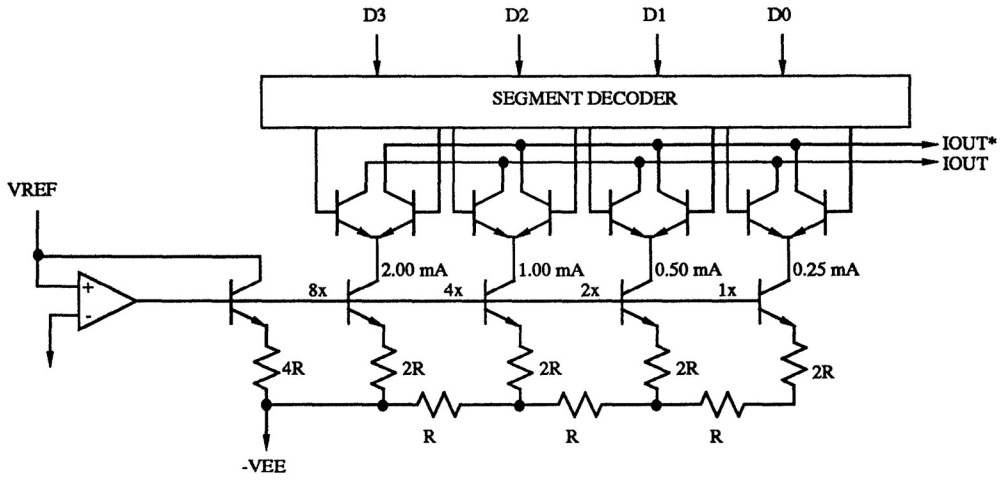

Figure 7. Typical R-2R DAC Network (4-Bit DAC).

DAC Internal Architecture

To generate the individual current steps, the simplest form of a DAC will use a R-2R summing resistor network. For an 8-bit DAC, eight current sources are used in a binary fashion to generate 256 output steps. While minimal components, the weaknesses of this design are: 1) the resistor ladder tolerances are critical, 2) the individual current steps range from large to small values, and 3) the temperature tracking of resistor pairs. Due to device tolerances, in order to obtain less than ± 1 LSB integral linearity error and ± 1 LSB of differential linearity error, it is necessary to match the resistors by laser trimming resistor links.

Figure 7 illustrates a typical R-2R DAC network. An improved type of circuit architecture, called a segmented DAC, offers low glitch energy and no trimming of resistors to obtain the needed accuracy. The segmented DAC utilizes the fact that monolithic transistors and resistors of the same geometry can match closely to each other and that cumulative geometry errors can be effectively averaged over the monolithic device area.

Some segmented DACs may use 256 individual current source transistors or a combination of segmentation for the higher order bits and a R-2R network for the lower order bits where speed, tolerance, and area determines the partition. Figure 8 shows a fully segmented DAC circuit topology.

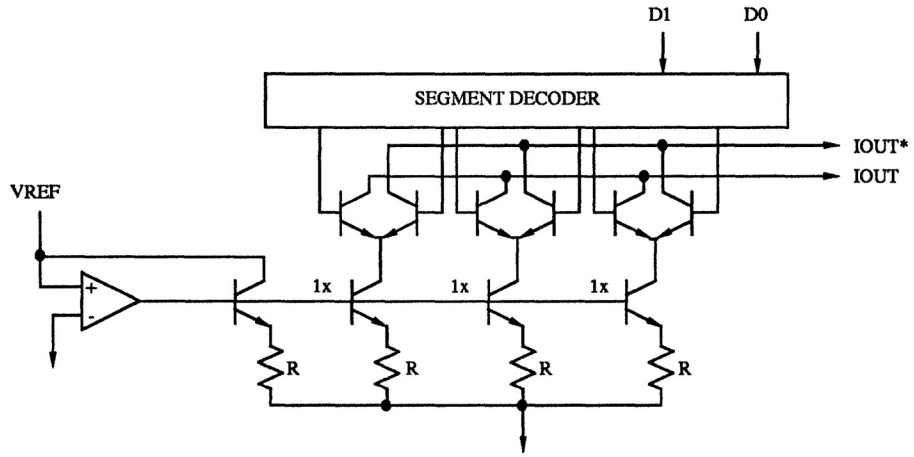

Figure 8. Segmented DAC Topology (2-Bit DAC).

Comparison of NTSC, PAL and SECAM Video Formats

There are several international standards for specifying the amplitude and video components of a waveform for use with television and video monitors which use a subcarrier for color or chrominance information.

In North America and Japan, the NTSC format is the standard, while PAL and SECAM video formats are used in Europe. A comparison of the various video levels is shown in Table 1 for reference, and Figure 1 is a drawing of a composite video waveform. The newer international standards specify a voltage amplitude of 0.714 volts between the blanking level and the white level for the video portion of the waveform (blanked video signal) and is defined as having 100 IRE units. The black to blank level (typically referred to as the setup) is used to shut off the beam during the retrace time and varies between the formats. The total amplitude is about 140 IRE units (143 IRE units for PAL and SECAM) from sync tips to reference white for monochrome, with a saturated subcarrier.

An older standard known as RS170A is also used in the United States and differs from RS343A level for the voltage level from blank to white. The RS170A blanked video level is 1.00 volts as compared to the RS343A, PAL, and SECAM levels of 0.714 volts.

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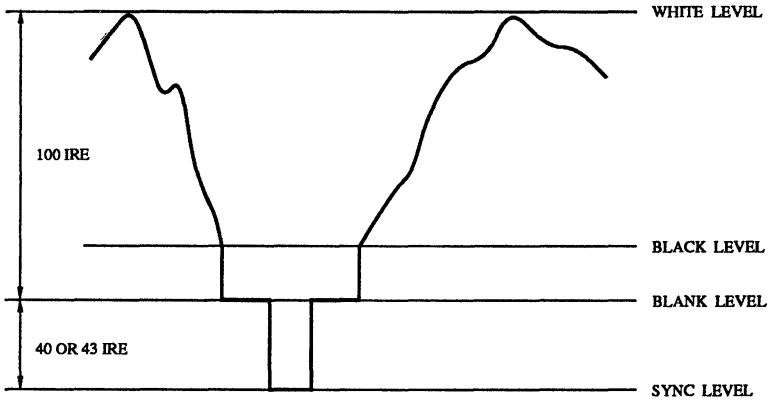

Figure 1. Composite Video Waveform.

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The monochrome version of the RS-170A standard (RS-170) does not have a subcarrier for color or chrominance information.

The sync levels (40 IRE units for NTSC and 43 IRE units for PAL and SECAM) are sufficiently close enough in tolerance that the 40 IRE levels of the Brooktree VIDEODACs and RAMDACs will meet the PAL and SECAM tolerance.

The RS-343A standard is commonly used for computer graphics, and of the four standards previously mentioned, it and RS-170 are the only ones that do not use a subcarrier for color or chrominance information. Rather, three separate signals (red, green, and blue) are generated, each containing intensity and blanking information. Typically, only the green channel contains sync information.

To assist users who need to determine the output current when terminated into 75 ohm and 37.5 ohm (doubly-terminated 75-ohm) loads, a comparison chart is shown in Table 1. Brooktree DACs are specified to drive doubly-terminated 75-ohm loads, while many competitor DACs can only drive a singly-terminated 75-ohm load and develop the proper video output voltage level.

	Video Output Levels	IRE Units	Volts	mA (typ.) (75-ohm load)	mA (typ.) (37.5-ohm load)
NTSC RS-343A*	Blank to White	100 IRE	0.714 ± 0.1	9.52	19.04
	Blank to Black	7.5 ± 5 IRE	typ. 0.054	0.714	1.43
	Blank Level		0	0	0
	Blank to Sync	typ. 40 IRE	- 0.286 ± 0.05	- 3.81	- 7.62
NTSC RS-170*	Blank to White	100 IRE	1.0 ± 0.05	13.33	26.67
	Blank to Black	7.5 ± 2.5 IRE	typ. 0.075	1	2
	Blank Level		0	0	0
	Blank to Sync	40 ± 5 IRE	typ. - 0.4	- 5.33	- 10.67
NTSC RS-170A**	Blank to White	100 IRE	1.0 ± 0.05	13.33	26.67
	Blank to Black	7.5 ± 2.5 IRE	typ. 0.075	1	2
	Blank Level		0	0	0
	Blank to Sync	40 ± 5 IRE	typ. - 0.4	- 5.33	- 10.67
PAL**	Blank to White	100 IRE	typ. 0.714	9.52	19.04
	Blank to Black	0 IRE	0v	0	0
	Blank Level		0v	0	0
	Blank to Sync	typ. 43 IRE	typ. - 0.307	- 4.09	- 8.19
SECAM**	Blank to White	100 IRE	typ. 0.714	9.52	19.04
	Blank to Black	0 to 7 IRE	0 to 0.049	0	0
	Blank Level		0	0	0
	Blank to Sync	typ. 43 IRE	typ. - 0.307	- 4.09	- 8.19

*no color or chrominance subcarrier -- requires three channels for RGB.
**uses color or chrominance subcarrier -- Bt102 is suggested VIDEODAC.

Table 1. Comparison Of Video Formats.

Other items of interest when comparing the various video formats are the number of lines per frame, field frequency, and normal video bandwidth:

	RS-170A	PAL	SECAM
Number of lines per frame	525	625	625
Field frequency	60	50	50
Luminance Bandwidth (MHz)	4.2	5	6
Chrominance Subcarrier (MHz)	3.58	4.43	4.3 to 4.4
Chrominance Bandwidth (MHz)	0.5 to 1.5	1.3	1.3

Table 2. Comparison of Video Formats.

Since chrominance subcarrier formats generate output levels between blank and sync levels (to generate color burst information during the back porch time), the sync and blank control inputs to most DACs cannot be used in such applications. The 20 IRE gap between sync and the most negative color burst level represents a 15% loss in gray scale range just to encode the sync.

This can be improved by asserting sync information through an external current sink rather than through the DAC data bits. Figure 2 shows a circuit using a transistor array (3227) biased off a negative supply voltage. The delay through the external sync switch should roughly match that through the DAC including any pipeline delays. Fast CMOS switches (4316 type) can perform the same function using resistor summing (rather than current summing), with some attendant degradation in output impedance match or return loss (3% or 30 dB is common for industrial grade, while 10% or 20 dB suffices for consumer applications).

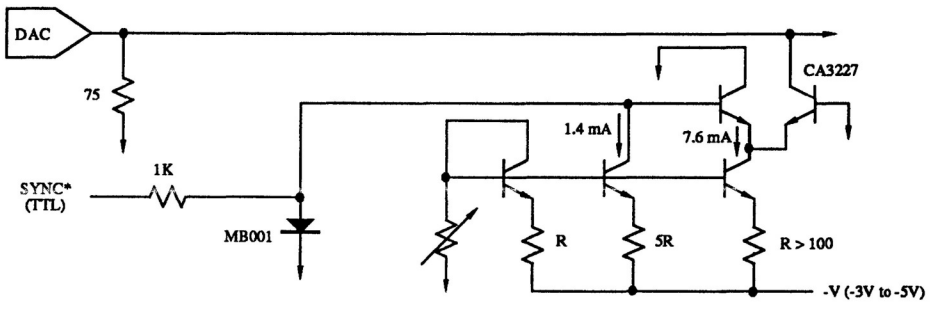

Figure 2. External Sync Circuit for NTSC RS-170A, PAL, and SECAM.

Component Analog Video Formats

In recent years, the trend has been toward component analog video (CAV) formats, much like the RGB format of most computer graphics systems.

The major video equipment CAV formats currently in use are summarized in Table 3 at a standard color saturation level of 75%, which is the common "legal" limit to the chrominance subcarrier's amplitude range in the NTSC format.

GBR is the matrix decoded version of NTSC with sync added to all three channels, which may be extended to 700 mV gray scale at 100% saturation with a PLUGE offset for monitor black/white adjust. Reversal of the non-complex RGB to GBR format is consistent with the green signal corresponding to the Y or luminance signal in the other color difference (B - Y and R - Y) formats.

The BetaCam and MII are the popular Sony and Matsushita formats respectively, each of which come in 3 or 2 wire versions and involve the Component Time Division Multiplexed (CTDM or CTCM) nomenclature in the latter case.

The Society for Motion Picture and Television Engineers (SMPTE) and the European Broadcasting Union (EBU) have adopted their own color difference formats in order to remove brand name association. Most CAV formats sample the color difference components at half the rate or bandwidth of the luminance signal (the common 4:2:2 hierarchy, not to be confused with the RS-422 interface). Most CAV formats have no use for the 7.5 IRE setup used in NTSC, which represents a 7.5% loss in dynamic range. Hence, the newer CAV standards (GRB and SMPTE/EBU) call for no setup pedestal.

Format	Video Output Function	Signal Amplitude (Volts)	Comments
GRB	G, R, B Sync	+ 0.700 - 0.300	at 100% saturation, 0% setup three wire = (G + sync), (R + sync), (B + sync)
BetaCam*	Y Sync R - Y, B - Y	+ 0.714 - 0.286 ± 0.350	at 75% saturation, 7.5% setup on Y only three wire = (Y + sync), (R - Y), (B - Y)
BetaCam*	Y Sync CTDM R - Y CTDM B - Y Sync	+ 0.714 - 0.286 ± 0.350 ± 0.350 - 0.630	at 100% saturation, 7.5% setup on Y only two wire = (Y + sync), CTDM [(R - Y), (B - Y + sync)]
MII†	Y Sync R - Y B - Y	+ 0.700 - 0.300 ± 0.324 ± 0.324	at 100% saturation, 7.5% setup on Y only three wire = (Y + sync), (R - Y), (B - Y)
MII†	Y Sync CTCM R - Y CTCM B - Y Sync	+ 0.700 - 0.300 ± 0.350 ± 0.250 - 0.650	at 75% saturation, 7.5% setup on Y only two wire = (Y + sync), CTCM [(R - Y), (B - Y + sync)]
SMPTE	Y Sync PB PR	+ 0.700 - 0.300 ± 0.350 ± 0.350	at 100% saturation, 0% setup three wire = (Y + sync), PB, PR

*Trademark of Sony Corporation.
†Trademark of Matsushita Corporation.

Table 3. Popular Component Analog Video Output Formats.

Using the Overlay Palettes on Brooktree RAMDACs

What are Overlay Palettes?

Brooktree RAMDACs usually include an overlay palette, consisting of one or more registers, in addition to the normal color palette RAM. For triple RAMDACs, each overlay register contains 12 or 24 bits of color information (for triple 4-bit or triple 8-bit D/A converters, respectively). For single RAMDACs, each overlay register contains 8 bits of color information (assuming an 8-bit D/A converter).

To support the overlay palette, besides the normal pixel input ports, the RAMDACs have palette selection inputs, OLx. These inputs specify, on a pixel basis, whether color information is to be provided by the color palette RAM or one of the overlay registers.

Why are Overlays Useful?

In many instances, the graphics application software is primarily concerned with the generation and manipulation of images in the frame buffer. The system software, on the other hand, is usually responsible for cursor movement, menu insertion and deletion, and user messages, with minimal concern about the graphics image.

The use of one or two additional bit planes for overlays enables the system software to control user interface graphics independently of the graphics image. Graphics performance is improved, as the image in the frame buffer need not be modified each time the cursor is moved or a menu is displayed or removed. The problem of cursor avoidance during the image drawing process is also solved by implementing the cursor using an overlay approach.

Generating Overlay Information

Overlay information may be generated by using additional bit planes in the frame buffer, which would be interfaced directly to the overlay inputs of the RAMDAC. Thus, the designer is able to keep the graphics data and overlay data in separate memory, simplifying software and increasing graphics performance.

If a VLSI graphics processor is used, the cursor output may be connected to the one of the overlay inputs of the RAMDAC. Thus, whenever the graphics controller outputs cursor information, the appropriate overlay register is automatically selected. Additional bit planes or external hardware may still be used for menus, grids, alphanumeric overlays, etc., by using any other overlay inputs of the RAMDAC.

Some high performance graphics systems implement hardware cursors using discrete or VLSI logic. Again, the cursor information may interface directly to one of the overlay inputs of the RAMDAC. Additional bit planes or hardware, connected to the other overlay inputs may be used for any additional overlay functions. Four bits of overlay can emulate an enhanced graphic adaptor window atop the main graphics image.

Summary

Overlays provide a means of simplifying the implementation of user interface mechanisms such as cursors, menus, and any type of graphics or text information that is to be displayed independent of the main graphics image.

The separation of system user interface software and graphics generation software will usually increase graphics performance and simplify software interfacing to the graphics system.

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Rev. B

Expanding Personal System/2® Graphics With the Bt471/476/478 Family

The new IBM Personal System/2 introduces more graphics display versatility to personal computer software and calls for more versatile digital-to-analog converters to take advantage of the greater software power. The Bt471/476/478 family of pin compatible RAMDACs support the basic capabilities of the IBM hardware as well as several added performance features which help differentiate board-level products in the compatible PC and expansion board markets.

The Bt471/476/478 family features more palette colors, higher speeds, overlay planes, simultaneous composite video and read-back, and surface mount packaging. These features afford the board designer flexibility and component savings for positioning his product in a dynamic marketplace.

Performance Features

Enhancements to the IBM hardware implementation (based on their Video Graphics Array) include:

A. Programmable choice of 262K or 16.7 million color palette. On the Bt478, a single pin programs the length of the palette word to be either 6 or 8 bits per color channel. For business graphics or false color renderings 6 bits is adequate, but for pleasing pictures of subtly shaded objects, 8 bits per channel is now standard on most Computer Aided Engineering (CAE) workstations and in the new Apple Macintosh II. More precise color segmentation can compensate for monitor inconsistencies (such as gamma effect) and reduce the "cartoon" appearance of color-limited palettes.

B. A 4-bit overlay port on the Bt471 and Bt478 makes special effects, such as cursors, borders, or even full EGA windows easy to implement on pixel-by-pixel boundaries, without the additional microprocessor burden of updating the pixel read mask for special effects.

C. A fully synchronous read-mask feature eliminates the need to externally synchronize the MPU write strobe to the pixel clock.

D. Support of both sync and MPU read-back on the Bt471 and Bt478 provides direct compatibility with RS-343 monitors without sacrificing future software system or self testing capabilities. The IMSG171 device offers one or the other of these features, but not both, in one unit. Selectable setup levels (0 or 7.5 IRE) allow the user to optimize the retrace intensity for each monitor assuring international hardware compatibility.

E. The Bt471/476/478 family also offers a choice of more stable voltage references, or a cheaper current reference that is 100% compatible with the existing PS/2® hardware.

F. More robust output capability for driving doubly terminated cables greater distances (or looped thru more monitors) with crisper transitions and lower reflection "ghosts". Brooktree guarantees linearity in terms of peak errors (not RMS) under doubly-terminated conditions. The coaxial medium between the DAC output and the monitor input calls for superior pulse fidelity to reduce amplitude ringing and monitor mistermination which can make pixels appear fuzzy, jittery or to have shadows.

G. An efficient 44-pin PLCC surface mount package occupies less board area than the 28-pin DIP counterpart. The lower PLCC profile improves power supply feedthrough and grounding as well by lowering package inductance 50%.

H. The Bt476 offers a pin-compatible solution to the IMSG176, and is available in both the 44-pin PLCC and the 28-pin DIP package.

8

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Implementing Enhanced Graphic Overlays

The new PS/2 graphics format is distinguished by its higher vertical resolution, variable frame rate, and its 8-bit pixel architecture. To take advantage of multi-frequency monitors, the IBM 8514A resorts to interlacing at higher resolutions to provide near megapixel displays at a reasonable price, supporting interlaced 1024 x 768 resolution at a 43.5 Hz refresh rate. Since interlacing compromises display phosphor response to reduce flicker, faster pixel rates are desirable to achieve 60 Hz refresh rates without flicker or smearing. Non-interlaced 60 Hz formats of 1024 x 768 or 1024 x 1024 can be supported by the 80 MHz Bt471/478.

The non-interlaced formats keep the full 640 pixel horizontal resolution of the previous CGA, EGA and PGC formats while giving the preferred 4:3 aspect with 480 vertical lines at a frame rate of 60 to 70 hertz (320 x 200 with pixel replication). The 8-bit pixel word size provides for 256 simultaneous colors from a palette of 262K colors (6 bits per channel) or 16.7 million colors (8 bits per channel with the Bt478).

As the power of the VGA to do complex graphic operations in real time becomes fully supported by the software industry, it will be possible to mix various formats on screen to create sophisticated windows, cursors and overlays. The independent palette access provided by the overlay ports on the Bt471/478 will enable parallel generation of graphic effects without imposing additional MPU limitations.

The use of a read mask in the IMSG171 to generate special effects is fully supported (internally synchronous) in the Bt471/476/478, but it's update rate is limited by the MPU write cycle time of 3 to 4 pixel clocks. This means that the mask effect will appear no finer than several pixels on the screen. This may save palette RAM size but prohibits high resolution overlays such as an EGA style window over a large part of the viewing screen. In situations where pixel frequency must be agile and independent of the MPU clock, the synchronous buffering of the Bt471/476/478 prevents corruption of the palette contents, something that can occur with asynchronous IMSG171s when the pixel clock is not locked to the MPU clock.

The four overlay inputs to the color palette can be loaded and invoked in the same manner as the standard palette. An additional register select pin(RS2) is provided for loading and reading back the overlay values. In the read mode the overlay inputs override the P0 - P7 pixel inputs, so any unused pixel and overlay inputs should be tied low. This parallel palette access simplifies cursor or cross hair generation to where a single chip (such as the Bt431) can manage this function with direct connection to the overlay inputs of the Bt471 or the Bt478.

With proper synchronization and raster scaling through the feature connector common on EGA cards, direct superposition of an EGA image over a VGA display is possible without burdening the VGA interface. This multi-path approach to high resolution windows is inherently faster and more interactive than software driven techniques and compares with hardware window features found on the more sophisticated graphics systems processors. This technique can be done on a pixel-by-pixel or bit-by-bit basis so that the full resolution capability of the multi-frequency monitor can be used.

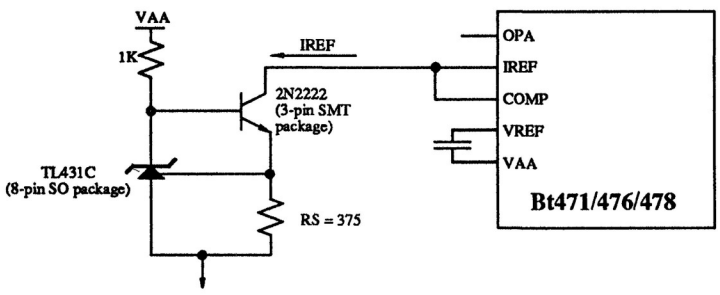

Figure 1. External Current Reference.

Suitable References

The quality of the image produced by the DAC can depend on the stability and regulation of it's reference. The Bt471/476/478 family offers the user a choice of current or voltage references so that either drop-in compatibility or optimum performance can be provided. The 28-pin DIP version of the Bt476 supports the only current reference.

The Bt471/476/478 family uses the voltage reference in a closed feedback loop control circuit which provides each individual current cell with a stable voltage reference. This common voltage reference can be externally decoupled at the compensation pin to minimize noise disturbance due to current switching. The combination of closed-loop stability, direct reference decoupling, and compatibility with low temperature coefficient voltage references gives the Bt471/476/478 superior amplitude stability and noise immunity. This results cleaner images on the graphics display monitor.

Figure 1 shows a typical current reference circuit for the Bt471/476/478. All these components are available in surface mount packages, but you will note the current reference approach requires 2 or 3 additional passive components. The simplest 4 mA current reference available, a Motorola MCL1304 or Siliconix CR430 type JFET device, offers only ±15% to ±25% accuracy, which would only be tolerable in analog-EGA applications or where the monitor contrast adjustment could compensate.

Setup and Sync

While the IBM-PC graphics standards have always provided for separate TTL synchronization lines, traditional analog monitors work with composite synchronization super-imposed on the green video channel. The Bt471/478 devices provide composite sync on all channels by asserting a low pulse on the SYNC* pin, which turns off an internal 40 IRE pedestal on each video channel.

Blank assertion in the composite format is more reliable (form a noise standpoint) if a 7.5 IRE pedestal distinguishes the black and blank voltage levels. This setup level provides for blacker-than-black CRT beam retraces which reduce visible retrace lines on bright displays. For this reason a selectable setup pedestal is provided to optimize the sync and blank interface for most multi-frequency analog monitors and various international raster video formats (NTSC, PAL, SECAM, CCIR, etc).

Optimum Termination

The analog interface between the RAMDAC and the display monitor must have transmission line properties to assure proper pixel definition on the display. Where TTL monitors can tolerate pulse ringing and cable echoes due to their binary nature, analog displays must settle to within 1% amplitude accuracy well within the pixel duration to render 6- or 8-bit color values faithfully. Double termination of the coaxial cable with the characteristic impedance of the cable is desirable in that it lowers the lumped time-constant at the DAC node and attenuates signal reflections from the monitor (or loop through nodes), which can produce pixel smearing or ghosting with cables longer than 2 meters.

A lower termination resistance at the DAC node neutralizes the connector and cable capacitance but forces the DAC to put out as much as 30 milliamps to produce 1v peak to peak at the monitor input. A lower time constant produces faster transitions and settling, which means crisper pixels on the display with truer color rendition.

Figures 2 and 3 depict the 64 code steps of the IMSG171 and Bt471 driving a 75-ohm doubly-terminated load. A Tektronix 2465 scope was used in the expanded sweep mode to highlight the mid-scale glitch that occurs during the binary 31 to 32 code transition. The characteristic 1/4 - 1/2 - 3/4 scale glitches of the IMSG171 are evident on the 700 mV amplitude waveform.

The expanded scale is calibrated to give graticle square areas of 500 pV-sec (100 mV * 5 ns). The mid-scale glitch of the IMSG171 consists of clock feedthrough with an approximate impulse area approaching 200 pV-sec, while the Bt471 mid-scale glitch area is less than 50 pV-sec. Clock feedthrough has no visible aberration on the monitor since it represents an equal amount of energy every pixel. However, glitch impulse may be visible since it occurs only on specific code transitions.

Resolution

The Bt478 offers an upgrade path to 8 bits of resolution in the same pin compatible package as the Bt471 and Bt476. Figures 4 and 5 show a comparison between 6 bits and 8 bits of resolution for a 3D solid model.

The gray scale shading can been seen limited and annoying to the eye on the 6-bit rendering offering only 64 shades, while the 8-bit image offers 256 gray shades and fine shading. The 8-bit photo clearly shows the smooth shading required for 3D modeling or professional slide presentations.

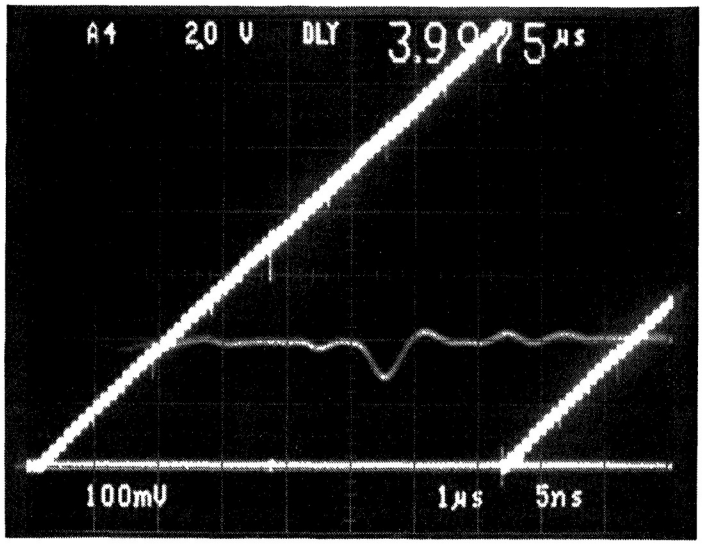

Figure 2. IMSG171 Output Waveform.

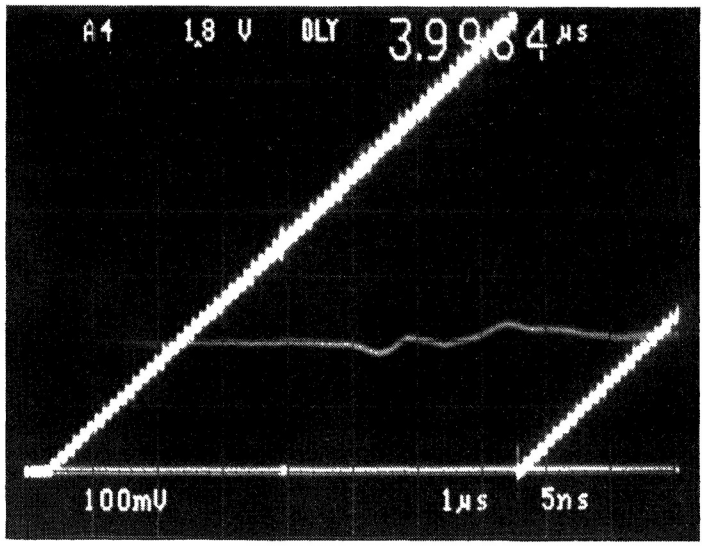

Figure 3. Bt471/478 Output Waveform.

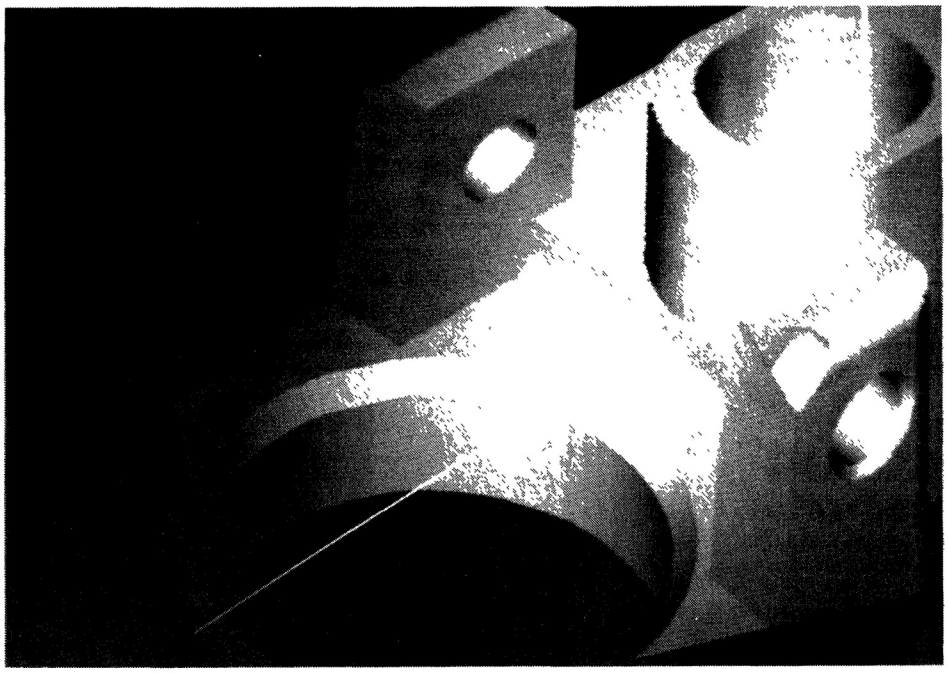

Figure 4. 6-Bit Resolution Example.

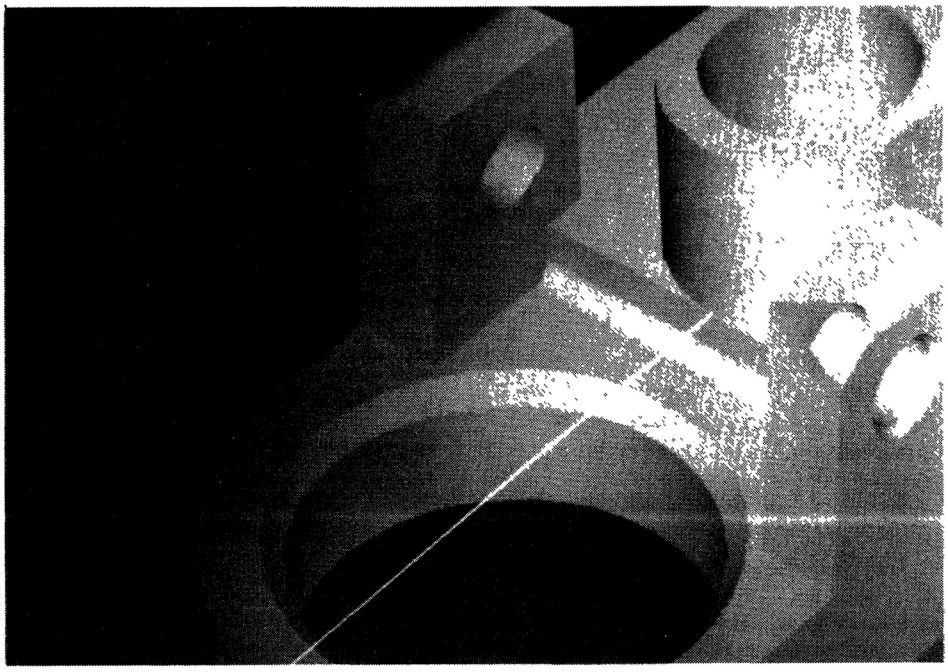

Figure 5. 8-Bit Resolution Eample.

Packaging

The IMSG171 is photographed side by side with the Bt471/478 in Figure 6. The Bt471/478 is shown in the ceramic 44-pin package and occupies considerably less area than the IMSG171 in the 28-pin DIP.

Note the internal chip capacitor in the specially-tooled 28-pin DIP package of the IMSG171. The chip capacitor mounted in the cavity serves to compensate for the DIP package inductance. This is less effective in terms of glitch suppression than the inherently lower inductance of the 44-pin PLCC package.

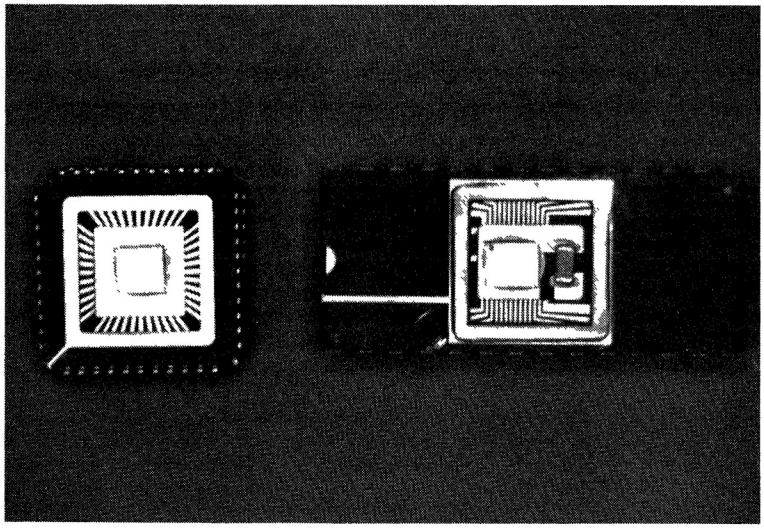

Figure 6. Packaging Comparison.

PC Board Layout Tips

Printed wiring board design considerations for analog output devices can be more critical than for pure digital. Four-or-more layer boards are better for lower power and ground noise as well as for segregating the analog outputs and reference from the digital inputs. This becomes even more important as speed migration from 25 MHz to 75 MHz dictates faster devices which generate more power supply spikes and radiation. Migrating from 6 bits per channel to 8 bit quantization compounds the need for low inductance power and ground returns if true color rendition and low electromagnetic emissions are to be achieved.

The effect of supply and ground noise and digital edges on the palette DAC is to produce image-dependent artifacts on the display which are especially perceptible when images are superimposed. Even the best CMOS DACs couple about 10% of any supply noise to the analog output. Care should be taken to limit supply noise at the DAC (in the bandwidth of the analog channel, typically the pixel rate) to 10 times the amplitude of the least significant bit.

Multiple ground planes make it possible to isolate the DAC current return to the system supply from other digital circuitry while maintaining low plane-plane potentials which affect the digital noise margins and contribute to electromagnetic emissions. It is desirable to reduce DAC ground noise to less than 10 mV during the active display line for clean looking 6-and 8-bit displays.

Performance Comparision Chart of Bt471/476/478 vs IMSG171

	Bt471	Bt476	Bt478	IMSG171
IBM PS/2 Compatible	YES	YES	YES	YES
Number of Displayable Colors	256 + 15	256	256 + 15	256
Maximum Number of Bit Planes	12 (8 + 4)	8	12 (8 + 4)	8
Total Palette Size	256K	256K	256K or 16M	256K
Frequency (MHz)	35 / 50 / 66 / 80	35 / 50 / 66	35 / 50 / 66 / 80	35 / 50
Palette Read-Back	YES	YES	YES	YES
On-Board Sync	YES	NO	YES	NO
Full Scale Reference	Voltage + Current	Voltage + Current	Voltage + Current	Current
RS-343A and CCIR Standards	YES	YES	YES	NO
Integral Linearity	0.25 LSB (0.5%)	0.5 LSB (1%)	1 LSB (0.5%)	0.5 LSB (1%)
Differential Linearity	0.25 LSB (0.5%)	0.5 LSB (1%)	1 LSB (0.5%)	monotonic
Glitch Impulse	75 pV-sec	75 pV-sec	75 pV-sec	200 pV-sec
Overlay Capability	YES	NO	YES	NO
Rise/Fall Time	3 ns	3 ns	3 ns	8 ns**
Memory Technology	Fully Static	Fully Static	Fully Static	Req. Constant Clock***
Compatible Family	YES	YES	YES	Almost*
Monolithic	YES	YES	YES	On Board Chip Cap
Surface Mountable	YES	YES	YES	NO
Package	44-pin PLCC	44-pin PLCC or 28-pin DIP	44-pin PLCC	28-pin DIP

* Due to limited number of pins in the INMOS pin-out, trade-offs have been made between products. For example, the pin that allows the color palette to be read in the IMSG171/3/6 is used for SYNC in the IMSG170/2/4 thereby inhibiting the ability to read back the color palette on the later parts. Also, the 6-bit data used in the IMSG170/1/2/3 can not be used directly with the 8-bit IMSG174/6 because the 6 bits are located in the LSBs and would result in an output 1/4 the brightness. Brooktree has a 6/8-bit pin that allows 6-bit code written for either the Bt471/476 or the IMSG170/1/2 to run on the 8 bit Bt478.

**single 75-ohm termination
***psuedo-static RAM cell

NOTE: Comparisons are based on the Brooktree Bt471/476/478 specification sheet L478001 Rev. L and the IMSG171 specification sheet 42-1008-00 dated April 1987.

Troubleshooting Your Brooktree CMOS VIDEODAC or RAMDAC

Power Supply Considerations

The noise on the power pins must be kept to a minimum. Brooktree devices offer some power supply rejection, however, this noise rejection decreases with frequency. In particular, about 10% of any frequency components over about 1 MHz will be coupled onto the output. The VREF and COMP pins should be checked to assure noise is minimized. This can be accomplished by keeping PCB and lead lengths to decoupling capacitors short and wide. Decoupling VREF and COMP pins to VAA is vital to reducing switching noise and overshoot on the DAC output.

Another useful technique is to mount a three terminal regulator close to the power supply pins to provide immunity to power supply transients, and use the fact that the regulator will provide excellent power supply ripple rejection. When operating from a switching supply with greater than 100 mV of noise, a two stage VAA decoupling filter is advisable. A CLC pie filter combination ahead of the attenuator bead should have a time constant value much less than the switching frequency to be effective. With a VAA filter approach, care should be taken to assure VAA power is applied before the inputs to prevcnt latch-up.

Always probe the power supply signals with an oscilloscope probe at the device pins. The DAC can have significantly more noise than is seen on the supply bus. Probe ground (AC coupled) less than one inch on DAC ground. Measure VREF noise relative to VAA.

Decoupling Capacitors

One of the most common problems is choosing the proper power supply decoupling capacitors and keeping the leads short enough. Refer to recommended capacitor types in individual datasheets. All capacitors exhibit a self-resonant point at which they no longer look like capacitors, but inductors. This resonant point is a function of frequency, capacitor material, lead length, and the PCB trace length of the power and ground traces where the capacitor is soldered into. Above self resonance, a capacitor looks like a series resonant inductor (with approximately 1 nH per 0.1 inch of lead length).

For example, a 0.1 µF ceramic radial lead capacitor with 1/4 inch leads generally resonates around 10 MHz. A 0.01 µF ceramic radial lead may resonate around 40 to 60 MHz while a 0.01 µF ceramic chip capacitor may resonant around 400 MHz.

As power supply transient frequencies approach the resonant point, the capacitor offers less effective filtering. At resonance, it is neither a capacitor nor inductor. Past resonance, it becomes an inductor, and may exhibit transmission line effects.

To overcome these problems, the parallel connection of a 0.1, 0.01, and 0.001 µF capacitors will generally overcome the most difficult transients. For the lower frequencies, a 10 µF tantalum capacitor is the best choice, mounted near the power and ground pins.

Attenuator Beads

The purpose of the ferrite attenuator beads is two-fold. First, they isolate fast transients (i.e., less than 1 ns) on the regular PCB power and ground planes from the device. They will reduce any fast transients and act as increasing AC resistance with frequency. These frequency vs. impedance characteristics are diagramed in Application Note 1. Therefore a decoupling capacitor close to the bead and the DAC power pin for long lead length is needed. Second, the ferrite beads also isolate high-frequency noise generated by the VIDEODAC or RAMDAC from being coupled back onto the main PCB power and ground planes.

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Experience has found that the ferrite beads are usually not required where the video bandwidth is less than one tenth the time constant of the logic. As an approximation, if the clock rate is less than 10 MHz beads are usually not necessary, but become increasingly important for frequencies above 50 MHz.

Many of Brooktree devices have signal edges on the order of 2 or 3 ns, which produces harmonic components in the 300 MHz to 500 MHz range. The beads attenuate these components from the PCB supply planes.

When using Surface Mount Technology (SMT) beads, watch the current rating. Bipolar DACs may use ferrite breads on their power pins for stability, while CMOS DACs are for noise rejection. Attenuator beads in the DAC ground return must have tens of ohms resistance at high frequency to be an effective attenuator. However, this can produce ground potentials of greater than the intrinsic noise margin when DAC currents are greater than 100 mA. Therefore ground beads are not recommended for DACs with dynamic currents of greater than 100 mA.

Digital Input Considerations

Some of the newer TTL logic families have very fast rise/fall times. It is possible for these fast transients to couple onto the analog outputs, resulting in excessively noisy analog signals.

Possible solutions are to put a 33 to 100 ohm limiting resistor in series with the digital inputs at their source, or use a resistor terminating network (220/330 ohm) at the expense of additional power. A slower logic family, such as ALS, LS, may be used if possible to reduce the input rise/fall times where pixel rates are less than 25 MHz. Noise on three-state lines should be avoided through termination.

ESD and Latchup Considerations

Correct ESD handling procedures are required to prevent damage which can produce symptoms of catastrophic failure or an erratic device behavior with somewhat leaky inputs.

Latchup can be prevented by assuring all power pins are at the same potential, that VAA is applied before the inputs voltage (power-up sequencing), and that there is no overshoot/undershoot on the input/outputs (schottky clamping diodes can limit these excursions).

No Video Information

Verify all power pins should have the correct voltage.

If a constant DC output is generated, it indicates that the DACs are probably not functioning correctly. The voltage on the VREF pin should be checked first to verify that the external voltage reference (if required) is operational. Decoupling of VREF to VAA near the DAC is vital to reduce switching noise on the DAC output.

The voltage on FS ADJUST should be very close to the VREF voltage. If the device contains an on-chip reference, the measured voltage at the FS ADJUST pin should be approximately equal to the specified internal reference voltage. Offsets of greater than 10 mV may indicate damage to the internal op-amp.

The COMP pin must be coupled to VAA through a ceramic capacitor and the lead lengths keep to an absolute minimum. The voltage on the COMP pin is nominally 3v to 4v. A voltage close to 0v or 5v indicates a bad COMP capacitor, a COMP trace shorted to power or ground, or a bad device. The output traces for video information should be checked for shorts to power and ground supplies.

The control, pixel, and overlay input setup and hold times should be verified. To ensure reliable operation over the full temperature and power supply range, the CLOCK input should be buffered by a single dedicated buffer that assures fast edges, with glitch free levels.

Incorrect Analog Output Information

If sync and blank information are output, but they are not the correct levels, verify the RSET resistor value, the voltage on VREF and FS ADJUST (they should match), and the output load. When looking at the voltage levels on the video outputs, the oscilloscope probe must have 75-ohm termination, to form the other termination of the doubly-terminated 75-ohm load.

If the sync and blank levels are correct, the analog section of the device is probably operational, and the problem is probably the microprocessor or pixel data interface.

Ensure that all of the control registers and color palette RAM are properly initialized following power-up. The contents of the control registers and RAM may be read back by the MPU to verify their contents. The chip select or chip enable input should always be a logical one, except when the MPU is accessing the device.

Nonlinear Gray Scale Analog Output

If the gray scale video appears to be nonlinear or compressed at one end of the gray scale, the compliance limits of the device are probably being exceeded.

Voltage levels on the analog outputs outside the compliance limits forces the DACs to operate in a nonlinear fashion. The greater the exceeded voltages, the more nonlinear the D/A operation will be. Incorrect output loading, a wrong value for the RSET resistor, or an incorrect reference voltage are the primary causes.

Noisy Analog Output

Excessively noisy analog outputs indicates that either the power supply pins, the COMP pin, or the VREF input have an excessive amount of power supply noise that is not being decoupled, or there is excessive undershoot/overshoot on the digital inputs.

Refer to Application Note 1 or contact the Brooktree technical hotline for further assistance at:

(800) VIDEO IC

RAMDAC Initialization

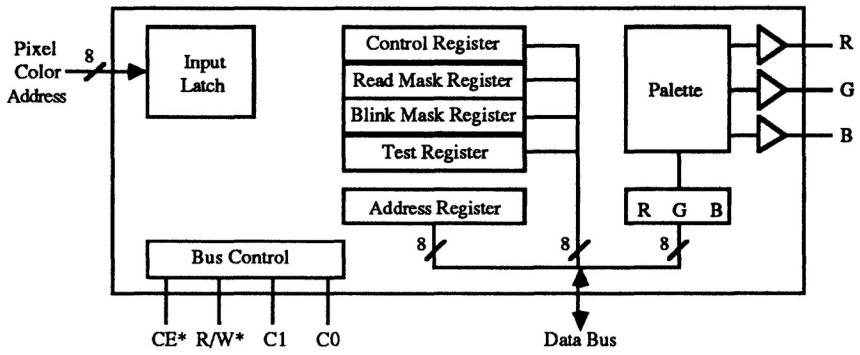

Figure 1. Bt458 Ports

Brooktree RAMDACs need to be initialized through the microprocessor port after power-on. This application note gives step-by-step instructions to the software programmer.

The initialization procedure differs slightly depending on how many control registers the RAMDAC contains. This application note uses the Bt458 as an example. Figure 1. shows the four Bt458 control registers, the pixel port (fast port), MPU port and bus control (slow port), and the DAC outputs. The microprocessor initializes the Bt458 through the MPU port. The following procedure explains a typical initialization of the Bt458.

Initialization Procedure

1. Initialize the control registers:

- Write 0,0 to C1,C0 ; set to write address register
- Put 06H on data bus ; address of command register
- Pull R/W* low ; write mode
- Strobe CE* ; write address to address register
- Write 1,0 to C1,C0 ; set to write command register
- Put 40H on data bus ; data to command register
- R/W* low, Strobe CE* ; write to command register

Note: 40H in the command register configures the device as follows:

- 4:1 mux
- Enable color palette RAM
- Blink rate = 16/48
- Blink disable
- Forces overlay inputs to logical zero

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Repeat the control register sequence using the following values to initialize the other command registers. Set R/W* and strobe CE* after every line.

C1,C0	Data Bus	
• 0, 0	04H	; write read mask address
• 1, 0	FFH	; FF hex to read mask register
• 0, 0	05H	; write blink mask address
• 1, 0	00H	; 00 hex to blink mask
• 0, 0	07H	; write test register address
• 1, 0	00H	; 00 hex to test register

2. Write the color palette starting with location 00 hex. Set R/W* and strobe CE* after every line.

C1,C0	Data Bus	
• 0, 0	00H	; write palette address 00H
• 0, 1	rrH	; write red value (hex)
• 0, 1	ggH	; write green value (hex)
• 0, 1	bbH	; write blue value (hex)

Note: At this point, the palette address pointer auto-increments to address 01H. One must rewrite the address pointer to access locations other than 01H.

C1,C0	Data Bus	
• 0, 1	rrH	; write red value (hex)
• 0, 1	ggH	; write green value (hex)
• 0, 1	bbH	; write blue value (hex)

3. To read back the palette or control registers, use the same sequencing but set R/W* high.

4. To write/read the overlay palette; set C1,C0 to 1,1 and continue as in step **2.**

Conclusion

This application note explains a basic program flow for initializing a Bt458 RAMDAC. The Brooktree databook contains further information concerning operation of this and other RAMDACs.

Bt458 INITIALIZATION PROGRAMMING SEQUENCE

TABLE OF OPERATIONS

	STEP	CE*	R/W*	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0	COMMENT
Command Register	1	↓	0	0	0	X	X	X	X	X	X	X	X	WRITE ADDRESS REGISTER
	2	↑	X	X	X	0	0	0	0	0	1	1	0	DATA 06H INTO ADDRESS REGISTER
	3	↓	0	1	0	X	X	X	X	X	X	X	X	POINT TO CONTROL REGISTER
	4	↑	X	X	X	0	1	0	0	0	0	0	0	DATA 40H INTO CONTROL REGISTER
Read Mask	5	↓	0	0	0	X	X	X	X	X	X	X	X	WRITE TO ADDRESS REGISTER
	6	↑	X	X	X	0	0	0	0	0	1	0	0	DATA 04H TO ADDRESS REGISTER
	7	↓	0	1	0	X	X	X	X	X	X	X	X	POINT TO READ MASK
	8	↑	X	X	X	1	1	1	1	1	1	1	1	DATA FFH TO READ MASK
Blink Mask	9	↓	0	0	0	X	X	X	X	X	X	X	X	WRITE TO ADDRESS REGISTER
	10	↑	X	X	X	0	0	0	0	0	1	0	1	DATA 05H TO ADDRESS REGISTER
	11	↓	0	1	0	X	X	X	X	X	X	X	X	POINT TO BLINK MASK
	12	↑	X	X	X	0	0	0	0	0	0	0	0	DATA 00H TO BLINK MASK
Test Register	13	↓	0	0	0	X	X	X	X	X	X	X	X	WRITE TO ADDRESS REGISTER
	14	↑	X	X	X	0	0	0	0	0	1	1	1	DATA 07H TO ADDRESS REGISTER
	15	↓	0	1	0	X	X	X	X	X	X	X	X	POINT TO TEST REGISTER
	16	↑	X	X	X	0	0	0	0	0	0	0	0	DATA 00H TO TEST REGISTER
Write Color Palette	17	↓	0	0	0	X	X	X	X	X	X	X	X	WRITE TO ADDRESS REGISTER
	18	↑	X	X	X	0	0	0	0	0	0	0	0	DATA 00H TO ADDRESS REGISTER
	19	↓	0	0	1	X	X	X	X	X	X	X	X	POINT TO PALETTE RED
	20	↑	X	X	X	RED VALUE								DATA TO RED PALETTE
	21	↓	0	0	1	X	X	X	X	X	X	X	X	POINT TO PALETTE GREEN
	22	↑	X	X	X	GREEN VALUE								DATA TO GREEN PALETTE
	23	↓	0	0	1	X	X	X	X	X	X	X	X	POINT TO PALETTE BLUE
	24	↑	X	X	X	BLUE VALUE								DATA TO BLUE PALETTE
Read OVL0	25	↓	0	0	0	X	X	X	X	X	X	X	X	WRITE TO ADDRESS REGISTER
	26	↑	X	X	X	0	0	0	0	0	0	0	0	DATA 00H TO ADDRESS REGISTER
	27	↓	1	1	1	X	X	X	X	X	X	X	X	POINT TO OVERLAY PALETTE 0
	28	↑	X	X	X	RED VALUE								RED VALUE AVAILABLE
	29	↓	1	1	1	X	X	X	X	X	X	X	X	POINT TO OVERLAY PALETTE 0
	30	↑	X	X	X	GREEN VALUE								GREEN VALUE AVAILABLE
	31	↓	1	1	1	X	X	X	X	X	X	X	X	POINT TO OVERLAY PALETTE 0
	32	↑	X	X	X	BLUE VALUE								BLUE VALUE AVAILABLE

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Building a 4K Lookup Table with the Bt457

Palette Applications

The need for a 4K lookup table for graphics is found in such applications as medical imaging, solids modeling and electronic publishing. A discrete implementation using three Bt457 single channel RAMDACs, twenty-four 4K x 4 static rams and miscellaneous MSI circuitry is all that is needed to implement this application.

The circuitry for one of the three channels is shown in Figure 1. This would be duplicated for each of the Red, Green and Blue channels. Each channel interfaces to the twelve plane frame buffer with two F374 devices. Four sets of 12-bit pixels are supplied to the registers from the frame buffer. Since the RGB planes use the same address, these registers can be used for all three channels.

The register's outputs are sent to the address inputs of the 4K x 4 static rams. Eight of these are needed for each of the three channels. The output data is then input into another set of F374 registers. The data has now been reduced to eight bits, which is used as pixel data. Four sets (A-D) of 8-bit pixel data is provided to the pixel inputs of the DACs for color generation. This provides 4:1 multiplexing of the Bt457 input.

Mapping the Bt457 internal LUT RAM allows the pixel data to be used as 8-bit data for the D/A converter, or the Bt457 RAMs can be programmed so that gamma correction, image manipulation or window palette switching can be performed.

MPU Interface

The microprocessor interface to the color palette is provided by a 12-bit address bus and an 8-bit data bus for each of the channels.

The address bus is presented to the RAMs by way of 2 F244 devices. These provide an output enable such that during a display, the F374s are always enabled and the F244s are disabled. The same address would be provided to each of the look-up tables.

The MPU data interface is a bit different. First, a bidirectional bus is needed so that the data stored in the color palette can be read back by the MPU. For this reason F245 devices are used. Second, each of the RGB channels is provided with it's own 8-bit Data bus. By using a 32-bit bus the red, green, and blue palettes can be written simultaneously. A counter can be included to generate the addresses so that the 4K addresses can be auto-incremented. The direction of the data bus is determined by the value on the RD* line. 8-bits are also needed for the RAMDAC MPU interface.

If direct color generation is needed, the Bt457 palette wouldn't be used as a lookup table, and the pixel address would be the same as the data. If gamma correction, or any other image transformation is needed, then the RAMDAC would need to be programmed accordingly.

Performance

The limiting factor in building the 4K solution discretely is the overall performance of the video generator. The screen resolution is directly related to the speed of the MSI circuitry and the static RAMs. The delay of the pipelines is as follows:

F374 Clock to Q	10 ns
Static RAM access(read)	20 ns
F374 Setup Time	2 ns
Interconnect delay	4 ns
Total delay	36 ns

Because 4:1 multiplexing is used, the time for each pixel generated is 36/4 = 9 ns. This corresponds to a clock frequency of 111 MHz. With this implementation a 1280 x 1024 resolution system (with 60Hz refresh) can be achieved. To increase the performance of the system, use of faster VRAMs (33 MHz), or a 2:1 multiplexing between the VRAMs and LUT is required.

An 8:1 LUT architecture could also be used. This would require multiplexing the output of the LUT to the Bt457 and also a significant cost increase due to a doubling in the amount of SRAMs.

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Another approach to increase the resolution of the system is to use faster RAMs as they become available. By using SRAMs with a 15 ns access time, the given architecture can achieve a video rate of 129 MHz.

True Color Application

A true color (36 plane) system can be achieved by multiplexing data from a frame buffer with the LUT output as shown in the diagram. The F374 outputs would be disabled via True Color Select, and the true color data would be enabled on the red, green , and blue channels.

Summary

Using the Brooktree Bt457 RAMDAC, a 4K color palette system can be created with the use of standard MSI products and CMOS Static RAMs. The 4K palette provides enough simultaneous color for modeling applications and medical imagery. It can be easily implemented using the methods described in this application note.

This information is intended for stimulating design interest and has not been breadboarded. Brooktree accepts no liability for designs contained in this application note. All users are cautioned to verify their own design.

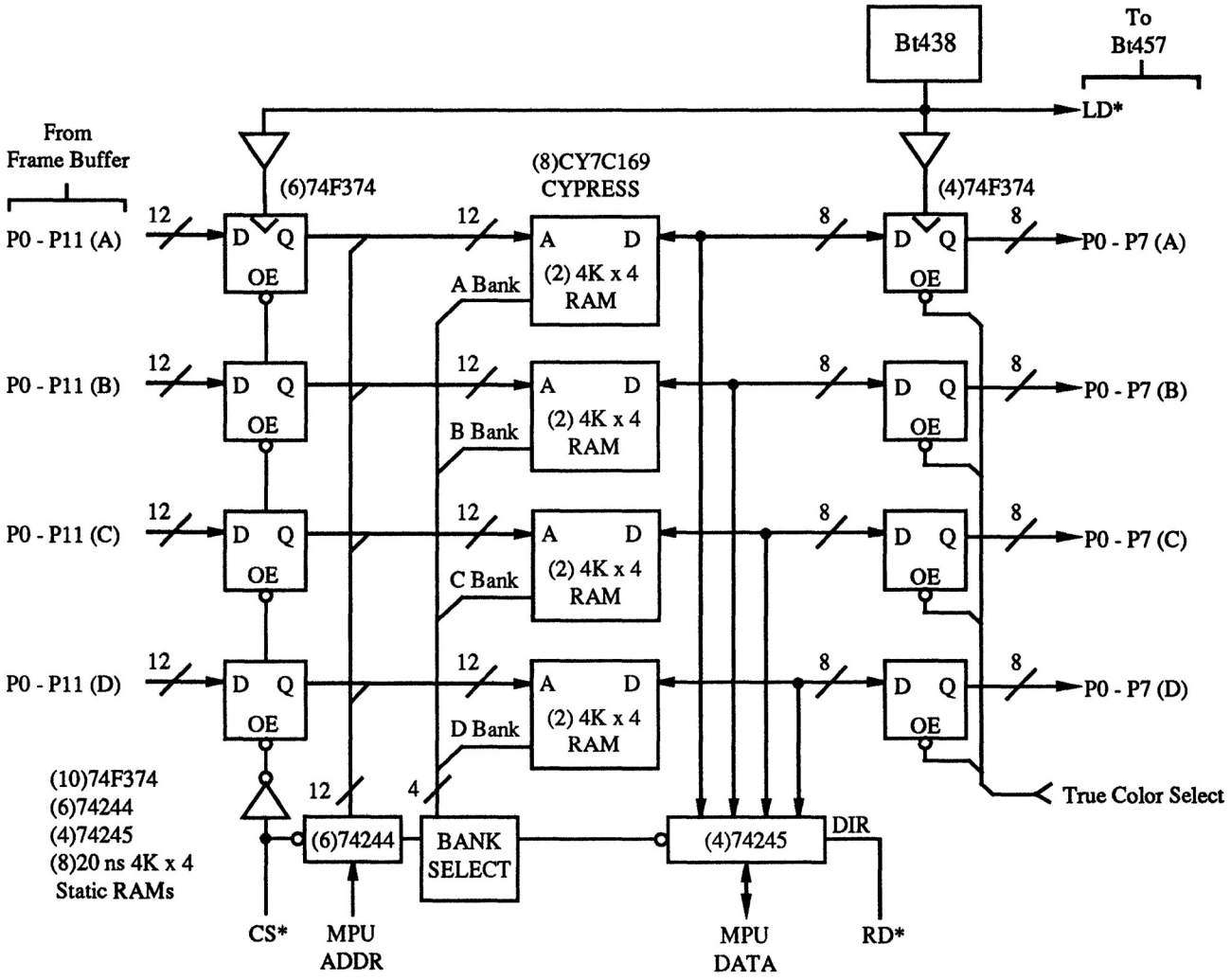

Figure 1. 4K Lookup Table Solution using the Bt457

Bt471/476/478 Power Saving Features

This application note will discuss various circuit configurations which will allow significant savings in power requirements when used with the Bt471/476/478. Laptop computers which support VGA graphics capabilities represent an application that can benefit from utilizing these power saving configurations. When operated from battery power in the portable mode, laptops use liquid crystal displays which do not require the VGA RAMDAC to be active. In such circumstances, the Bt471/476/478 power saving modes can be used to reduce supply requirements and extend battery life by powering down.

The Bt471/476/478 may be powered down in the following ways:

Power Down Mode	Registers/Memory Accessible
• VREF - shut down the DACs.	Yes
• IREF - shut down the DACs.	Yes
• Stop the clock.	No

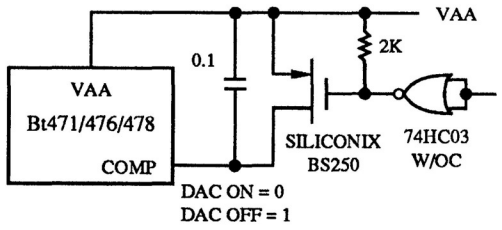

Figure 1. DAC Shutdown Using the COMP Pin.

Siliconix alternate sources:
Philips #BS250
Topaz #VP106

BS250 Typical Parameters:
IDSS @ VGS = 0v = - 0.5 mA
VGS @ ID = 1 mA = - 2.75v
BVDSS @ VGS = 0v = - 20v

VREF Power Down Mode

The VREF implementation provides an order of magnitude improvement in amplitude stability and noise immunity over an IREF implementation. For this reason, using a voltage reference is recommended over a current reference.

To eliminate the full scale output current and associated supply current to the DACs, open circuit the RSET resistor or pull the COMP pin up to VAA. Figure 1 shows a circuit for pulling the COMP pin to VAA. The 0.1 µF capacitor acts as a bypass capacitor between the VAA and COMP pins. This capacitor should be mounted as close as possible to the RAMDAC, with the leads kept short. The P-channel MOSFET with the source connected to VAA turns on when the gate voltage drops below four volts. The output of the 74HC03 open drain NAND gate pulls up through a 2K-ohm resistor to VAA. A logical one at the input to the NAND gate turns the DACs off.

Shutting down the DACs typically cuts the supply current by forty percent. For the Bt471, each DAC outputs three times the current flowing through the RSET resistor. To get a DAC output current of 21 mA, the current through RSET must be 7 mA (the actual value will be slightly less to achieve the 19.05 mA value specified in the databook). When the DACs are shut off, the total current saved will be 3 x 7 x 3 = 63 mA. At nominal supply voltage and room temperature, the Bt471/476/478 typically requires 130 mA. The power down current is therefore 160 - 63 = 97 mA.

Caution: Brooktree guarantees linearity specifications for output voltages up to 1.4 volts and for output currents down to one half of full scale.

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IREF Power Down Mode

For systems using a reference current (IREF), shut down the DACs by open circuiting IREF. Like the VREF mode above, the IREF current is proportional to the DAC output current. Figure 2 shows a circuit for supplying a constant current to the IREF pin. Drive the base of the NPN transistor with a low TTL logic signal to turn the DACs off. In the power down mode, the RAMDAC is fully register/memory compatible.

Powering down Bt471/476/478 typically cuts the supply current by forty percent and also saves the IREF current. For the Bt471 as discussed in the previous section the supply current is 160 - 63 - 7 = 90 mA.

Stopping the Clock

This mode is useful in applications where the designer does not need register compatibility or active video. The Bt471/476/478 static RAM does not require clocking to retain memory data. With the DACs on, this power down mode saves about 10 mA. Shutting off the clocks with the DAC powered down saves 2 to 3 mA. See Figure 3.

Summary

This application note shows several methods to reduce power consumption on Brooktree's Bt471/476/478 RAMDACs. Designers will find these power savings useful in laptop computers with VGA graphics capabilities. System designers may use the Bt471/476/478 power down capabilities to differentiate their products and improve performance.

This information is intended for stimulating design interest. Brooktree accepts no liability for designs contained in this application note. All users are cautioned to verify their own design.

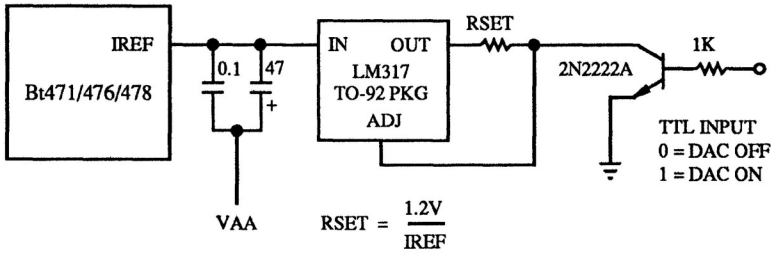

Figure 2. Open Circuit IREF.

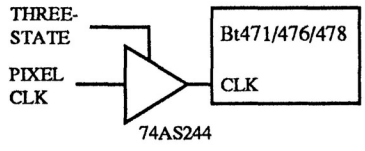

Figure 3. Clock Stopper Circuit.

Support Components

Brooktree's Technical Hotline has received many requests for assistance in identifying and locating components used with Brooktree products. Brooktree's data book and data sheets recommend components that are not always available in all areas. The following is a list of suggested manufacturers and components that will assure optimum performance of Brooktree products.

Crystal Oscillators

Many of the Brooktree CMOS RAMDACs require a positive ECL differential clock. Common 10K and 100K ECL crystal oscillators powered from +5 volts will provide this positive clock.

The following crystal oscillators come in a 14 pin DIP outline package. Pin 7 is ground, pin 14 is +5V, pin 8 is the clock output, and when a complimentary output is available, it is on pin 1.

Manufacturer/ Supplier	Model/Part Number	Description
Monitor Products 502 Via Del Monte Oceanside, CA 92054 (619) 433-4510	907EA 907EA1 907T	• For 10K ECL clocks to 200 MHz, case floating, open emitter output. • For 10K ECL clocks to 200 MHz, case floating, complimentary open emitter outputs. • For TTL clocks to 80 MHz.
Vectron Laboratories, Inc. 166 Glover Ave. Norwalk, CT 06850 (203) 853-4433 *In the U.K.:* Lyons Instruments (099-24) 67161	CO-633 CO-450	• For ECL clocks to 200 MHz • For 100K complimentary ECL clocks from 5- 400 MHz
Fox Electronics 6225 Presidential Court Fort Myers, FL 33907 (813) 482-7212	F5L F1100	• For 10KH ECL clocks to 200 MHz - Pin 7 (case ground) is an option • For TTL clocks to 80 MHz
Conner-Winfield 1865 Selmarten Road Aurora, IL 60505 (312) 851-4722	ECLA-1 ECLA-2 S15R6 S17R6	• For 10K, 8-150 MHz, case tied to pin 14 • For 100K, 8-150 MHz, case tied to pin 14 • For TTL, 0° to 70° C, 256 KHz-80 MHz • For TTL, 55° to 125° C, 256 KHz-80 MHz

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Ferrite Beads

Decoupling the power to Brooktree's products through a ferrite bead is recommended to prevent power supply noise from being coupled into the video outputs. Use of a ferrite bead is also recommended for suppressing interference caused by the fast switching times of the DACs.

Ferrite beads have a very low impedance at low frequencies which increases at higher frequencies. Refer to **AN-1** for a typical impedance curve. Beads are selected for their impedance at a standard frequency of 100 MHz, typical.

Manufacturer/ Supplier	Model/Part Number	Description
Fair-Rite Products Corporation P.O.Box J Wallkill, NY 12589 (914) 895-2055 *In the U.K.:* Apex Inductive Devices (01) 903-2944	2743001111 2743021446	• Axial lead, 71 ohms @ 100 MHz • Surface mount, 89 ohms @ 100 MHz
TDK Corporation 4711 West Golf Road #300 Skokie, IL 60076 (312) 679-8200	CB30-1210 BF45-4001	• Surface mount, 52 ohms @ 100 MHz • Axial lead, 85 ohms @ 100 MHz
Ferroxcube 5083 Kings Hwy Saugerties, NY 12477 (914) 246-2811 Canada: (416) 561-9311	5659065-3B	• 38 ohms @ 100 MHz

Sockets

For high speed operations and proper heat dissipation, it is generally recommended that Brooktree products be soldered directly to the PC board. However, when prototyping or operating at clock rates less than 50 MHz, sockets can be used. The following is a listing of commonly requested sockets.

The following sockets are recommended for use with Brooktree's PLCC packages:

Manufacturer/ Supplier	Model/Part Number	Description
AMP Inc. Harrisburg, PA 17105 (717) 564-0100 Canada: (416) 475-6222 U.K.: 44-1-954-2356 W. Germany: 49-6103-7090 Japan: 81-3-404-7171	641444-2 641746-2 641343-2 641747-2 643151-2 643066-2	• 28 pin, surface mount • 28 pin, solder tail • 44 pin, surface mount • 44 pin, solder tail • 84 pin, surface mount • 84 pin, solder tail
Burndy Corporation P.O. Box 5200 Richards Ave. Norwalk, CT 06856 (203) 838-4444	QILE28P-410T QILE44P-410T QILE84P-410T QILEXT-1	• 28 pin, solder tail • 44 pin, solder tail • 84 pin, solder tail • PLCC Removal tool
McKenzie Technology 44370 Old Warm Springs Blvd Fremont, CA 94538 (415) 651-2700	PLCC-28-P-T PLCC-44-P-T PLCC-84-P-T	• 28 pin • 44 pin • 84 pin

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Sockets (continued):

The following sockets are recommended for use with Brooktree's PGA packages.

Manufacturer/ Supplier	Model/Part Number	Description
Augat 33 Perry Ave. Attleboro, MA 02703 (617) 222-2202 U.K.: (0908) 67665 W. Germany: (089) 576085 Japan: (03) 465-8457	PPS069-2A1130-L PPS084-2A1212-L PPS132-2A1414-L	• 69 pin PGA, for 68 pin PGA package* • 84 pin PGA* • 132 pin PGA* • 144 pin PGA* *PGA package to PC board standoff distance : 0.166"
Robinson Nugent, Inc. 800 East Eighth St. New Albany, IN 47150 (812) 945-0211 Switzerland: (066) 229822	PGA-068CM3-S-TG PGA-084AM3-S-TG PGA-132AM3-S-TG	• 68 pin PGA* • 84 pin PGA* • 132 pin PGA* *PGA package to PC board standoff distance : 0.175"
Yamaichi U.S. Distributers: Nepenthe 2471 East Bayshore Rd. Suite 520 Palo Alto, CA 94303 (415) 856-9332	IC93-10803-G4	• 84 pin PGA* *PGA package to PC board standoff distance : 0.236"
McKenzie Technology 44370 Old Warm Springs Blvd Fremont, CA 94538 (415) 651-2700	PGA69H003B1-1130T PGA84H003B1-1212T PGA132H003B1-1414T PGA145H003B1-1521T	• 69 pin PGA, for 68 pin PGA package* • 84 pin PGA* • 132 pin PGA* • 144 pin PGA* *PGA package to PC board standoff distance : 0.165"

1.2V Voltage References

To meet RS170/RS343 tolerances, Brooktree DACs require a voltage reference of 1.2V ± 5%. The following devices meet this requirement.

Manufacturer/ Supplier	Model/Part Number	Description
National Semiconductor 2900 Semiconductor Drive Santa Clara, CA 95051 (408) 721-5000	LM385Z-1.2	
Motorola Semiconductor Products 5005 East McDowell Road Phoenix, AZ 85008 (602) 244-7100 Japan: (03)440-3311 Hong Kong: 0-223111 U.K.: 0296-35252 W. Germany: (089) 92720	LM385Z-1.2	
Maxim Integrated Products 510 North Pastoria Sunnyvale, CA 94086 (408) 737-7600	ICL8069	

Video Buffers

Brooktree's DACs are intended to drive transmission line loads, which most monitors are rated as. Transmission line cable lengths greater than 10 meters can attenuate and distort high frequency pulses. Booster buffers can compensate for some cable distortion but must have 6-12 dB voltage gain into the cable load to be effective. Select buffers with ± 30 mA drive, 3 - 4 volt output swing, and full power bandwidth greater than that of the monitor. Buffers usually require negative supply voltages and thermal considerations.

Manufacturer/ Supplier	Model/Part Number	Description
Elantec 1996 Tarob Court Milpitas, CA 95035 (408) 945-1323 U.K.: 0844-68781	EL2003 EL2020	• 3dB/50 MHz Unity Gain into 50 Ω • 3dB/50 MHz Gain ≥ 1 into 50 Ω
Harris Semiconductor 2401 Palm Bay Road Palm Bay, FL 32905 (305) 724-7418	HA-5033 HA1-2542	• 3dB/50 MHz Unity Gain into 50 Ω • 3dB/50 MHz Gain 2 into 150 Ω
Comlinear Corporation 4800 Wheaton Drive P.O. Box 20600 Fort Collins, CO 80522 (303) 226-0500	CLC400	• 3dB/200 MHz Gain 2 into 100 Ω

Other Components

Metal film resistors are recommended for use with Brooktree's products because of low temperature coefficients and low current noise.

For assistance in locating other components, call the Brooktree Technical Hotline at (800) VIDEO IC.

Brooktree Product Evaluation Boards

Brooktree offers a wide range of Evaluation Module (EVM) and Device Under Test (DUT) boards to assist the designer in product evaluation. These boards are available through your sales representative or the Brooktree area sales office.

EVM boards are complete evaluation modules and include all the logic for initial evaluation of the Brooktree product. These boards are designed to offer a functional evaluation with minimal equipment, usually only a power supply and an oscilloscope are required.

DUT boards are a general purpose device test board and contain only the Brooktree product with design emphasis placed on the proper operating environment for layout and component placement. These boards will require all inputs, clocks, and power to be supplied through an external DIN connector. The power and ground layout on these boards has been optimized for best performance.

Printed circuit artwork for the EVM and DUT boards is available upon request. For further information call the Brooktree Technical Hotline at (800) VIDEO IC.

Device	Board Number	Description
Bt101	Bt101 EVM	Includes logic to generate full scale ramp and square wave outputs at full rated clock speeds.
Bt102	Bt102 EVM	Same as the Bt101 EVM
Bt103	Bt103 EVM	Same as the Bt101 EVM
Bt104/105	Bt104/105 EVM	Does not include logic. Uses a half wide DIN connector for power/data and an SMA connector for analog video out.
Bt106	Bt106 EVM	Same as the Bt101 EVM
Bt471/478	Bt471/478 EVM	This is an adapter which allows the Bt471/478KPJ to be evaluated in a 28-pin socket. Includes circuitry for an optional voltage reference. Access to overlay input via header. 4 optional jumpers.
Bt604	Bt604 EVM	Includes the necessary logic to evaluate the Bt604. Requires external trigger and -5.2V.

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