Advance Data Sheet

T7220 Twisted-Pair Medium Attachment Unit (TPMAU) Issue 2.2

Features

- Compliance with IEEE 802.3 standards for AUI-interface
- Compliance with IEEE 802.3 I/D11 10BASE-T draft standard*
- Direct interface to AUI transformer and TP filters
- Internal pre-distortion generation
- Internal squelch circuits
- Selectable end-of-packet SQE test
- Selectable link-integrity test
- LED control for transmit, receive, jabber, and collision
- Single 5 V supply and low-power CMOS technology
- Lower TP threshold option

Description

The T7220 Twisted-Pair Medium Attachment Unit (TPMAU) simplifies the design and implementation of a minimal-part-count, cost-effective medium attachment unit (MAU) between an Ethernet attachment unit interface (AUI) and the twisted-pair wire media. Ethernet users can now use twisted-pair wiring for LAN construction and/or expansion and still use existing Ethernet-interface cards. An MAU built with the TPMAU provides the electrical interface between the Ethernet transceiver cable (IEEE AUI) and the twisted-pair wire.

Standard features of the TPMAU include level-shifted data passthrough from one transmission media to another, collision detection, and internal pre-distortion generation. Additional features include selectable signal quality error (SQE) test generation, LED control for IC status, link-integrity strapping option, and a squelch function. The T7220 TPMAU is fabricated by using linear CMOS technology and is available in a 28-pin, plastic DIP or in a 28-pin, plastic SOJ.

* The 10BASE-T draft standard is not finalized and is subject to change without notice.

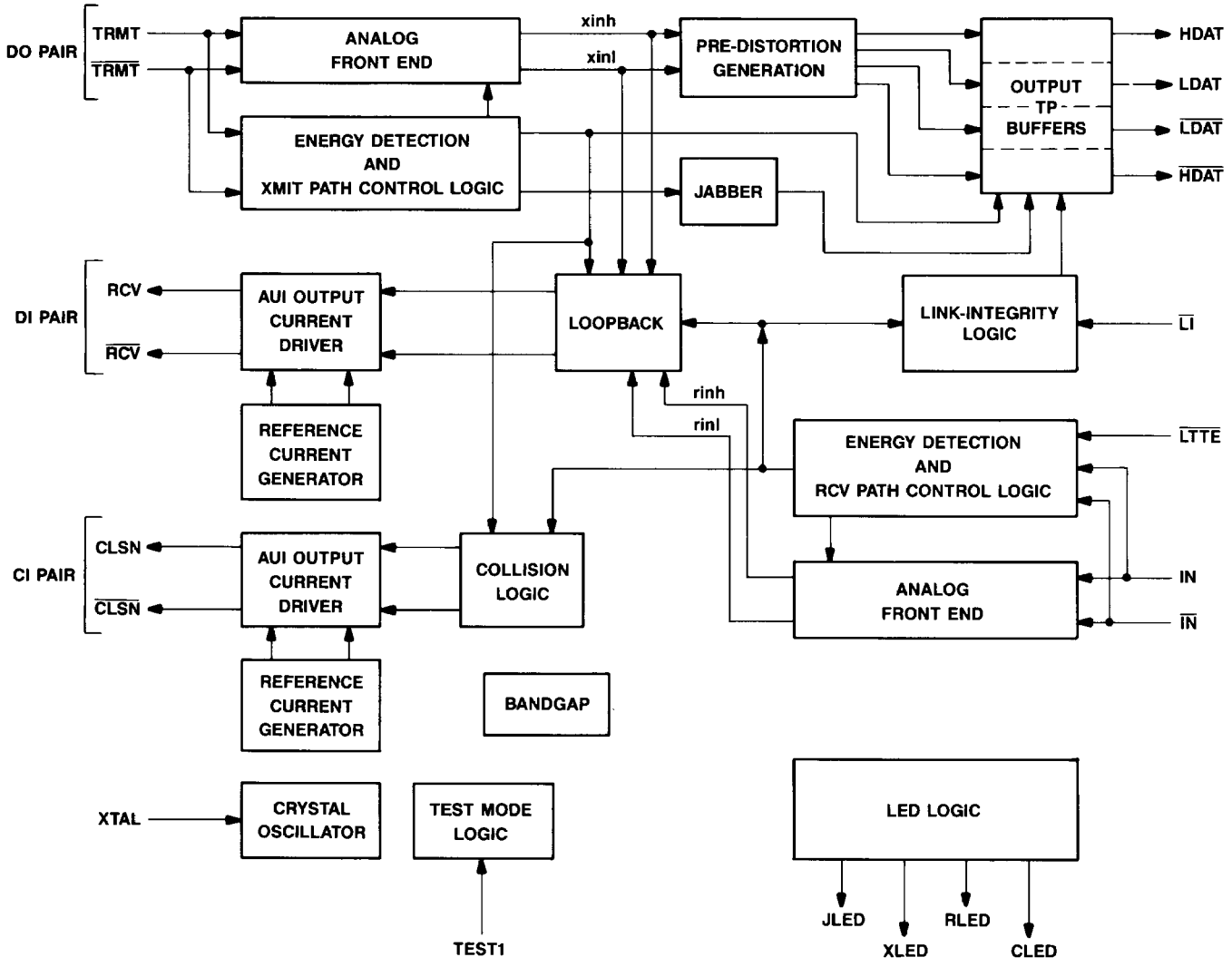

Figure 1. Block Diagram

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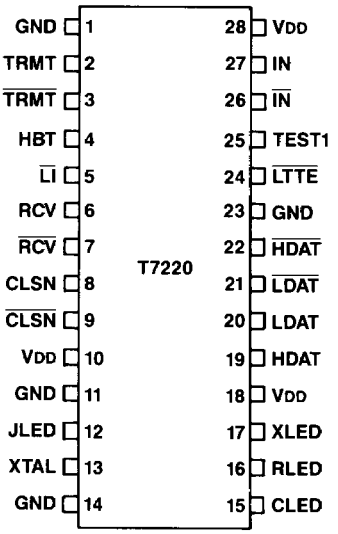


Figure 2. Pin Diagram

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Function
1,11, 14,23	GND	—	**Ground.**
2,3	TRMT, TRMT	I	**Transmit Data Pair.** A differential receiver input pair from the DO circuit that receives 10 Mbits/s Manchester-encoded data from the AUI-transceiver cable, which is driven by the DTE (terminal or computer). The receiver must be isolated from the AUI-transceiver cable by a pulse transformer.
4	HBT	I	**SQE Test Sequence Select (Heartbeat).** A strapping option that when tied high (VDD) allows the SQE test sequence to be transmitted on the collision pair of the AUI-transceiver cable after every successful transmission onto the media. A low (VSS) on this pin disables the SQE test sequence transmission. The disabling of the SQE test sequence is required when a MAU is connected to a repeater. This pin is connected to an internal pull-up device.

Table 1. Pin Descriptions (Continued)

Pin	Symbol	Type	Name/Function
5	$\overline{LI}$	I	**Link-Integrity Enable (Active-Low).** A strapping option that when tied low (V_{SS}) activates the link-integrity function of the TPMAU. When this pin is enabled, the receive traffic indicator turns off if it is determined that the receive twisted-pair link is not present. Also, the TPMAU transmits periodic link-integrity pulses in the absence of transmit traffic. If this pin is tied high (V_{DD}), all link-integrity functions are disabled. This pin is connected to an internal pull-up device.
6,7	RCV, $\overline{RCV}$	O	**Receive Data Pair.** An output current driver pair to the DI circuit that drives the AUI-transceiver cable with the 10 Mbits/s Manchester-encoded data received from the twisted-pair wire of the network. This driver must be isolated from the AUI-transceiver cable by a pulse transformer.
8,9	CLSN, $\overline{CLSN}$	O	**Collision Presence Pair.** An output current driver pair to the CI circuit that drives the AUI-transceiver cable with 10 MHz ± 15%, 50% nominal, 40% or 60% worst-case, duty-cycle square waves. This output pair is activated when a collision is detected on the network, either during self-test (heartbeat) as the SQE test sequence or after the watchdog timer has expired to indicate that the twisted-pair transmitter is disabled. This pair must be isolated from the AUI-transceiver cable by a pulse transformer.
10,18 28	V_{DD}	—	**5 V Power Supply.**
12	JLED	O	**Jabber Indicator.** Indicates watchdog timer has timed out and the twisted-pair drivers have been disabled.
13	XTAL	I	**Crystal In.** This pin is a 20 MHz, frequency-reference input for internal chip timing.
15	CLED	O	**Collision Indicator.** Indicates a collision has been detected by the TPMAU.
16	RLED	O	**Receive Indicator.** Indicates a reception from the TP network is in progress.
17	XLED	O	**Transmit Indicator.** Indicates a transmission onto the TP network is in progress.
19—22	HDAT, $\overline{HDAT}$, LDAT, $\overline{LDAT}$	O	**TP Transmit Pair Drivers.** These four outputs constitute the twisted-pair drivers with pre-distortion capability. The HDAT/$\overline{HDAT}$ outputs generate the 10 Mbits/s Manchester encoded data. The LDAT/$\overline{LDAT}$ outputs mirror the HDAT/$\overline{HDAT}$ outputs except for fat-bit* occurrences. During the second half of a fat bit (either high or low), the LDAT/$\overline{LDAT}$ outputs are inverted with respect to HDAT/$\overline{HDAT}$ outputs. This signal behavior reduces the amount of jitter by preventing overcharge on the twisted-pair media.
24	$\overline{LTTE}$	—	**Lower TP Threshold Enable (Active-Low).** For 10BASE-T compatible operation, this pin must be left open. But, if this pin is grounded, the TP receiver threshold is lowered by approximately 4.5 dB from the nominal 10BASE-T required specification. By using this lower-threshold option and by selecting different compensation resistor values for wave-construction circuits, a customized interface is possible for non-10BASE-T applications. However, once this lower threshold is invoked, the wiring used must not be a bundled system (e.g., 25 pair) where other services reside (e.g., voice, other 10BASE-T users, etc.).
25	TEST1	I	**Test1.** During normal operation, this pin should be tied to ground.
26,27	IN, $\overline{IN}$	I	**TP Receive Pair.** A differential receiver tied to the receive transformer pair of the twisted-pair wire. The receive pair of the twisted-pair medium is driven with 10 Mbits/s Manchester-encoded data.

* Fat bit is the midbit-to-midbit time during the CD0 to CD1 transition or CD1 to CD0 transition, each of which is nominally 100 ns.

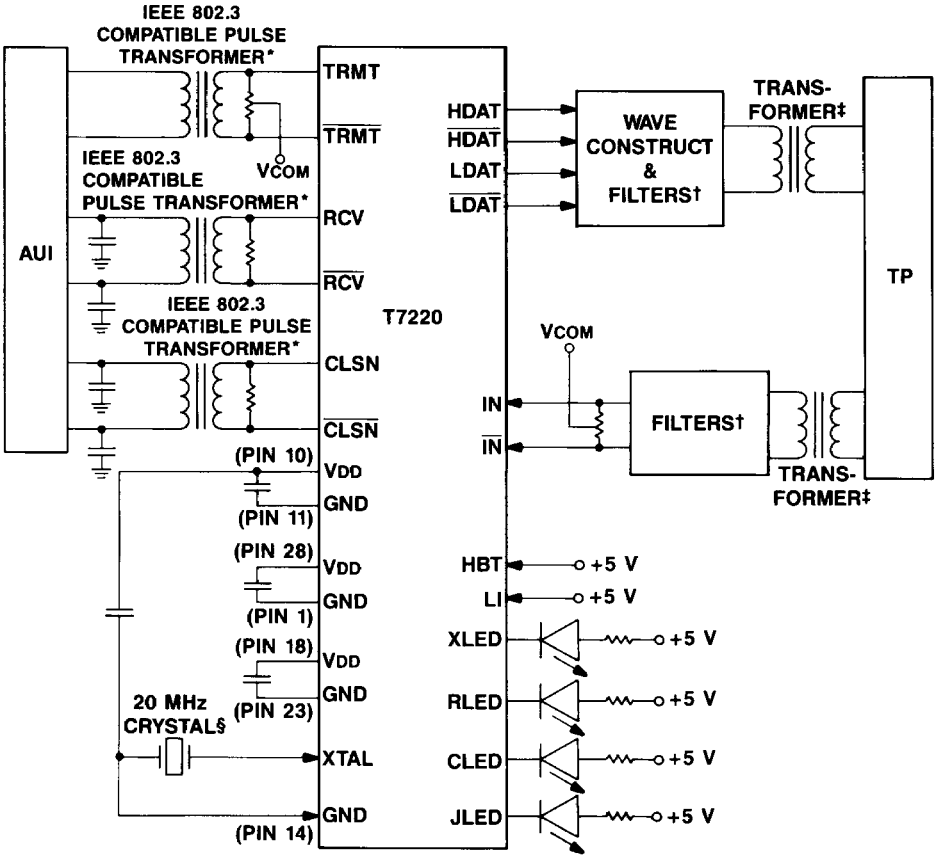
Overview

The T7220 device provides the transmit, receive, and collision-detection functions as specified by the IEEE 802.3 10BASE-T draft standard for use in a 10 Mbits/s CSMA/CD Ethernet on a twisted-pair LAN application. It is an equivalent of Ethernet's transceiver chip but is used as the interface to the twisted pair.

The transmit section transfers data from the AUI cable to the twisted-pair network, and the receive section transfers data from the twisted pair to the AUI. The collision-detection capability senses data being simultaneously transmitted and received. It reacts by sending a 10 MHz square wave onto the AUI-CI circuit.

In addition to these functions, there are two strapping options: link-integrity and SQE-test-sequence select. Enabling the link-integrity strapping option causes a pulse to be transmitted in the absence of data transmission. The receiver recognizes link-integrity pulses, acknowledging that in the absence of receive traffic, the link is up. When the SQE-test-sequence-select strapping option is enabled, it allows the SQE test sequence to be transmitted to the DTE after every successful transmission on the twisted-pair network.

There are four drivers capable of driving four LEDs to indicate the status of the receive, transmit, collision, and jabber functions.



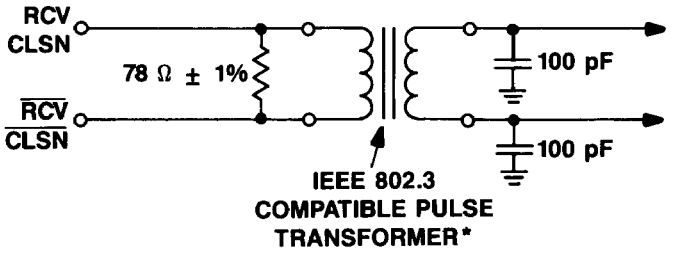
* Required transformers for the AUI interface are the Pulse Engineering Inc. (PE64503), TDK Corp. (TLA-100-3E), Coilcraft (LAXET304 or LO323-A), or equivalents.

† The contents of the filters should comply with the most recent version of the 10BASE-T draft specifications. Possible filters are the Pulse Engineering Inc. (PE32101), TDK Corp. (0921ES), CTS Corp. — Knight Div. (9561928-01), Coilcraft (K9686-B), or equivalents.

‡ Required transformers for the TP interface are the AT&T (2759A), Pulse Engineering (PE65263), Coilcraft (LAXIOT-200), or equivalents.

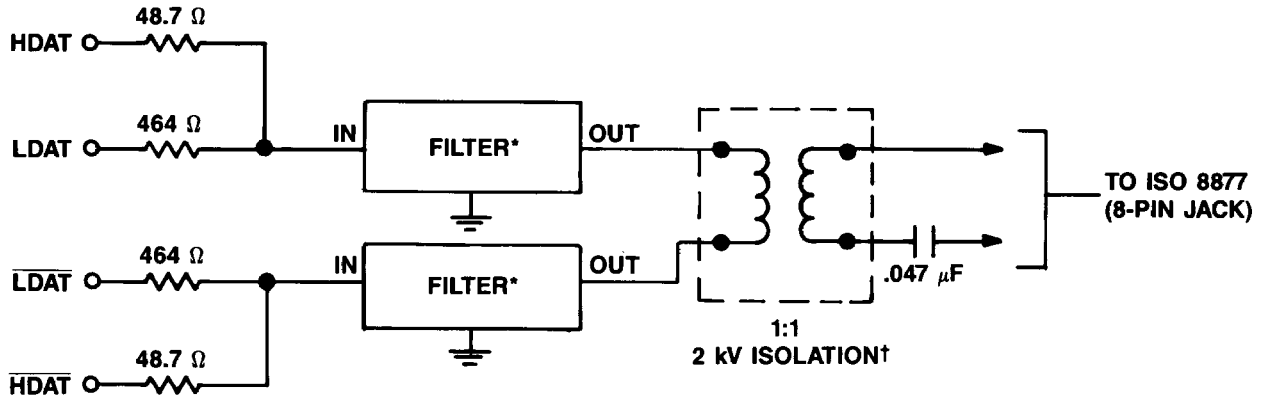
§ The recommended crystal is MTRON MP-1 (20 MHz).

Figure 3. Typical System Configuration



* Required transformers are the Pulse Engineering Inc. (PE64503), TDK Corp. (TLA-100-3E), Coilcraft (LAXET304 or LO323-A), or equivalents.

Figure 4. Typical Load Output on the Outputs of RCV/$\overline{\text{RCV}}$ and CLSN/$\overline{\text{CLSN}}$



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† Required transformers are the AT&T (2759A), Pulse Engineering (PE65263), Coilcraft (LAXIOT-200), or equivalents.

Figure 5. Example of Transmit Circuitry

Architecture

Transmit Path (AUI to TP)

AUI Receiver. The TPMAU receives transmit data via the TRMT/$\overline{\text{TRMT}}$ pins from the data terminal equipment (DTE) on the AUI-DO circuit, as described in IEEE 802.3 draft standard, and transmits this data onto a twisted-pair network. The inputs must be transformer-coupled to the AUI circuit. The dc biasing should be provided externally to the chip, with the common-mode voltage set to nominal $V_{DD}/2$. The dc differential input impedance of the TRMT/$\overline{\text{TRMT}}$ pins is 20 kΩ ± 20%.

A single-level biasing scheme is used to reject spurious noise on the TRMT/$\overline{\text{TRMT}}$ pins and prevent it from propagating onto the network. The squelch stays on if the differential input signal is less than 160 mV peak or exceeds this magnitude for less than 20 ns. All signals at the TRMT/$\overline{\text{TRMT}}$ inputs are ignored while the squelch is on. The squelch is turned off if the differential input exceeds 300 mV peak for more than 75 ns. The squelch remains off until an IDL pulse is detected or until the input does not exceed the detection threshold for 500 ns ± 100 ns.

AUI Receive Signal Levels. The receiver can resolve differential signals as small as 300 mV peak. Internal circuitry samples the common-mode voltage to provide fully differential signal detection.

TP Driver Characteristics. The drivers output CMOS logic levels with a source resistance less than 10 Ω and a maximum current rating of 25 mA dc.

All TP output driver pins are driven low as a result of any of the following: there is an AUI IDL pulse of at least 200 ns duration, the output driver is jabbed, the link-integrity option is enabled and there is a link failure, or an IDL pulse is not detected at the end of a packet and the input does not exceed the detection threshold for 500 ns ±100 ns.

When the driver detects that it has finished sending an IDL pulse onto the TP, a timer of not more than 500 ns is started. While this timer is active, activity on the TRMT/$\overline{\text{TRMT}}$ inputs is ignored.

Receive Path (TP to AUI)

AUI Driver Characteristics. This driver differentially drives a current onto the load connected between the RCV and $\overline{\text{RCV}}$ pins. The current through the load results in an output voltage between ±0.6 V and ±1.2 V measured differentially between the two pins. An external resistor (78 Ω) and capacitor (100 pF) must be connected for proper termination, as shown in Figure 4.

The output, when properly terminated, is in accordance with IEEE 802.3 draft standard, Section 7.4.1 for MAUs.

When the driver detects that it has finished sending an IDL pulse onto the AUI, a timer of not more than 500 ns is started. While this timer is active, activity on the IN/$\overline{\text{IN}}$ inputs is ignored, and the AUI driver discharges the current stored in the inductive load.

TP Receiver Thresholds. The TP receiver is connected to a band-limiting filter, whose input is transformer-coupled to the twisted pair. The receiver is able to resolve differential signals as small as 350 mV peak. The common-mode input voltage of the input signals is required from the band-limiting filters to be mid-supply voltage ($V_{DD}/2$). The dc differential input impedance of the IN/$\overline{\text{IN}}$ pins is 20 kΩ ± 20%.

The receiver rejects the following signals:

1. All signals which when measured through the recommended input filter produce a peak magnitude of less than 300 mV.
2. All continuous sinusoidal signals of amplitude less than 3.1 Vpeak and frequency less than 2 MHz.
3. All single sinusoidal cycles with amplitude less than 3.1 Vpeak and starting with either polarity where the frequency is between 2 MHz and 15 MHz. For a period of 4 BT before and after this single cycle, the received signal must conform to 1 above.

Collision

The CS0 signal is placed on the AUI-CI circuit whenever a collision condition exists. A state of collision exists whenever there are valid signals being input to the TPMAU from the network and from the DTE simultaneously and the TPMAU is not in a link-failure state.

The CS0 signal is a periodic square wave at 10 MHz ± 15% with a duty cycle no worse than 40/60 or 60/40. This signal is presented to the AUI-CI circuit no more than 9 BT after the chip detects a collision. Refer to IEEE 802.3, Section 8.2.1.3.

If the receive inputs, IN/$\overline{\text{IN}}$, become active while there is activity on the transmit inputs, TRMT/$\overline{\text{TRMT}}$, the loopback data on RCV/$\overline{\text{RCV}}$ switches from transmit data to receive data without generating code violations. Refer to Section 14.2.3 of the 10BASE-T draft.

If a collision condition exits with IN/$\overline{\text{IN}}$ having gone idle while TRMT/$\overline{\text{TRMT}}$ are still active, SQE continues for 7 BT ± 2 BT. If a collision condition exits with TRMT/$\overline{\text{TRMT}}$ having gone idle while IN/$\overline{\text{IN}}$ are still active, SQE can continue for up to 9 BT.

Collision AUI Driver. This driver has the same electrical characteristics as the AUI driver for the receive path, except as already noted regarding signal requirements.

Jabber (Watchdog Timer)

The chip contains a self-interrupt capability to inhibit transmit data from being passed onto the network from a defective DTE. The chip provides a nominal window of 50 ms, during which time a normal data link frame can be transmitted. If the frame length exceeds this duration, the chip immediately inhibits all further transmission of that frame and starts the collision-presence function by placing a CS0 signal on the AUI-CI circuit. Refer to IEEE 802.3, Section 8.2.1.5.

When activity on the AUI-DO circuit has ceased, the chip continues to present the CS0 signal to the AUI-CI circuit for 0.5 second ± 50%. The chip then returns to the idle state. Refer to IEEE 802.3, Section 8.2.1.5.

The transmission of link-integrity pulses from the TP drivers is not inhibited when the TPMAU is jabbed and the $\overline{LI}$ pin is pulled active-low.

SQE Test (Heartbeat)

When the AUI-DO circuit has gone idle after a successful transmission of a frame to the twisted-pair network and the HBT strapping input is high, the chip presents the CS0 signal to the AUI-CI circuit.

Upon the conclusion of a successful transmission onto the network media, the chip presents the CS0 signal within 11 BT ± 5 BT of the end of activity on the AUI-DO circuit. The CS0 signal is presented for 10 BT ± 5 BT (this is known as "heartbeat" or SQE test sequence), after which the chip presents an IDL on the AUI-CI and returns to the idle state. Refer to IEEE 802.3, Section 8.2.1.1.

A successful transmission is defined as an uninterrupted packet transmission onto the network media. Interruption sources include collision, jabber, or link failure.

Link Integrity

The chip can determine if the receive twisted-pair link is faulty. Enabling the $\overline{LI}$ strapping option allows the RLED receive traffic indicator to display the status of the receive twisted-pair link. It also permits the active disabling of the transmit and loopback paths onboard the TPMAU chip in response to a link-integrity fault.

In the absence of receive traffic, the twisted-pair receiver on the chip can detect periodic link-integrity pulses on the receive pair. A link-integrity pulse is described as a 100 ns ± 20% high signal with predistortion followed by a return to idle. The chip provides a link-integrity reception window, during which a link pulse is expected in the absence of receive traffic. The link-integrity window nominally opens 6.5 ms after the receipt of a link-integrity pulse or the end of a data frame. The window closes nominally 104 ms after the receipt of a link-integrity pulse or the end of a data frame. If a link pulse is received before the link-integrity reception window opens, it is ignored. If no link-integrity pulse is received while the link-integrity reception window is open, there is a link failure. The RLED indicator is turned off, and the chip's transmit, loopback, and receive functions are disabled. If a link-integrity pulse or receive traffic is received while the link-integrity reception window is open, the timers involved are reset, and the RLED indicator remains on or flashes, as described in the LED Status section.

Once the TPMAU has detected a link failure, one of two events must occur before the TPMAU re-enables transmission and reception of data. The first possible event is the reception of two consecutive link-integrity pulses which must both fall within the link-integrity reception window and be separated by at least a nominal 6.5 ms. The second possible event is the reception of a data packet from the twisted pair. With either of these events, the TPMAU enters a wait-state and continues to disable loopback, transmit, and receive functions. This continues until the TPMAU determines that there is no traffic going in either the transmit or receive direction, whereupon the part enters the idle state, and the RLED indicator shows the link is present.

When $\overline{LI}$ is enabled, the TPMAU also transmits link-integrity pulses onto the transmit twisted-pair link. In the absence of transmit traffic, a link-integrity pulse is transmitted at a nominal rate of once per 16 ms. Link-integrity pulses continue to be transmitted when the part is jabbed by the watchdog timer or there is link-integrity failure.

If the $\overline{LI}$ strapping option is disabled, the RLED indicator remains on in the absence of receive traffic, and no link-integrity pulses are transmitted in the absence of traffic. Received link-integrity pulses are also ignored at the IN/$\overline{IN}$ inputs.

LED Status

Four LEDs provide the user with a visual indication of the status and operation of the MAU. The TPMAU provides the logic signals to drive the LEDs.

XLED. The following XLED values (on or off) indicate transmission status:

- The LED is normally on. This indicates there is no transmission in progress.
- The LED is turned off when a valid packet is transmitted and remains off for a duration of fixed off-time (100 ms ± 10 ms), after which the LED is turned back on.
- The LED remains on for a duration of at least a minimum on-time (6 ms ± 2 ms) until turned off if and when the next packet is transmitted.

RLED. The following RLED values indicate the status of reception from the twisted pair.

When $\overline{LI}$ is disabled:

- The LED is normally on, indicating there is no current receive traffic.
- The LED is turned off when a valid packet is received and remains off for a duration of fixed off-time (100 ms ± 10 ms), after which the LED is turned back on.
- The LED remains on for a duration of a minimum on-time (6 ms ± 2 ms) until turned off if and when the next packet is received.

When $\overline{LI}$ is enabled:

- The LED is normally on. This indicates no receive traffic and successful reception of the link-integrity pulse.
- The LED turns off if the TPMAU determines there is a link failure, as previously described. This visually indicates that the link is down. The LED remains off until a link-integrity pulse or receive traffic is successfully detected, after which the LED is turned on with a minimum on-time of 1 second ± 50%.
- If the link is up, the LED can also be turned off when a valid data packet is received from the twisted pair. When a packet is received, the LED is turned off for a duration of fixed off-time (100 ms ± 10 ms), after which the LED is turned back on.
- The LED remains on for a minimum on-time (6 ms ± 2 ms), after which it is turned off when the next packet is received.

CLED. The following CLED values indicate collision status:

- The LED is normally off, indicating no collision.
- The LED is turned on when a collision is detected. It remains on for a nominal on-time of 15 ms ± 5 ms, after which it is turned back off.
- The LED is turned back on immediately upon detection of another collision. There is no minimum off-time.
- If a collision occurs while the LED is lit from a previous collision, the LED remains on for the nominal on-time following the last collision detection.

JLED. The following JLED values indicate jabbing status:

- The LED is normally off, indicating a no-jab condition.
- The LED is turned on when the watchdog timer jabs the twisted-pair network drivers. It remains on while the chip continues to jab the TP drivers.
- The LED is turned off after the watchdog timer counts out the 0.5 second ± 50% reset time and stops jabbing the TP drivers.

LED Drivers

The LED drivers require an external resistor in series with the LED, which is in turn connected to VDD. The driver pulls the pin low to turn the LED on and can sink up to 15 mA of drive current from the resistor with an output impedance of less than 50 Ω.

Crystal Oscillator

A 20 MHz, parallel-resonant crystal (100 ppm recommended) is required to control the TPMAU's crystal oscillator. The oscillator is designed to operate with a quartz crystal with a series resistance of 25 Ω maximum and an expected crystal load of 20 pF. With this crystal, the total external capacitance, including crystal shunt capacitance C0, should not be more than 10 pF. This requires placing the crystal adjacent to the TPMAU. The crystal shunt capacitance (C0) should not exceed 5 pF.

The crystal is connected between the XTAL pin and the adjacent GND pin on the TPMAU.

An external MOS-level clock can be applied to the crystal oscillator input. A resistor should be added in series with the clock source to limit the amplitude of the voltage swing seen by the pin. A 500 Ω resistor works well in most cases. If users are concerned about the duty-cycle variation caused by driving the TPMAU with a clock source, the following test can be done on the bench to empirically determine the best resistor value for the user's application:

- Place the part in dc test mode, as described in the Test Mode section of this document.
- Attach an oscilloscope to the JLED pin. This pin outputs the internal clock source.
- Alter the resistor value to obtain an optimal duty-cycle ratio. Experiments have shown that a 500 Ω resistor works well for LS TTL logic levels; CMOS logic levels need a 1 kΩ resistor.

Under no circumstances should the clock be driven straight into the TPMAU. Also, under no circumstances should the clock stop, not even briefly, once power is applied to the TPMAU. If the clock to the TPMAU is stopped, power to the TPMAU must be removed to ensure proper behavior of the TPMAU.

Strapping Options

All strapping options are connected to internal pull-up resistors (nominally 100 kΩ). A resistor tying a strapping option low must be able to sink 70 μA.

Test Mode

When the TEST1 pin is held high, the chip enters the ac/dc test mode. The ac test mode is activated by holding the HBT pin high. In the ac test mode, the speed of the internal clocks is increased by three orders of magnitude, resulting in a shorter test time for the chip. When the HBT pin is held low, the dc test mode is activated. In this mode, the oscillator frequency and duty cycle can be tested on the JLED pin, and three internal clocks (ACK, BCK, and CCK) can be similarly tested on the XLED, RLED, and CLED pins, respectively. In addition, the AUI-driver current can be measured through a 39 Ω resistor between the RCV/RCVB pins.

Power Considerations

There are seven power connections to the TPMAU. There are three pairs of VDD and GND connections and a fourth GND pin for the XTAL oscillator. Table 2 describes which internal circuits are powered by each VDD/GND pair.

Table 2. Power Connections

Pins	Circuits
1, 28	Analog Supplies: Analog signal receivers Energy-detection circuits Delay-lock loop Band gap reference
10, 11	AUI Output Drivers: Digital polycells XTAL oscillator (V_{DD} only) LED drivers (V_{DD} only)
14	GND Only for XTAL Oscillator and Pins 15, 16, and 17
18, 23	TP CMOS Output Drivers Only

Characteristics

Electrical Characteristics

T_A = 0 °C to 70 °C, V_{DD} = 5 V ±10%, V_{SS} = 0.0 V

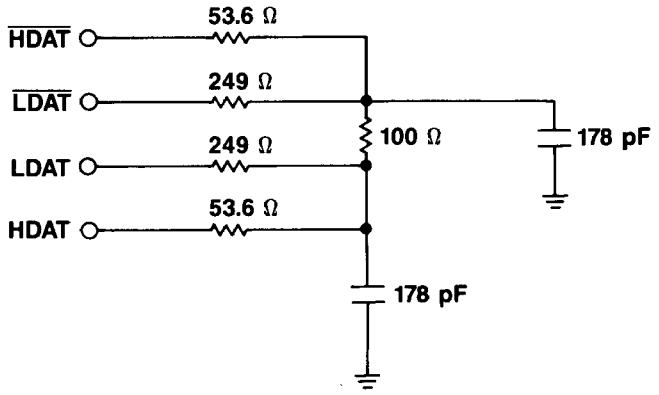
Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Voltage:					
AUI	V_{IDF}	—	.300	1.3	V_{DIFF}
TP	V_{IDF}	—	.350	2.0	V_{DIFF}
Strapping Options:					
Low	V_{IL}	—	—	0.2	V
High	V_{IH}	—	4	—	V
Output Voltage — HDAT/$\overline{\text{HDAT}}$/LDAT/$\overline{\text{LDAT}}$:	V_{OL} V_{OH}	V_{DD} = 5.0 V R_{LOAD} = 500 Ω	— 4.9	0.1 —	V V
LED Drivers:					
Low	V_{OL}	R_{LOAD} = 2000 Ω	—	0.130	V
High	V_{OH}	—	4.87	—	V
Power Supply Current:					
No traffic load	I_{DD}	V_{DD} = 5.0 V	—	100	mA
With traffic load	I_{DD}	V_{DD} = 5.0 V	—	145	mA
Power Dissipation:					
No traffic load	PD	V_{DD} = 5.0 V	—	500	mW
With traffic load	PD	V_{DD} = 5.0 V	—	600	mW
AUI Output Current	I_{AVEC}	—	18	25	mA
dc Output Series Impedance:		V_{DD} = 4.5 V			
TP drivers	RS	I = 25 mA max	—	10	Ω
LED drivers	RS	I = 10 mA max	—	50	Ω
Oscillator Characteristics — Frequency	fOSC	—	18	22	MHz
Output Rise and Fall Time:		Measured at 20% and 80% points			
HDAT/$\overline{\text{HDAT}}$/LDAT/$\overline{\text{LDAT}}$	tr	See Figure 6.	2	8	ns
	tf	See Figure 6.	2	8	ns
RCV/$\overline{\text{RCV}}$	tr	See Figure 7.	3	9	ns
	tf	See Figure 7.	3	9	ns

Absolute Maximum Ratings

Absolute maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage. External leads can be bonded or soldered safely at temperatures up to 300 °C.

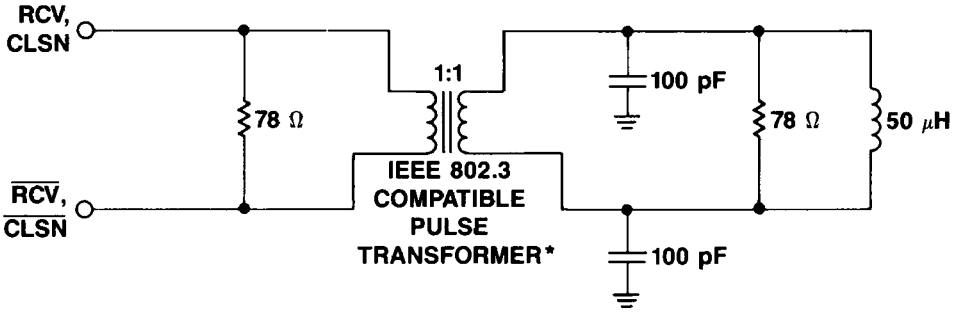
Ambient Operating Temperature (T_A) Range ..... 0 °C to 70 °C
Storage Temperature (Tstg) Range ..... −40 °C to +125 °C
Power Dissipation (PD) ..... 600 mW
Voltage on Any Pin with Respect to Ground ..... −0.5 V to V_{DD} + 0.5 V *

* Except as described elsewhere in the data sheet.



Note: The resistor and capacitor values are used for testing purposes only.

Figure 6. Test Condition Load for Measurement of TP Output Drivers' Rise and Fall Times



* Required transformers are Pulse Engineering Inc. (PE64503), TDK Corp. (TLA-100-3E), Coilcraft (LAXET304 or LO323-A), or equivalents.

Figure 7. Test Condition Load for Measurement of AUI Driver's Rise and Fall Times

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. AT&T employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 1000 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here is obtained by using these circuit parameters.

Human-Body Model ESD Threshold	
Device	**Voltage**
T7220-PC	2000 V
T7220-EC	2000 V

Timing Characteristics

Measurements are from 50% point unless otherwise noted.

Table 3. Transmit and Receive General Timing

Symbol	Parameter	Min	Max	Unit	Figure
tINVRCV	Receive Start-up Delay Time	0	500	ns	8
tTRVHDV	Transmit Start-up Delay Time	0	200	ns	9
tTRVRCV	Loopback Start-up Delay Time	0	500	ns	9
tHDVHDZ	IDL Duration Test	250	350	ns	10

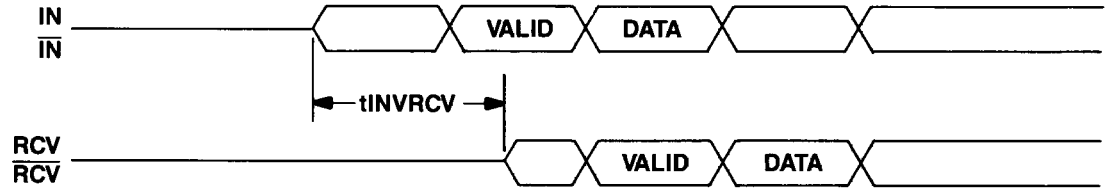


Figure 8. Receive General Timing

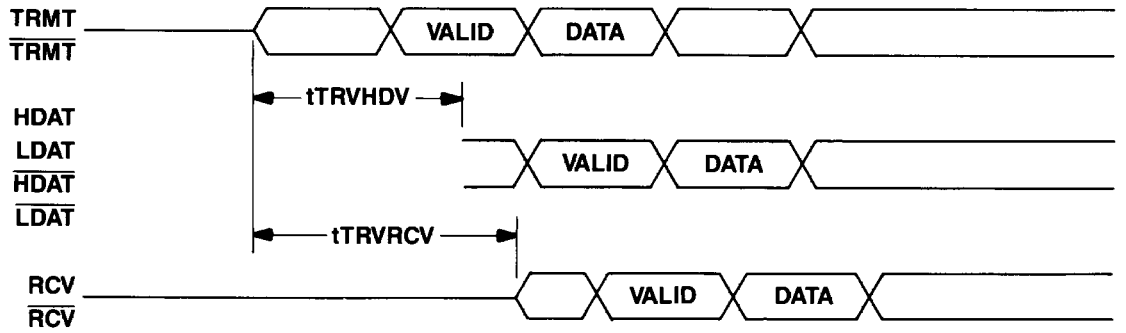
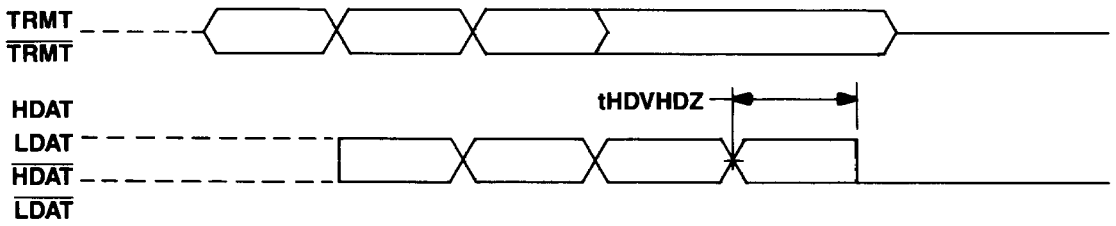


Figure 9. Transmit General Timing



Note: The AUI interface must accept very long IDL pulses on TRMT/$\overline{\text{TRMT}}$, and these pulses must be truncated to proper length before being introduced onto the TP network.

Figure 10. IDL Duration

Table 4. Collision Timing

Symbol	Parameter	Min	Max	Unit	Figure
tINVCLV	Arrival of Data at the IN/$\overline{\text{IN}}$ Input with the Other Path Already Active to the Appearance of CS0 Signal on CLSN/$\overline{\text{CLSN}}$	0	900	ns	11
tINVRCV	Time for the Chip to Switch from Loopback of the Input Data (TRMT/$\overline{\text{TRMT}}$) at the Outputs RCV/$\overline{\text{RCV}}$ to Receive Data from IN/$\overline{\text{IN}}$	1000	1600	ns	11
tTRVCLV	Arrival of Data at the TRMT/$\overline{\text{TRMT}}$ Input with the Other Path Already Active to the Appearance of CS0 Signal on CLSN/$\overline{\text{CLSN}}$	0	900	ns	12
tINZCLZ	Time that SQE Continues After IN/$\overline{\text{IN}}$ Have Gone Idle Given TRMT/$\overline{\text{TRMT}}$ are Still Active	500	900	ns	13
tTRZCLZ	Time that SQE Continues After TRMT/$\overline{\text{TRMT}}$ Have Gone Idle Given IN/$\overline{\text{IN}}$ are Still Active	0	900	ns	14
tCLHCLL	CS0 High Pulse Width	40	60	ns	15
tCLLCLH	CS0 Low Pulse Width	40	60	ns	15
tCLHCLH	CS0 Frequency	8.5	11.5	MHz	15

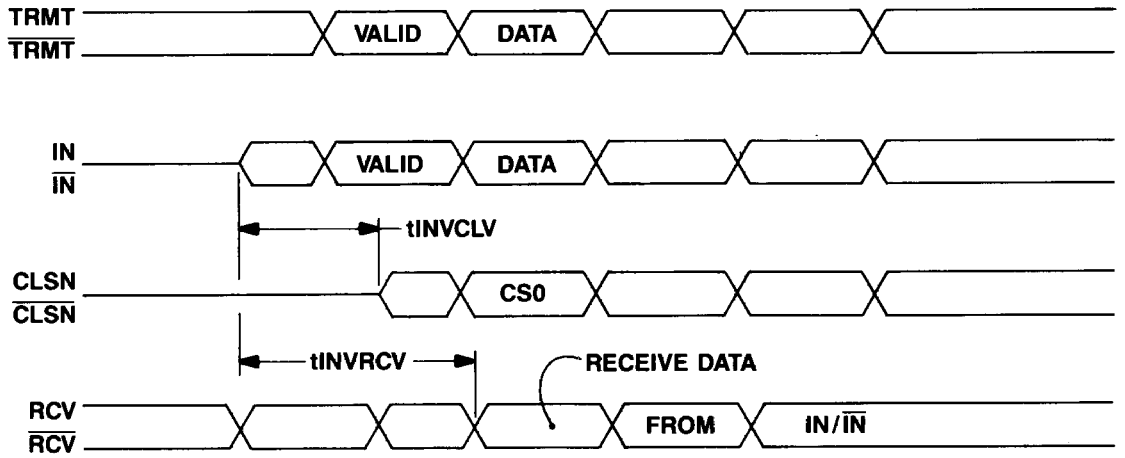


Figure 11. Collision Timing (Entry During Transmit)

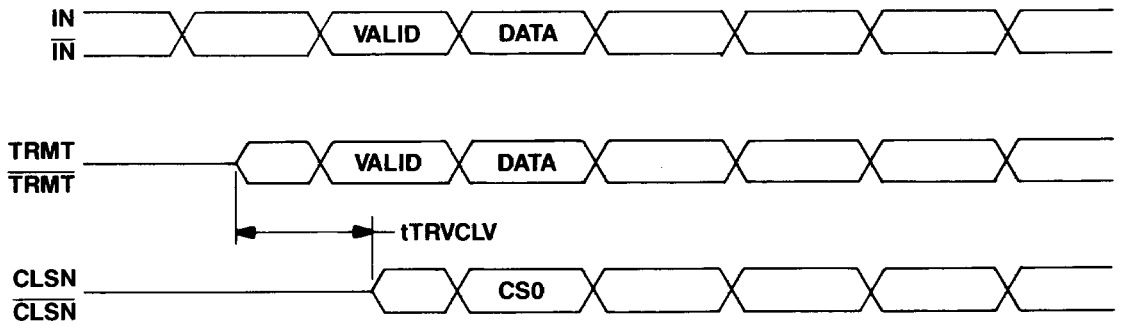


Figure 12. Collision Timing (Entry During Receive)

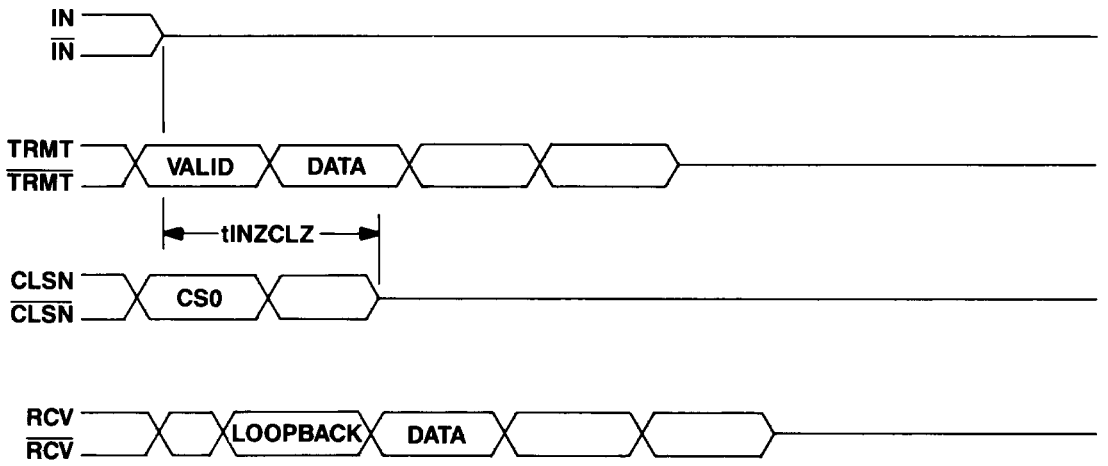


Figure 13. Collision Timing (Transmit Exit)

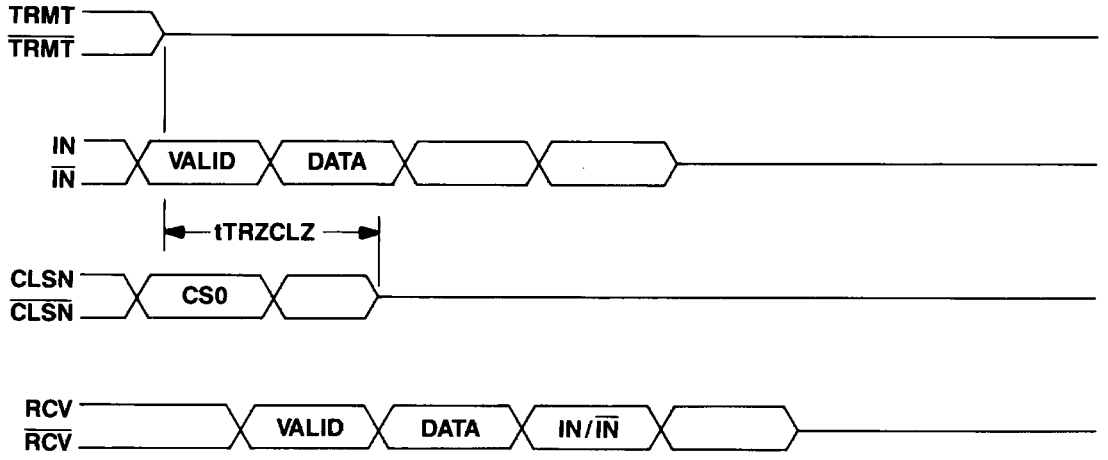


Figure 14. Collision Timing (Receive Exit)

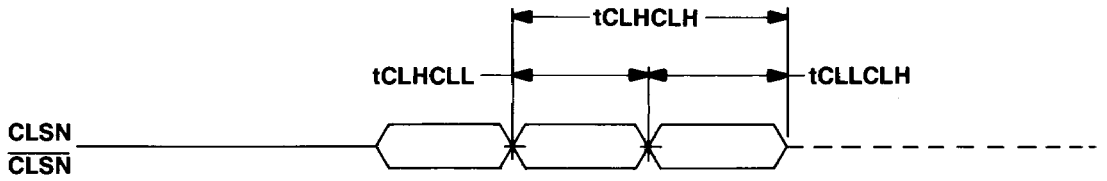


Figure 15. CS0 Characterization

Table 5. Jabber Timing (See Figure 16.)

Symbol	Parameter	Min	Max	Unit
tTRVHDX	Assertion of Valid Data at TRMT/$\overline{\text{TRMT}}$ to the Removal of Data at the Outputs HDAT/$\overline{\text{HDAT}}$/LDAT/$\overline{\text{LDAT}}$	45	55	ms
tHDXCLV	Time from the Jabbing of the TP Outputs HDAT/$\overline{\text{HDAT}}$/ LDAT/$\overline{\text{LDAT}}$ to the Appearance of a Valid CS0 Signal on CLSN/$\overline{\text{CLSN}}$	0	900	ns
tTRZCLZ	Time from the End of Activity on TRMT/$\overline{\text{TRMT}}$ to the Removal of the CS0 Signal on CLSN/$\overline{\text{CLSN}}$	250	750	ms

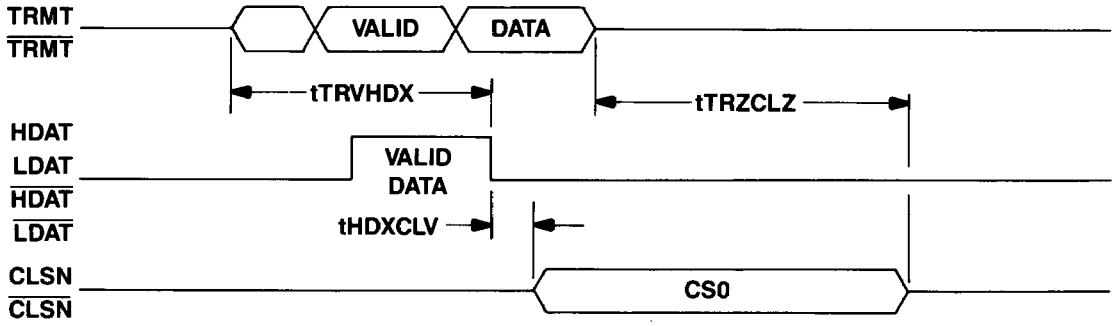


Figure 16. Jabber Timing

Table 6. Link-Integrity Pulse (See Figure 17.)

Symbol	Parameter	Min	Max	Unit
tHDLHDH	Time between Transmitted Link-integrity Pulses	8	24	ms
tHDHHDL	Transmitted Link-integrity Pulse Width	80	120	ns

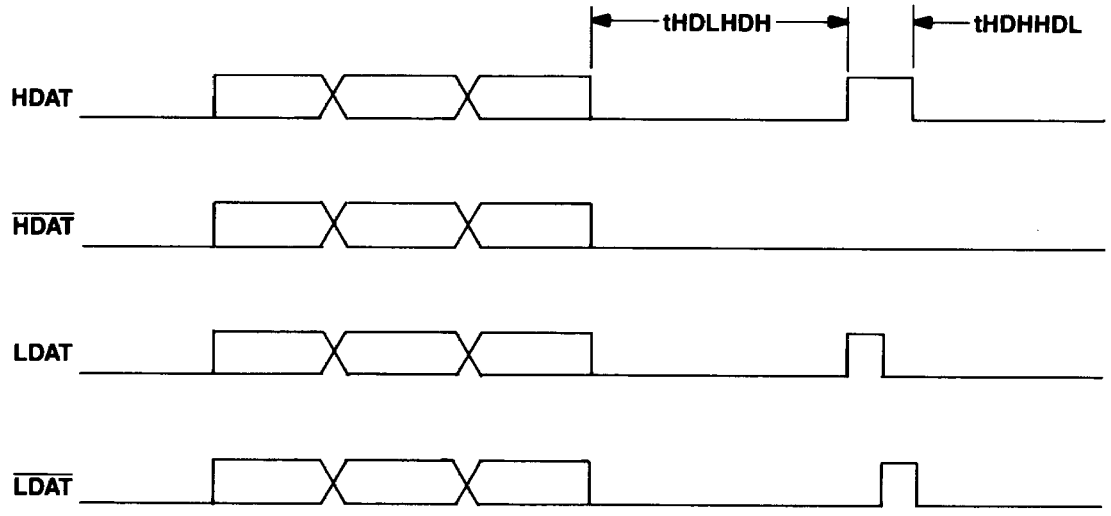


Figure 17. Transmitted Link-Integrity Pulses, $\overline{LI}$ Enabled

Table 7. Heartbeat Timing (See Figure 18.)

Symbol	Parameter	Min	Max	Unit
tTRVHBH	Setup Time for Heartbeat Strapping Option	—	10	μs
tTRZCLV	Time from the End of the IDL in the Transmit Path to the Assertion of the CS0 Heartbeat Signal on CLSN/$\overline{CLSN}$	600	1600	ns
tCLVCLZ	Time a Valid CS0 Signal, Not Including the Trailing IDL, is Present on the CLSN/$\overline{CLSN}$ Pins	500	1500	ns

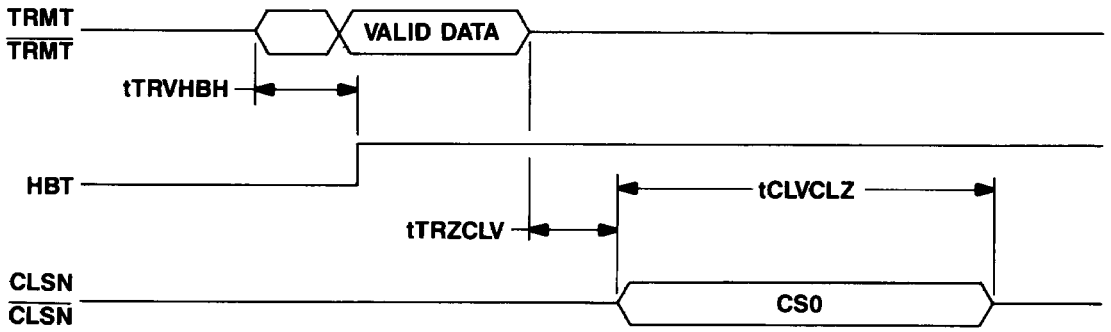


Figure 18. Heartbeat Timing

Table 8. LED Timing

Symbol	Parameter	Min	Max	Unit	Figure
tRLHRLL	RLED Fixed Off-time	90	110	ms	19
tRLLRLH	RLED Minimum On-time	4	8	ms	19
tRLL1RLH1	RLED — Time at Which the LED Turns Off Given that $\overline{LI}$ is Enabled and an Absence of Receive Traffic and Link-integrity Pulses Appear	50	150	ms	20
tRLH1RLL2	RLED — Time that the LED is Off Given that $\overline{LI}$ is Enabled, Until Receive Traffic or Link-integrity Pulses Appear	—	—	—	20
tRLL2RLH2	RLED — With $\overline{LI}$ Enabled, Minimum On Time After Receive Traffic or Link-integrity Pulses Appear	500	1500	ms	20
tTRVXLH	XLED — Time to Turn Off	—	10	μs	21
tXLHXLL	XLED — Fixed Off-time	90	110	ms	21
tXLLXLH	XLED — Minimum On-time	4	8	ms	21
tINVCDL	CLED — Time to Turn On	—	10	μs	22
tCDLCDH	CLED — Nominal On-time	10	20	ms	22
tHDXJLL	JLED — Time to Turn On	—	10	μs	23
tJLLJLH	JLED — On-time While TP Drivers are Jabbed	—	—	—	23

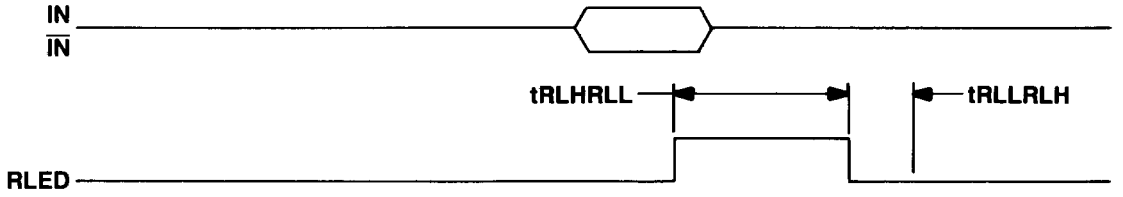


Figure 19. RLED Timing When Traffic Arrives, $\overline{LI}$ Disabled and Enabled

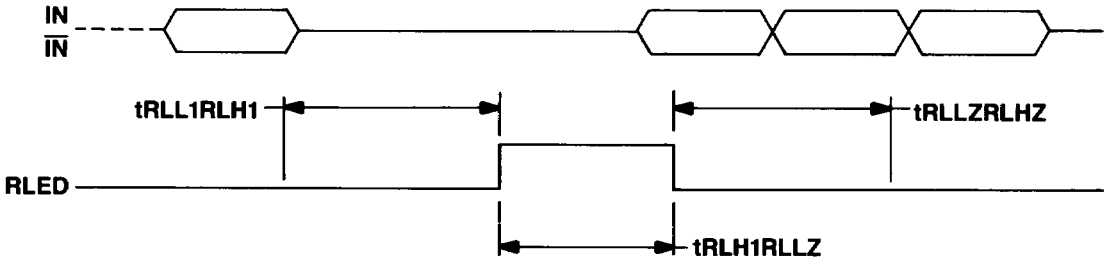


Figure 20. RLED Timing, $\overline{LI}$ Enabled

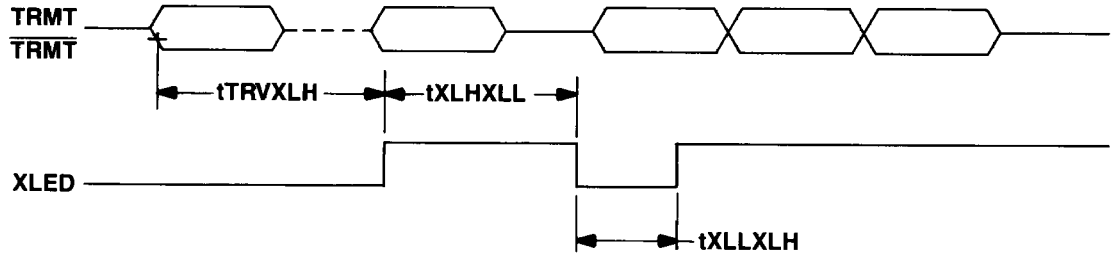


Figure 21. XLED Timing

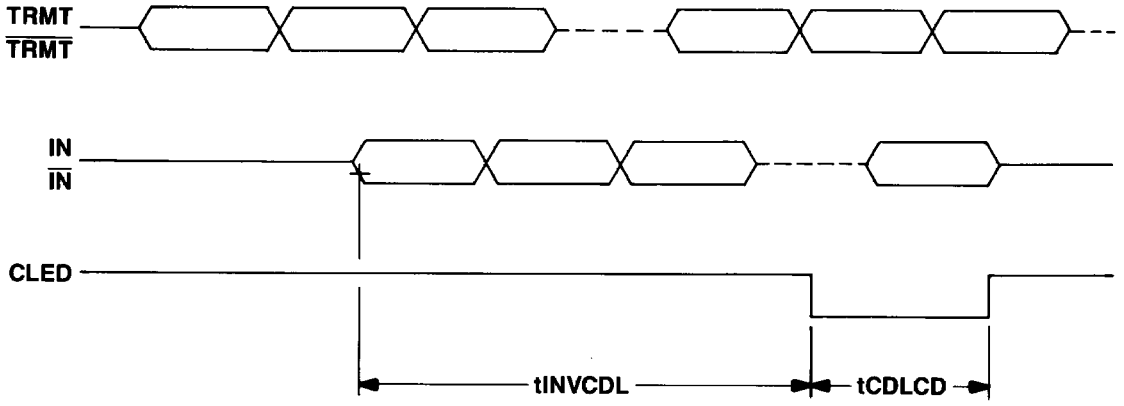


Figure 22. CLED Timing

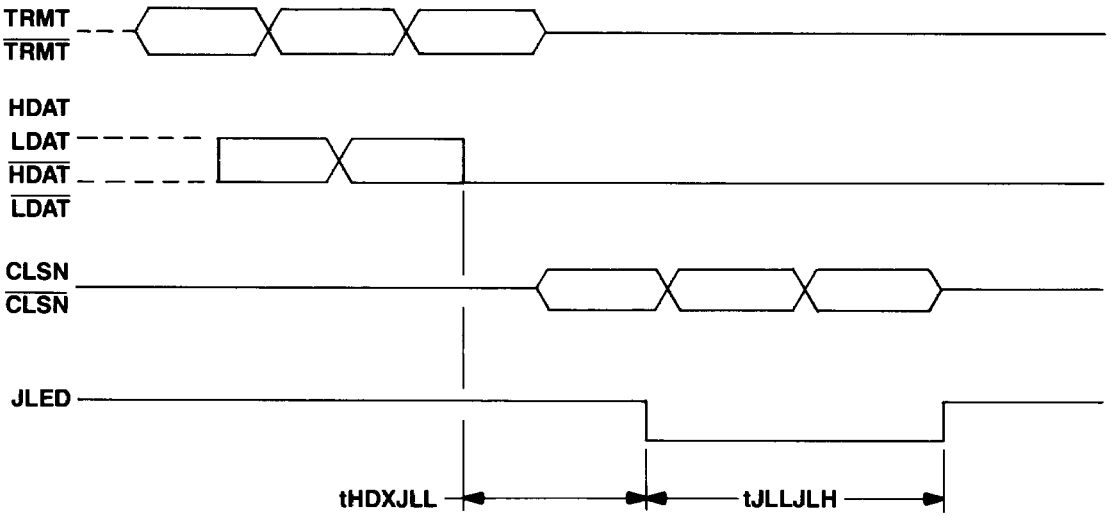
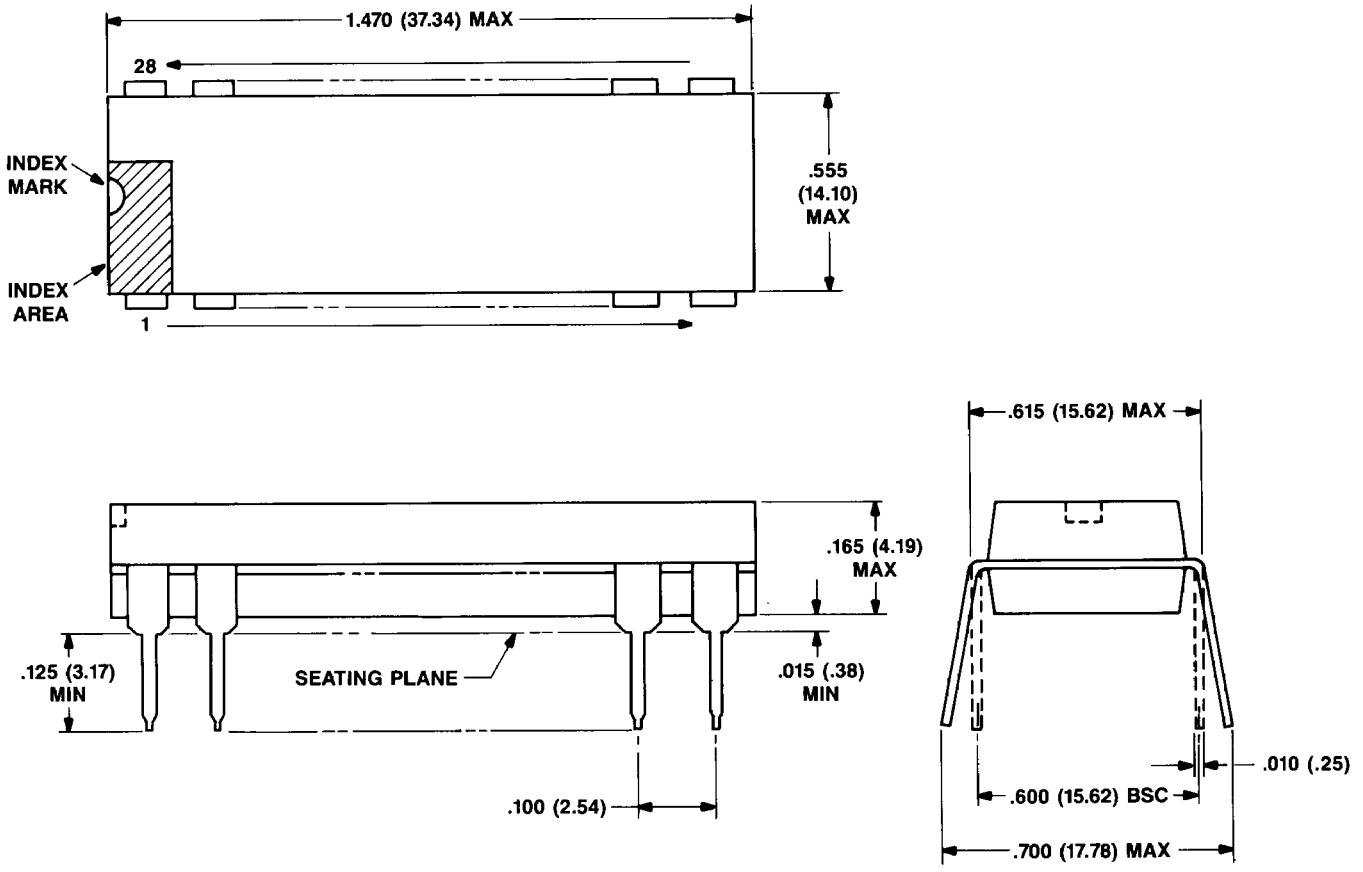


Figure 23. JLED Timing

Outline Diagrams

28-Pin, Plastic DIP

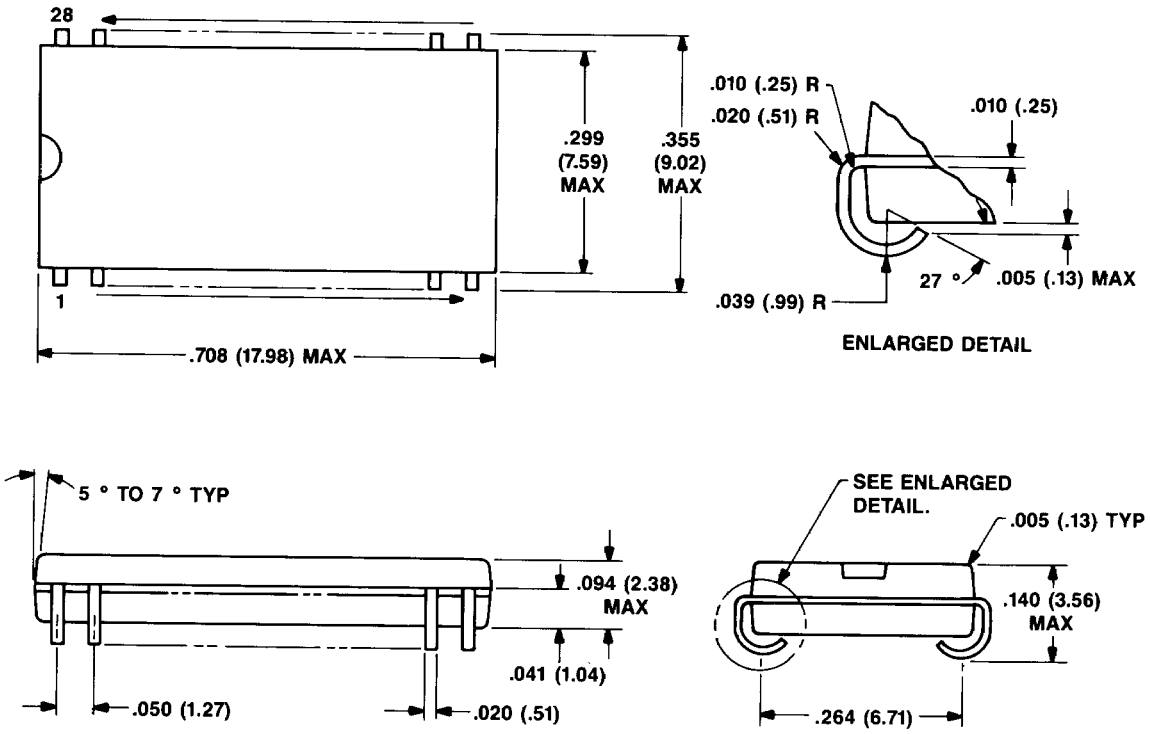
Dimensions are in inches and (millimeters).



Notes:
Meets JEDEC standards.
Index mark may be a semicircular notch or circular dimple located in the index area.

28-Pin, Plastic SOJ

Dimensions are in inches and (millimeters).



Note: Index mark may be a notch, dimple, or bevel located in the zone identified on the outline.

Ordering Information

Device Code	Package	Temperature
T7220-PC	28-Pin, Plastic DIP	0 °C to 70 °C
T7220-EC	28-Pin, Plastic SOJ	0 °C to 70 °C

Glossary

10BASE-T — A proposed addition to the 802.3 IEEE standard for using twisted-pair wiring as the physical media.

AUI — Attachment unit interface.

CD0 — Clocked data zero. A Manchester-encoding clock signal that is high for the first half of the bit cell and low for the second half of the bit cell.

CD1 — Clocked data one. A Manchester-encoding clock signal that is low for the first half of the bit cell and high for the second half of the bit cell.

CI — AUI collision input circuit.

Collision — A state of collision exists whenever there are valid signals being input to the TPMAU from the network and DTE simultaneously and the TPMAU is not in a link-failure state.

CS0 Signal — A signal that is placed on the CI circuit whenever a collision condition exists. It is a periodic square wave at 10 MHz ± 15 % with a duty cycle no worse than 40/60 or 60/40.

CSMA/CD — Carrier sense multiple access with collision-detect.

DI — AUI data input circuit.

DO — AUI data output circuit.

DTE — Data terminal equipment. Any piece of equipment at which a communication path begins or ends.

IDL Pulse — A logic-high pulse of 300 ns ± 50 ns duration that is appended to the end of a data frame to signify the end of the data frame.

Jabber — A function that disables continued transmission of a data frame to the media should that data frame exceed a specified duration.

LAN — Local area network.

Link Integrity — An internal function that determines if a remote MAU is attached and operating at the far end of the twisted-pair link.

Manchester Encoding — A type of encoding, defined by IEEE 802.3, that ensures transitions are present so that a clock can be recovered from the data stream.

MAU — Medium attachment unit.

ppm — Parts per million.

SQE — Signal quality error.

TP — Twisted pair.

TPMAU — Twisted-pair medium attachment unit.

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