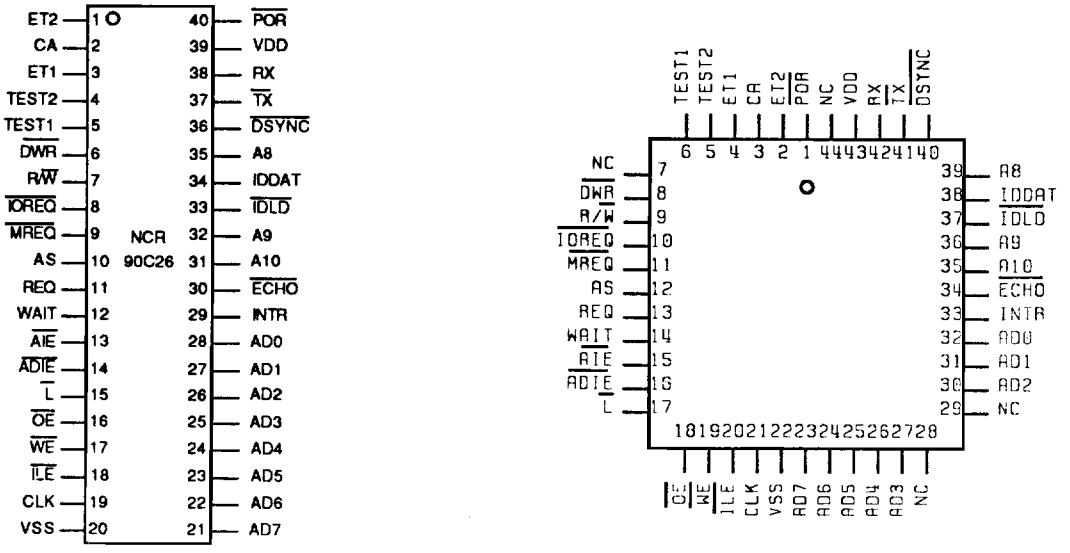
ARCNET®
Controller Chip

FEATURES

- Data transfers at 2.5 Megabits per second
- Supports up to 255 Local Area Network nodes
- Controls external SRAM containing host messages
- Token Passing Protocol gives predictable transfer intervals
- Interfaces with a variety of microprocessors
- Can transmit broadcast messages to all other nodes on LAN
- Transfers data between the AC and the actual LAN cable circuitry by using the NCR90C32 ARCNET Tranceiver 16-pin companion chip

INTRODUCTION

The NCR90C26 AC (ARCNET Controller) is a powerful token-passing communications chip that handles all data transfer functions for a node on an ARCNET Local Area Network (LAN). With a flexible microprocessor interface, the AC accepts commands from its host regarding message packets to be sent or received over the LAN. These packets are stored in an external Static RAM that may be accessed jointly by the host or the AC. When a node is added to or removed from the network, the active nodes will automatically "reconfigure" as directed by each AC. Figure 2 shows the detailed connections for the AC in an ARCNET node.



NCRMS004

Figure 1 40-pin DIP and 44-pin PLCC

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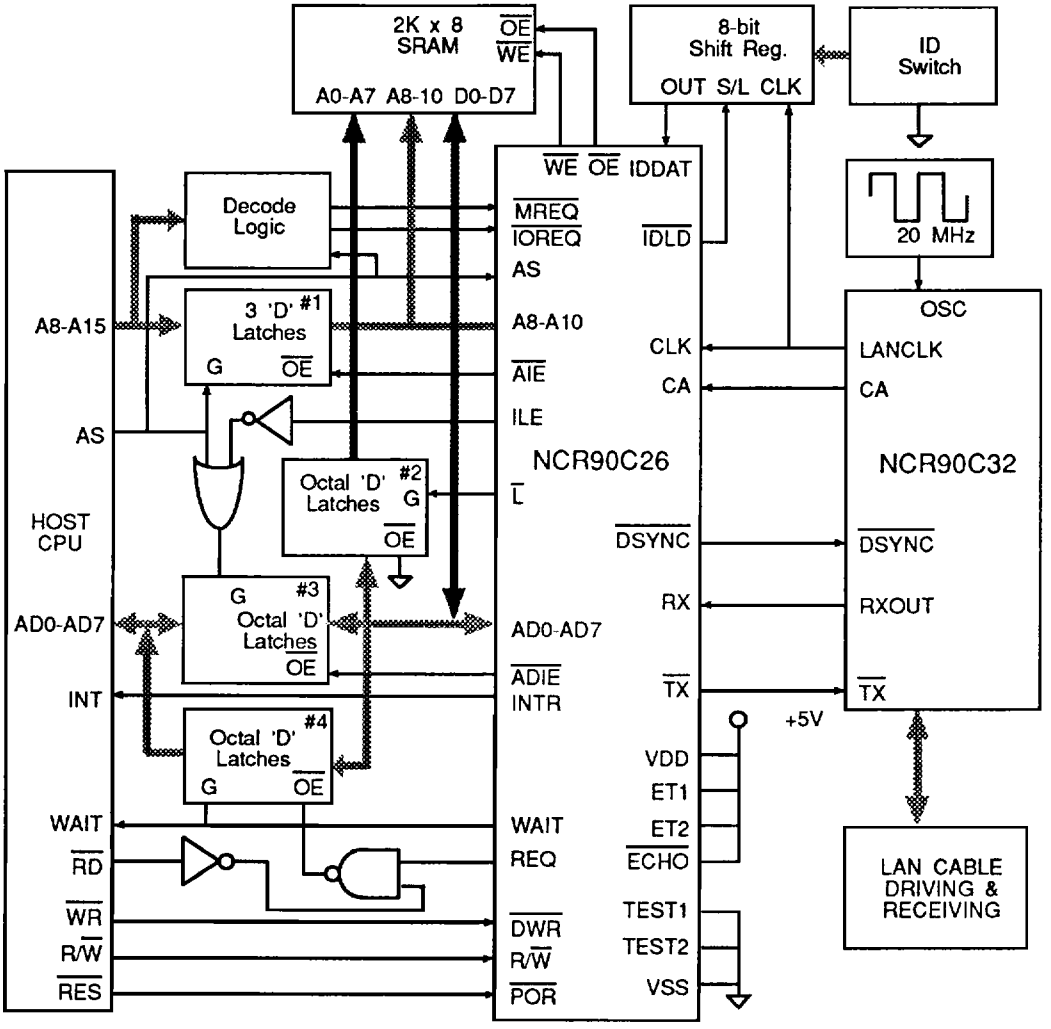


Figure 2 Typical system block diagram

Symbol	Pin No.		I/O	Name and Function
	40-pin DIP	44-pin PLCC		
A9, A10	32, 31	36, 35	O	PAGE SELECT: The two most significant address bits to the RAM buffer. These pins reflect the page value specified in the ENABLE TRANSMIT and ENABLE RECEIVE commands. For a 1K buffer they are connected to A8 & A9 of the RAM, and for a 2K buffer system, connect to A9 & A10 respectively.
A8	35	39	O	ADDRESS 8: Connects to RAM pin A8 in a 2K buffer system. This pin is left unconnected in systems with a 1K buffer.
AD0-AD7	28-21	32-23 28-29 =NC	I/O	ADDRESS-DATA BUS: The eight-bit data path to the AC, and the lower eight address bits of the RAM buffer. In addition, AD0 is used for command decoding of host status/control commands to the AC.
$\overline{\text{IOREQ}}$	8	10	I	I/O REQUEST: This signal is sampled by the AC on the falling edge of AS, and indicates that the host wishes to transfer status/control information over the Address-Data bus to the AC.
$\overline{\text{MREQ}}$	9	11	I	MEMORY REQUEST: This signal is sampled by the AC on the falling edge of AS, and indicates that the host plans to transfer data to or from the RAM buffer.
R/$\overline{\text{W}}$	7	9	I	READ/WRITE: Indicates the pending host access request is either a read or a write cycle. R/$\overline{\text{W}}$ is sampled on the falling edge of AS.
$\overline{\text{AS}}$	10	12	I	ADDRESS STROBE: Used by the AC to sample the state of R/$\overline{\text{W}}$, $\overline{\text{MREQ}}$, and $\overline{\text{IOREQ}}$. If necessary, the AC will initiate arbitration for the Address-Data bus on the falling edge of AS.
REQ	11	13	O	REQUEST: A feedback signal acknowledging that the AC has sampled a Memory or I/O request by the host.
WAIT	12	14	O	WAIT: This signal is asserted by the AC to indicate that it is not ready to transfer data at the beginning of host access requests. Wait is returned low when the AC is ready for the host to complete its transfer.
$\overline{\text{DWR}}$	6	8	I	DELAYED WRITE: A signal that informs the AC that valid data is set on the Address-Data bus, for host write cycles. $\overline{\text{DWR}}$ should be grounded, if the host will always be able to meet write data setup time.
INTR	29	33	O	INTERRUPT: The AC asserts this signal to indicate to the host that an enabled interrupt condition has occurred. INTR will return low upon the resetting of the interrupting status condition or the corresponding mask bit.
$\overline{\text{ILE}}$	18	20	O	INTERFACE LATCH ENABLE: The AC brings this signal low to gate the host's valid output data for host write cycles.
$\overline{\text{ADIE}}$	14	16	O	ADDRESS-DATA INPUT ENABLE: Tristates Address-Data Bus pins in the AC. Enables the host to drive the Address-Data bus.
$\overline{\text{AIE}}$	13	15	O	ADDRESS INPUT ENABLE: Tristates pins A8-A10 of the AC and enables the host to drive these signals.
$\overline{\text{L}}$	15	17	O	LATCH: Gates the Address-Data bus into an external latch. This latch is normally connected to A0-A7 of the RAM buffer.
$\overline{\text{WE}}$	17	19	O	WRITE ENABLE: This signal strobes data off the Address-Data bus into the RAM buffer. Data is taken by the RAM at the rising edge of $\overline{\text{WE}}$.
$\overline{\text{OE}}$	16	18	O	OUTPUT Enable: Enables the RAM buffer to drive the Address-Data bus on all RAM read cycles.
$\overline{\text{IDLD}}$	33	37	O	ID LOAD: When active, this signal synchronously loads the state of the ID switches into an external shift register.
IDDAT	34	38	I	ID DATA IN: This signal is the serialized ID switch setting from the ID switch register. The ID data is shifted into the AC MSB first, and with high level indicating logic 1.
ET1, ET2	3, 1	4, 2	I	EXTENDED TIMEOUT FUNCTIONS: The levels on these pins indicate the timeout durations of the AC in checking responses from the other nodes on the LAN. These pins should be tied high for normal operation.

Symbol	Pin No.		I/O	Name and Function
	40-pin DIP	44-pin PLCC		
$\overline{TX}$	37	41	O	TRANSMIT DATA: Serial output data to the Transceiver chip.
RX	38	42	I	RECEIVE DATA: Serial inpput data from the Transceiver chip.
TEST1, TEST2	5, 4	6, 5	I	TEST PINS 1 & 2: Used to set up special diagnostic tests. For normal operation, these pins are grounded.
$\overline{ECHO}$	30	34	I	ECHO DIAGNOSTIC ENABLE: When low, this signal enables a retransmit of messages whose length is less than 254 bytes, for level testing. This pin is normally tied high.
CLK	19	21	I	CLOCK: A free-running 5 MHz clock used for timing of AC bus cycles and other various chip functions.
CA	2	3	I	AUXILIARY CLOCK: A gated 5 MHz clock used to control operation of the AC sequencer. CA is periodically halted by DSYNC and restarted by RX.
$\overline{DSYNC}$	36	40	O	DELAYED SYNC: This signal is asserted by the AC to cause the clock generator circuit to halt the CA clock.
$\overline{POR}$	40	1	I	POWER ON RESET: Sets the AC sequencer counter to zero and initializes various internal control and status signals. Also sets the POR status bit which causes the INTR pin to be asserted.
VDD	39	43		+5 VOLT SUPPLY.
VSS	20	22		GROUND.

LINE PROTOCOL

The NCR90C26 ARCNET Controller implements an isochronous line protocol, with each character byte consisting of: 2 clock units of mark (logic 1), 1 clock unit of space (logic 0), and 8 clock units of data (the character). A single clock unit is 200 nanoseconds in duration, so a byte of data will be transmitted every 4.4 microseconds. Thus, the time to transmit any message can be determined exactly. All transmissions start with an ALERT BURST, which is 6 clock units of mark. The line idles in a spacing condition. The five types of ARCNET transmissions are now described:

INVITATIONS TO TRANSMIT:

AN ALERT BURST followed by three characters: one EOT (End Of Transmission) and two repeated DID (Destination IDentification characters. This message passes control (the "token") from one node to another.

FREE BUFFER ENQUIRIES:

AN ALERT BURST followed by three characters: one ENQ (ENQuiry) and two repeated DID characters. This message asks another node if it is able to accept a message packet.

PACKETS:

An ALERT BURST followed by 8 to 260 characters:

- one SOH (Start Of Header) character
- one SID (Source IDentification) character
- two repeated DID characters
- an inverse COUNT character = 256-N, for N data characters to be sent
- from 1 to 253 data characters
- two CRC (Cyclic Redundancy Check) characters

ACKNOWLEDGEMENTS:

An ALERT BURST followed by a single ACK (ACKnowledgement) character. This message is used as a positive respponse to FREE BUFFER ENQUIRIES, and also to acknowledge the valid reception of a PACKET.

NEGATIVE ACKNOWLEDGEMENTS:

An ALERT BURST followed by a single NAK (Negative AcKnowledgement) character. This message gives a negative response to FREE BUFFER ENQUIRIES.

The codes (all in HEX) for the special characters mentioned above are:

EOT-04, ENQ-05, SOH-01, ACK-06, NAK-15

The COUNT character for PACKETS may be equal to 512-N if a "long packet" is being sent. The CRC polynomial used for data packets is:

$$X^{16} + X^{15} + X^2 + 1$$

As a receiving node, the AC will verify all incoming transmissions by checking for: 1) at least one mark and exactly one space preceding each character 2) a valid EOT, ENQ, SOH, ACK, or NAK following the ALERT BURST 3) proper CRC for data packets 4) correct number of characters, depending on the transmission: can be from 1 to 260 5) at least nine spaces following the very last character.

NETWORK CONTROL

All nodes in an ARCNET system are distinguished by a unique 8-bit ID (IDentification) value which is determined by switches, typically a DIP switch, that is associated with each AC chip. An ID of '0' may not be assigned to any node however, since that ID indicates a BROADCAST to all nodes. Control of the Local Area Network (LAN) is based on an INVITATION TO TRANSMIT being passed between nodes. When an AC receives an INVITATION containing its own ID, it has "gotten the token," and it then takes control of the LAN. To pass a message, the host processor simply loads the message data and the destination ID into its AC's RAM buffer, and then writes an "Enable Transmit" command to the AC. An AC will know it has a message to send if it sees that TA (Transmitter Available) in its Status Register is LOW. When that AC has the token, it then transmits a FREE BUFFER ENQUIRY to the destination ID to see if it is able to take the message. If that destination is able to receive, it will transmit back an ACK. The controlling node then transmits the PACKET, complete with a 16-bit CRC. When an AC receives the token, but its TA is high (it has no message to send), it will send INVITATION TO TRANSMIT and thus pass on the token.

When an AC is sent FREE BUFFER ENQUIRY, it will poll its RI (Receiver Inhibited) Status bit. If the RI bit is set, that AC will transmit a NAK, and the controlling node will then pass the token. If an AC with a packet to send gets a NAK, then it will re-transmit a FREE BUFFER ENQUIRY the next time it receives the token. These attempts will continue until the AC "Times out," a process described in detail in a following section. Upon Timeout, the AC sets its TA bit and passes the token. After it has sent a PACKET, an AC waits a specified response time: if within that time, it receives ACK, it sets both the TMA (Transmit Message Acknowledged) and the TA Status bits and passes the token. If it does not receive ACK in time, it only sets TA and then passes the token.

All nodes recognize a PACKET when they see the SOH character, and all the ACs will write the SID into their Receive Buffer. If an AC perceives the first DID as its own, or the PACKET is a Broadcast (described below), the chip will write the second DID and the rest of the message into its Receive Buffer. Otherwise, the AC will ignore the rest of the PACKET. After the PACKET has been fully received, it must pass three conditions to be considered a valid message: a) the CRC comparison b) correct length of characters, and c) valid DID in byte 0 of the Receive Buffer. Valid DIDs are either '0' (indicating Braodcast), or the AC's own ID. If a message is valid by these conditions, then the AC will set its RI Status bit. However, if the DID is that of the AC, it will transmit an ACK first before setting RI. If any of the conditions fail, the AC ignores the message and will write it over with any future PACKETS.

RECONFIGURATION AND BROADCAST

Two activities involve all nodes on the ARCNET system. The first is a Reconfiguration of the network, which is performed any time a node is removed from, or added to the system. The second is a Broadcast Packet. PACKETS are described in the *Description of Line Protocol* section on page 5 .

Reconfiguration

An AC will instigate a Reconfiguration when it is first powered on, or when it has not received an INVITATION TO TRANSMIT within 840 milliseconds. It does this by transmitting a RECONFIGURATION BURST: 8 marks and 1 space repeated 765 times. This burst has the effect of terminating all activity on the network. Because it is longer than all the other types of transmissions, it will interfere with the next INVITATION TO TRANSMIT, in effect "destroying" the token, and thus no other node will take control of the line. The RECONFIGURATION BURST also provides enough line activity so that the AC that just sent the token will also release control of the network.

When any AC sees the line idle for 78μs, it will know that the network is being Reconfigured, and it will set an internal NID (Next ID) register to its own ID. The NID is normally the DID sent with an

INVITATION TO TRANSMIT. Besides resetting its NID, an AC also starts a timeout of 146us times the quantity 225 minus its own ID. If this timeout expires with no other line activity, the AC will start transmitting INVITATIONS TO TRANSMIT, with DID set pointing to itself. Only the AC with the largest ID value will actually timeout.

After sending an INVITATION TO TRANSMIT, the AC will look for any line activity, indicating that the DID is a valid node. If the sending AC detects no activity after 74µs, it increments its NID and sends another INVITATION. Eventually, the AC with the ID that should be next will see its ID in the INVITATION and it will take control of the line. The previous AC will then have its NID set correctly. The process repeats until each AC has a NID stored which will represent a truly active node to which it will always pass the token. No time will be wasted in trying to send the token to nonexistent nodes. If for some reason a node is removed from an active network, when the previous node tries to pass the token, it will timeout. The previous AC will go through a cycle of incrementing its NID and transmitting INVITATIONS TO TRANSMIT, until it finds the next valid node. The total time to perform a Reconfiguration will vary depending on the system configuration, but is typically between 34ms to 61ms.

Broadcast

The other operation that pertains to all the nodes in the network is a Braodcast Packet. Broadcast Packets are a special subset of PACKETS. A PACKET is considered to be Broadcast if the DID is a value of '0.' No regular node may be assigned the Broadcast ID. Nodes are set up to receive Broadcasts by issuing an "ENABLE RECEIVE to Page nn" command to the corresponding AC, with the most significant bit of the command set to '1.' All the AC commands are described in a following section.

TIMECHECK FUNCTIONS

A standard baseband system using RG-62 coax cable (the ARCNET standard) can take up to 31µs for a one-way propagation, which corresponds to distance of about four miles. Also, the maximum turnaround time that any AC takes to respond to an incoming message is 12µs. Therefore, a maximum Response Time for any transmission should be 31 + 31 + 12 = 74µs. To allow margin, the AC uses 74.7 µs as its basic Response timeout, the interval within which a controlling node expects to perceive any line activity after it makes a transmission.

An IDLE Timeout is the interval that transpires at the onset of a Reconfiguration. After the RECONFIGURATION BURST, all the nodes will commence the Reconfiguration process after they have seen no line activity for the Idle timeout. In a standard network, the Idle timeout is 78.2µs. The TRANSFER Timeout is the ID-dependent interval that is also associated with Reconfiguration. This timeout is given by 146µs x (255-ID), and it will transpire only for the node with the highest ID on the network. The last timeout is the interval that instigates a Reconfiguration. In a standard network, if any node has not received an INVITATION TO TRANSMIT within a Reconfiguration timeout of 840ms, it will issue a RECONFIGURATION BUST and thus start a network Reconfiguration.

The above timeout values apply to a standard, or "basic" network with no two nodes farther apart than about four miles. The network may operate over longer distances by appropriately setting the ET1 and ET2 inputs. The table below shows the effect of ET1 and ET2 on two of the more pertinent timeouts. It is important that ET1 and ET2 be set to the SAME VALUE for all nodes on the network.

ET2	ET1	RESPONSE TIMEOUT	RECONFIGURATION TIMEOUT
1	1	74.7 µs	0.84 second
1	0	283.4 µs	1.68 seconds
0	1	561.8 µs	1.68 seconds
0	0	1118.6 µs	1.68 seconds

HOST INTERFACE

The "Typical ARCNET Node" diagram on page 2 of this manual illustrates the hardware aspects of a host processor interface to the 90C26 AC. The block on the left contains the signals of a generic processor with 8 bits of multiplexed address-data. The upper address bits are used to decode whether a pending host access is to/from the RAM buffer, or the AC. The RAM buffer in the drawing, a 2Kx8 Static RAM, can hold four pages at 512 bytes per page. Entire PACKETS are stored in a page in the RAM buffer. A 512 byte page corresponds to a Long Packet. Short Packets require 256 byte pages and a RAM buffer which is only a 1Kx8 SRAM. Leave A8 (from both the AC and the host) unconnected for a Short Packet network. The #1 latches capture the

host's upper address signals for RAM buffer accesses. The #2 8-bit latch always contains the lower 8 address bits for RAM buffer accesses, by both the AC and the host. For host write cycles, latch #3 buffers both lower RAM address and Data under control of the AC. Finally, latch #4 holds Data that the host has asked for in a read cycle. A recommended device for these latches is 74LS373.

In dealing with an ARCNET node, the host need only be concerned with two I/O locations, described below, and the 1K or 2K bytes in the Message RAM buffer. The AC chip was designed to allow speedy data transfers between the host and the Local Area Network. The organization of the four pages in the RAM allow for one message to be read out while concurrently a follow-on message is being written into the RAM. By transparently making accesses, the AC gets a dual-port implementation out of a standard component RAM. Since the host makes its access requests at arbitrary times, the AC synchronizes the host by asserting WAIT at every access attempt by the host. In addition to passing messages, the host also uses the Address-Data bus and the latches to access the AC directly. A low level on $\overline{IOREQ}$ at the falling edge of AS identifies I/O cycles which are used to read the AC's Status, or to write commands to the AC. The I/O accesses pass through two I/O ports within the AC. The ports and their direction are decoded by the states of AD0 (at the host) and R/$\overline{W}$ (at the AC) at the falling edge of AS as follows:

AD0	WRITE OPERATION (R/W low)	READ OPERATION (R/W high)
0	Write Interrupt Mask	Read Status Register
1	AC Command	(reserved function)

HOST COMMANDS

The six valid host commands to the AC are followed by a summary of the Status Register bits:

DATA	FUNCTION
0000 0001	DISABLE TRANSMITTER: Causes an AC to cancel any pending transmit command. This command will cause the TA bit to be set the next time the AC receives the token.
0000 0010	DISABLE RECEIVER: Causes a pending receive command to be canceled. This command will cause the RI bit to be set the next time the AC receives the token. If a PACKET has already started arriving, then this command will have no effect.
000n n011	ENABLE TRANSMIT from Page nn: Tells the AC to prepare for a transmit operation out of RAM buffer page nn when it next receives the token. The TA and TMA bits are reset by an AC receiving this command. The TA bit is set to logic '1' at completion of the transmision; the TMA bit may already be set at that time if the destination node has sent back an acknowledgment. If TA is not true, this command should not be issued.
b00n n100	ENABLE RECEIVE to Page nn: Allows the AC to receive messages into RAM buffer page nn. The RI status bit is set to '0' by this command. If 'b' in the command is '0', then only messages addressed to the AC's ID will be received. If 'b' is '1', then Broadcast messages will also be accepted. RI will be set by a successful message reception.
0000 s101	DEFINE BUFFER SIZE: Tells an AC the size of its RAM buffer. If bit 's' is '0', the buffer is 1K bytes, and only short packets may be sent and received. If 's' is a '1', the buffer is 2K bytes, and both short and long packets may be handled.
000r p110	CLEAR FLAGS: Resets the POR and/or the RECON status bits depending on the variable bits. If r = 1, the RECON flag is cleared, and if p = 1, then POR is cleared.

STATUS REGISTER

BIT	NAME	DESCRIPTION
0	TA	Transmitter Available: When = 1, this bit indicates that the node is available to carry out a transmit sequence, and any previous ENABLE TRANSMIT process has been completed.
1	TMA	Transmit Message Acknowledged: This bit, when set to 1, indicates that a message sent from a pervious ENABLE TRANSMIT command was acknowledged by the receiving node.
2	RECON	Reconfiguration Flag: When = 1, this bit indicates that a system Reconfiguration took place due to the expiration of an Idle timeout. RECON is reset by the CLEAR FLAGS command.
3	TEST	Test Flag: Intended for test and diagnostic purposes. This bit will be equal to 0 under normal operating conditions.
4	POR	Power on Reset: When this bit = 1, indicates that AC has experienced a Power Reset due to an active signal on the POR input. POR is reset by CLEAR FLAGS.
5	ETS1	Extended Timeout Status 1: The state of this bit reflects the logic level on the ETS1 pin. ETS1 will be equal to 1 under normal operating conditions.
6	ETS2	Extended Timeout Status 2: Reflects the level on the ETS2 pin. Normally = 1.
7	RI	Receiver Inhibited: When = 1, this bit indicates that the AC is not taking any messages from other nodes. If an ENABLE RECEIVE command has been issued to the AC and no Power Reset has occurred, then RI = 1 means that a message has been received into the RAM buffer over the network.

Note: If an AC experiences a Power Reset, then the Status Register assumes the following states, where 'x' indicates "same as previous state."

Bit:	7	6	5	4	3	2	1	0
State:	1	x	x	1	0	0	0	1

Status Condition	Receive Inhibit	Test	Recon Timeout	Transmitter Available
Mask Bit	7	3	2	0

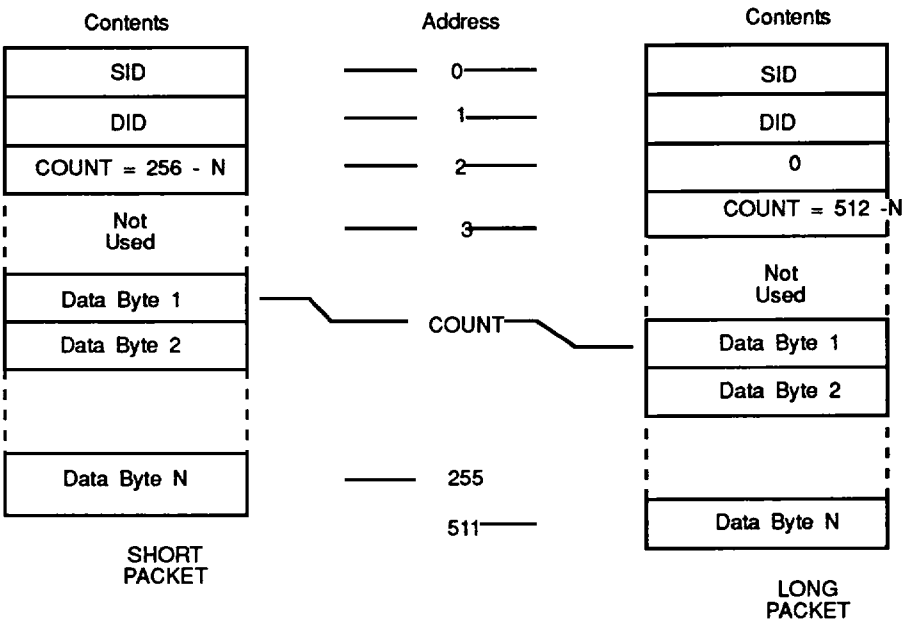
HOST INTERRUPTS

The 90C26 AC is able to generate an interrupt signal on the INTR pin in response to most of the conditions that cause Status bits to be set. A POR condition causes an unconditional (nonmaskable) interrupt. There is a Mask Interrupt Register where any combination of four other Status conditions may be set to cause interrupts. Status bits TMA, ETS1, and ETS2 have no corresponding mask bits and can never cause interrupts. The four maskable Status bits are grouped in the above table.

Setting any of these bits equal to 1 will cause the INTR signal to become active whenever the corresponding Status Condition becomes true. The other 4 bits in the Mask Register should be considered as "don't care." Once the INTR signal is active (high), it can be deasserted by either A) getting the corresponding Status Register bit to reset, or B) resetting the Mask Register bit directly.

RAM BUFFER MAP

The host needs to know the proper locations of the components in a message PACKET. Figure 3 shows these locations for both Short Packets (stored in 256-byte pages) and Long Packets (stored in 512-byte pages).



NOTE:: Addresses shown are relative to a Page, not absolute. SID=Source ID (not written in Transmit Packets). DID=Destination ID (set=0 for Broadcasts). N=Message Length. "Not Used" bytes imply message less than Maximum length. These bytes whould be written for Max Messages: SHORT=253 bytes, LONG=508. Messages: SHORT=253 bytes, LONG=508. When the AC senses an active POR it writes the lowest 2 bytes of the RAM buffer with: Addr 0: $D1 (indicates good self test); Addr 1: local ID value.

Figure 3 RAM Buffer Map

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM STRESS RATINGS

Voltage on VDD pin with respect to V .....-0.3 to +7.0V

Power on any signal pin.....-0.3 to VDD + 0.3

Power Dissipation.....100 mW

Operating Temperature Range.....0°C to 70°C

Storage Temperature Range.....-65°C to +150°C

The values listed above are absolute maximums which if exceeded could cause permanent damage to the device. Voltages are with respect to circuit ground.

DC Characteristics (V_{DD}=4.5V to 5.5V, V_{SS}=0V, T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{IL}	Input Voltage, Low	V_{SS} -0.3	0.8	V
V_{IH}	Input Voltage, High	2.2	V_{DD}	V
V_{IH} CLK	Clock Input Voltage High (CA and CLK pins)	V_{DD} -0.5	V_{DD} +0.3	V
V_{OH}	Output Voltage, High (I_{OH} = -50μA)	2.4		V
V_{OL}	Output Voltage, Low (I_{OL} = 2mA)		0.4	V
C_{IN}	Input Capacitance		20	pf
C_{BS}	Data Bus Capacitance		50	pf
C_X	Remaining Pins, Capacitance		30	pf
I_I	Input Leakage Current		±10	μA
I_{DD}	Power Supply Current (V_{DD} =5.25V)		19	mA

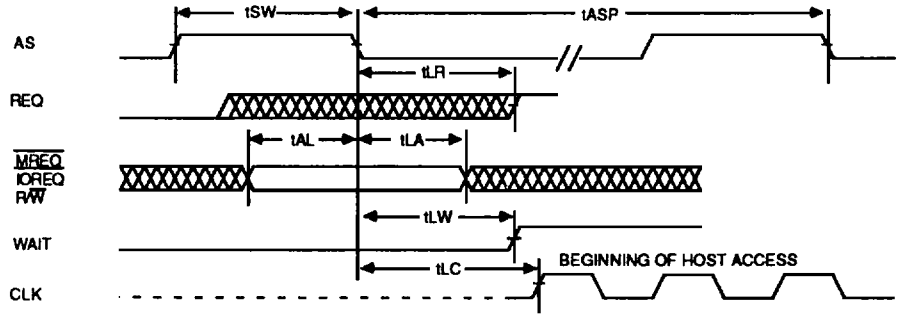


Figure 4 Processor Access Timing

NAME	DESCRIPTION	MIN	MAX	UNITS	NOTES
tSW	AS Strobe Width	50		ns	tCKP and tCAP are defined in diagram below.
tASP	Period of AS	3.5tCAP		ns	
tLR	REQ delay after AS falling edge	0	100	ns	
tAL	Control Valid before AS falling edge	50		ns	
tLA	Control Hold after AS falling edge	50		ns	
tLW	WAIT delay after AS	0	200	ns	
tLC	Processor Cycle delay	tCKP	2tCKP+100	ns	

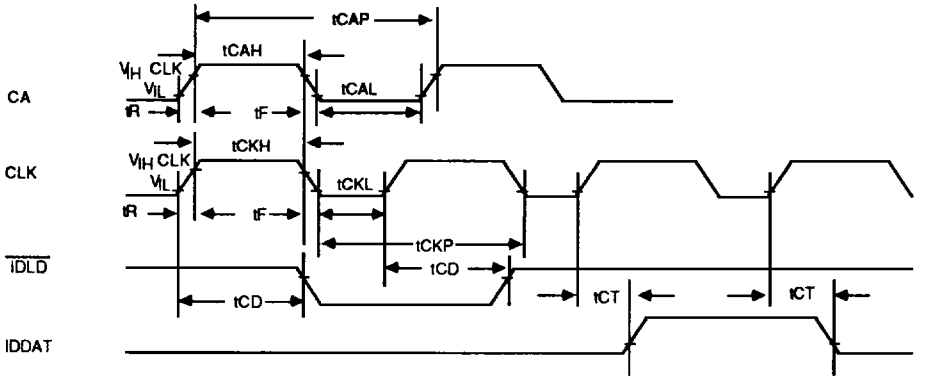


Figure 5 Clock Pulses & ID Input Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
tCAH	CA Pulse High Duration	60			ns
tCAL	CA Pulse Low Duration	60	100	300	ns
tR	Rise Time for CLK & CA			20	ns
tF	Fall Time for CLK & CA			20	ns
tCAP	CA Period	190			ns
tCKH	CLK Pulse High Duration	65			ns
tCKL	CLK Pulse Low Duration	65			ns
tCKP	CLK Period	190	200		ns
tCD	IDLD Delay from CLK Rising Edge	0		120	ns
tCT	IDDAT Delay from CLK Rising Edge	0		50	ns

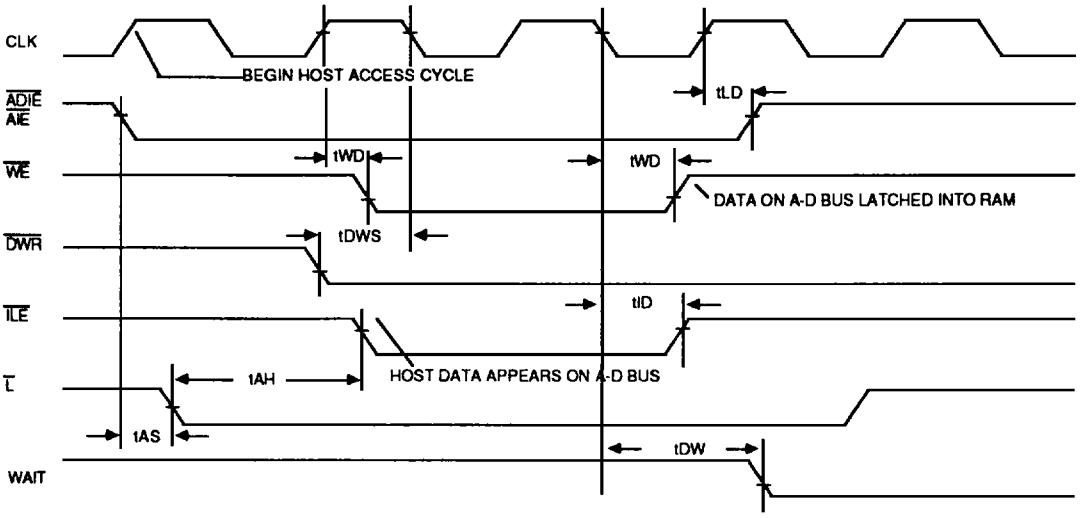


Figure 6 Write RAM by Host Timing

NAME	DESCRIPTION	MIN	MAX	UNITS	NOTES
tWD	$\overline{WE}$ Delay from Clock edges	0	100	ns	tLD, tAH and tAS are specified below.
tDWS	$\overline{DWR}$ Setup before Clock	50		ns	
tID	$\overline{ILE}$ Hold after Clock	10	100	ns	
tDW	WAIT Hold after Clock	20	100	ns	

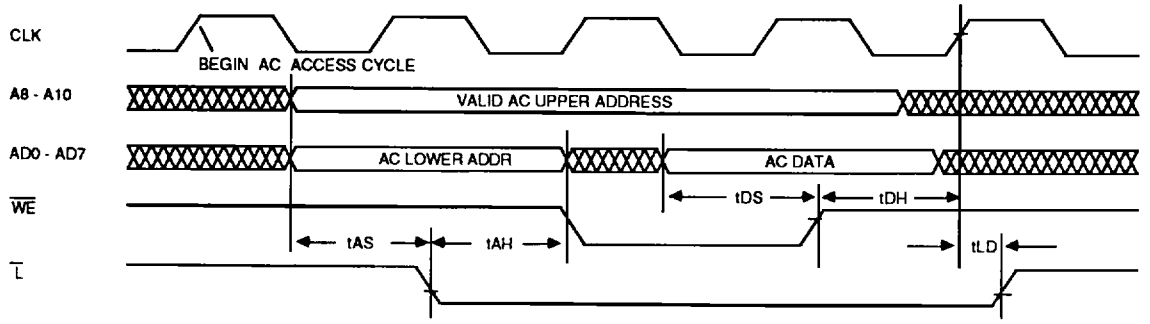


Figure 7 Write RAM by AC timing

NAME	DESCRIPTION	MIN	MAX	UNITS
tAS	Address Setup to $\overline{L}$	50		ns
tAH	Address Hold from $\overline{L}$	50		ns
tDS	Data Setup to $\overline{WE}$	60		ns
tDH	Data Hold from $\overline{WE}$	50		ns
tLD	$\overline{L}$ turnoff delay from clock	0	100	ns

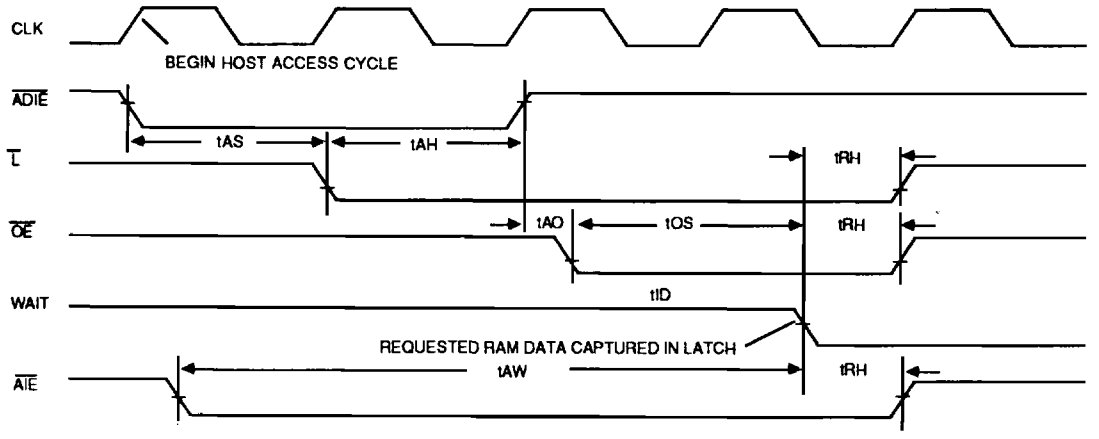


Figure 8 Read RAM by Host Timing

NAME	DESCRIPTION	MIN	MAX	UNITS
tRH	Read Data Hold after Wait	20		ns
tAO	Delay from $\overline{ADIE}$ to $\overline{OE}$ Active	40		ns
tOS	$\overline{OE}$ Setup to WAIT Turnoff	140		ns
tAW	$\overline{AIE}$ Active before WAIT	300		ns
tAS	Address Setup to $\overline{L}$	50		ns
tAH	Address Hold from $\overline{L}$	50		ns

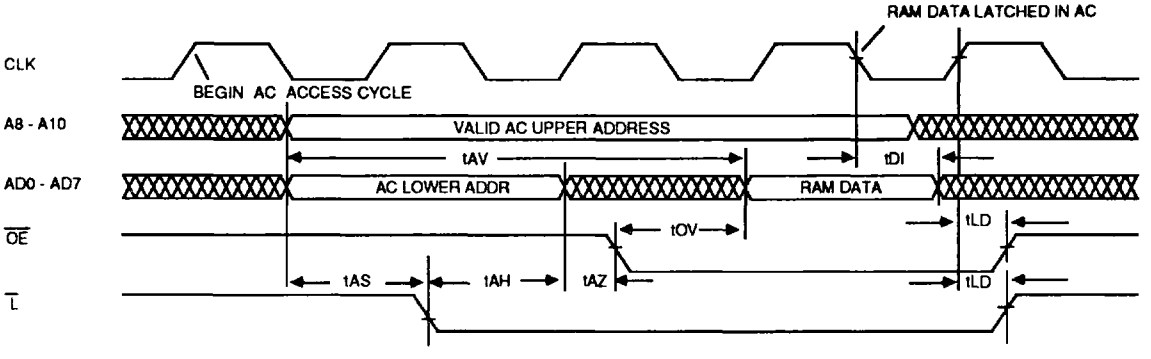


Figure 9 Read RAM by AC Timing

NAME	DESCRIPTION	MIN	MAX	UNITS	NOTES
tAV	Address Valid before RAM Data		300	ns	tAH and tAS are specified above.
tDI	RAM Data Hold for AC	80		ns	
tOV	RAM Data Delay after $\overline{OE}$	0	140	ns	
tAZ	A-D Bus Hi Impedance before $\overline{OE}$	0		ns	
tLD	$\overline{L}$ turnoff delay from clock	0	100	ns	

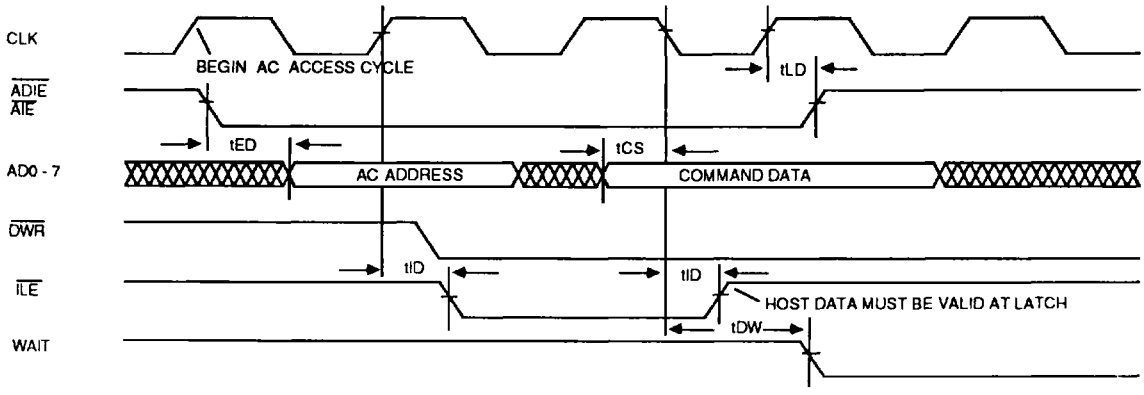


Figure 10 Write AC by Host Timing

NAME	DESCRIPTION	MIN	MAX	Units
tED	Enable Setup before Address		50	ns
tCS	Command Setup before Clock	125		ns
tID	$\overline{ILE}$ Delay after Clock	10	100	ns
tDW	WAIT hold after Clock	20	100	ns
tLD	Enable turnoff after Clock	0	100	ns

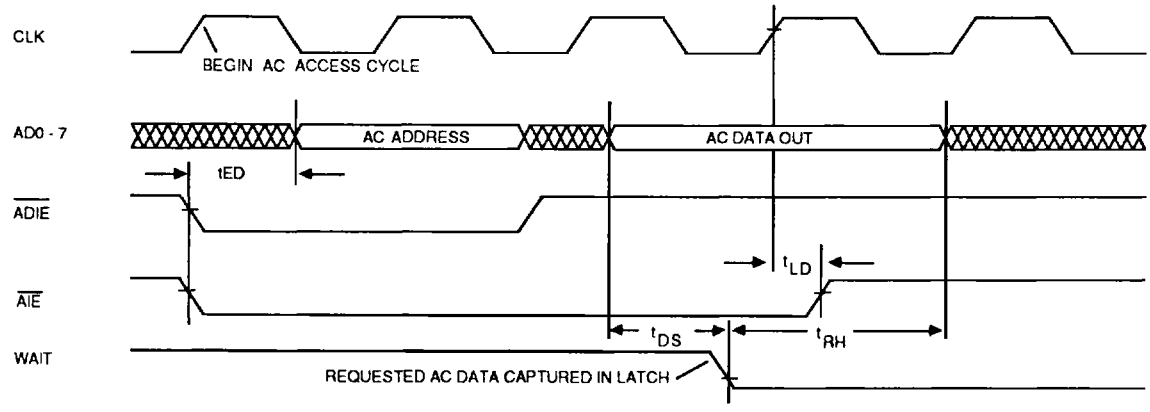


Figure 11 Read AC by Host Timing

NAME	DESCRIPTION	MIN	MAX	UNITS
tED	Enable Setup before Address		50	ns
tDS	AC Data Setup before WAIT	60		ns
tRH	AC Data Hold after WAIT	20		ns
tLD	$\overline{AIE}$ turnof after Clock	0	100	ns

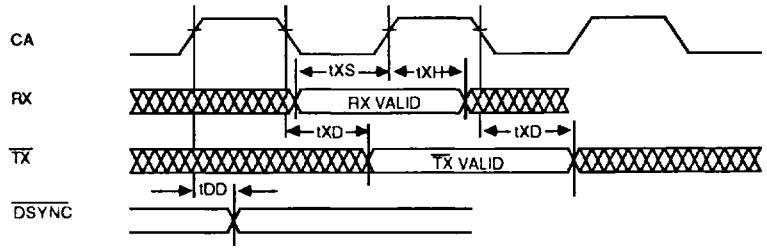


Figure 12 Receive & Transmit Timing

NAME	DESCRIPTION	MIN	MAX	UNITS
tXS	RX Setup to Clock Rising Edge	80		ns
tXH	RX Hold from Clock Rising Edge	30		ns
tXD	$\overline{TX}$ Valid delay from Clock Falling Edge	10	150	ns
tDD	Delay of $\overline{DSYNC}$ from Clock Rising Edge	10	150	ns

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SOUTHWEST

NCR Microelectronics
1940 Century Park East
Los Angeles, CA 90067
(213) 556-5396

EUROPE

NCR GMBH
Microelectronics Europe
Gustav-Heinemann-Ring 133
8000 Munchen 83
West Germany
(49) 89 - 63 22 02

ASIA

NCR Asia/Pacific
2501 Vicwood Plaza
199 Des Voeux Rd.
Central Hong Kong
5 859 6888

SOUTHWEST

NCR Microelectronics
3300 Irvine Ave., Suite 255
Newport Beach, CA 92660
(714) 474-7095

NCR Microelectronics
Communications Group MS 550A
2001 Danfield Ct.
Fort Collins, CO 80525
(303) 226-9500